Zilog **Product Specification**

November 1987

Z86C91 CMOS ROMless Z8® Microcomputer

FEATURES

- □ Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.
- □ 256-byte register file, including 236 general-purpose registers, 3 I/O port registers, and 16 status and control registers.
- □ Vectored, priority interrupts for I/O, counter/timers, and UART.
- □ On-chip oscillator that accepts crystal or external clock drive.
- □ Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- □ Register Pointer so that short, fast instructions can access any one of the sixteen working-register groups.
- □ Single +5V power supply—all I/O pins TTL compatible.
- □ **12 and 16 MHz**
- □ CMOS process
- □ Standby modes—Halt and Stop

GENERAL DESCRIPTION

The Z86C91 is a CMOS ROMless version of the Z8 single-chip microcomputer. It offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcomputer to be used in low volume applications or where code flexibility is required.

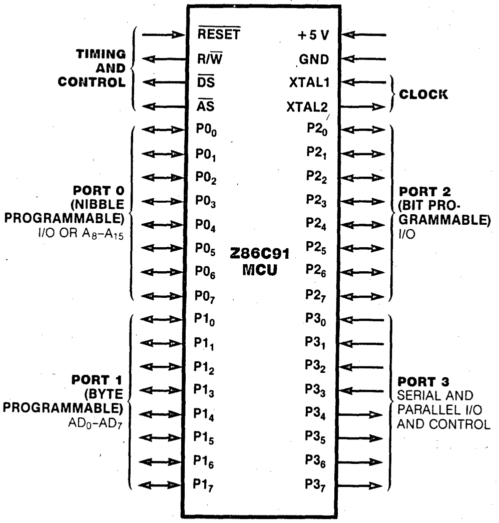


Figure 1. Pin Functions

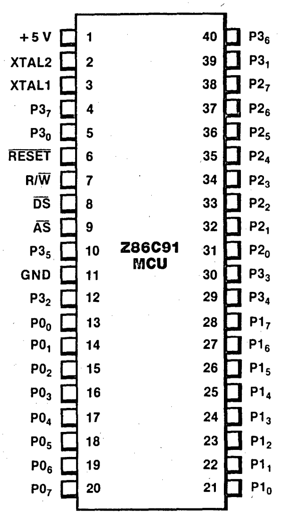


Figure 2a. 40-pin Dual-In-Line Package (DIP), Pin Assignments

The Z86C91 can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD_0-AD_7) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A_8-A_{15}.

Available address space can be doubled (up to 128K bytes) by programming bit 4 of Port 3 ($P3_4$) to act as a data memory select output ($\overline{DM}$). The two states of $\overline{DM}$ together with the 16 address outputs can define separate data and memory address spaces of up to 64K bytes each.

There are 256 bytes of RAM located on-chip and organized as a register file of 236 general-purpose registers, 16 control and status registers, and three I/O port registers. This register file can be divided into sixteen groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

The pin functions and the pin assignments of the Z86C91 package are illustrated in Figures 1 and 2.

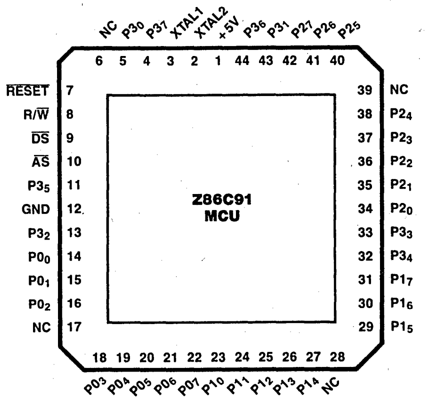


Figure 2b. 44-pin Chip Carrier, Pin Assignments

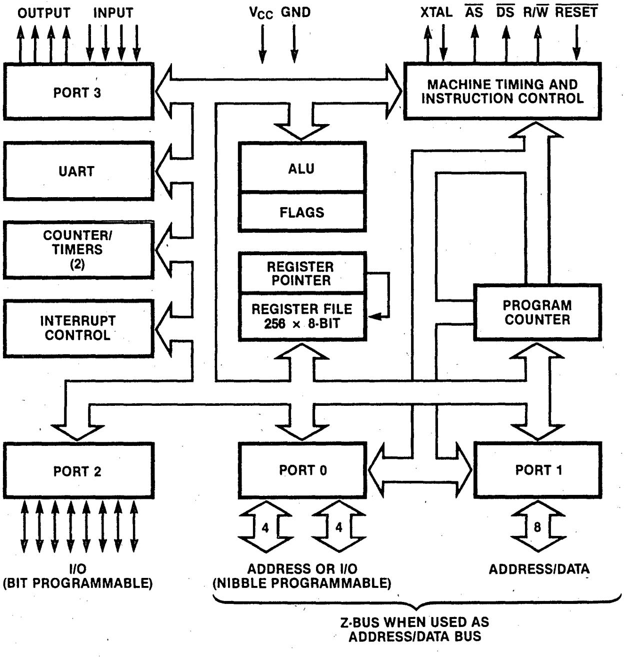


Figure 3. Functional Block Diagram

ARCHITECTURE

Architecture is characterized by a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features that are helpful in many applications.

Microcomputer applications demand powerful I/O capabilities. The Z86C91 fulfills this with 24 pins available for input and output. These lines are grouped into three ports of eight lines each and are configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address bus for interfacing external memory.

Three basic address spaces are available: program memory, data memory and the register file (internal). The 256-byte random-access register file is composed of 236 general-purpose registers, three I/O port registers, and 16 control and status registers.

To unburden the program from coping with real-time problems such as serial data communication and counting/timing, an asynchronous receiver/transmitter (UART) and two counter/timers with a large number of user-selectable modes are offered on-chip. Hardware support for the UART is minimized because one of the on-chip timers supplies the bit rate. Figure 3 shows the block diagram.

POWER DOWN INSTRUCTIONS

The Z86C91 has two instructions to reduce power consumption during standby operation. HALT turns off the processor and UART while the counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active.

When an interrupt occurs the processor resumes execution after servicing the interrupt. STOP turns off the clock to the entire Z86C91 and reduces the standby current to 10 microamps. The stop mode is terminated by reset, which causes the processor to restart the application program at address 12.

PIN DESCRIPTION

$\overline{\text{AS}}$. *Address Strobe* (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Addresses output via Port 1 for all external program or data memory transfers are valid at the trailing edge of $\overline{\text{AS}}$.

$\overline{\text{DS}}$. *Data Strobe* (output, active Low). Data Strobe is activated once for each external memory transfer.

$P0_0$-$P0_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$. *I/O Port Lines* (input/outputs, TTL-compatible). These 24 lines are divided into three 8-bit I/O ports that can be configured under program control for I/O or external memory interface (Figure 3).

$P1_0$-$P1_7$. *Address/Data Port* (bidirectional). Multiplexed address (A_0-A_7) and data (D_0-D_7) lines used to interface with program and data memory.

$\overline{\text{RESET}}$. *Reset* (input, active Low). $\overline{\text{RESET}}$ initializes the Z86C91. After RESET the MCU is in the extended memory mode. When $\overline{\text{RESET}}$ is deactivated, program execution begins from program location $000C_H$.

R/$\overline{\text{W}}$. *Read/Write* (output). R/$\overline{\text{W}}$ is Low when the Z86C91 is writing to external program or data memory.

XTAL1, XTAL2. *Crystal 1, Crystal 2* (time-base input and output). These pins connect a parallel-resonant crystal to the on-chip clock oscillator and buffer.

ADDRESS SPACES

Program Memory. The Z86C91 addresses 64K bytes of external program memory space (Figure 4).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at location $000C_H$ after a reset.

Data Memory. The Z86C91 can address 64K bytes of external data memory. External data memory may be included with or separated from the external program memory space. $\overline{\text{DM}}$, an optional I/O function that can be programmed to appear on pin $P3_4$, is used to distinguish between data and program memory space.

Register File. The 256-byte register file includes three I/O port registers (R0, R2, R3), 236 general-purpose registers (R4-R239) and 16 control and status registers (R240-R255). These registers are assigned the address locations shown in Figure 5.

Z86C91 instructions can access registers directly or indirectly with an 8-bit address field. This also allows short 4-bit register addressing using the Register Pointer (one of the control registers). In the 4-bit mode, the register file is divided into sixteen working-register groups, each occupying 16 contiguous locations (Figure 5). The Register Pointer addresses the starting location of the active working-register group (Figure 6).

Note: Register Bank E0-EF can only be accessed through working register and indirect addressing modes.

Stacks. Either the internal register file or the external data memory can be used for the stack. A 16-bit Stack Pointer (R254 and R255) is used for the external stack, which can reside anywhere in data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239).

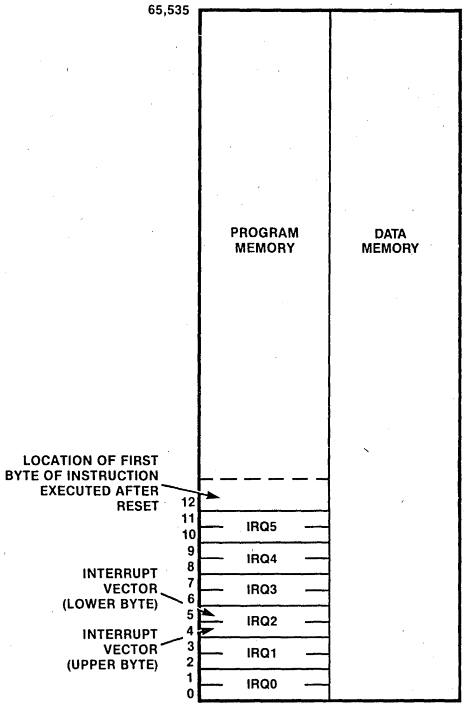

65,535
PROGRAM MEMORY
DATA MEMORY
LOCATION OF FIRST BYTE OF INSTRUCTION EXECUTED AFTER RESET
INTERRUPT VECTOR (LOWER BYTE)
INTERRUPT VECTOR (UPPER BYTE)
12
11
10
9
8
7
6
5
4
3
2
1
0
IRQ5
IRQ4
IRQ3
IRQ2
IRQ1
IRQ0

Figure 4. Z86C91 Program Memory Map

DECIMAL		HEX	IDENTIFIERS
255	STACK POINTER (BITS 7-0)	FF	SPL
254	STACK POINTER (BITS 15-8)	FE	SPH
253	REGISTER POINTER	FD	RP
252	PROGRAM CONTROL FLAGS	FC	FLAGS
251	INTERRUPT MASK REGISTER	FB	IMR
250	INTERRUPT REQUEST REGISTER	FA	IRQ
249	INTERRUPT PRIORITY REGISTER	F9	IPR
248	PORTS 0-1 MODE	F8	P01M
247	PORT 3 MODE	F7	P3M
246	PORT 2 MODE	F6	P2M
245	T0 PRESCALER	F5	PRE0
244	TIMER/COUNTER 0	F4	T0
243	T1 PRESCALER	F3	PRE1
242	TIMER/COUNTER 1	F2	T1
241	TIMER MODE	F1	TMR
240	SERIAL I/O	F0	SIO
239		EF	
	GENERAL-PURPOSE REGISTERS		
4		04	
3	PORT 3	03	P3
2	PORT 2	02	P2
1	PORT 1	01	P1
0	PORT 0	00	P0

Figure 5. The Register File

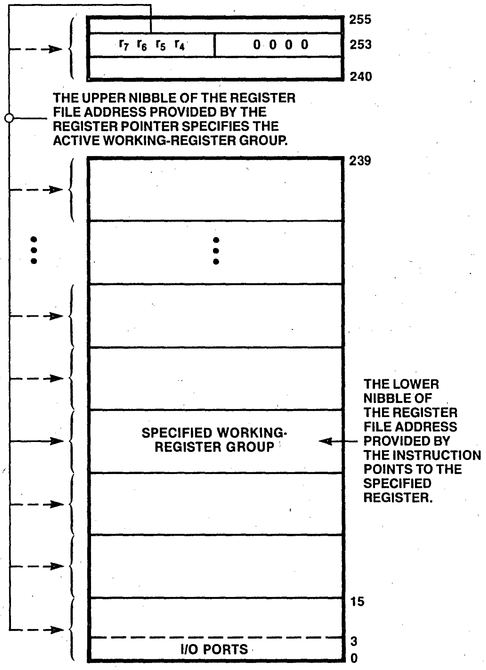

255
r_7 r_6 r_5 r_4
0 0 0 0
253
240
THE UPPER NIBBLE OF THE REGISTER FILE ADDRESS PROVIDED BY THE REGISTER POINTER SPECIFIES THE ACTIVE WORKING-REGISTER GROUP.
239
SPECIFIED WORKING-REGISTER GROUP
THE LOWER NIBBLE OF THE REGISTER FILE ADDRESS PROVIDED BY THE INSTRUCTION POINTS TO THE SPECIFIED REGISTER.
15
3
I/O PORTS
0

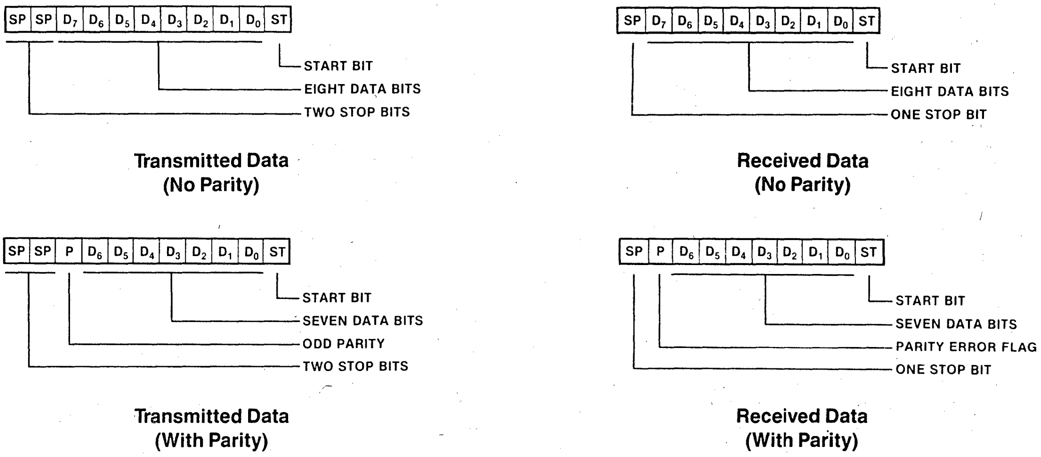
Figure 6. The Register Pointer

SERIAL INPUT/OUTPUT

Port 3 lines $P3_0$ and $P3_7$ can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer 0, with a maximum rate of 93.75K bits/second at 12 MHz.

The Z86C91 automatically adds a start bit and two stop bits to transmitted data (Figure 7). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth data bit is used as the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.



Transmitted Data (No Parity)

Received Data (No Parity)

Transmitted Data (With Parity)

Received Data (With Parity)

Figure 7. Serial Data Formats

COUNTER/TIMERS

The Z86C91 contains two 8-bit programmable counter/timers (T_0 and T_1), each driven by its own 6-bit programmable prescaler. The T_1 prescaler can be driven by internal or external clock sources; however, the T_0 prescaler is driven by the internal clock only.

The 6-bit prescalers can divide the input frequency of the clock source by any number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request—IRQ4 (T_0) or IRQ5 (T_1)—is generated.

The counters can be started, stopped, restarted to continue, or restarted from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode). The counters, but not the prescalers, can be read any time without disturbing their value or count mode.

The clock source for T_1 is user-definable; it can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input as an external clock, a trigger input that can be retriggerable or nonretriggerable, or as a gate input for the internal clock. The counter/timers can be programmably cascaded by connecting the T_0 output to the input of T_1. Port 3 line $P3_6$ also serves as a timer output (T_{OUT}) through which T_0, T_1 or the internal clock can be output.

I/O PORTS

The Z86C91 has 24 lines available for input and output. These lines are grouped into three ports of eight lines each and are configurable as input, output or address. Under software control, the ports can be programmed to provide address outputs, timing, status signals, serial I/O, and parallel I/O with or without handshake. All ports have active pull-ups and pull-downs compatible with TTL loads.

Port 1 is a dedicated Z-BUS® compatible memory interface. The operations of Port 1 are supported by the Address Strobe ($\overline{AS}$) and Data Strobe ($\overline{DS}$) lines, and by the Read/Write (R/$\overline{W}$) and Data Memory ($\overline{DM}$) control lines. The low-order program and data memory addresses (A_0-A_7) are output through Port 1 (Figure 8) and are multiplexed with data in/out (D_0-D_7). Instruction fetch and data memory read/write operations are done through this port.

Port 1 cannot be used as a register nor can a handshake mode be used with this port.

The Z86C91 wakes up with the 8 bits of Port 1 configured as address outputs for external memory. If more than eight address lines are required, additional lines can be obtained by programming Port 0 bits as address bits. The least-significant four bits of Port 0 can be configured to supply address bits A_8-A_{11} for 4K byte addressing or both nibbles of Port 0 can be configured to supply address bits A_8-A_{15} for 64K byte addressing.

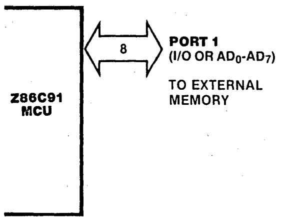


Figure 8. Port 1

Port 0 can be programmed as a nibble I/O port, or as an address port for interfacing external memory (Figure 9). When used as an I/O port, Port 0 can be placed under handshake control. In this configuration, Port 3 lines $P3_2$ and $P3_5$ are used as the handshake controls DAV_0 and RDY_0. Handshake signal assignment is dictated by the I/O direction of the upper nibble $P0_4$-$P0_7$.

For external memory references, Port 0 can provide address bits A_8-A_{11} (lower nibble) or A_8-A_{15} (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing.

Port 0 lines are configured as address lines A_8-A_{15} after a Reset. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

To permit the use of slow memory, an automatic wait mode of two oscillator clock cycles is configured for bus timing after each reset. The initialization routine could include reconfiguration to eliminate this extended timing mode.

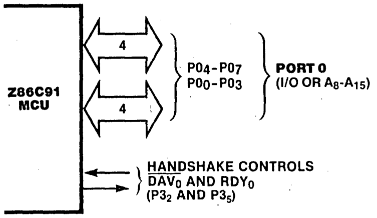


Figure 9. Port 0

Port 2 bits can be programmed independently as input or output (Figure 10). This port is always available for I/O operations. In addition, Port 2 can be configured to provide open-drain outputs.

Like Port 0, Port 2 may also be placed under handshake control. In this configuration, Port 3 lines $P3_1$ and $P3_6$ are used as the handshake controls lines $\overline{DAV_2}$ and RDY_2. The handshake signal assignment for Port 3 lines $P3_1$ and $P3_6$ is dictated by the direction (input or output) assigned to bit 7 of Port 2.

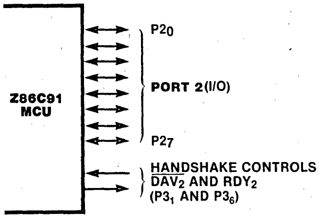


Figure 10. Port 2

Port 3 lines can be configured as I/O or control lines (Figure 11). In either case, the direction of the eight lines is fixed as four input ($P3_0$-$P3_3$) and four output ($P3_4$-$P3_7$). For serial I/O, lines $P3_0$ and $P3_7$ are programmed as serial in and serial out, respectively.

Port 3 can also provide the following control functions: handshake for Ports 0 and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}) and Data Memory Select ($\overline{DM}$).

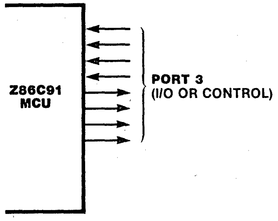


Figure 11. Port 3

INTERRUPTS

The Z86C91 allows six different interrupts from eight sources: the four Port 3 lines $P3_0$-$P3_3$, Serial In, Serial Out, and the two counter/timers. These interrupts are both maskable and prioritized. The Interrupt Mask register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.

All interrupts are vectored through locations in program memory. When an interrupt request is granted, an interrupt machine cycle is entered. This disables all subsequent interrupts, saves the Program Counter and status flags, and accesses the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. The Z86C91 takes 26 system clock cycles to enter an interrupt subroutine.

Polled interrupt systems are also supported. To accommodate a polled structure, any or all of the interrupt inputs can be masked and the Interrupt Request register polled to determine which of the interrupt requests needs service.

CLOCK

The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal or to any suitable external clock source (XTAL1 = Input, XTAL2 = Output).

The crystal source is connected across XTAL1 and XTAL2, using the recommended capacitance (C_L = 15 pf maximum) from each pin to ground. The specifications for the crystal are as follows:

- AT cut, parallel-resonant
- Fundamental type
- Series resistance, $R_S \leqslant 100\Omega$
- **16 MHz maximum**

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

dst	Destination location or contents
src	Source location or contents
cc	Condition code (see list)
@	Indirect address prefix
SP	Stack pointer (control registers 254-255)
PC	Program counter
FLAGS	Flag register (control register 252)
RP	Register pointer (control register 253)
IMR	Interrupt mask register (control register 251)

Assignment of a value is indicated by the symbol "←". For example,

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr(n)" is used to refer to bit "n" of a given location. For example,

dst (7)

refers to bit 7 of the destination operand.

Flags. Control Register R252 contains the following six flags:

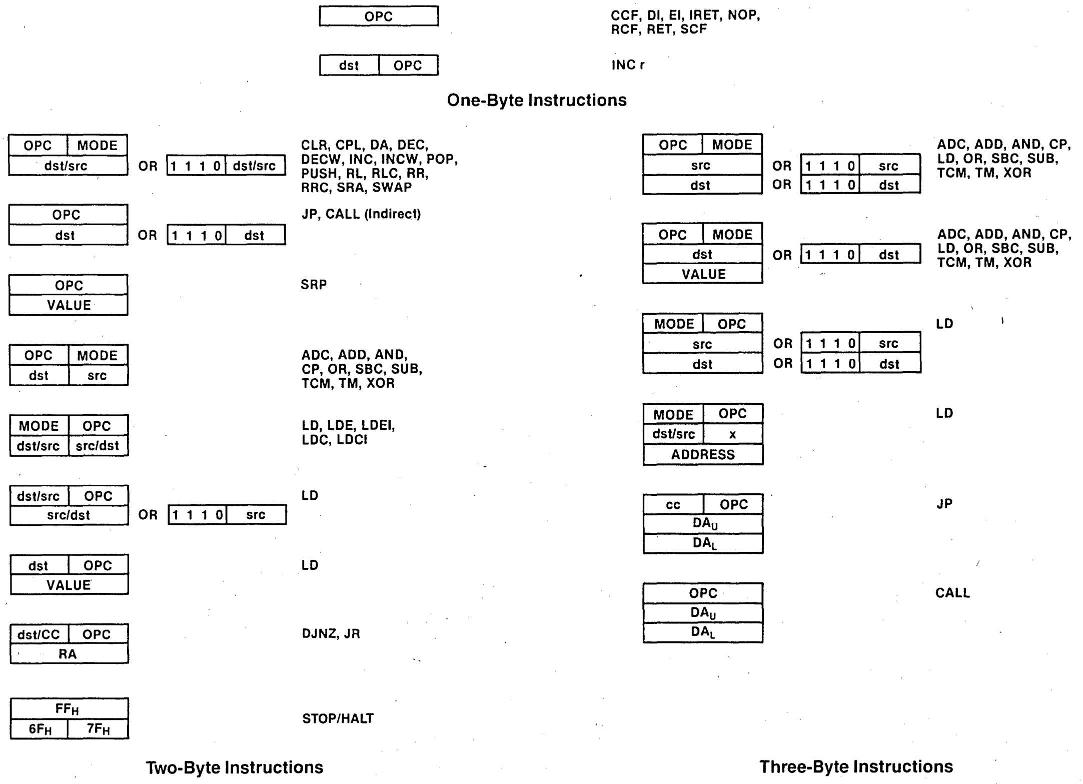
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Cleared to zero
1	Set to one
*****	Set or cleared according to operation
—	Unaffected
X	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always true	—
0111	C	Carry	C = 1
1111	NC	No carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000		Never true	—



One-Byte Instructions

Two-Byte Instructions

Three-Byte Instructions

Figure 12. Instruction Formats

INSTRUCTION SUMMARY

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
ADC dst,src dst ← dst + src + C	(Note 1)		1□	*	*	*	*	0	*
ADD dst,src dst ← dst + src	(Note 1)		0□	*	*	*	*	0	*
AND dst,src dst ← dst AND src	(Note 1)		5□	—	*	*	0	—	—
CALL dst SP ← SP − 2 @SP ← PC; PC ← dst	DA IRR		D6 D4	—	—	—	—	—	—
CCF C ← NOT C			EF	*	—	—	—	—	—
CLR dst dst ← 0	R IR		B0 B1	—	—	—	—	—	—
COM dst dst ← NOT dst	R IR		60 61	—	*	*	0	—	—
CP dst,src dst − src	(Note 1)		A□	*	*	*	*	—	—
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	—	—
DEC dst dst ← dst − 1	R IR		00 01	—	*	*	*	—	—
DECW dst dst ← dst − 1	RR IR		80 81	—	*	*	*	—	—
DI IMR (7) ← 0			8F	—	—	—	—	—	—
DJNZ r,dst r ← r − 1 if r ≠ 0 PC ← PC + dst Range: +127, −128	RA		rA r = 0 − F	—	—	—	—	—	—
EI IMR (7) ← 1			9F	—	—	—	—	—	—
HALT			7F	—	—	—	—	—	—
INC dst dst ← dst + 1	r R IR		rE r = 0 − F 20 21	—	*	*	*	—	—
INCW dst dst ← dst + 1	RR IR		A0 A1	—	*	*	*	—	—

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H

IRET
FLAGS ← @SP; SP ← SP + 1
PC ← @SP; SP ← SP + 2; IMR (7) ← 1
			BF	* * * * * *

JP cc,dst if cc is true PC ← dst	DA IRR		cD c = 0 − F 30	— — — — — — —
JR cc,dst if cc is true, PC ← PC + dst Range: +127, −128	RA		cB c = 0 − F	— — — — — — —
LD dst,src dst ← src	r	Im	rC	— — — — — — —
	r	R	r8	
	R	r	r9 r = 0 − F	
	r	X	C7	
	X	r	D7	
	r	Ir	E3	
	Ir	r	F3	
	R	R	E4	
	R	IR	E5	
	R	IM	E6	
	IR	IM	E7	
	IR	R	F5	
LDC dst,src dst ← src	r Irr	Irr r	C2 D2	— — — — — — —

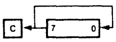
LDCI dst,src
dst ← src
r ← r + 1; rr ← rr +
1
	Ir
	Irr
		Irr
		Ir
			C3
			D3
				— — — — — — —

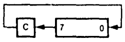
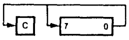
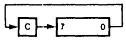
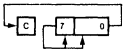
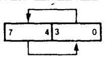
LDE dst,src dst ← src	r Irr	Irr r	82 92	— — — — — — —

LDEI dst,src
dst ← src
r ← r + 1; rr ← rr + 1
	Ir
	Irr
		Irr
		Ir
			83
			93
				— — — — — — —

NOP			FF	— — — — — — —
OR dst,src dst ← dst OR src	(Note 1)		4□	— * * 0 — —

POP dst
dst ← @SP;
SP ← SP + 1
	R
	IR
			50
			51
				— — — — — — —

PUSH src SP ← SP − 1; @SP ← src		R IR	70 71	— — — — — — —
RCF C ← 0			CF	0 — — — — — —
RET PC ← @SP; SP ← SP + 2			AF	— — — — — — —
RL dst 	R IR		90 91	* * * * — —

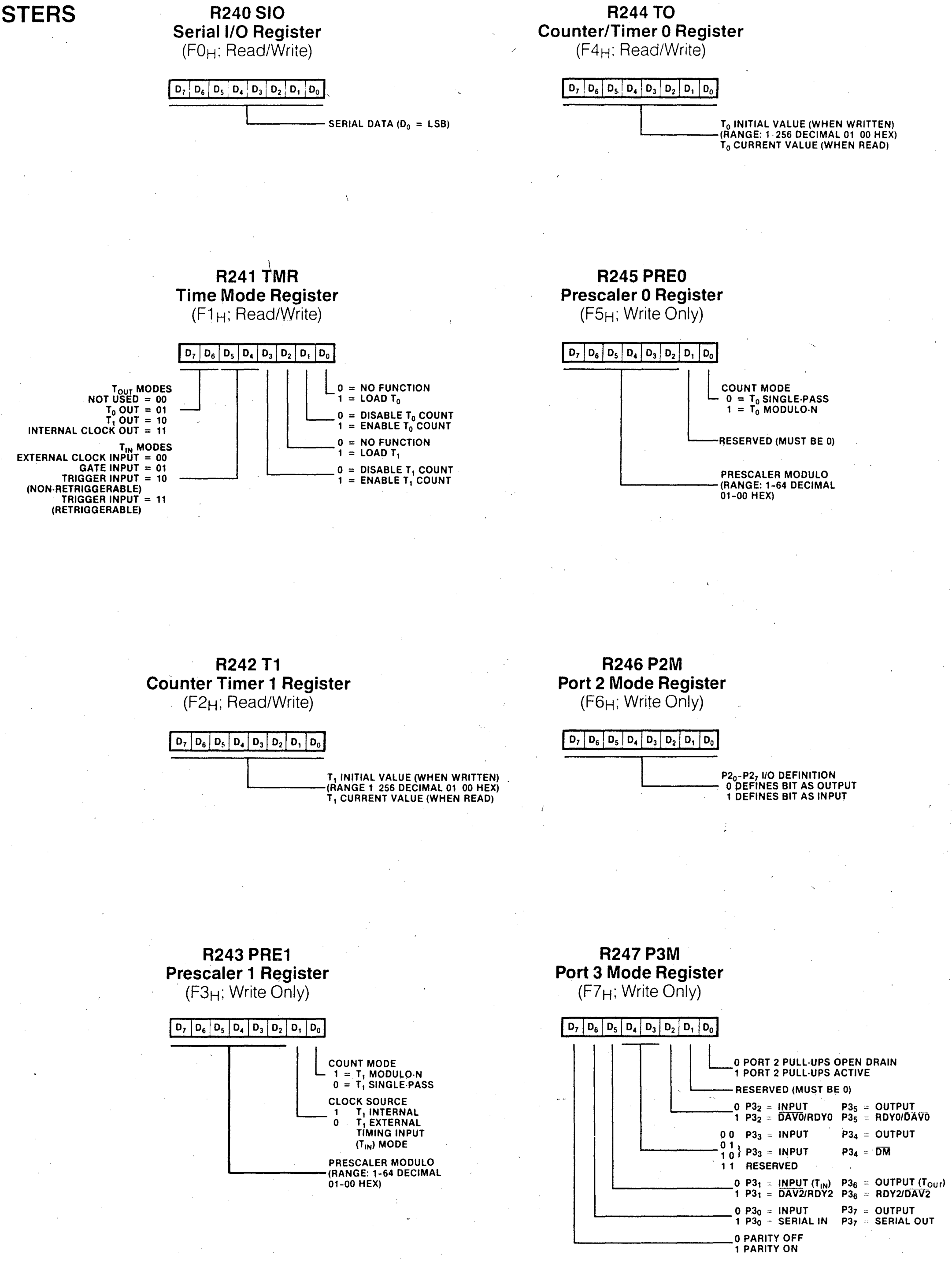
Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
RLC dst 	R IR		10 11	* * * * — —
RR dst 	R IR		E0 E1	* * * * — —
RRC dst 	R IR		C0 C1	* * * * — —
SBC dst,src dst ← dst ← src ← C	(Note 1)		3□	* * * * 1 *
SCF C ← 1			DF	1 — — — — —
SRA dst 	R IR		D0 D1	* * * 0 — —
SRP src RP ← src		Im	31	— — — — — — —
STOP			6F	— — — — — — —
SUB dst,src dst ← dst ← src	(Note 1)		2□	* * * * 1 *
SWAP dst 	R IR		F0 F1	X * * X — —
TCM dst,src (NOT dst) AND src	(Note 1)		6□	— * * 0 — —
TM dst,src dst AND src	(Note 1)		7□	— * * 0 — —
XOR dst,src dst ← dst XOR src	(Note 1)		B□	— * * 0 — —

NOTE: These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a □ in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Addr Mode dst	Addr Mode src	Lower Opcode Nibble
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

REGISTERS



R240 SIO
Serial I/O Register
(F0$_H$: Read/Write)

R244 TO
Counter/Timer 0 Register
(F4$_H$: Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0
T0 INITIAL VALUE (WHEN WRITTEN)
(RANGE: 1-256 DECIMAL 01 00 HEX)
T0 CURRENT VALUE (WHEN READ)

R241 TMR
Time Mode Register
(F1$_H$; Read/Write)

R245 PRE0
Prescaler 0 Register
(F5$_H$; Write Only)

R242 T1
Counter Timer 1 Register
(F2$_H$; Read/Write)

D7 D6 D5 D4 D3 D2 D1 D0
T1 INITIAL VALUE (WHEN WRITTEN)
(RANGE 1 256 DECIMAL 01 00 HEX)
T1 CURRENT VALUE (WHEN READ)

R246 P2M
Port 2 Mode Register
(F6$_H$; Write Only)

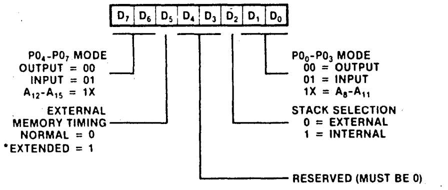
R243 PRE1
Prescaler 1 Register
(F3$_H$; Write Only)

R247 P3M
Port 3 Mode Register
(F7$_H$; Write Only)

D7 D6 D5 D4 D3 D2 D1 D0
0 PORT 2 PULL-UPS OPEN DRAIN
1 PORT 2 PULL-UPS ACTIVE
RESERVED (MUST BE 0)
0 P32 = INPUT P35 = OUTPUT
1 P32 = DAV0/RDY0 P35 = RDY0/DAV0
0 0 P33 = INPUT P34 = OUTPUT
0 1 / 1 0 } P33 = INPUT P34 = DM
1 1 RESERVED
0 P31 = INPUT (TIN) P36 = OUTPUT (TOUT)
1 P31 = DAV2/RDY2 P36 = RDY2/DAV2
0 P30 = INPUT P37 = OUTPUT
1 P30 = SERIAL IN P37 = SERIAL OUT
0 PARITY OFF
1 PARITY ON

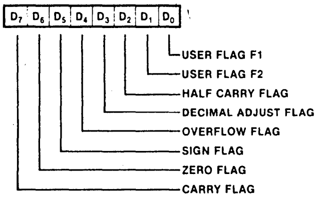
Figure 13. Control Registers

R248 P01M
Port 0 Mode Register
(F8H; Write Only)

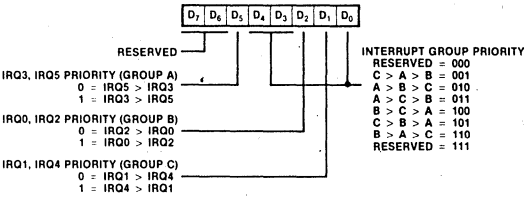


*ALWAYS EXTENDED TIMING AFTER RESET

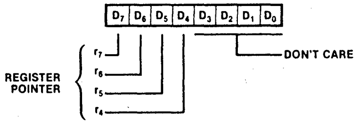
R252 FLAGS
Flag Register
(FCH; Read/Write)



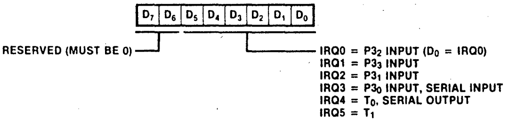
R249 IPR
Interrupt Priority Register
(F9H; Write Only)



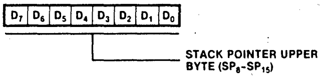
R253 RP
Register Pointer
(FDH; Read/Write)



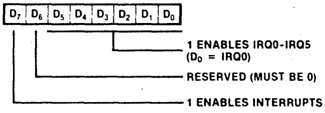
R250 IRQ
Interrupt Request Register
(FAH; Read/Write)



R254 SPH
Stack Pointer
(FEH; Read/Write)



R251 IMR
Interrupt Mask Register
(FBH; Read/Write)



R255 SPL
Stack Pointer
(FFH; Read/Write)

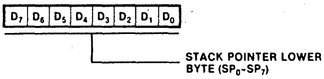
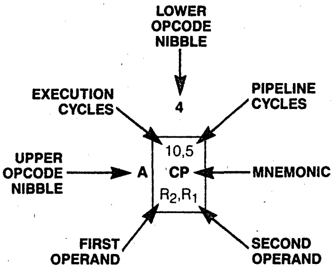


Figure 13. Control Registers (Continued)

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R_1	6.5 **DEC** IR_1	6.5 **ADD** r_1.r_2	6.5 **ADD** r_1.Ir_2	10.5 **ADD** R_2.R_1	10.5 **ADD** IR_2.R_1	10.5 **ADD** R_1.IM	10.5 **ADD** IR_1.IM	6.5 **LD** r_1.R_2	6.5 **LD** r_2.R_1	12/10.5 **DJNZ** r_1.RA	12/10.0 **JR** cc.RA	6.5 **LD** r_1.IM	12/10.0 **JP** cc.DA	6.5 **INC** r1	
1	6.5 **RLC** R_1	6.5 **RLC** IR_1	6.5 **ADC** r_1,r_2	6.5 **ADC** r_1,Ir_2	10.5 **ADC** R_2,R_1	10.5 **ADC** IR_2,R_1	10.5 **ADC** R_1,IM	10,5 **ADC** IR_1,IM	↓	↓	↓	↓	↓	↓	↓	
2	6.5 **INC** R_1	6,5 **INC** IR_1	6.5 **SUB** r_1.r_2	6,5 **SUB** r_1.Ir_2	10.5 **SUB** R_2.R_1	10,5 **SUB** IR_2.R_1	10.5 **SUB** R_1.IM	10,5 **SUB** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	
3	8.0 **JP** IRR_1	6.1 **SRP** IM	6.5 **SBC** r_1.r_2	6.5 **SBC** r_1.Ir_2	10.5 **SBC** R_2.R_1	10.5 **SBC** IR_2.R_1	10.5 **SBC** R_1.IM	10,5 **SBC** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	
4	8.5 **DA** R_1	8.5 **DA** IR_1	6.5 **OR** r_1.r_2	6.5 **OR** r_1.Ir_2	10.5 **OR** R_2.R_1	10.5 **OR** IR_2.R_1	10.5 **OR** R_1.IM	10.5 **OR** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	
5	10.5 **POP** R_1	10.5 **POP** IR_1	6.5 **AND** r_1.r_2	6.5 **AND** r_1.Ir_2	10.5 **AND** R_2.R_1	10.5 **AND** IR_2.R_1	10.5 **AND** R_1.IM	10.5 **AND** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	
6	6.5 **COM** R_1	6.5 **COM** IR_1	6.5 **TCM** r_1.r_2	6.5 **TCM** r_1.Ir_2	10.5 **TCM** R_2.R_1	10.5 **TCM** IR_2.R_1	10.5 **TCM** R_1.IM	10.5 **TCM** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	6.0 **STOP**
7	10/12.1 **PUSH** R_2	12/14.1 **PUSH** IR_2	6.5 **TM** r_1.r_2	6.5 **TM** r_1.Ir_2	10.5 **TM** R_2.R_1	10.5 **TM** IR_2.R_1	10.5 **TM** R_1.IM	10.5 **TM** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	7.0 **HALT**
8	10.5 **DECW** RR_1	10.5 **DECW** IR_1	12.0 **LDE** r_1.Irr_2	18.0 **LDEI** Ir_1.Irr_2					↓	↓	↓	↓	↓	↓	↓	6.1 **DI**
9	6.5 **RL** R_1	6.5 **RL** IR_1	12.0 **LDE** r_2.Irr_1	18.0 **LDEI** Ir_2.Irr_1					↓	↓	↓	↓	↓	↓	↓	6.1 **EI**
A	10.5 **INCW** RR_1	10.5 **INCW** IR_1	6.5 **CP** r_1.r_2	6.5 **CP** r_1.Ir_2	10.5 **CP** R_2.R_1	10.5 **CP** IR_2.R_1	10.5 **CP** R_1.IM	10.5 **CP** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	14.0 **RET**
B	6.5 **CLR** R_1	6.5 **CLR** IR_1	6.5 **XOR** r_1.r_2	6.5 **XOR** r_1.Ir_2	10.5 **XOR** R_2.R_1	10.5 **XOR** IR_2.R_1	10.5 **XOR** R_1.IM	10.5 **XOR** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	16.0 **IRET**
C	6.5 **RRC** R_1	6.5 **RRC** IR_1	12.0 **LDC** r_1.Irr_2	18.0 **LDCI** Ir_1.Irr_2				10.5 **LD** r_1.x.R_2	↓	↓	↓	↓	↓	↓	↓	6.5 **RCF**
D	6.5 **SRA** R_1	6.5 **SRA** IR_1	12.0 **LDC** r_2.Irr_1	18.0 **LDCI** Ir_2.Irr_1	20.0 **CALL*** IRR_1		20.0 **CALL** DA	10.5 **LD** r_2.x.R_1	↓	↓	↓	↓	↓	↓	↓	6.5 **SCF**
E	6.5 **RR** R_1	6.5 **RR** IR_1		6.5 **LD** r_1.IR_2	10.5 **LD** R_2.R_1	10.5 **LD** IR_2.R_1	10.5 **LD** R_1.IM	10.5 **LD** IR_1.IM	↓	↓	↓	↓	↓	↓	↓	6.5 **CCF**
F	8.5 **SWAP** R_1	8.5 **SWAP** IR_1		6.5 **LD** Ir_1.r_2		10.5 **LD** R_2.IR_1			↓	↓	↓	↓	↓	↓	↓	6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

NOTE: The blank areas are not defined.

*2-byte instruction; fetch cycle appears as a 3-byte instruction

ABSOLUTE MAXIMUM RATINGS

Voltages on all pins except $\overline{\text{RESET}}$
with respect to GND . . . . −0.3V to +7.0V
Operating Ambient
Temperature. . . . . .See Ordering Information
Storage Temperature . . . . −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- $+4.5V \leq V_{CC} \leq +5.5V$
- GND = 0V
- 0°C $\leq T_A \leq$ +70°C for S (Standard temperature)
- −40°C $\leq T_A \leq$ +100°C for E (Extended temperature)

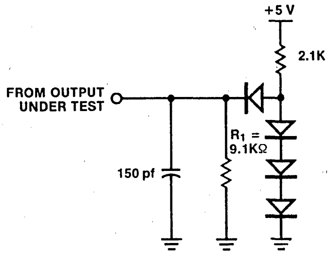


Figure 14. Test Load 1

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	3.8		V_{CC}	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	−0.3		0.8	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{RH}	Reset Input High Voltage	3.8		V_{CC}	V	
V_{RL}	Reset Input Low Voltage	−0.3		0.8	V	
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -250\,\mu A$
V_{OH}	**Output High Voltage**	**V_{CC} -100mV**			**V**	**$I_{CC} = -100\mu A$**
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = +2.0$ mA
I_{IL}	Input Leakage	−10		10	μA	$V_{IN} = 0V, 5.25V$
I_{OL}	Output Leakage	−10		10	μA	$V_{IN} = 0V, 5.25V$
I_{IR}	Reset Input Current			−50	μA	$V_{CC} = +5.25V, V_{RL} = 0V$
I_{CC}	Supply Current			30	mA	All outputs and I/O pins floating
I_{CC1}	Standby Current		**5**		mA	Halt Mode
I_{CC2}	Standby Current			**10**	μA	Stop Mode

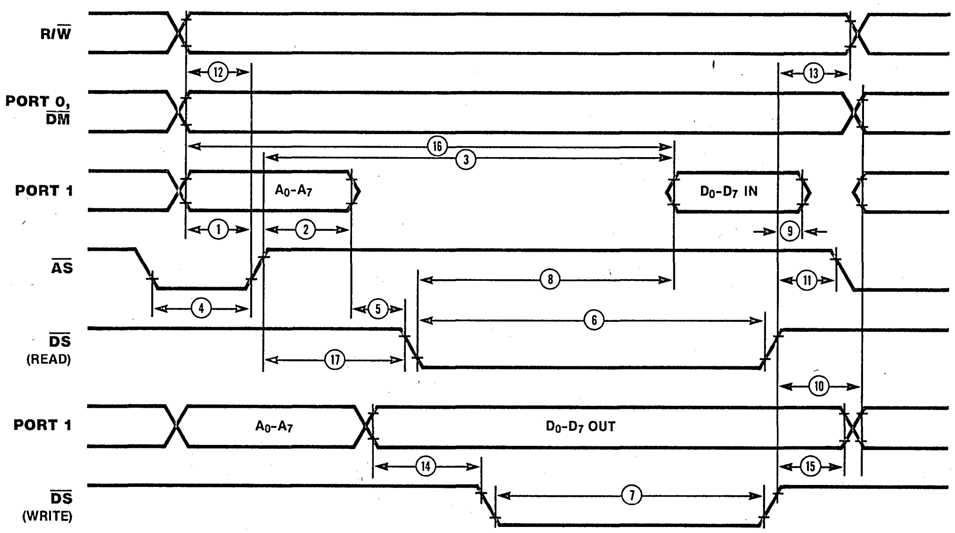


Figure 15. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing

			12 MHz		16 MHz		
Number	Symbol	Parameter	Min	Max	Min	Max	Notes
1	TdA(AS)	Address Valid to $\overline{\text{AS}}$ ↑Delay	35		20		2,3
2	TdAS(A)	$\overline{\text{AS}}$ ↑ to Address Float Delay	45		30		2,3
3	TdAS(DR)	$\overline{\text{AS}}$ ↑ to Read Data Required Valid		220		180	1,2,3
4	TwAS	$\overline{\text{AS}}$ Low Width	55		35		2,3
5	TdAz(DS)	Address Float to $\overline{\text{DS}}$ ↓	0		0		
6	TwDSR	$\overline{\text{DS}}$ (Read) Low Width	185		135		1,2,3
7	TwDSW	$\overline{\text{DS}}$ (Write) Low Width	110		80		1,2,3
8	TdDSR(DR).	$\overline{\text{DS}}$ ↓ to Read Data Required Valid		130		75	1,2,3
9	ThDR(DS)	Read Data to $\overline{\text{DS}}$ ↑ Hold Time	0		0		2,3
10	TdDS(A)	$\overline{\text{DS}}$ ↑ to Address Active Delay	45		35		2,3
11	TdDS(AS)	$\overline{\text{DS}}$ ↑ to $\overline{\text{AS}}$ ↓Delay	55		25		2,3
12	TdR/W(AS)	R/$\overline{\text{W}}$ Valid to $\overline{\text{AS}}$ ↑ Delay	30		20		2,3
13	TdDS(R/W)	$\overline{\text{DS}}$ ↑ to R/$\overline{\text{W}}$ Not Valid	35		25		2,3
14	TdDW(DSW)	Write Data Valid to $\overline{\text{DS}}$ (Write) ↓ Delay	35		25		2,3
15	TdDS(DW)	$\overline{\text{DS}}$ ↑ to Write Data Not Valid Delay	35		25		2,3
16	TdA(DR)	Address Valid to Read Data Required Valid		255		200	1,2,3
17	TdAS(DS)	$\overline{\text{AS}}$ ↑ to $\overline{\text{DS}}$ ↓ Delay	55		40		2,3

NOTES:
1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle time dependent characteristics table.
4. 16 MHz timing is preliminary and subject to change.

* All units in nanoseconds (ns).
† Test Load 1
° All timing references use 2.0V for a logic "1" and 0.8V for a logic "0".

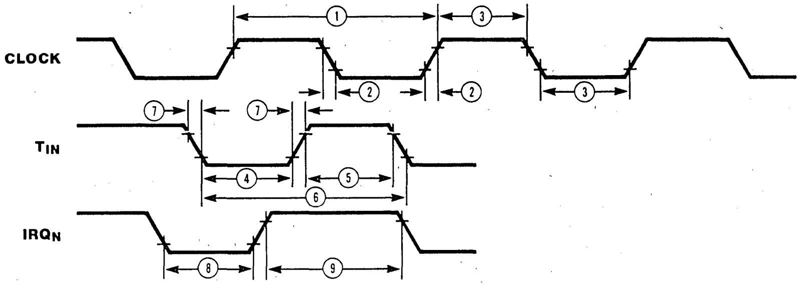


Figure 16. Additional Timing

AC CHARACTERISTICS

Additional Timing Table

Number	Symbol	Parameter	8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Notes
1	TpC	Input Clock Period	125	1000	83	1000	62.5	1000	1
2	TrC,TfC	Clock Input Rise and Fall Times		25		15		10	1
3	TwC	Input Clock Width	37		70		21		1
4	TwTinL	Timer Input Low Width	100		70		50		2
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC		2
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		2
7	TrTin,TfTin	Timer Input Rise and Fall Times		100		100		100	2
8A	TwIL	Interrupt Request Input Low Time	100		70		50		2,4
8B	TwIL	Interrupt Request Input Low Time	3TpC		3TpC		3TpC		2,5
9	TwIH	Interrupt Request Input High Time	3TpC		3TpC		3TpC		2,3

NOTES:
1. Clock timing references use 3.8V for a logic "1" and 0.8V for a logic "0".
2. Timing references use 2.0V for a logic "1" and 0.8V for a logic "0".
3. Interrupt request via Port 3.
4. Interrupt request via Port 3 ($P3_1$-$P3_3$)
5. Interrupt request via Port 3 ($P3_0$)
6. 16 MHz timing is preliminary and subject to change.
* Units in nanoseconds (ns).

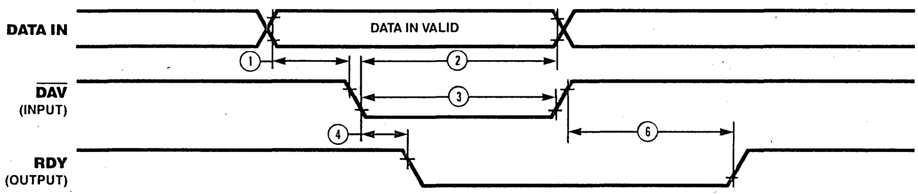


Figure 17a. Input Handshake Timing

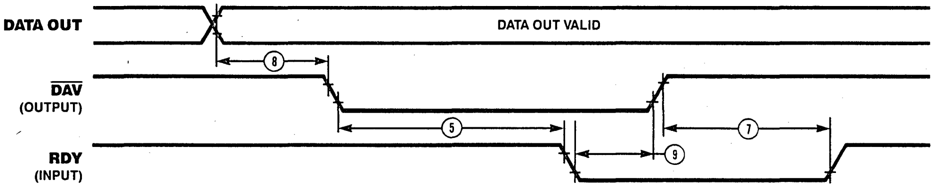


Figure 17b. Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing

Number	Symbol	Parameter	8, 12, 16 MHz Min	Max	Notes
1	TsDI(DAV)	Data In Setup Time	0		
2	ThDI(DAV)	Data In Hold Time	145		
3	TwDAV	Data Available Width	110		
4	TdDAVIf(RDY)	DAV ↓ Input to RDY ↓ Delay		115	1,2
5	TdDAVOf(RDY)	DAV ↓ Output to RDY ↓ Delay	0		1,3
6	TdDAVIr(RDY)	DAV ↑ Input to RDY ↑ Delay		115	1,2
7	TdDAVOr(RDY)	DAV ↑ Output to RDY ↑ Delay	0		1,3
8	TdDO(DAV)	Data Out to DAV ↓ Delay	Tpc		1
9	TdRDY(DAV)	Rdy ↓ Input to DAV ↑ Delay	0	130	1

NOTES:
1. Test load 1
2. Input handshake
3. Output handshake
4. 16 MHz timing is preliminary and subject to change.
† All timing references use 2.0V for a logic "1" and 0.8V for a logic "0".
* Units in nanoseconds (ns).