ZILOG

PRELIMINARY PRODUCT SPECIFICATION

Z86L06

LOW VOLTAGE CMOS Z8® CCP™ CONSUMER CONTROLLER PROCESSOR

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FEATURES

- 8-bit CMOS microcontroller
- 18-pin DIP package
- Low cost
- 2.0 to 3.6 volt operating range
- Two standby modes - STOP and HALT
- 14 input/output lines (two with comparator inputs)
- 1 Kbyte of ROM
- 124 bytes of RAM
- Four expanded registers (file control registers)
- Two programmable 8-bit Counter/Timers
- High current output: (1)-7 ma source at 2 volts, (1)-10 ma sink at 2 volts.
- 6-bit programmable prescaler
- Six vectored, priority interrupts from five different sources
- Clock speed 8 MHz @ 2.0V
- Watch-Dog/Power-On-Reset Timer
- Two comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC, or external clock drive.
- Low EMI noise mode
- From 0°C to +70°C operation
- Brown-Out protection
- Auto Latches

GENERAL DESCRIPTION

The Z86L06 low voltage CCP (Consumer Controller Processor) is a member of the Z8 single-chip microcontroller family with 1 Kbyte of ROM, and 124 bytes of general-purpose RAM. The device is housed in an 18-pin DIP, and is manufactured in low voltage CMOS technology. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. Now with the low voltage process this same processor may operate down to 2.0 volts.

The Z86L06 architecture is based on Zilog's 8-bit microcontroller core with the addition of an Expanded Register File which allows access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many consumer, industrial, automotive, and advanced scientific applications.

The device applications demand powerful I/O capabilities. The CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 124 bytes of general-purpose registers, two I/O port registers and fifteen control and status registers. The Expanded Register File consists of three control registers.

With powerful peripheral features such as on-board comparators, counter/timers, watch-dog timer, and serial peripheral interface, the Z86L06 meets the needs for most sophisticated controller applications (Figure 1).

GENERAL DESCRIPTION (Continued)

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.:
B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

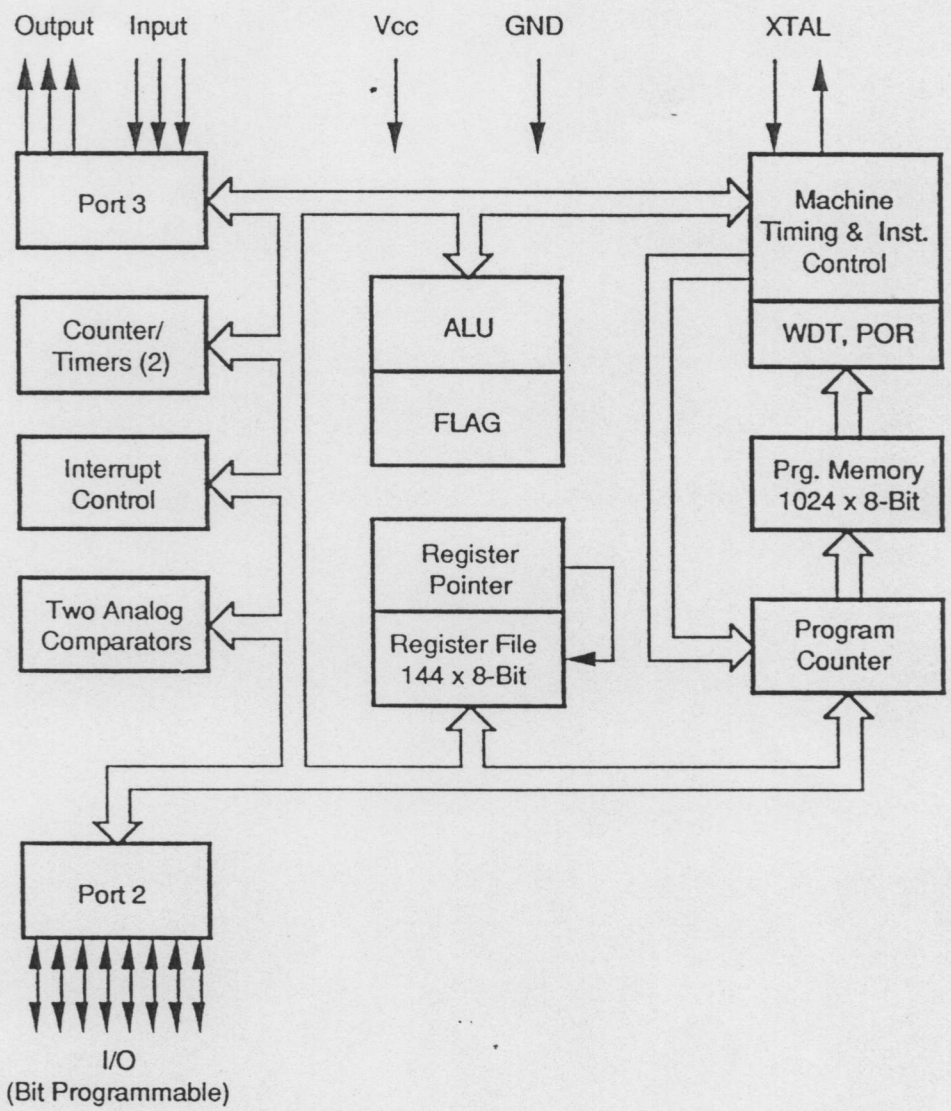


Figure 1. Functional Block Diagram

PIN DESCRIPTION

Table 1. Pin Identification

No	Symbol	Function	Direction
1-4	P24-7	Port 2 pin 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-3	Port 3 pin 1, 2, 3	Fixed Input
11-13	P34-6	Port 3 pin 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-3	Port 2 pin 0, 1, 2, 3	In/Output

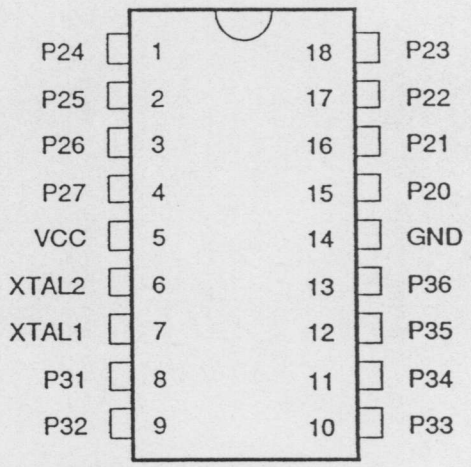


Figure 2. Pin Configuration

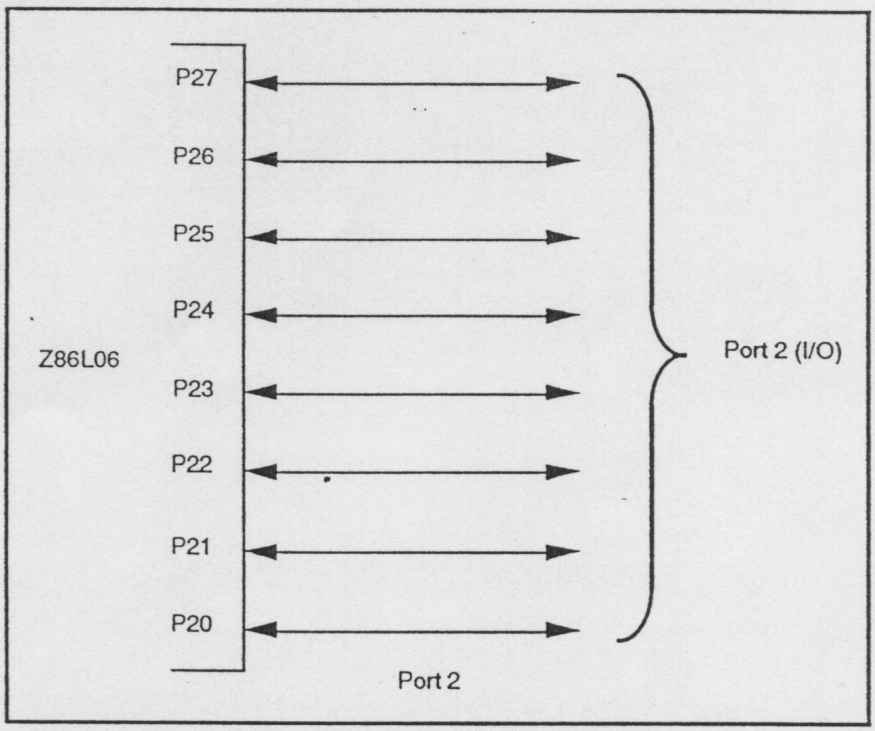
PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 P20-P27. Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open drain (Figure 3).

Port 3 P31-P36. Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32 and P33 are standard CMOS inputs and pins P34, P35, and P36 are push-pull outputs. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (bit 1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). (Figures 4a and 4b).



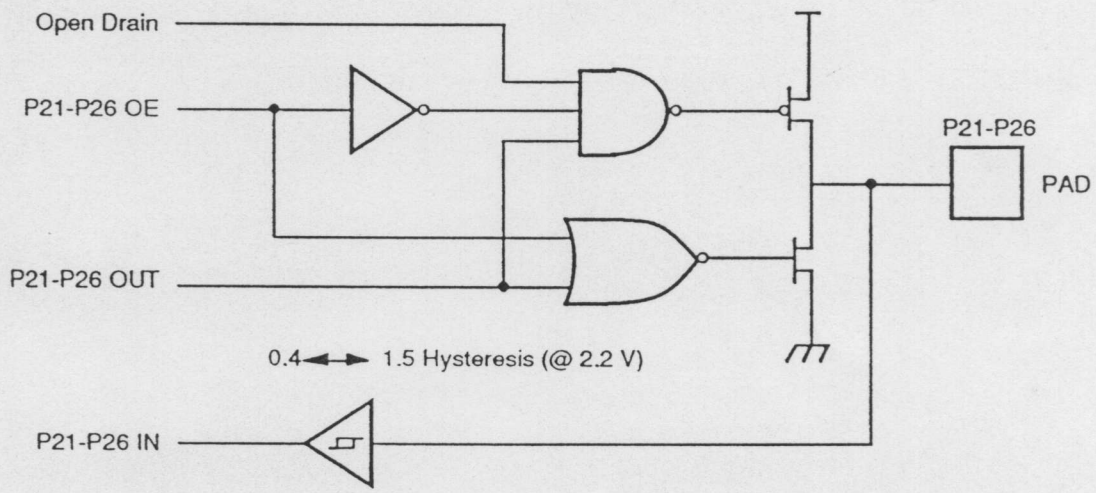
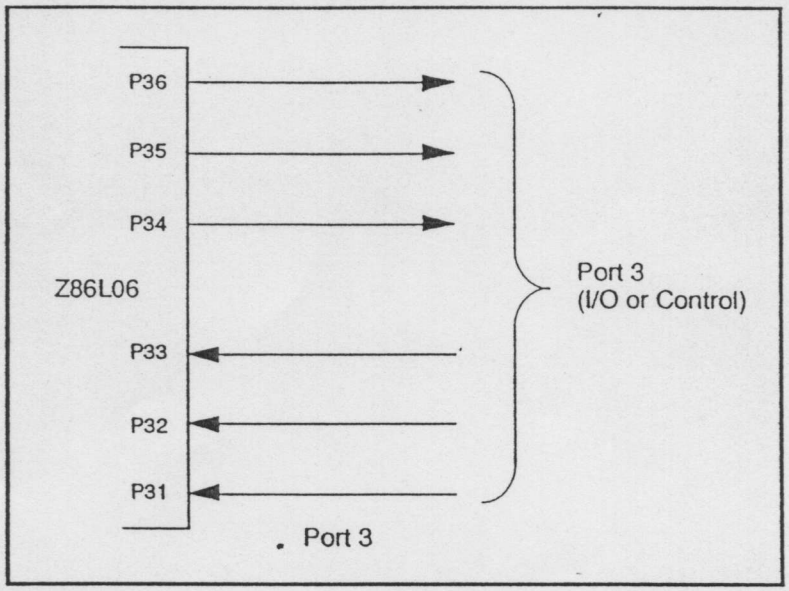


Figure 3. Port 2 Configuration



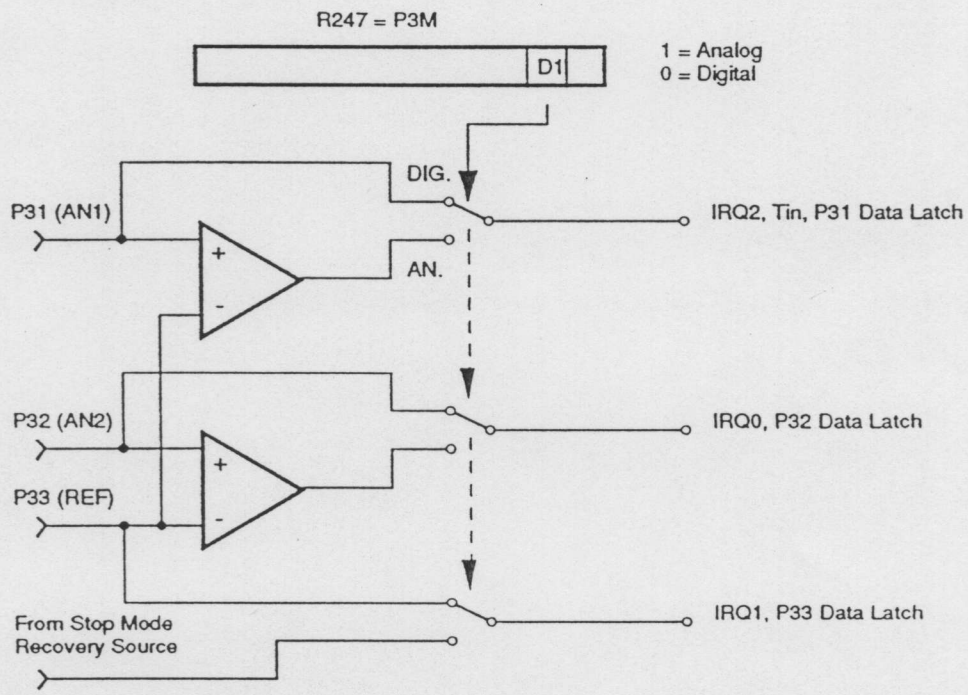


Figure 4a. Port 3 Configuration

PIN FUNCTIONS (Continued)

PORT Configuration Register (PCON). The Port Configuration Register (PCON) configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 5). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35 (Figure 4b), and a 0 releases the Port to its standard I/O configuration. Bits 5 and 6 of this register configure Ports 2 and 3, respectively, for low EMI operation. A 1 in these locations configures the port for standard operation, and a 0 configures the port for low EMI operation. Finally, bit 7 of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low noise drive. Note that the PCON Register is reset upon the occurrence of a STOP Mode Recovery, any WDT Reset, and Power-On Reset.

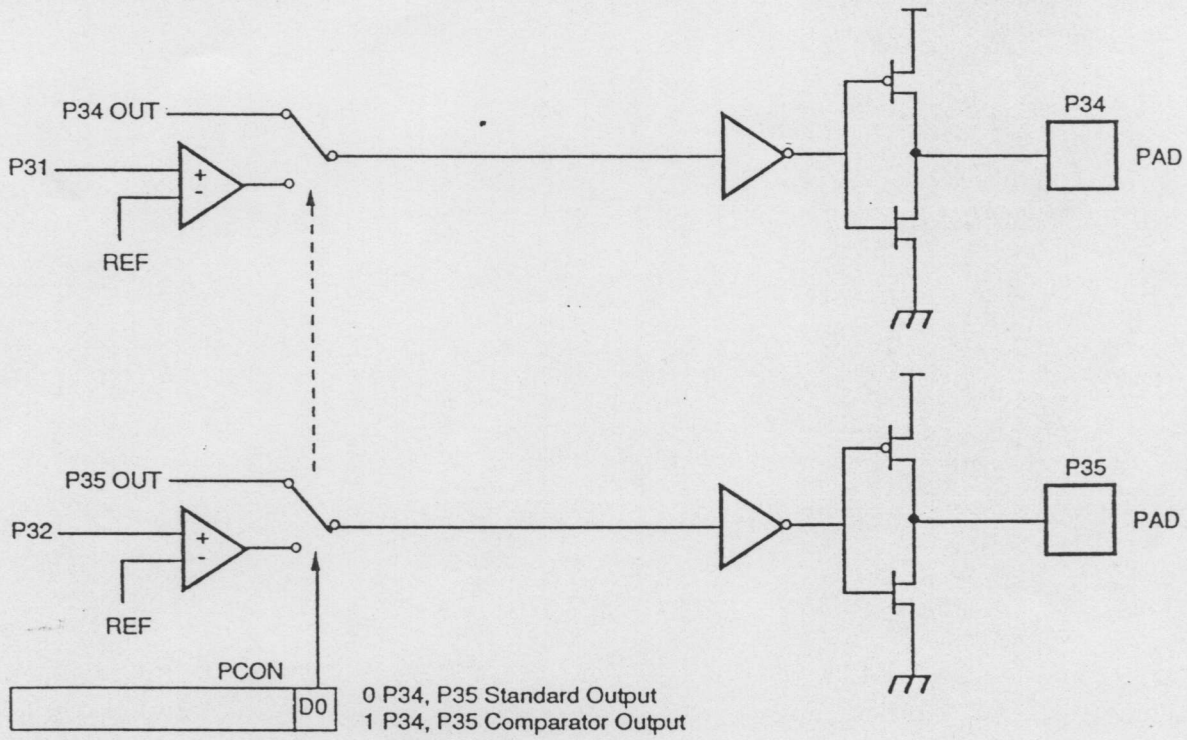
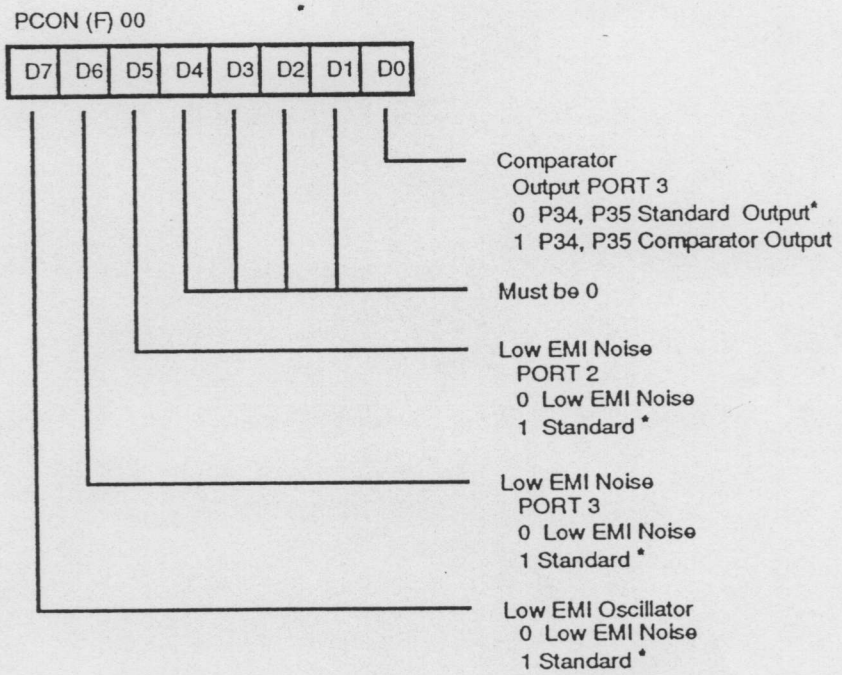


Figure 4b. Port 3 Configuration

Low EMI Option. The Z86L06 can be programmed to operate in a low EMI emission mode by the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- Low current consumption during the HALT mode.
- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 800 Ohms (typical).
- Internal SLCK/TCLK operation limited to a maximum of 4 MHz (25 ns cycle time).

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. The internal P33 register and its corresponding IRQ1 is connected to the STOP Mode Recovery source selected by the SMR. In this mode, any of the STOP Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 source (Figure 5).



* Default setting from STOP Mode Recovery, Power-On Reset, and any WDT Reset.

Figure 5. PORT Configuration Register (PCON)