



# Z89332

## DIGITAL TELEVISION CONTROLLER

### FEATURES

Device	ROM (KW)	RAM* (Words)	PWM (8-Bit)	Voltage Range
Z89332	24	640	8	4.5 to 5.5V

**Note:** \*General-Purpose

- 42-Pin SDIP and 48-Pin Ceramic Packages with 42- to 48-Pin Adapter Socket
- 0°C to +70°C Temperature Range

- Fully Customized Character Set
- Character-Control and Closed-Caption Modes
- Keypad User Control
- TV Tuner Serial Interface
- Direct Video Signals
- Speed: 12 MHz

### GENERAL DESCRIPTION

The Z89332 Digital Television Controller is designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The television controller features a Z89C00 RISC processor core that controls the on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character-Control Mode and the Closed-Caption Mode. The Character-Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes. Closed-caption text can be decoded directly from the composite video signal and displayed on-screen with the assistance of the processor's digital signal processing (DSP) capabilities.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position off-set delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tuning adjustments, may be accessed through the industry-standard I<sup>2</sup>C port.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

#### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

GENERAL DESCRIPTION (Continued)

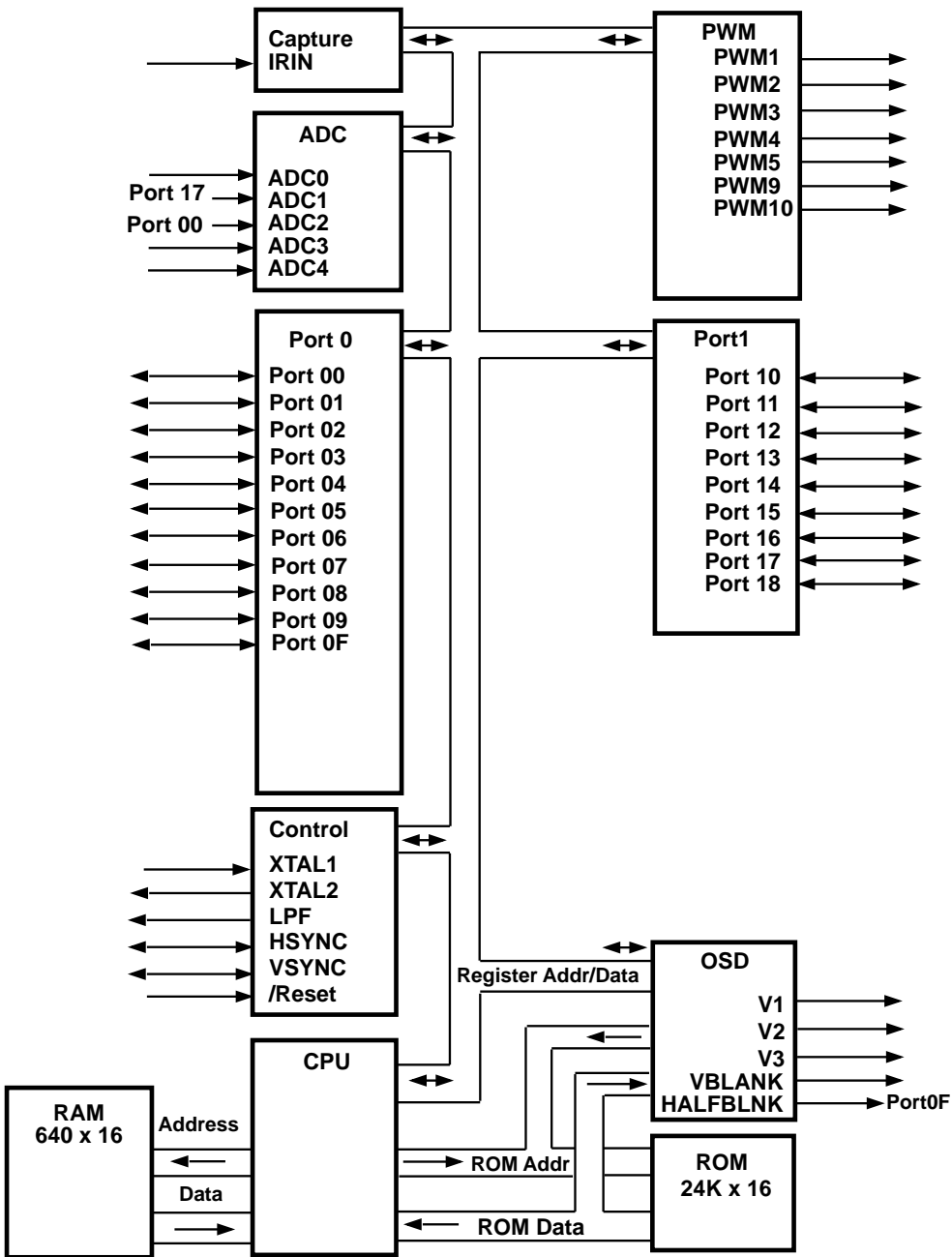
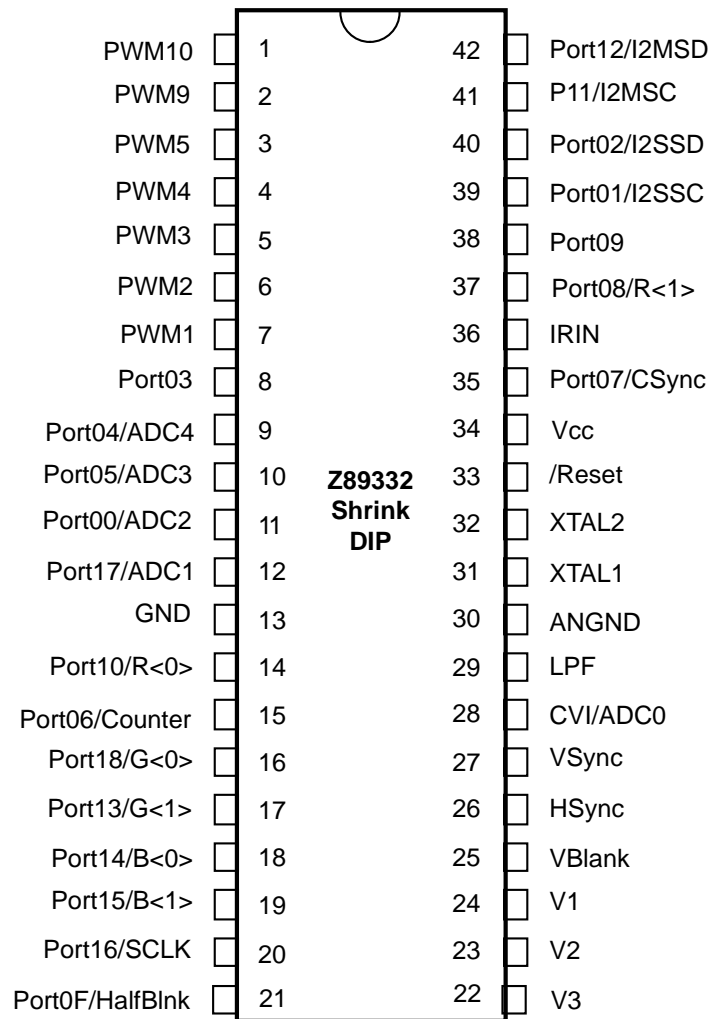


Figure 1. Functional Block Diagram

## PIN DESCRIPTION



**Figure 2. 42-Pin Shrink DIP and 48-Pin Ceramic Pin Configurations with 42- to 48-Pin Adapter Footprint**

**Table 1. 42-Pin SDIP Pin Identification**

Name	Function	Z89332	Direction	Reset	Notes
V <sub>CC</sub>	+ 5 Volts	34	PWR	–	
GND	0 Volts	13, 30	PWR	–	
IRIN	Infrared Remote Capture Input	36	I	I	
ADC[4:0]	4-Bit A/D Converter Input	9, 10, 11, 12, 28	AI	I	
PWM10, PWM9	14-Bit Pulse Width Modulator Output	1, 2	O	O	
PWM[5:1]	8-Bit Pulse Width Modulator Output	3, 4, 5, 6, 7	OD/O*	O	
Port0[F:0]	Bit Programmable Input/Output Ports	21, -, -, -, -, -, 38, 37, 35, -, -, 15, 8, 40, 39, 11	B	I	[1]
Port1[8:0]	Bit Programmable Input/Output Ports	16, 12, 20, 19, 18, 17, 42, 41, 14	B	I	
SCL	I <sup>2</sup> C Clock I/O	39 or 41	BOD		[2]
SCD	I <sup>2</sup> C Data I/O	40 or 42	BOD		[3]
XTAL1	Crystal Oscillator Input	31	AI	I	
XTAL2	Crystal Oscillator Output	32	AO	O	
LPF	Loop Filter	29	AB	O	
HSYNC	H_SYNC	26	B	I	
VSNC	V_SYNC	27	B	I	
/Reset	Device Reset	33	I	I	
V[3:1]	OSD Video Output Typically Drive B, G, and R Outputs	22, 23, 24	O	O	
Blank	OSD Blank Output	25	O	O	
HalfBlank	OSD Half-Blank Outpu	21	O		[4]
RGB Digital Outputs	R[1:0], G[1:0], and B[1:0] Outputs of the RGB Matrix	37, 14, 17, 16, 19, 18	O		[5]
SCLK	Internal Processor SCLK	20	O		[6]

**Notes:**

- 1) Port 0 [E:A] is not available on the 42-pin SDIP version.
- 2) SCL I/O pin is shared with Port 0 or Port 11.
- 3) SCD I/O pin is shared with Port 02 or Port 12.
- 4) Half Blank output is a function shared with Port 0F.
- 5) Digital RGB outputs and the internal SCLK are shared with Port 1 [5:0].
- 6) Internal processor SCLK is shared with Port 16.

\* PWM outputs are push/pull in Revision Z89332EA and later.

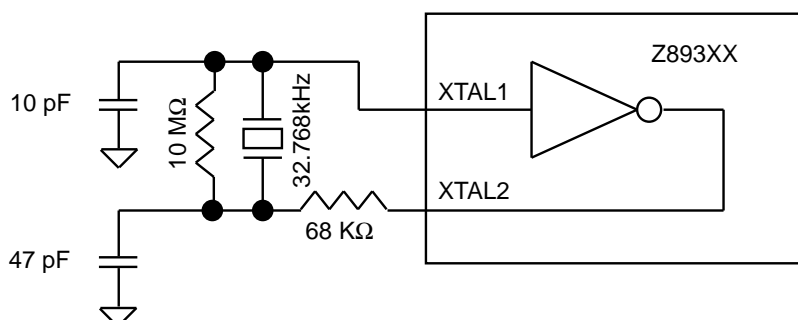
## V1, V2, V3 ANALOG OUTPUT

Specifications  $V_{CC} = 5.25V$  and  $V_{CC} = 4.75V$

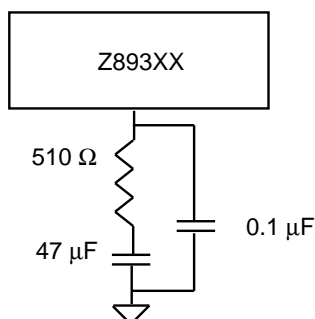
$V_{CC} = 5.25V$	Condition	Limit
Output Voltage	Bit = 11	$4.2V \pm 0.4V$
	Bit = 10	45% – 0.15V to 55% of actual data = 11 value
	Bit = 01	$0.60V \pm 0.4V$
	Bit = 00	74% to 89% of actual data = 11 value
Setting Time	70% of DC Level, 10 pF Load	< 50 nsec

$V_{CC} = 4.75V$	Condition	Limit
Output Voltage	Bit = 11	$3.6V \pm 0.4V$
	Bit = 10	45% – 0.15V to 55% of actual data = 11 value
	Bit = 01	$0.60V \pm 0.4V$
	Bit = 00	74% to 89% of actual data = 11 value
Setting Time	70% of DC Level, 10 pF Load	< 50 nsec



**Figure 3. 32K Oscillator Recommended Circuit**



**Figure 4. Recommended Low Pass Filter Circuit**

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
$V_{CC}$	Power Supply Voltage	0	7	V	
$V_{ID}$	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Digital Inputs
$V_{IA}$	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Analog Inputs (A/D0...A/D4)
$V_O$	Output Voltage	-0.3	$V_{CC} + 0.3$	V	All Push-Pull Digital Output
$V_O$	Output Voltage	-0.3	$V_{CC} + 8$		Open-Drain PWM Outputs (PWM1...PWM8)
$V_O$	Output Voltage	-0.3	$V_{CC} + 0.3$	V	Push/Pull PWM Outputs (PWM1...PWM8) = Z89332EA and Later Revisions
$I_{OH}$	Output Current High		-10	mA	One Pin
$I_{OH}$	Output Current High		-100	mA	All Pins
$I_{OL}$	Output Current Low		20	mA	One Pin
$I_{OL}$	Output Current Low		200	mA	All Pins
$T_A$	Operating Temperature	0	70	°C	
$T_A$	Storage Temperature	-65	150	°C	

## DC CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{V}$  to  $+5.5\text{V}$ ;  $F_{OSC} = 32.768\text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units	Conditions
$V_{IL}$	Input Voltage Low	0	$0.2 V_{CC}$	0.4	V	
$V_{IH}$	Input Voltage High	$0.7 V_{CC}$	$V_{CC}$	3.6	V	
$V_{PU}$	Max. Pull-Up Voltage		$V_{CC} + 0.3$		V	All Pins
$V_{OL}$	Output Voltage Low		0.4	0.16	V	@ $I_{OL} = 1\text{ mA}$
$V_{OH}$	Output Voltage High	$V_{CC} - 0.4$		4.75	V	@ $I_{OL} = 0.75\text{ mA}$
$V_{XL}$	Input Voltage XTAL1 Low		$0.3 V_{CC}$	1.0	V	External Clock
$V_{XH}$	Input Voltage XTAL1 High	$V_{CC} - 2.0$		3.5	V	Generator Driven
$V_{HY}$	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
$I_{IR}$	Reset Input Current		150	90	$\mu\text{A}$	$V_{RL} = 0\text{V}$
$I_{IL}$	Input Leakage	-3.0	3.0	0.01	$\mu\text{A}$	@ 0V and $V_{CC}$
$I_{CC}$	Supply Current		100	60	mA	
$I_{ADC}$	Input Current		0.5		mA	AE Revision
$I_{ADC}$	Input Current		10		$\mu\text{A}$	CC,CA,EA & Later Rev.

### Notes:

A) The Z89332 should not be operated for extended periods with the crystal oscillator disconnected, except in the defined power-down modes. In the event that the Z89332 is operated with the oscillator disconnected, the device may draw higher than typical current.

B) Each line of the on-screen display can consist of any number of characters, up to a maximum of 30 characters.

## AC CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ ;  $F_{OSC} = 32.768\text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
$T_{pC}$	Input Clock Period	16	100	32	$\mu\text{S}$
$T_{RC}, T_{FC}$	Clock Input Rise and Fall			12	$\mu\text{S}$
$T_{DPOR}$	Power-On Reset Delay	0.8		1.2	Sec

## AC CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ ;  $F_{OSC} = 32.768\text{ KHz}$

Symbol	Parameter	Min	Max	Typical	Units
$T_{WRES}$	Power-On Reset Min. Width		5 TPC		$\mu\text{S}$
$T_{DH_S}$	H_Sync Incoming Signal Width	5.5	12.5	11	$\mu\text{S}$
$T_{DV_S}$	V_Sync Incoming Signal Width	0.15	1.5	1.0	mS
$T_{DES}$	Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	-12	+12	0	$\mu\text{S}$
$T_{DOS}$	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	$\mu\text{S}$
$T_{WHV_S}$	H_Sync/V_Sync Edge Width		2.0	0.5	$\mu\text{S}$

### Note:

All timing of the I<sup>2</sup>C bus interface are defined by related specifications of the I<sup>2</sup>C bus interface.

