

Z90219/213/212/211/218

Z8[®] DIGITAL TELEVISION CONTROLLERS

FEATURES

| Device | ROM (KB) | RAM* (Bytes) | I/O Lines | Voltage Range |
|--------|-----------|--------------|-----------|---------------|
| Z90211 | 16 (OTP) | 237 | 20 | 4.5V to 5.5V |
| Z90218 | 8 | 237 | 20 | 4.5V to 5.5V |
| Z90212 | 12 | 237 | 20 | 4.5V to 5.5V |
| Z90213 | 16 | 237 | 20 | 4.5V to 5.5V |
| Z90219 | 32 (ext.) | 237 | N/A | 4.5V to 5.5V |

Note: OTP and Z9021x products under development

Z8-Based CMOS Microcontroller for Consumer Television, Cable Box, and Satellite Receiver Applications.

- 42-Pin SDIP Package
- Z8[®] Microcontroller Core at 6 MHz
- Mask ROM sizes Available in 8, 12 and 16 Kbytes
- Eleven Pulse Width Modulators

- On-Chip Infrared (IR) Capture Registers
- Four Channel 3-bit Analog-to-Digital Converter
- Twenty General Purpose I/O Pins
- I²C Serial Communication Port)

On Screen Display (OSD) Section

- Supports Displays up to 10 rows by 24 Columns with 256 Characters
- Character Cell Resolution of 14 Pixels by 18 Scan lines
- Variable Inter-row Spacing from 0-15 Horizontal Scan Lines
- Foreground and Background Colors Fully Programmable by Character

GENERAL DESCRIPTION

The Z9021x Digital Television Controller (DTC) family is Zilog's latest and most powerful Z8-based DTC product offering. These parts feature larger system RAM and ROM options, together with a host of new features including a new color palette system, flexible inter-row spacing, higher character cell resolution, background mesh effect, dedicated I.R. capture registers, on-chip Analog-to-Digital conversion, and a hardware Master mode I²C interface. The familiar Z8 core in combination with these advanced features makes the Z9021x family an ideal choice for low to mid-range televisions in both PAL and NTSC markets.

The Z9021x family consists of two basic device types; Z9020x and Z9021x. The only difference between the two types is the presence of a hardware I²C serial communication port and half-tone OSD circuitry on the Z9021x family. Of course I²C communication is supported on the Z9020x family in software with the dedication of any two I/O pins to the task.

The Z9021x family takes full advantage of the Z8's expanded register file space to offer greater flexibility in On Screen Display creation.

BLOCK DIAGRAM

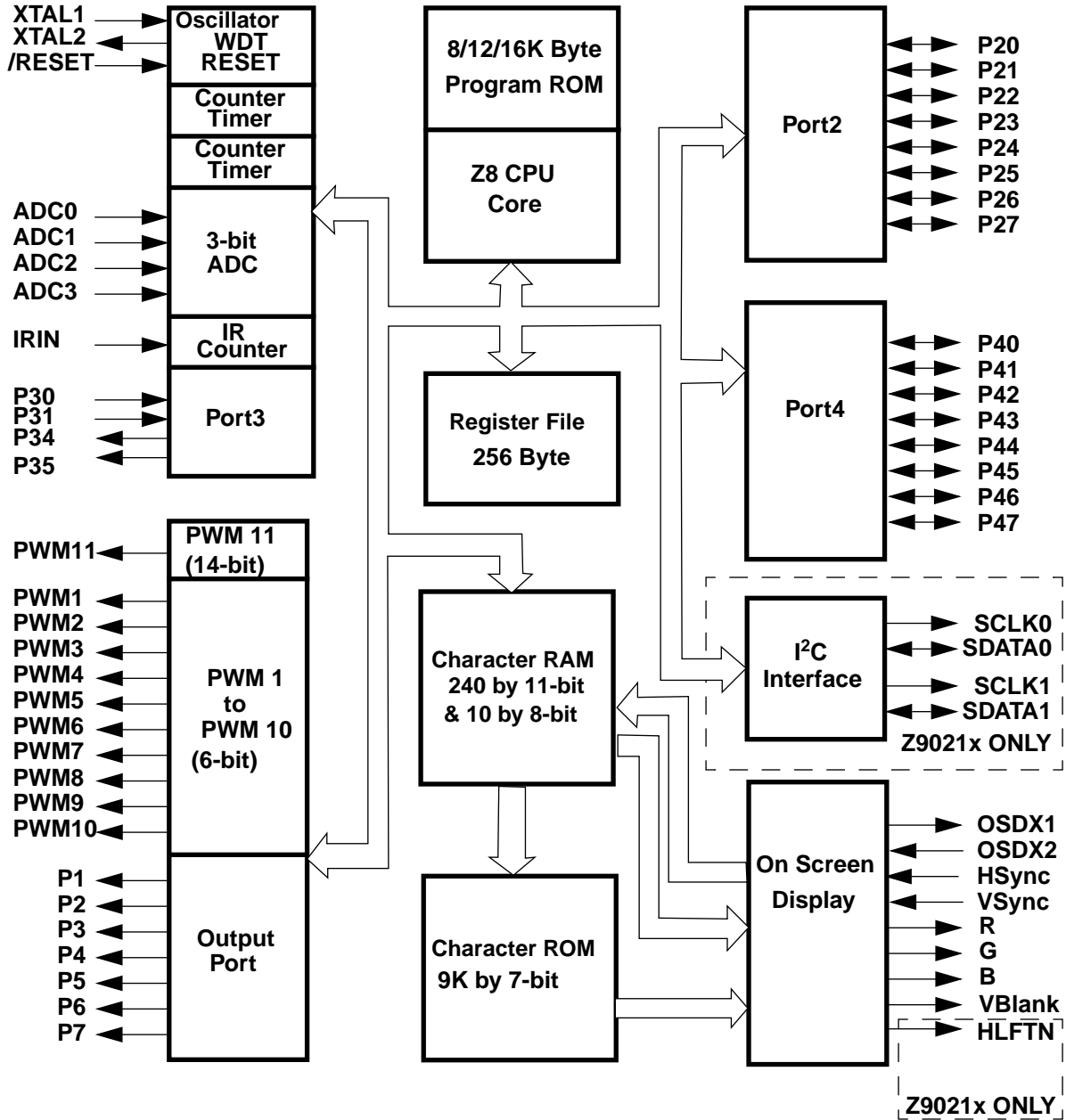
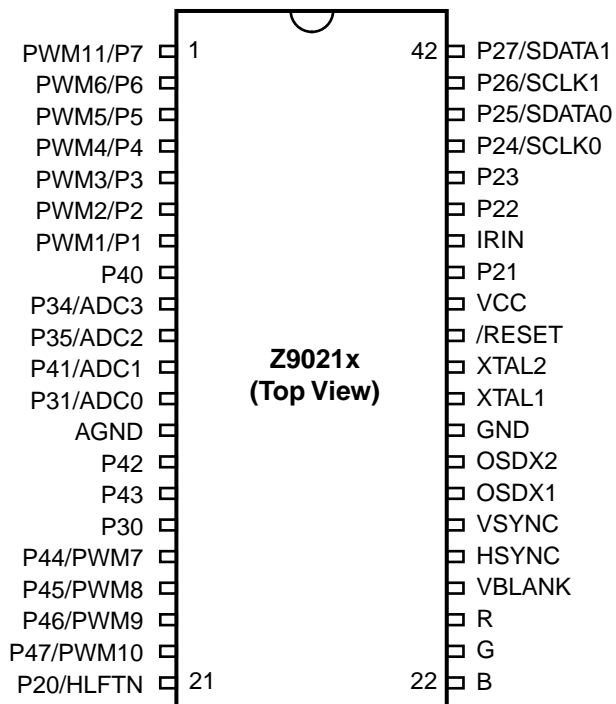


Figure 1. Functional Block Diagram

PIN IDENTIFICATION



PIN IDENTIFICATION

Table 1. Z9021x 42L SDIP Package

| Pin Function | Pin Number | I/O/PWR | Reset State | Name |
|---|-------------------------|---------|-------------|-----------|
| +5 Volts | 34 | PWR | PWR | VCC |
| 0 Volts | 30,13 | PWR | PWR | GND,AGND |
| Infra Red remote capture input | 36 | I | I | IRIN |
| 14-bit Pulse Width Modulator output | 1 | O | O | PWM11 |
| 6-bit Pulse Width Modulator output | 20,19,18,17,2,3,4,5,6,7 | O | O | PWM[10:1] |
| Fixed output ports | 7,6,5,4,3,2,1 | O | O | P[1:7] |
| Bit programmable Input/Output ports | 42,41,40,39,38,37,35,21 | I/O | I | P2[7:0] |
| Half tone output | 21 | O | I | HLFTN |
| I ² C Data | 40,42 | I/O | I | SDATA0,1 |
| I ² C Clock | 39,41 | O | I | SCLK0,1 |
| Fixed output ports | 10,9 | O | O | P3[5:4] |
| Fixed input ports | 12,16 | I | I | P3[1:0] |
| Bit programmable Input/Output ports | 20,19,18,17,15,14,11,8 | I/O | I | P4[7:0] |
| Crystal oscillator input | 31 | I | I | XTAL1 |
| Crystal oscillator output | 32 | O | O | XTAL2 |
| Dot clock oscillator input | 28 | I | I | OSDX1 |
| Dot clock oscillator output | 29 | O | O | OSDX2 |
| Horizontal Sync | 26 | I | I | HSYNC |
| Vertical Sync | 27 | I | I | VSYNC |
| Video blank | 25 | O | O | VBLANK |
| Video R,G,B | 24,23,22 | O | O | R,G,B |
| 3-bit Analog to Digital converter input | 9,10,11,12 | AI | I | ADC[3:0] |
| Device reset | 33 | I | I | /RESET |

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sec-

tions of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Table 2.

| Symbol | Parameters | Min | Max | Units | Notes |
|-----------|-----------------------|------|--------------|-------|------------|
| V_{CC} | Power Supply Voltage | -0.3 | +7 | V | |
| V_i | Input Voltage | -0.3 | $V_{CC}+0.3$ | V | |
| V_o | Output Voltage | -0.3 | $V_{CC}+0.3$ | V | |
| I_{oh} | Output Current High | | -10 | mA | per pin |
| I_{oh} | Output Current High | | -100 | mA | per device |
| I_{ol} | Output Current Low | | 20 | mA | per pin |
| I_{ol} | Output Current Low | | 200 | mA | per device |
| T_a | Operating Temperature | 0 | 70 | °C | |
| T_{STG} | Operating Temperature | -55 | 150 | °C | |

DC CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$; $V_{CC} = +4.5\text{V}$ to $+5.5\text{V}$; $F_{OSC} = 6\text{MHz}$

Table 3.

| Symbol | Parameter | Min | Typical | Max | Units | Conditions |
|-----------|------------------------|--------------|---------|--------------|---------------|-------------------------------------|
| V_{CC} | Power Supply Voltage | 4.75 | 5.00 | 5.25 | V | |
| V_{ih} | Input Voltage High | $0.7V_{CC}$ | 3.0 | V_{CC} | V | |
| V_{il} | Input Voltage Low | 0 | 1.48 | $0.2V_{CC}$ | V | |
| V_{ihc} | Input XTAL/Osc in High | $0.8V_{CC}$ | 3.2 | V_{CC} | V | |
| V_{ilc} | Input XTAL/Osc In Low | | 0.98 | $0.07V_{CC}$ | V | |
| V_{oh} | Output Voltage High | $V_{CC}-0.4$ | 4.75 | | V | $I_{oh}=-0.75\text{mA}$ |
| V_{ol} | Output Voltage Low | | 0.16 | 0.4 | V | $I_{ol}=1.00\text{mA}$ |
| V_{hy} | Schmitt Hysteresis | $0.1V_{CC}$ | 0.8 | | V | |
| I_{ir} | Reset Input Current | | -46 | -80 | μA | $V_{ri}=0\text{V}$ |
| I_{il} | Input Leakage | -3.0 | 0.01 | 3.0 | μA | $0\text{V}, V_{CC}$ |
| I_{ol} | Tri-State Leakage | -3.0 | 0.02 | 3.0 | μA | $0\text{V}, V_{CC}$ |
| I_{CC} | Supply Current | | 13.2 | 20 | mA | All inputs at rail;outputs floating |
| I_{CC1} | Sleep Mode Current | | 3.2 | 6 | mA | All inputs at rail;outputs floating |
| I_{CC2} | Stop Mode Current | | 0.1 | 10 | μA | All inputs at rail;outputs floating |

Note: Typical values measured at 25°C . Minimum and Maximum values given from 0°C to 70°C .

AC CHARACTERISTICS

Table 4.

| No | Symbol | Parameter | Min | Max | Unit |
|----|------------------------|--|-----------|-----------|------|
| 1 | T_{pC} | Input clock period | 166 | 1000 | ns |
| 2 | T_rC, T_fC | Clock input raise and fall | | 25 | ns |
| 3 | T_wC | Input clock width | 35 | | ns |
| 4 | T_wT_{inL} | Timer input low width | 70 | | ns |
| 5 | T_wT_{inH} | Timer input high width | $3T_{pC}$ | | |
| 6 | T_pT_{in} | Timer input period | $8T_{pC}$ | | |
| 7 | T_rT_{in}, T_fT_{in} | Timer input raise and fall | | 100 | ns |
| 8 | T_wIL | Int request input low | 70 | | ns |
| 9 | T_wIH | Int request input high | $3T_{pC}$ | | |
| 10 | T_dPOR | Power-On reset delay | 25 | 100 | ms |
| 11 | $T_dLVIRES$ | Low voltage detect to internal RESET condition | 200 | | ns |
| 12 | T_wRES | Reset minimum width | $5T_{pC}$ | | |
| 13 | T_dH_sOI | H_{sync} start to V_{osc} stop | $2T_{pV}$ | $3T_{pV}$ | |
| 14 | T_dH_sOh | H_{sync} start to V_{osc} start | | $1T_{pV}$ | |

AC TIMING DIAGRAMS

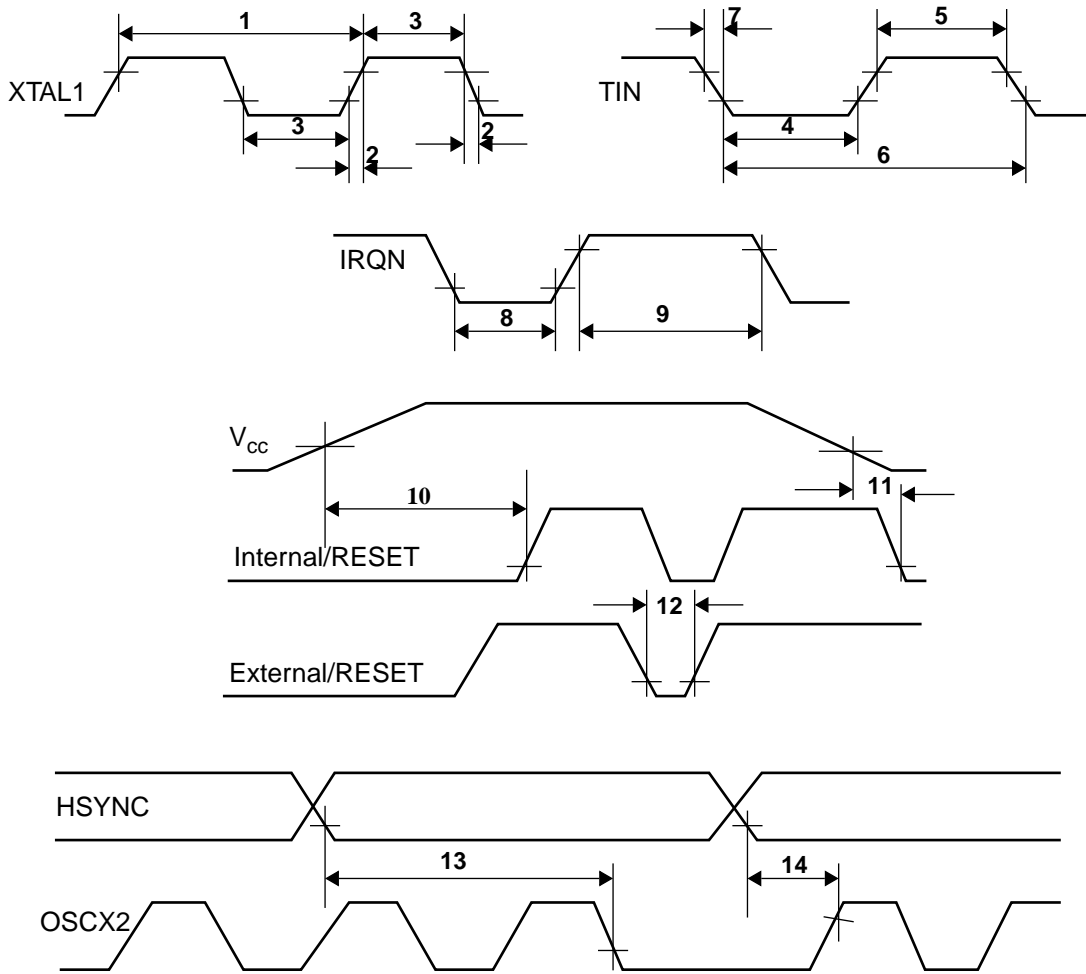


Figure 2. Timing Diagram

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