ANALOG SOLUTIONS™
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ZAD1202

13-Bit High-Speed Sampling A/D Converter

T-51-10-90

Applications

- ☐ Scientific Instrumentation
- ☐ Medical Imaging
- ☐ Industrial Process Control

Key Features

- ☐ True 12-bit performance, 13-bit resolution
- ☐ Guaranteed Spectral Performance
- ☐ 350 ns A/D conversion time
- ☐ 2MHz total throughput
- ☐ Built-In Ultra-Linear Sample/Hold
- ☐ Tri-State Outputs
- ☐ Integral Stable Reference
- ☐ Multiple Output Codings
- ☐ Multiple Input Ranges
- ☐ Pin Compatible with
  ZAD2764 14-bit 500 kHz SADC
  ZAD2846 16-bit 300kHz SADC

Solutions for Data Conversion

13-bit ADC combined with proprietary, ultra-linear S/H provides the best spectral performance for this class of product. The product is conservatively specified to meet spectral performance over the complete temperature range. The ZAD1202 is the new benchmark in high performance and low cost data conversion.

General Description

The ZAD1202, a 13 bit ADC combined with proprietary, ultra-linear S/H, delivers true 12-bit performance over its rated temperature range. It is pin and package compatible with the industry standard ZAD2764/2836/2846 family of high performance 14-bit and 16-bit sampling A/D (SADC) converters. This feature allows the designer to choose between 12-bit video speed, 14 bit high speed, or 16 bit high performance without the need to re-design or re-configure the system for different applications.

Description of Converter

The ZAD1202 utilizes a two-pass Digitally Corrected Sub-Ranging (DCSR) technique in conjunction with a low distortion, fast-aperture sample and hold design to provide superior performance.

Sample/Hold design is the key to spectral performance of high-resolution A/D converters.

The design of the ZAD1202 Sample/Hold has been optimized for low harmonic distortion and excellent signal-to-noise ratio by careful attention to aperture delays, switch signal drive, and amplifier selection and compensation.

This superior design, coupled with factory production test capability, assures that ZAD1202 production units consistently meet the demanding requirements of today's frequency-domain signal-acquisition applications.

PERFORMANCE SPECIFICATIONS
ZAD1202 HIGH-SPEED 13-BIT SAMPLING A/D CONVERTER

ANALOG INPUT (J1 pin 15)

Full-scale range (FSR)	
Bipolar	±2.5V (.61mV/LSB)
Unipolar[3]	0V to +5V
Input Impedance	100K Ohm/10pf
Bias Current	50μA max.
Safe Input Voltage	±15V max.

ACCURACY

Resolution	13 bits
FSR Factory-Calibrated to	±0.05%[4]
Offset Factory-Calibrated to	±5mV[4]
Relative Accuracy incl. internal S/H	±0.02% max.
Differential Linearity @ 12 bits	±0.25 LSB typical, ±0.75 LSB max.
Monotonicity	Guaranteed
Missing Codes	None
Noise	500μV RMS max. (including quantizing noise)

AC CHARACTERISTICS

Sampling Rate	DC to 2.00 MHz.
A/D Conversion Time	350nS
S/H Acquisition Time	150nS
S/H Slew Rate	35V/μS
S/H Aperture Delay	8nS
S/H Aperture Jitter	50pS RMS max.
S/H Feedthrough	
100 KHz ±2.5V sinewave	−72dB max.
1.0 MHz ±2.5V sinewave	−65dB max.

STABILITY

Temperature Coefficient of Gain	±50 ppm/deg. C max.
Temperature Coefficient of Offset	±150 ppm FSR/deg. C max.
Power Supply Sensitivity:	
Gain	±10 ppm/% change in power supply
Offset	±20 ppm FSR/% change in power supply
Warm-Up Time	10 minutes

REFERENCE OUTPUT (J1 pin 10)

Voltage	-8V, ±0.2V. Tracks GAIN adjustment
Load	5 mA max.

SPECTRAL PERFORMANCE[5]

Harmonic Distortion[6]	
100 KHz	
Full-scale input	−80dB typ, −73dB max.
1MHz	
Full-scale input	−71dB typ, −65dB max.
Two-Tone Distortion[6]	
90 KHz + 110 KHz Peak Full-scale input	−74dB typ, −70dB max.
Signal-to-noise Ratio, 100 KHz	
Full-scale input	
without harmonics	−70db min.
including harmonics	−69dB min.

SMALL-SIGNAL FREQUENCY RESPONSE

DC to 56 KHz	0dB to −0.1dB
to 170 KHz	to −0.3dB
to 2.4 MHz	to −3dB

GAIN/OFFSET ADJUSTMENTS

Gain adjustment input (J1 Pin 2)	
Sensitivity	0.1%/V
Maximum Input	±25V
Gain adjustment trimpot	
Adjustment range	±0.6%
Offset adjustment Input (J1 Pin 1)	
Sensitivity	0.2% FSR/V
Maximum Input	±25V
Offset adjustment trimpot	
Adjustment range	±1.2% FSR

DIGITAL CONTROLS

Trigger Input:	
Compatibility	HCMOS[7]
Trigger Width (negative pulse)	20nS min. 70% of Encode Period max.
Byte Enables Lines:	
Compatibility	LSTTL
Outputs Enabled	Low
Tri-state	High
Propagation Delay	30nS max.

DIGITAL OUTPUTS

Parallel Data:	
Output levels	LSTTL
Data Coding	Binary, Offset Binary, 2's Complement[8]
Data Valid	80nS max. after trigger + 1 pipeline delay[9]
End of Conversion (EOC):	
Output levels	HCMOS
Timing	330nS min. to 400nS max. after falling edge of TRIGGER

POWER

+15V ±0.75V	120mA max.
−15V ±0.75V	130mA max.
+5V ±0.25V	240mA max.
Consumption	5W max.

ENVIRONMENTAL

Temperature Range:	
Full rated Performance	10°C to 60°C
Operating	0°C to 70°C
Storage	−25°C to 85°C
Relative Humidity	5 to 95% non-condensing

MECHANICAL

Packaging:	
Dimensions	3.2″×4.5″×0.562″
Shielding	Electromagnetic 5 sides Electrostatic 6 sides
Case Potential	Analog Ground

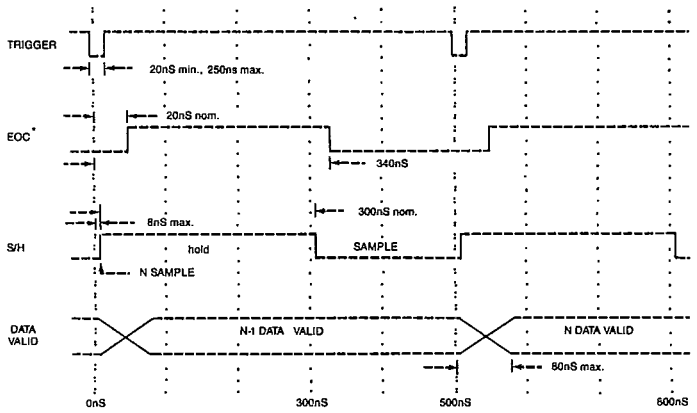
NOTES: see page 4

Interfacing

An important design objective with high-speed converters such as the ZAD 1202, is to minimize the coupling of transient noise from the digital data path to the analog input of the converter. Factors influencing this coupling are; loading of converter output pins, data timing, and grounding. Keep traces from the 13 digital outputs short to minimize data dependent ground return currents to the module. Buffer data outputs near module rather than directly driving backplane data busses.

Output data on the 1202 is timed to change after the following conversion cycle is triggered (pipe read data). This prevents disturbances on the analog input during the critical 150nS before TRIGGER when the on-board track and hold is acquiring the input for the next conversion cycle. This practice can be extended outside the module: the preferred time to enable the tri-state outputs or clock latches to receive data from the module would be 100nS to 200nS after the TRIGGER pulse.

Transients on power inputs to the module (switching power supply noise, digital logic transient) return through the supply bypass capacitors inside the module, and can induce noise across the ANALOG RETURN connections to the module. This condition can be resolved by incorporating L.C. filters in the module power supply lines.



ZAD1202 Timing Diagram

*Data valid falling edge EOC

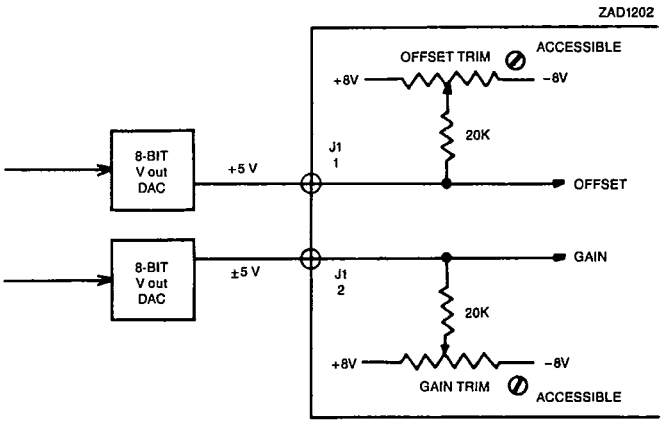
PC Board Layout

Tie all ANALOG RETURNS on connector J1 to analog ground plane. The module case may also be tied to the analog ground plane to improve shielding performance. Make this connection to either PC board mounting screw hole on the analog connector (J1) side of the module.

Depending on application, best signal results may be obtained by tying the analog and digital ground planes together between module connectors J1 and J2.

Dynamic Adjustment of Gain and Offset:

In addition to the accessible gain and offset adjust trimpots, provision has been made for external adjustment via pins 1 and 2 on connector J1. By driving these pins with external voltage output D/A's, the gain and offset of the A/D can be dynamically adjusted by the host computer. Adequate adjustment range is available to null out typical system gain and offset errors.



External Offset and Gain Adjustment

The figure above illustrates the interaction between the gain and offset trimpots and the external adjustment pins. The polarity for the external adjustment pins is as follows: Increasing voltage + at the gain trim input expands the full-scale input range. Increasing voltage at the offset trim input makes the input range more negative. Note that driving the adjustment pins with a voltage source overrides the internal gain and offset trimpots.

Coding

The ZAD1202 has available a variety of output codes including Binary, Offset Binary, and 2's Complement as shown below:

Output Coding

Unipolar (Binary)	Bipolar (Offset Binary)	Output Code MSB LSB
+4.9987V	+2.4987V	11 11
+2.5000V	+0.0000V	10 00
+0.0000V	−2.5000V	00 00

Note: For 2's complement coding, use the BIT 1 output in place of the BIT 1 output.

Input range selection:

Range	Connect
UNIPOLAR 0 to +5V	J1 Pin 9 to J1 Pin 10
BIPOLAR ±2.5V	J1 Pin 9 not connected

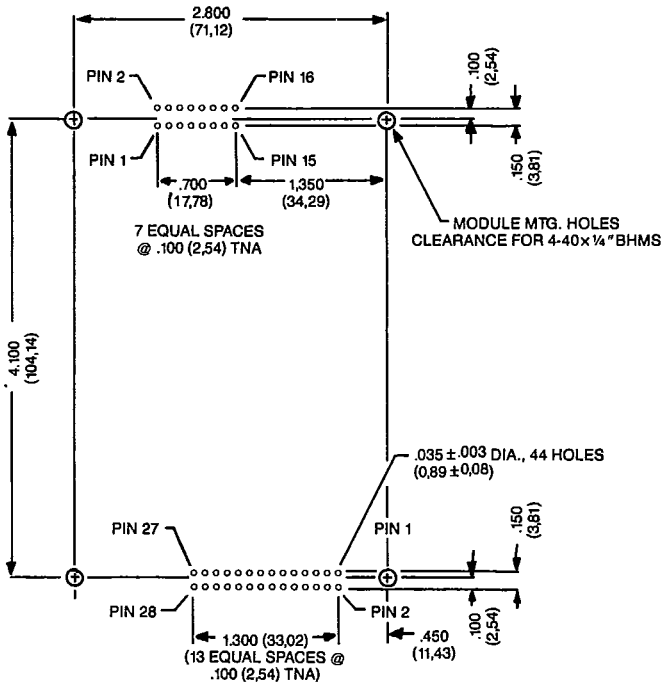
J1 Pin Assignment

1. OFFSET ADJ[1]
2. GAIN ADJ[1]
3. −15V POWER
4. −15V POWER
5. ANALOG RTN[2]
6. ANALOG RTN
7. +15V POWER
8. +15V POWER
9. BIPOLAR[4]
10. REFERENCE OUT
11. S/H OUT
12. ANALOG RTN
13. ANALOG RTN
14. ANALOG RTN
15. ANALOG IN
16. ANALOG RTN

J2 Pin Assignment

1. TRIGGER
2. EOC
3. DO NOT CONNECT
4. DO NOT CONNECT
5. +5V
6. +5V
7. DIGITAL RTN
8. DIGITAL RTN
9. BIT 1 MSB
10. DIGITAL RTN
11. N/C[7]
12. N/C[7]
13. BIT 13
14. N/C[7]
15. BIT 11
16. BIT 12
17. BIT 9
18. BIT 10
19. LO BYTE ENABLE[6]
20. HI BYTE ENABLE[5]
21. BIT 7
22. BIT 8
23. BIT 5
24. BIT 6
25. BIT 3
26. BIT 4
27. BIT 1 MSB
28. BIT 2

NOTES: 1) LEAVE OPEN IF NOT USED.
2) DIGITAL AND ANALOG RETURNS INTERNALLY CONNECTED.
3) COVER IS TIED TO ANALOG GROUND.
4) OPEN = BIPOLAR RANGE; PIN 9 TIED TO PIN 10 = UNIPOLAR RANGE
5) GROUND = BIT 1 THROUGH BIT 5, AND BIT 1 ENABLED; OPEN = TRI-STATE
6) GROUND = BIT 6 THROUGH BIT 13 ENABLED; OPEN = TRI-STATE
7) N/C: NOT CONNECTED (OPEN CIRCUIT)



Drill Pattern-Component Side
Outline and Pin Assignments

ZAD1202 Compatibility

The ZAD1202 is a member of the ZAD2764 14-bit and ZAD2836/46 16-bit family of A/D converters. All modules share a common pinout and basic functional compatibility. The following differences should be noted:

- The ZAD1202 12-bit A/D converter module occupies just 85% of the area of the 14-bit and 16-bit modules [width is 3.2 inch vs. 3.8 inch for the 14/16-bit modules].
- Output data valid timing is pipelined on ZAD1202 to minimize interference to analog input at high operating speeds (refer to timing diagram).
- Consult individual data sheets for partitioning of output bits between high and low bytes [tri-state enable controls], and termination of unused bits.
- Unipolar range is selected by adding jumper between pins 9 and 10 on J1.

Ordering Guide

To Order Specify:
ZAD1202 12-Bit High-Speed Sampling A/D Converter.

Place your order by contacting Analog Solutions at (408) 433-1900.

NOTES FROM PERFORMANCE SPEC. PG 2:
1. All MIN/MAX specifications are guaranteed over the rated performance temperature of +10 deg. C to +60 deg. C. All other specifications are typical values.
2. The ZAD1202 is a 13-bit A/D converter. All 13 bits of data are made available at the output pins. Converter accuracy (see specifications in ACCURACY box on page 2) is specificed to the 12-bit level.
3. For Unipolar (0V to +5V) operation, tie pins 9 and 10 together on J1.
4. External adjustments available via trimpot access and external GAIN/OFFSET adjustment pins (J1 pins 1 and 2).
5. Spectral performance rated using all 13 output bits.
6. Specification denotes maximum amplitude of any single harmonic, in-band spurious, or intermodulation product (two-tone test) relative to the amplitude of a full-scale sinewave.
7. TRIGGER input is terminated internally with 10K ohm to +5V. Use an additional 1K pullup resistor to +5V when driving HCMOS compatible TRIGGER input with TTL logic.
8. Data coding: see OUTPUT CODING table on page 4.
9. Data for Sample N is valid from 80nS after falling edge of the N +1 TRIGGER pulse until 10nS after falling edge of the N +2 TRIGGER pulse.

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