ZC0302

VGA USB PC Camera Processor

Vimicro Corporation

Data Sheet

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1. Features

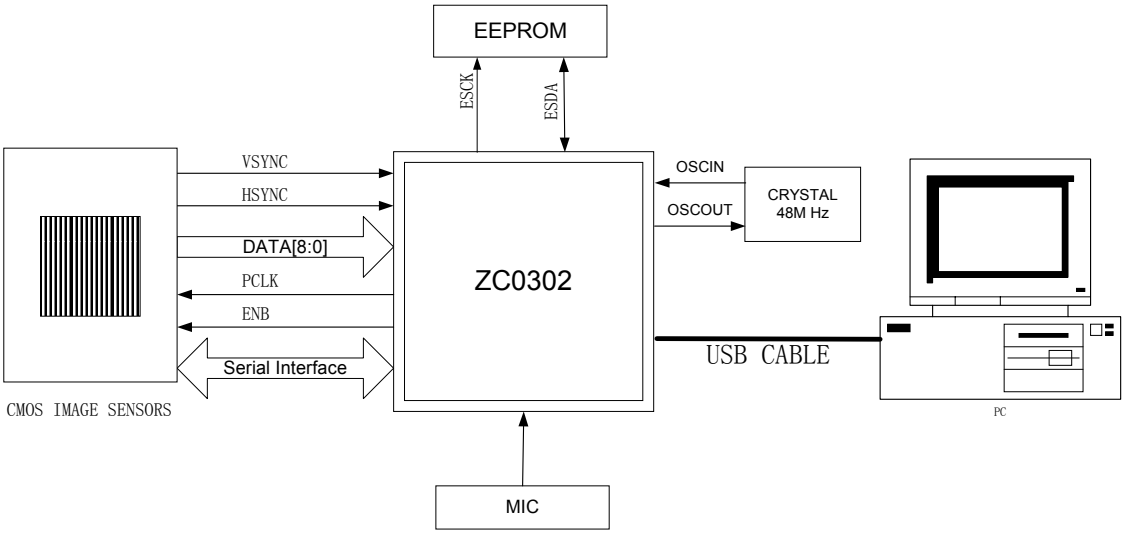

FIGURE 1 USB PC CAMERA SYSTEM BLOCK DIAGRAM

The ZC0302 chip provides a cost effective single chip solution for the PC camera application. It communicates with PC host via Universal Serial Bus (USB) port. All major image processing functions, such as image signal processing (ISP), image data compression and data transfer units are built in the chip. Meanwhile ZC0302 also provides high quality audio sampling function for sound recording. The audio function complies with USB audio class 1.0.

ZC0302 is designed as a cost-effective single-chip device replacing the complex and costly chip sets used in current PC camera designs with embedded USB device controller and transceiver, 48-QFP package, and no external DRAM requirement. Advanced on-chip image signal processor and JPEG encoder produce images with superior quality.

1.1. General Features

- Low cost, single chip solution for high resolution USB PC camera applications
- Audio function complying to USB audio device class 1.0
- Support up to 15 fps VGA video display without DRAM
- USB Device Controller compliant with USB protocol 1.1
- USB parameter configurable through EEPROM
- Support 9/8-bit RGB Bayer pattern raw data input from CMOS image sensors
- Support programmable color correction and gamma correction
- Support programmable Auto Exposure/Auto White Balance
- Support Auto Gain Control
- Support ISO/IEC 10918-1 (JPEG) standard image compression
- Support 4 quantization tables for programmable image quality
- Support raw data output for high quality still image
- 3.3V I/O, 2.5V core
- No external DRAM required
- Flexible system level solution support

2. Architecture

2.1. ZC0302 Block Diagram

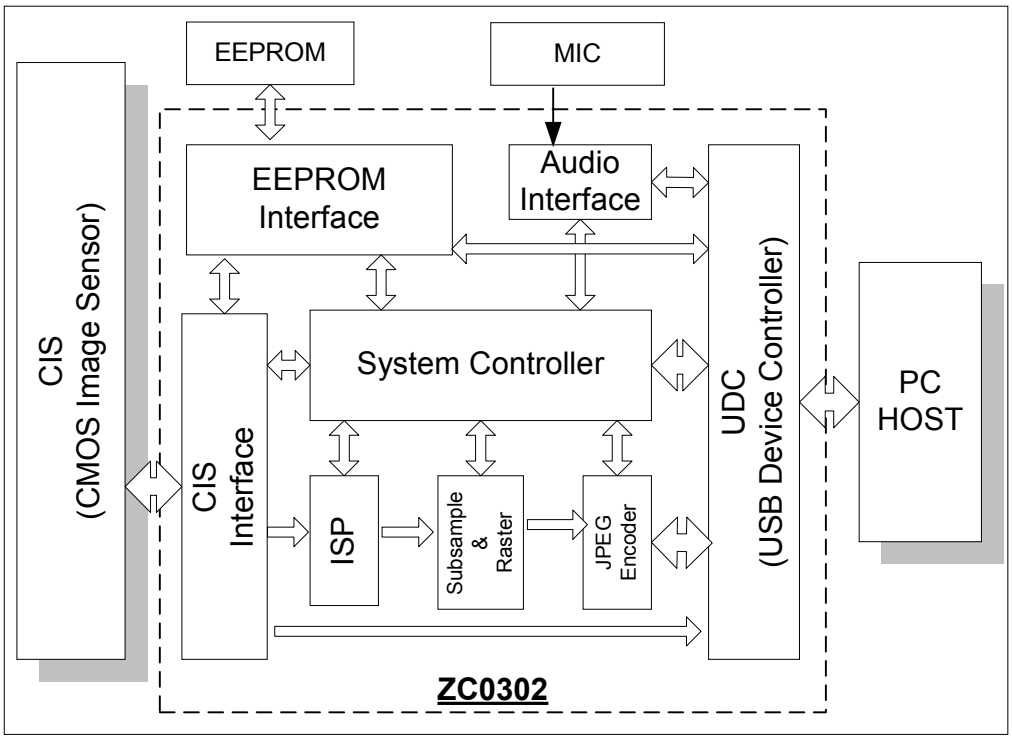

FIGURE 2 BLOCK DIAGRAM OF ZC0302

Figure 2 shows the block diagram of ZC0302. The ISP block receives RGB raw data from CMOS image sensor interface and performs various image processing tasks such as white balance, color correction, gamma correction, histogram equalization and so on. The Sub-sample & Raster block handles the input image data scaling and converts input image data to 8x8 block data format required by DCT module. The JPEG Encoder block compresses the image data from ISP block into JPEG format data. The compressed image data is then transferred to PC host via USB Device Controller (UDC) block for display.

The Audio Interface takes the audio input in mono 16-bit PCM format, and then transfers it to PC Host through the audio streaming pipe in UDC.

2.2. CMOS Image Sensor Interfaces

- Support sensors from most CMOS image sensor vendors including Agilent, Hynix, IC Media, TASC, PixArt, Photobit, OmniVision, and Century
- 9bit/8bit camera input interface

2.3. USB Features

- Built-in USB transceiver
- Suspend and Remote wakeup
- 3 interface for video, audio and control
- Programmable OEM USB parameters by EEPROM including: vendor ID, product ID, MaxPower, serial Number, manufacture descriptor, product descriptor and chip revision.

2.4. Image Signal Processing

- Hardware Dead Pixel Detection/Concealment
- 8/9-bit RGB raw data input from CMOS image sensor
- 2-wire/3-wire serial bus interface to CMOS image sensor
- Programmable white balance, color correction and gamma correction
- Support automatic Exposure Control, automatic White Balance, automatic CMOS Reset Level Control, automatic Gain Control and auto/manual Histogram Equalization
- Support programmable AE/AWB windows
- Support edge enhancement and noise removal
- Support 2x2 Sub-Sampling

2.5. Raster

- The output data format is 4:2:2 YCbCr
- Change the input image data to 8x8 block data format required by the DCT

2.6. Compression Engine

- Standard JPEG compression engine comply to ISO/IEC 10918-1 (JPEG)
- 2 AC and 2 DC Huffman code table
- 4 quantization tables for different image quality
- Adjustable compression rate by Bit Rate Control (BRC) engine
- Simplified JPEG header for better performance are programmable
- VGA @ 15fps, CIF/SIF up to 30 fps
- Adjustable frame rate for efficient bandwidth usage

2.7. Audio Interface

- Built-in 16-bit mono audio ADC for audio recording through microphone
- Sampling rate @ 8K/16K Hz
- USB audio device class 1.0 compliance

2.8. System Controller

- Providing the control to ISP, JPEG, and USB blocks
- Configuring the control registers
- Chip clock generation

- Error detection and handling through USB interface

3. Pin Definition

3.1. Pin Assignment

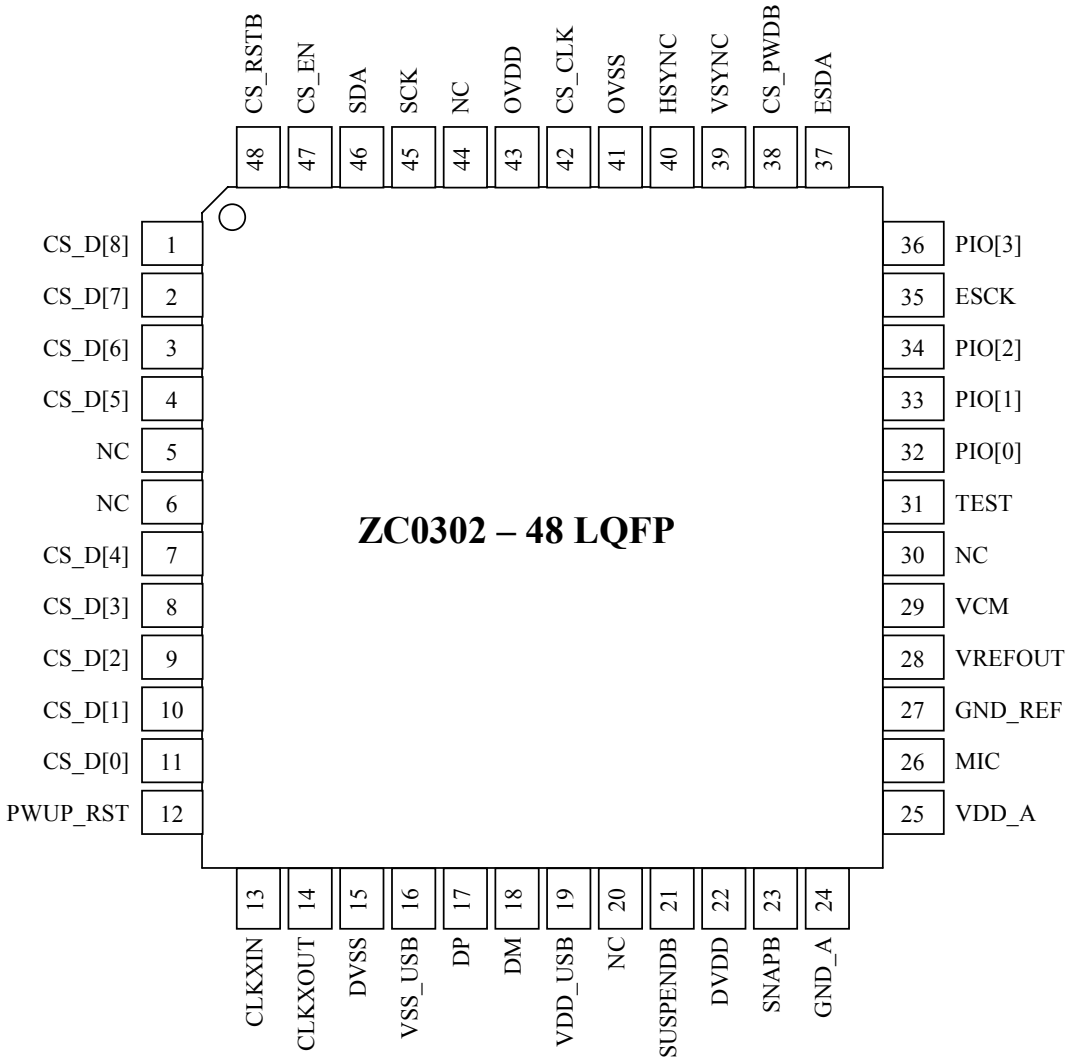

FIGURE 3 48-PIN LQFP PACKAGE

3.2. Pin Description

Pin	Type	Function	48 Pin LQFP
CS_D[8]	I, PD	Sensor data	1
CS_D[7]	I, PD	Sensor data	2
CS_D[6]	I, PD	Sensor data	3
CS_D[5]	I, PD	Sensor data	4

Pin	Type	Function	48 Pin LQFP
CS_D[4]	I, PD	Sensor data	7
CS_D[3]	I, PD	Sensor data	8
CS_D[2]	I, PD	Sensor data	9
CS_D[1]	I, PD	Sensor data	10
CS_D[0]	I, PD	Sensor data	11
PWUP_RST	I, Schmitt	Power on reset, active low	12
CLKXIN	I	Crystal input	13
CLKXOUT	O	Crystal output	14
DVSS	P	Core ground	15
VSS_USB	P	USB transceiver ground	16
DP	I/O	USB data	17
DM	I/O	USB data	18
VDD_USB	P	USB transceiver power	19
SUSPENDB	O	Active-low suspend	21
DVDD	P	Core power	22
SNAPB	I, PU	Snapshot and remote wake up, active low	23
GND_A	P	IADC analog ground	24
VDD_A	P	IADC analog power	25
MIC	A	IADC microphone input	26
GND_REF	A	IADC input ground reference	27
VREFOUT	A	IADC reference voltage	28
VCM	A	IADC common-mode voltage	29
TEST	I, PD	Manufacturing test mode	31
PIO[0]	I/O, PD	General purpose I/O	32
PIO[1]	I/O, PD	General purpose I/O	33
PIO[2]	I/O, PD	General purpose I/O	34
ESCK	O	SEEPROM clock	35
PIO[3]	I/O, PD	General purpose I/O	36
ESDA	I/O, Schmitt	EEPRPOM data	37
CS_PWDB	O	Power-down pin controlling DC/DC regulator	38
VSYNC	I/O, PD	Vertical synchronous signal	39
HSYNC	I/O, PD	Horizontal synchronous signal	40
OVSS	P	I/O ground	41
OVSS	P	I/O ground	41
CS_CLK	O	Sensor clock	42
OVDD	P	I/O power	43
SCK / SICLK	O, PD	Serial interface clock	45
SDA / SIVAL	I/O, Schmitt	Serial interface data	46
CS_ENB / SI_EN	O, PD	Sensor power enable / Serial interface enable	47
CS_RSTB / AECNT	O, PD	Sensor reset / auto exposure for TASC VGA sensor	48

TABLE 3.1 ZC0302 PIN DESCRIPTIONS

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Ambient temperature	0oC to 70oC
Storage temperature	-40oC to 125oC
DC supply voltage	3.0V to 3.6V
I/O pin voltage with respect to VSS	-0.3V to VDD + 0.3V

TABLE 4.1 ABSOLUTE MAXIMUM RATINGS

4.2. DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VDD3V	3.3V Power Supply		3.0	3.6	V
VDD2V	2.5V Power Supply		2.25	2.75	V
V_{il}	Input Low voltage		-0.5	1.0	V
V_{ih}	Input High voltage		2.3	5.5	V
V_{ol}	Output Low Voltage		-	0.4	V
V_{oh}	Output High Voltage		2.4	-	V
I_{pd}	Suspend current		-	500	uA
I_{do}	Active current		-	80	mA

TABLE 4.2 DC CHARACTERISTICS

4.3. USB Transceiver AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{FR}	Rise time	CL=50p	4	20		ns
T_{FF}	Fall time	CL=50p	4	20		ns
T_{FRFF}	Rise and fall time matching	$T_{LRLF}=T_{LR}/T_{LF}$	90	111.11		%

TABLE 4.3 FULL-SPEED DRIVER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min Typ Max	Unit
T_{LR}	Rise time	CL=50p CL=600p	75 300	ns
T_{LF}	Fall time	CL=50p CL=600p	75 300	ns

T_{LRLF}	Rise and fall time matching	$T_{LRLF}=T_{LR}/T_{LF}$	80 125	%

TABLE 4.4 LOW-SPEED DRIVER ELECTRICAL CHARACTERISTICS

4.4. RESET Timing AC Characteristics

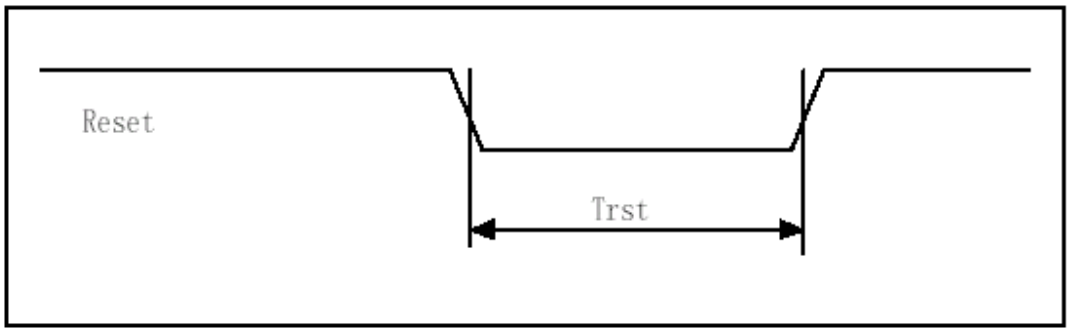

FIGURE 4 RESET TIMING AC CHARACTERISTICS DIAGRAM

Symbol	Parameter	Conditions	Min	Max	Unit
T_{rst}	Reset Pulse Width		--	20	ms

TABLE 4.5 RESET SIGNAL AC CHARACTERISTICS

4.5. Clock AC Characteristics

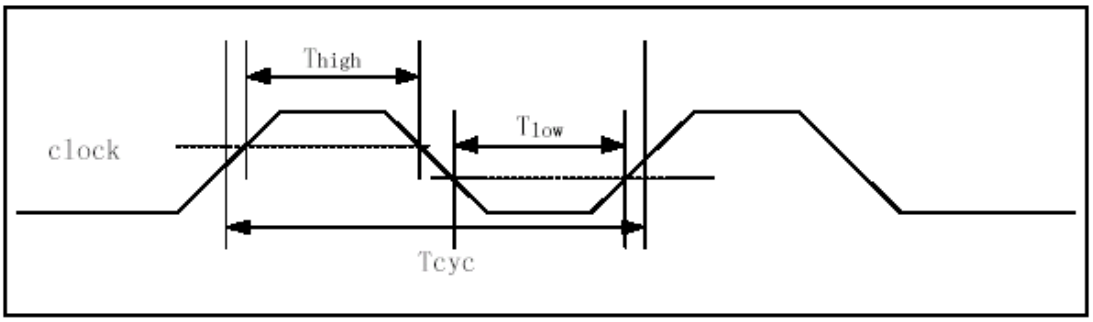

FIGURE 5 CLOCK TIMING AC CHARACTERISTICS DIAGRAM

Symbol	Parameter	Conditions	Min	Max	Unit
1/Tcyc	Oscillator Frequency	48@10PPM	-	-	Mhz
T_{high}	Oscillator Clock High Time		8.3	-	Ns

T_{low}	Oscillator Clock Low Time		8.3	-	Ns

TABLE 4.6 CLOCK SIGNAL AC CHARACTERISTICS

4.6. Input Signal AC Characteristics

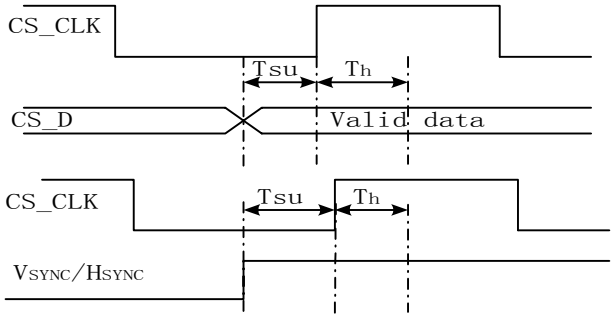

FIGURE 6. INPUT SIGNAL AC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
T_{su}	Input setup time			45	ns
T_h	Input hold time		0	-	ns

TABLE 4.7 CS_D INPUT SIGNAL AC CHARACTERISTICS

Symbol	parameter	conditions	Min	Max	Unit
T_{su}	Input setup time			20	ns
T_h	Input hold time		0	-	ns

TABLE 4.8 VSYNC / HSYNC INPUT AC CHARACTERISTICS

4.7. Output Signal AC Characteristic

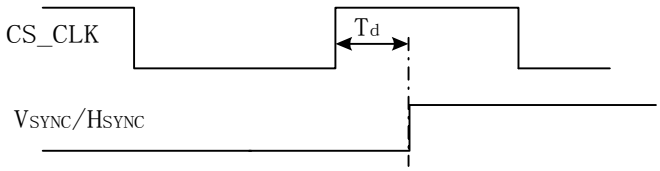

FIGURE 7. VSYNC/HSYNC OUTPUT AC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
T_d	Output delay		-	1.5	ns

TABLE 4.9 VSYNC/HSYNC OUTPUT AC CHARACTERISTICS

5. Mechanical Information

FIGURE 8. 48-PIN LQFP PACKAGE DIAGRAM (OMITTED)

Lead Count		48
Body Size	D1	7
	E1	7
Stand-Off	A1	0.1
Body Thickness	A2	1.4
Lead Width	b	0.2
Lead Thickness	c	0.127
Lead Pitch	e	0.5

TABLE 5.1 ZC0302 PACKAGE DIMENSION (unit: mm)

6. Appendix

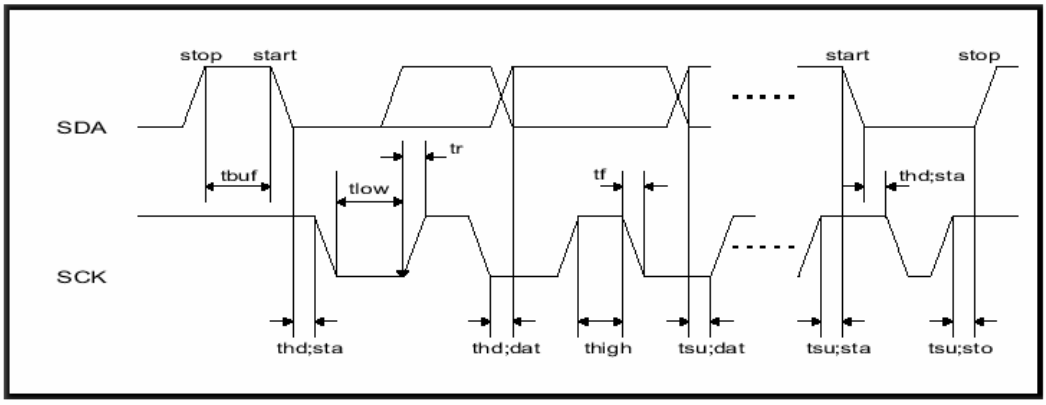

FIGURE 9. SERIAL BUS TIMING DIAGRAM

Parameter	Symbol	Min	Max.	Unit
SCK clock frequency	f_{sck}	0	100	KHz
Time that I^2C bus must be free before a new transmission can start	t_{buf}	4.7	-	us
Hold time for a START	$t_{hd};S_{ta}$	4.0	-	us
LOW period of SCK	t_{low}	4.7	-	us
HIGH period of SCK	t_{high}	4.0	-	us
Setup time for START	$t_{su};S_{ta}$	4.7	-	us
Data hold time	$t_{hd};d_{at}$	0	-	us
Data setup time	$t_{su};d_{at}$	200	-	ns
Rise time of both SDA and SCK	t_r	-	1	us
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su};S_{tp}$	4.7	-	us
Capacitive load of each bus lines (SDA, SCK)	C_b	-	-	pf

TABLE 7. SERIAL BUS TIMING TABLE