

MODE OF DISPLAY

Viewing direction Display mode Display condition TN positive **Reflective type** 6 O' clock TN negative Transflective type 12 O' clock Transmissive type STN : Yellow green 3 O' clock Grey Others 9 O' clock Blue (negative) **FSTN** positive **FSTN** negative LCD MODULE NUMBER NOTATION: ZCV4162T- L W - B T - W 6 -*(1)---Model number of standard LCD Modules *(2)---Backlight type (2) (3) (4) (5) (6) (7) (8)(1)N – No backlight E – EL backlight L – Side-lited LED backlight M-Array LED backlight C - CCFL*(3)---Backlight color N – No backlight A – Amber B - BlueO-Orange W–White Y – Yellow green *(4)---Display mode T - TNV – TN (Negative) S – STN Yellow green G – STN Grey B – STN Blue (Negative) F – FSTN N-FSTN (Negative) *(5)---Rear polarizer type **R** – Reflective F – Transflective T – Transmissive *(6)---Temperature range N – Normal W-Extended *(7)---Viewing direction 6 - 6 O'clock 2 – 12 O'clock 3 - 3 O'clock 9 - 9 O'clock *(8)---Special code for other requirements (Can be omitted if not used) B – Reverse the backlight A, K pin

GENERAL DESCRIPTION

Display mode	:	16 characters x 2 lines LCD module
Interface	:	4-bit or 8-bit parallel
Driving method	:	1/16 duty, 1/5 bias
IC driver	:	Wuxi I-CORE AIP31066 & AIP31065 or Equivalence For the detailed information, please refer to IC specifications.

MECHANICAL DIMENSIONS

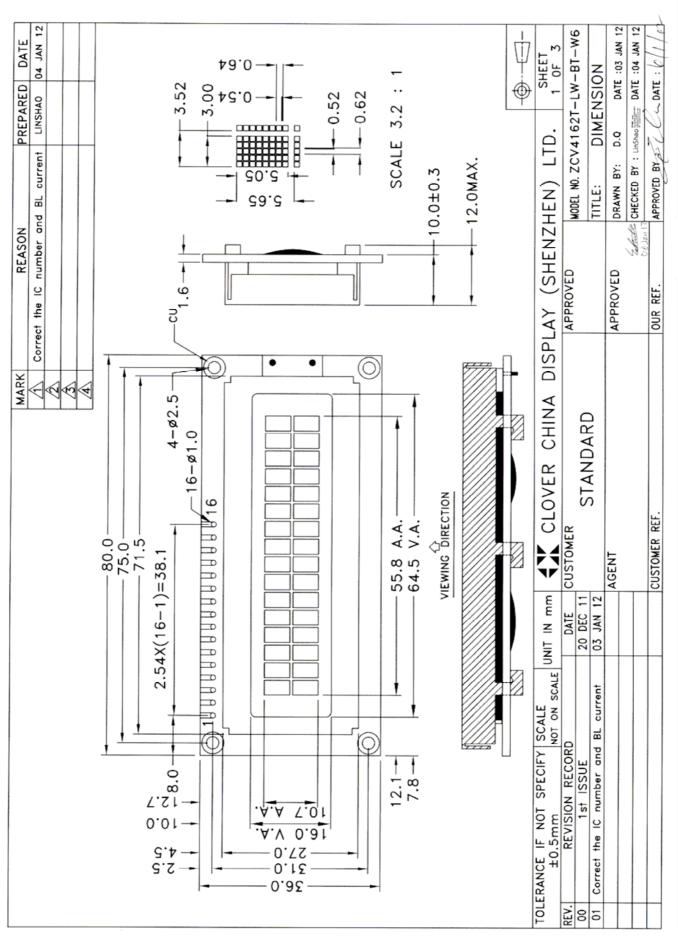
Item	Dimension	Unit	Item	Dimension	Unit
Outline Dimension	80.0(L) x 36.0(W) x 12.0(H)	mm	Character Pitch	3.52(L) x 5.65(W)	mm
Viewing Area	64.5(L) x 16.0(W)	mm	Dot Size	0.52(L) x 0.54(W)	mm
Character Size	3.0(L) x 5.05(W)	mm			

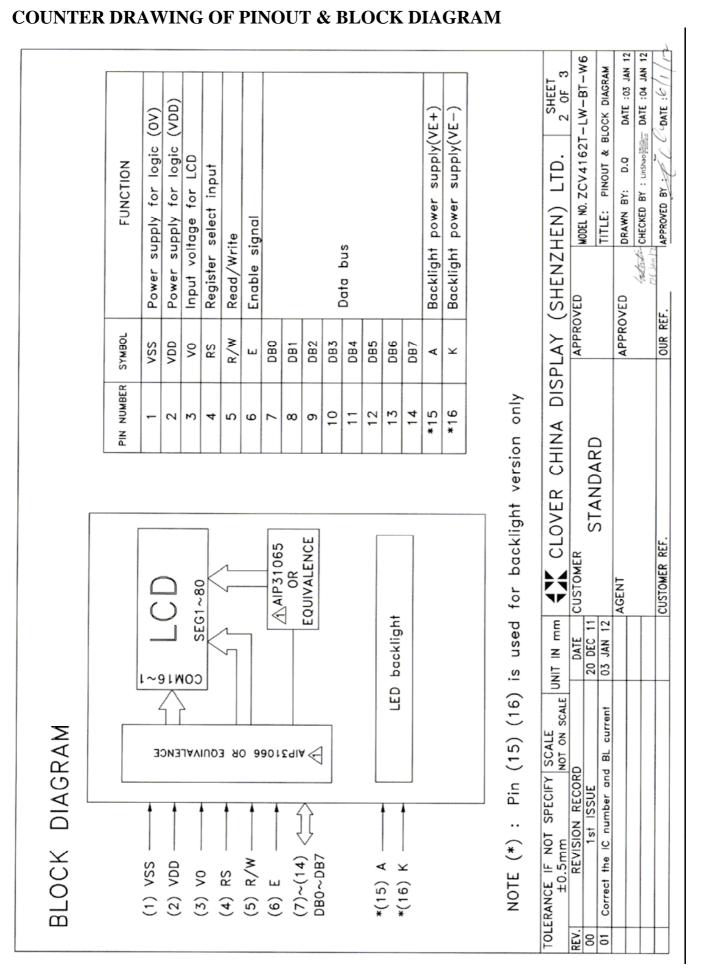
CONNECTOR PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	Vss	Power supply for logic (0V)	9	DB2	
2	Vdd	Power supply for logic	10	DB3	
3	Vo	Input voltage for LCD (0V to VDD)	11	DB4	
4	RS	Register select input	12	DB5	Data bus
5	R/W	Read/Write	13	DB6	
6	Е	Enable signal	14	DB7	
7	DB0		15	А	Backlight power supply (+)
8	DB1	Data bus	16	K	Backlight power supply (-)

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COUNTER DRAWING OF MODULE DIMENSION





SPEC. REV.00

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ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, @Ta=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit	Item	Symbol	MIN.	TYP.	MAX.	Unit			
Supply Voltage	VDD	4.8	5.00	5.2	V	"H"Level Input Voltage	VIH	2.2	_	VDD	V			
Supply Current	IDD	_	1.41	1.73	mA	"L''Level Input Voltage	VIL	0	_	0.6	V			
Backlight Voltage	Backlight Voltage							Backlight Current						
Array LED						Array LED								
Yellow Green	VBL	4.8	5.0	5.2	v	Yellow Green	IBL	-	14.8	17	mA			

ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions

Item	Symbol	Rating (for wide temperature)	Unit
Supply Voltage	VDD	-0.3 to 7	V
Input Voltage	VT	-0.3 to VDD +0.3	V
Operating Temperature	Topr	-20 to 70	°C
Storage Temperature	Tstg	-30 to 80	°C

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INSTRUCTIONS

					Code							Execution Time	
Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	(max) (when fcp or fosc is 250 kHz)	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display	1.53ms	
Return Home	0	0	0	0	0	0	0	0	1	*	Moves cursor to first position. DD RAM contents remain unchanged.	1.53ms	
Entry Mode Set	0	0	0	0	0	0	0	1	I / D	S	Sets cursor move direction and specifies shift of display. These operations are performed during write and read.	39us	
Display On/Off Control	0	0	0	0	0	0	1	D	С	В	Sets display (D) ON/OFF, cursor ON/OFF (C), and blinking ON/OFF (B).	39us	
Cursor or Display Shift	0	0	0	0	0	1	S / C	R / L	*	*	Shifts display or moves cursor (S/C) and sets Displayed to shift RIGHT/LEFT (R/L)	39us	
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets 8-bit/4-bit interface (DL), no. of lines displayed (N) and character font (F).	39us	
Set CG RAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Sets CG RAM address. CG RAM data is sent and received after setting.	39us	
Set DD RAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Sets DD RAM address. DD RAM data is sent and received after this setting.	39us	
Read Busy Flag & Address	0	1	BF	AC o		Reads Busy flag (BF) indicating internal operation is being performed. Reads address counter contents.	al 0 us						
Write Data	1	0		1		V	Write D	ata			Writes data into DD RAM or CG RAM.	1. 39us	
Read Data from CG or DD RAM	1	1]	Read D	ata			Reads data from DD RAM or CG RAM.	39us	
	S/C R/L R/L DL DL	= 0: 1 = 1: 1 $= 1: 1 = 1: 1$ $= 1: 0: 0$ $= 1: 8$ $= 0: 4$ $= 1: 2$ $= 0: 4$ $= 1: 2$ $= 0: 4$ $= 1: 1$	Display Cursor : shift to shift to 8 bits 4 bits 2 lines 1 line 5 x 10 c 5 x 7 do Internal	ent panies d shift move the righ the left lots	t						DD RAM: Display data RAM CG RAM: Character generator RAM ACG: CG RAM address ADD: DD RAM address : Corresponds to cursor address AC: Address counter used for both DD and CG RAM address. * Don't care		

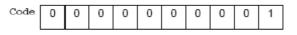
DISPLAY DD RAM AND CHARACTER POSITION

16x2, 1/16 DU	16x2, 1/16 DUTY CYCLE										
	1	2		16	DISPLAY POSITION						
line 1	00	01		0F	DD RAM ADDRESS						
line 2	40	41		4F							

FUNCTION DESCRIPTION

Clear Display

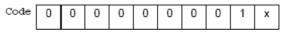
RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0



Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0



Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Entry Mode Set

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Code	0	0	0	0	0	0	0	1	I/D	S	
------	---	---	---	---	---	---	---	---	-----	---	--

Set the moving direction of cursor and display.

I/D : Increment / decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

S: Shift of entire display

When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If

S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D =

"1" : shift left, I/D = "0" : shift right).

S	I/D	Description				
Н	Н	Shift the display to the left				
н	L	Shift the display to the right				

FUNCTION DESCRIPTION(CONT.)

> DL : Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select

8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N : Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

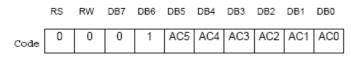
F : Display font type control bit

When F = "Low", it means 5 x 8 dots format display mode

When F = "High", 5 x11 dots format display mode.

Ν	F	No. of Display Lines	Character Font	Duty Factor
L	L	1	5x8	1/8
L	Н	1	5x11	1/11
Н	х	2	5x8	1/16

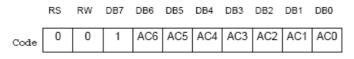
• Set CGRAM Address



Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

Set DDRAM Address



Set DDRAM address to AC.

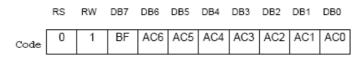
This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

FUNCTION DESCRIPTION(CONT.)

• Read Busy Flag and Address



When BF = "High", indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

Write Data to CGRAM or DDRAM

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0
------	---	---	----	----	----	----	----	----	----	----

Write binary 8-bit data to DDRAM/CGRAM.

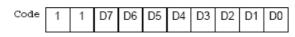
The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction

: DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data from CGRAM or DDRAM

RS RW DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0



Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

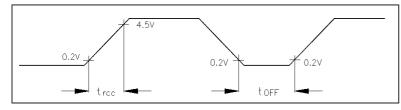
* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

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Parameters Symbol Recommended		Recommended timing	Parameters	Symbol	Recommended timing
Enable Cycle Time	tC (min)	1000ns	Set-up Time	tB(min)	140ns
Enable Pulse Width			R/W and RS built in	tsu2	60ns
			Time	(min)	
High level	tW(min)	450ns	R/W and RS hold Time	tH1 (min)	20ns
Low level	tL (min)	450ns	Output Data Delay	tD(Max)	360ns
			Time		
Enable Raise Time	tr (max)	25ns	Input Data Hold Time	tH (min)	10ns
Enable Fall Time	tf (max)	25ns	Output Data Hold Time	tH2 (min)	20ns

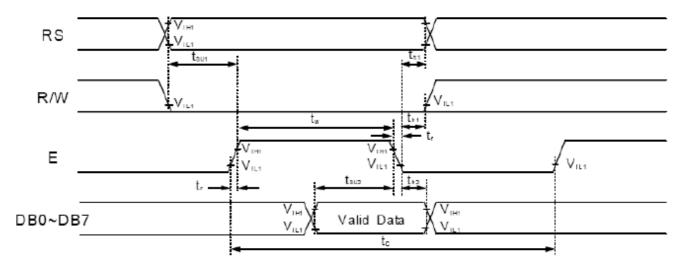
ΤΕΡΙΩΤΙΩΩ ΛΕ ΩΛΛΡΑΤΙΡΙ Ε ΩΛΝΤΡ т CITIDO **FD**

Power On Timing Diagram Figure 1

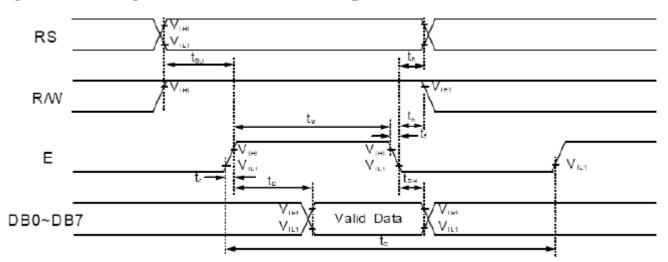


Note: Power on initialization depends on the rise time of the power supply when it is turned on. When the above power supply conditions is not met, the internal reset circuit will not operate normally and initialization will not be performed. Initialization by manual instruction is required. Use the procedure in figures 4 and 5 for initialization.

Timing Characteristics of Write Operation Figure 2



Timing Characteristics of Read Operation Figure 3



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INITIALIZATION METHOD

The module will automatically perform initialization using internal reset circuit when power is turned on. The following instructions are executed during initialization.

 $= 0:5 \times 7$ dot character font

- 1. Display Clear
- The busy flag is kept in busy state high (BF=1). The busy state is 15ms..

F

- 2. Function set: DL = 1:8 bit long interface data
 - N = 0: 1 line display
- 3. Display on / off control:
- D = 0: Display off
- C = 0: Cursor off
- **B** = 0: Blink off
- 4. Entry mode set:
- I / D = 1: +1 (increment) S = 0: No shift

Figure 4 Initialization for 8-Bit Interface

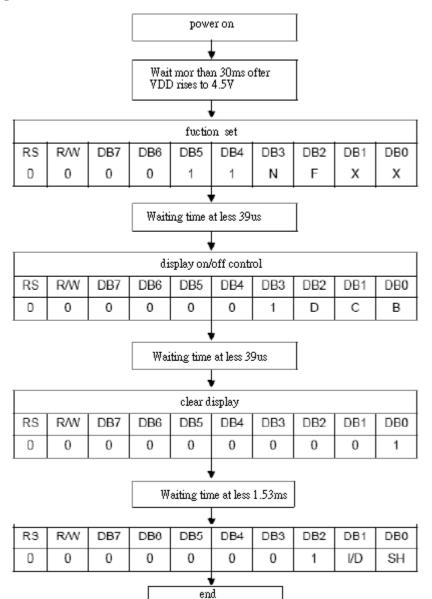
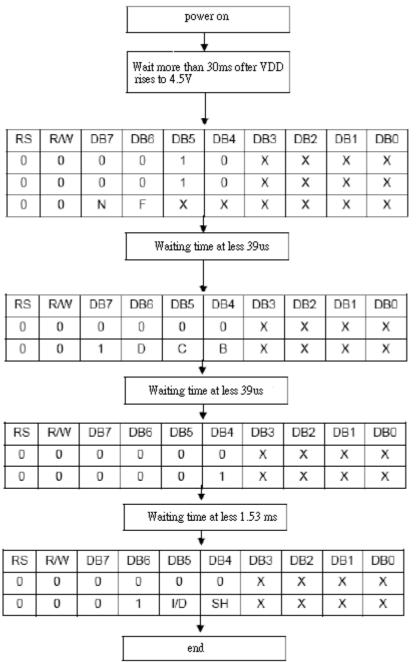


Figure 5 Initialization for 4-Bit interface



QUALITY STANDARD OF LCD MODULE

1.0	Sampling Method Sampling Plan : MIL STD 105 E			
	Critical : 0.25% Major 0.65% Minor 1.5%			
2.0	Defect Group	Failure Category	Failure Reasons	
	Critical Defect	Malfunction	Open	
	0.25%(AQL)		Short	
			Burnt of dead component	
			Missing part/improper part P.C.B.	
			Broken	
	Major Defect	Poor Insulation	Potential short	
	0.65%(AQL)		High current	
			Component damage or scratched	
			or Lying too close improper coating	
		Poor Conduction	Damage joint	
			Wrong polarity	
			Wrong spec. part	
			Uneven/intermittent contact	
			Loose part	
			Copper peeling	
			Rust or corrosion or dirt's	
	Minor Defect	Cosmetic Defect	Minor scratch	
	1.5%(AQL)		Flux residue	
			Thin solder	
			Poor plating	
			Poor marking	
			Crack solder	
			Poor bending	
			Poor packing	
			Wrong size	

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING & CLEANING

Use soft cloth with solvent (recommended below) to clean the display surface and wipe lightly. - Isopropyl alcohol, ethyl alcohol, trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent; -water, ketone, aromatics

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommend that any unused input terminal would be connected to V_{DD} or V_{SS} , do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

(3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed direct to sunshine or high temperature/humidity.

(4) CAUTION FOR OPERATION

It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. The use of direct current drive should be avoided because an electrochemical reaction due to direct current causes LCD's undesirable deterioration.

Response time will be extremely delayed at low temperature, and LCD's show dark color at high temperature. However those phenomena do not mean malfunction or out of order with LCD's.

Some font will be abnormally displayed when the display area is pushed hard during operation. But it resumes normal condition after turning off once.

(5) SAFETY

For crash damaged or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.

When any liquid leaked out of a damaged glass cell comes in contact with your hands, wash it off with soap and water.

WARRANTY

CLOVER CHINA will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Clover china is limited to repair and/or replacement. Clover china will not be responsible for any subsequent or consequential event.