

## Precision 11.6 MHz CMOS Rail-to-Rail Input/Output Operational Amplifiers

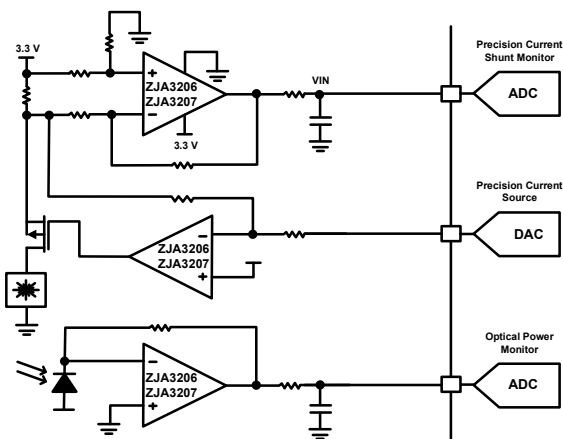
### Features

- Continuous Time Amplifier, No Chopper or Auto-zero Glitch
- Low Offset Voltage: 50  $\mu\text{V}$  max
- Low Offset Voltage Drift: 0.2  $\mu\text{V}/^\circ\text{C}$   
1  $\mu\text{V}/^\circ\text{C}$  max
- Low Input Bias Current: 0.6 pA  
3 pA max
- Low Noise: 6.2  $\text{nV}/\sqrt{\text{Hz}}$  @ 1 kHz  
5  $\text{nV}/\sqrt{\text{Hz}}$  @ 10 kHz  
0.1 Hz to 10 Hz 1.86  $\mu\text{V}_{\text{P-P}}$
- High Unit Gain Bandwidth: 11.6 MHz
- High Slew Rate: 5.1  $\text{V}/\mu\text{s}$
- Fast Settling Time: 0.81  $\mu\text{s}$  to 0.01%
- Supply Current: 0.9 mA per amplifier
- Wide Supply Voltage: 2.7 V to 5.5 V;  $\pm 1.35\text{ V}$  to  $\pm 2.75\text{ V}$
- Rail-to-rail Input and Output
- Drive Large Capacitive Load Up to 10 nF
- Large Output Current:  $\pm 150\text{ mA}$
- Wide Temperature Range:  $-40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$

### Applications

- Multi-parameter Patient Monitor
- Chemistry and Gas Analyzer
- Multi-pole Filters
- Sensor Analog Front End
- ASIC Input or Output Amplifiers
- ADC Input Driver and DAC Output Buffer
- Photodiode Trans-impedance Amplifier

### Typical Application



### General Description

The ZJA3206 and ZJA3207 are rail-to-rail input and output, single-supply amplifiers featuring very low offset voltage, wide signal bandwidth, and low input voltage and current noise. The parts use a proprietary trimming technique that achieves superior precision without chopping glitches. The ZJA3206 and ZJA3207 are fully specified to operate from 2.7 V to 5 V single supply.

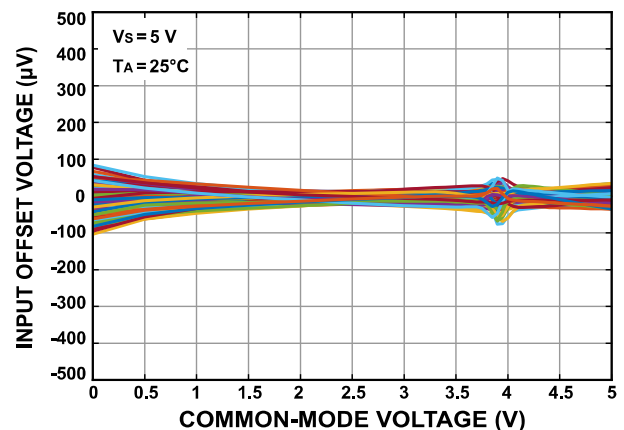
The combination of 11.6 MHz bandwidth, low offset, low noise, and low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of these features. AC applications benefit from the wide bandwidth and low distortion.

Applications for the parts include portable and low power instrumentation, audio amplification for portable devices and multi-pole filters. The ability to operate rail-to-rail both at the input and at the output enables designers to buffer ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.

ZJA3206-1 and ZJA3207 are available in 5-lead SOT23 package. ZJA3206-2 is available in 8-lead narrow SOIC and 8-lead MSOP packages. ZJA3206-4 is available in 14-lead SOIC and 14-lead TSSOP packages. All of them are specified over the  $-40\text{ }^\circ\text{C}$  to  $+125\text{ }^\circ\text{C}$  extended industrial temperature range.

Model	Channels	Package
ZJA3207	1	SOT23-5
ZJA3206	1	SOT23-5
	2	SOIC-8/MSOP-8
	4	SOIC-14/TSSOP-14

### Typical Characteristics



## Table of Contents

Features .....	1	Output Phase Reversal .....	15
Applications .....	1	THD+Noise.....	15
Typical Application .....	1	Total Noise Including Source Resistors.....	15
Typical Characteristics.....	1	Settling Time.....	16
Table of Contents.....	2	Overload Recovery Time.....	16
Version (Release B).....	3	Capacitive Load Drive .....	17
Revision History .....	3	Open-Loop Gain and Phase Response.....	18
Pin Configurations and Function.....	4	Photodiode Circuits .....	19
Absolute Maximum Ratings .....	7	Outline Information.....	21
Thermal Resistance .....	7	Ordering Guide.....	24
Specifications .....	8	Product Order Model.....	24
Typical Performance Characteristics .....	10	Related Parts .....	25
General Application Information .....	15		

## Version (Release B)<sup>1</sup>

### Revision History

#### **Dec. 2024—Release B**

Added ZJA3207

Updated Specifications, Figure 6/7/8

#### **Nov. 2024—Release A**

#### **Jul. 2024—Initial**

---

<sup>1</sup> Information furnished by ZJW Microelectronics is believed to be accurate and reliable. However, no responsibility is assumed by ZJW Microelectronics for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of ZJW Microelectronics. Trademarks and registered trademarks are the property of their respective owners.

Pin Configurations and Function

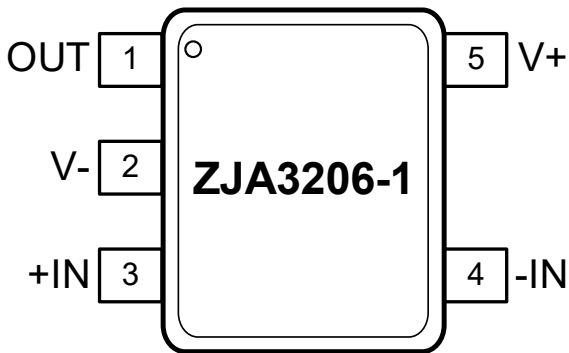


Figure 1. ZJA3206-1 Pin Configuration (5-lead SOT23)

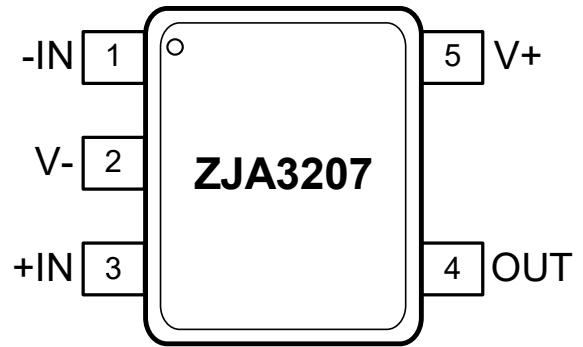


Figure 2. ZJA3207 Pin Configuration (5-lead SOT23)

Mnemonic	Pin No.	I/O	Description
OUT	1	AO	Amplifier output
V-	2	P	Negative power supply
+IN	3	AI	Amplifier non-inverting input
-IN	4	AI	Amplifier inverting input
V+	5	P	Positive power supply

Mnemonic	Pin No.	I/O	Description
-IN	1	AI	Amplifier inverting input
V-	2	P	Negative power supply
+IN	3	AI	Amplifier non-inverting input
OUT	4	AO	Amplifier output
V+	5	P	Positive power supply

<sup>1</sup> AI: Analog Input; P: Power; AO: Analog Output.

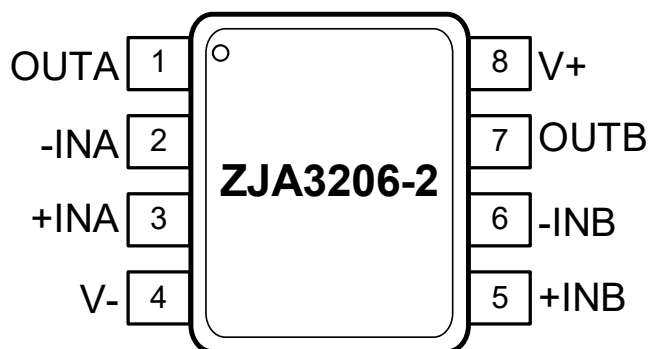


Figure 3. ZJA3206-2 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O <sup>1</sup>	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A Non-inverting input
V-	4	P	Negative power supply
+INB	5	AI	Channel B Non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
V+	8	P	Positive power supply

<sup>1</sup> AI: Analog Input; P: Power; AO: Analog Output.

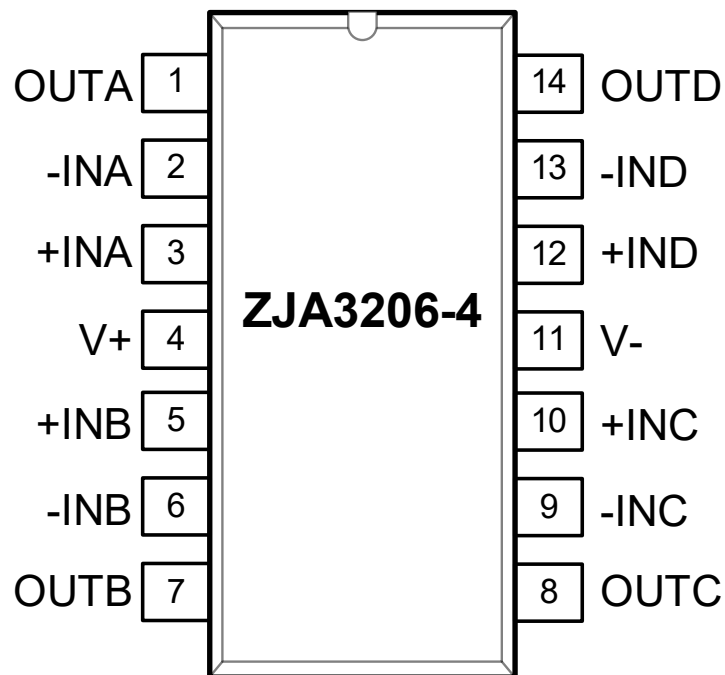


Figure 4. ZJA3206-4 Pin Configuration (14-lead SOIC and TSSOP)

Mnemonic	Pin No.	I/O <sup>1</sup>	Description
OUTA	1	AO	Channel A output
-INA	2	AI	Channel A inverting input
+INA	3	AI	Channel A non-inverting input
V+	4	P-	Positive power supply
+INB	5	AI	Channel B non-inverting input
-INB	6	AI	Channel B inverting input
OUTB	7	AO	Channel B output
OUTC	8	AO	Channel C output
-INC	9	AI	Channel C inverting input
+INC	10	AI	Channel C non-inverting input
V-	11	P	Negative power supply
+IND	12	AI	Channel D non-inverting input
-IND	13	AI	Channel D inverting input
OUTD	14	AO	Channel D output

<sup>1</sup> AI: Analog Input; P: Power; AO: Analog Output.

Absolute Maximum Ratings <sup>1</sup>

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V- to V+
Output Short-Circuit Duration to GND	Indefinite
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature Range	-65 °C to 150 °C
Lead Temperature, Soldering (10 sec)	300 °C
ESD Rating (ESD) <sup>2</sup>	
Human Body Model (HBM) <sup>3</sup>	6 kV
Charge Device Model (CDM) <sup>4</sup>	2 kV

Thermal Resistance <sup>5</sup>

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-lead SOT23	230	76	°C/W
8-lead SOIC	158	43	°C/W
8-lead MSOP	190	44	°C/W
14-lead SOIC	120	36	°C/W
14-lead TSSOP	240	43	°C/W

<sup>1</sup> These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

<sup>2</sup> Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry,

damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

<sup>3</sup> ANSI/ESDA/JEDEC JS-001 Compliant

<sup>4</sup> ANSI/ESDA/JEDEC JS-002 Compliant

<sup>5</sup>  $\theta_{JA}$  addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

## Specifications

The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at  $V_S = 5\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25\text{ °C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 2.5\text{ V}$ and $4.5\text{ V}$	●	10 70	50 150	$\mu\text{V}$ $\mu\text{V}$
		$V_{CM} = 0\text{ V}$ to $5\text{ V}$	●		500	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40\text{ °C} < T_A < +125\text{ °C}$	●	0.2	1	$\mu\text{V}/\text{°C}$
Input Bias Current	$I_B$		●	0.6	3 1000	$\text{pA}$ $\text{pA}$
		$-40\text{ °C} < T_A < +85\text{ °C}$			80	$\text{pA}$
Input Offset Current	$I_{OS}$		●		5 400	$\text{pA}$ $\text{pA}$
		$-40\text{ °C} < T_A < +85\text{ °C}$			20	$\text{pA}$
Input Capacitance	$C_{DIFF}$	Differential		2.9		$\text{pF}$
	$C_{CM}$	Common-Mode		6.5		$\text{pF}$
Input Voltage Range	IVR		0		5	$\text{V}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to $4.5\text{ V}$		80	105	$\text{dB}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V}$ to $4.5\text{ V}$		110	140	$\text{dB}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$	●	4.98 4.97	4.988	$\text{V}$ $\text{V}$
		$I_L = 10\text{ mA}$	●	4.85 4.80	4.895	$\text{V}$ $\text{V}$
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$	●		12 20 30	$\text{mV}$ $\text{mV}$ $\text{mV}$
		$I_L = 10\text{ mA}$	●		105 150 200	$\text{mV}$ $\text{mV}$ $\text{mV}$
Output Current	$I_{OUT}$			$\pm 150$		$\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		16.3		$\Omega$
<b>POWER SUPPLY</b>						
Supply Current Per Amplifier	$I_S$	$I_{OUT} = 0\text{ mA}$	●	0.9	1 1.1	$\text{mA}$ $\text{mA}$
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$		80	103	$\text{dB}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$			5.1	$\text{V}/\mu\text{s}$
Unit Gain Bandwidth	UGB				11.6	$\text{MHz}$
Settling Time		To 0.01%			0.81	$\mu\text{s}$
THD + Noise	THD + N				0.0004	%
Phase Margin	$\Phi_M$				39	Degree
Channel Separation	$C_S$	$f = 10\text{ kHz}$			-115	$\text{dB}$
		$f = 100\text{ kHz}$			-110	$\text{dB}$
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$			6.2	$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$			5	$\text{nV}/\sqrt{\text{Hz}}$
Peak-to-Peak Voltage Noise	$e_{n-P-P}$	0.1 Hz to 10 Hz			1.86	$\mu\text{V}_{P-P}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$			0.4	$\text{fA}/\sqrt{\text{Hz}}$



The ● denotes the specification which apply over the full operating temperature range, otherwise specifications are at  $V_S = 2.7\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25\text{ °C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_S = 3.5\text{ V}$ , $V_{CM} = 1.75\text{ V}$ and $3.0\text{ V}$		40	160	$\mu\text{V}$
		$V_S = 2.7\text{ V}$ , $V_{CM} = 0\text{ V}$ to $2.7\text{ V}$	●		500	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40\text{ °C} < T_A < +125\text{ °C}$	●	0.2	1	$\mu\text{V}/\text{°C}$
Input Bias Current	$I_B$		●	0.6	3 1000	pA pA
		$-40\text{ °C} < T_A < +85\text{ °C}$			80	pA
Input Offset Current	$I_{OS}$		●		5 400	pA pA
		$-40\text{ °C} < T_A < +85\text{ °C}$			20	pA
Input Capacitance	$C_{DIFF}$	Differential		2.9		pF
	$C_{CM}$	Common-Mode		6.5		pF
Input Voltage Range	IVR		0		2.7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to $2.2\text{ V}$	70	95		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V}$ to $2.2\text{ V}$	100	135		dB
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$	●	2.65 2.65	2.683	V V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$	●		17 50 50	mV mV mV
Output Current	$I_{OUT}$			$\pm 50$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$			16.3	$\Omega$
<b>POWER SUPPLY</b>						
Supply Current Per Amplifier	$I_S$	$I_{OUT} = 0\text{ mA}$	●		0.9 1 1.1	mA mA mA
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$		80	103	dB
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$			5.1	$\text{V}/\mu\text{s}$
Unit Gain Bandwidth	UGB				11.6	MHz
Settling Time		To 0.01%			0.9	$\mu\text{s}$
THD + Noise	THD + N				0.0004	%
Phase Margin	$\phi_M$				37	Degree
Channel Separation	$C_S$	$f = 10\text{ kHz}$			-115	dB
		$f = 100\text{ kHz}$			-110	dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$			6.2	$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$			5	$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$			0.4	$\text{fA}/\sqrt{\text{Hz}}$
Peak-to-Peak Voltage Noise	$e_{n-P-P}$	0.1 Hz to 10 Hz			1.86	$\mu\text{V}_{P-P}$

Typical Performance Characteristics

Unless otherwise stated,  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ .

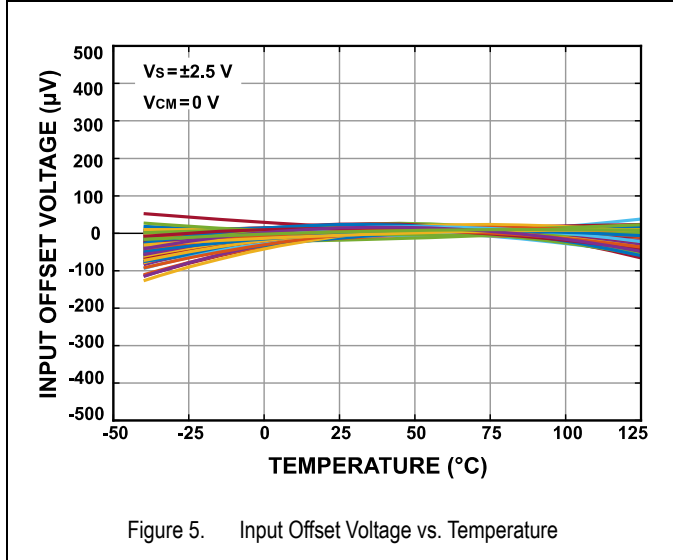


Figure 5. Input Offset Voltage vs. Temperature

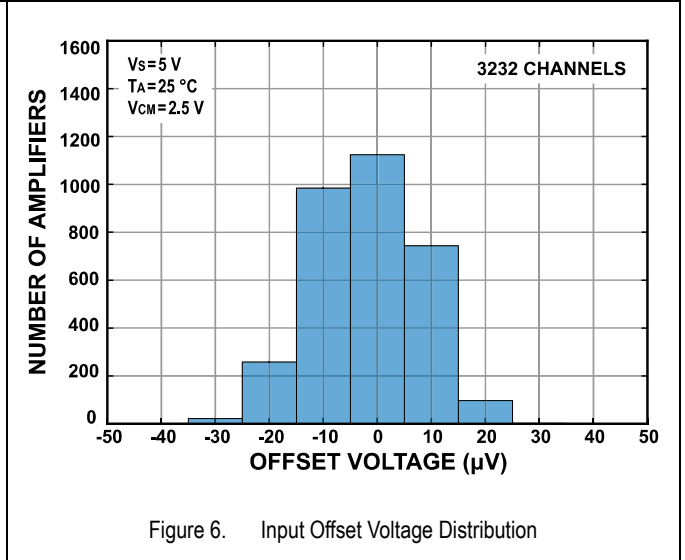


Figure 6. Input Offset Voltage Distribution

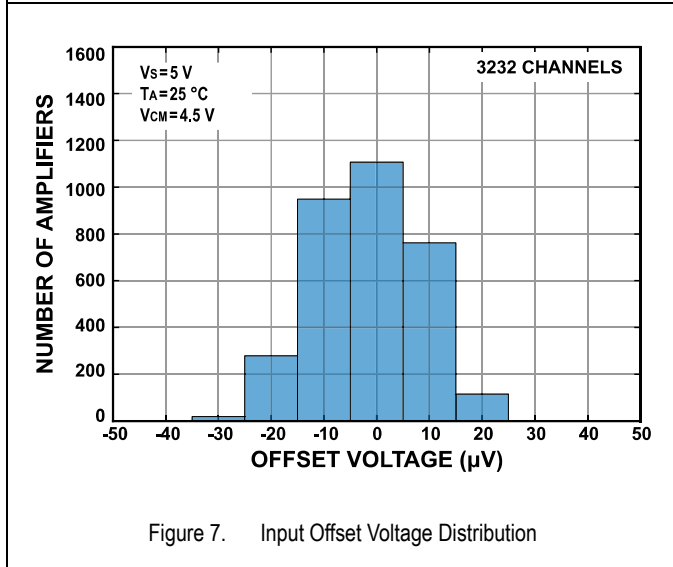


Figure 7. Input Offset Voltage Distribution

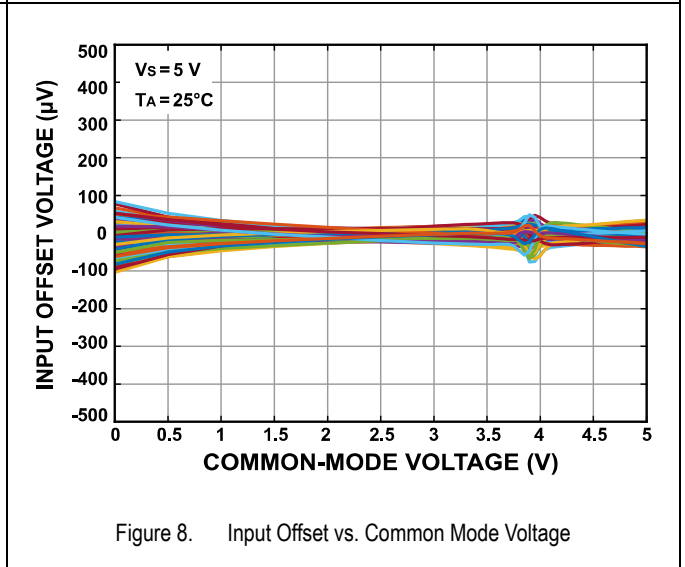


Figure 8. Input Offset vs. Common Mode Voltage

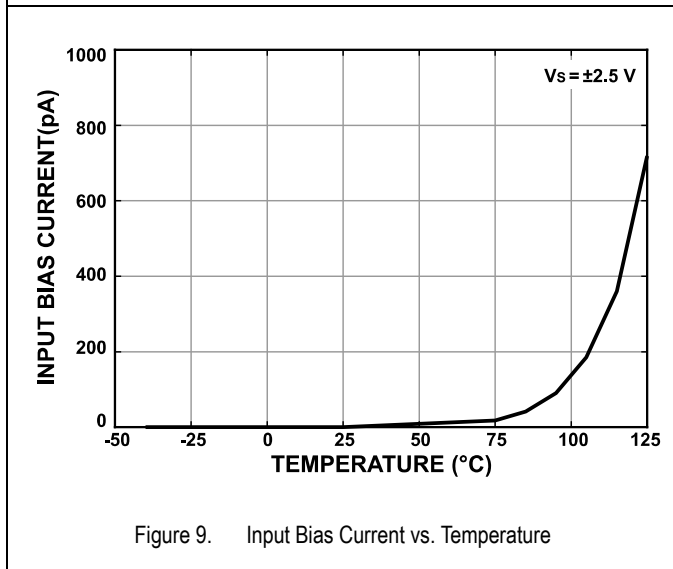


Figure 9. Input Bias Current vs. Temperature

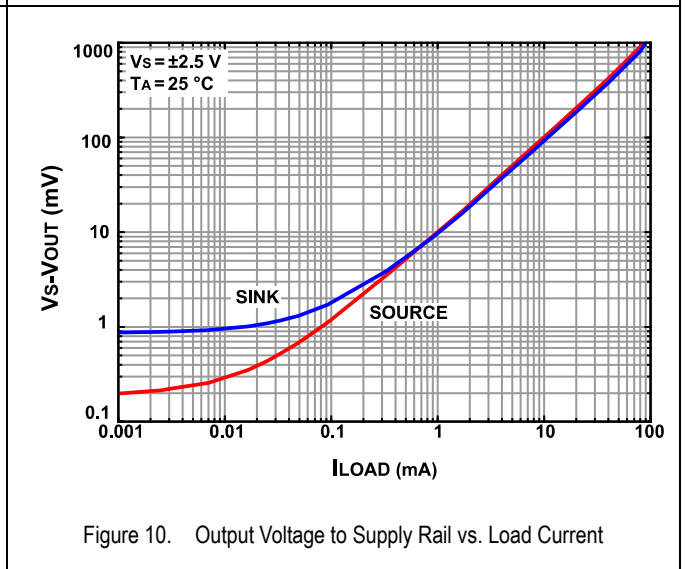
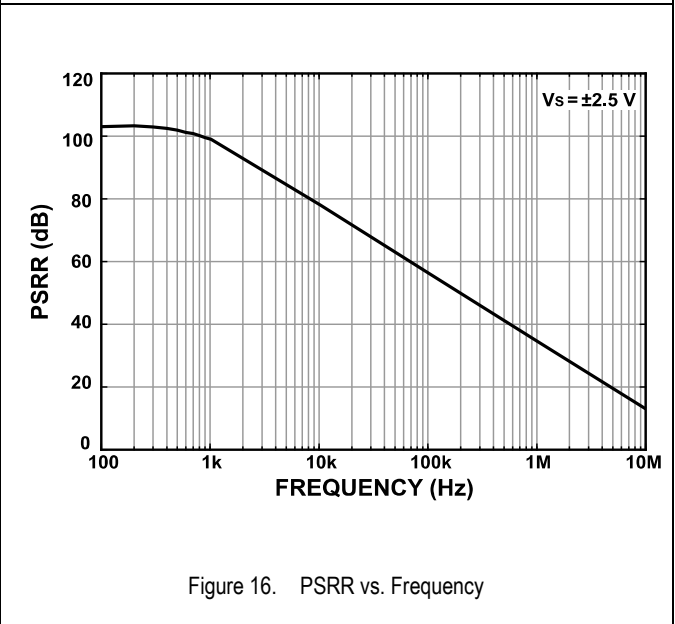
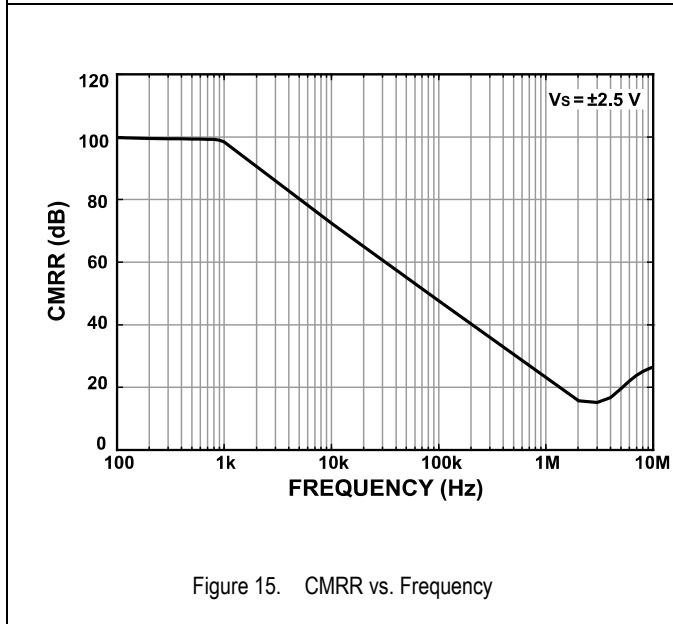
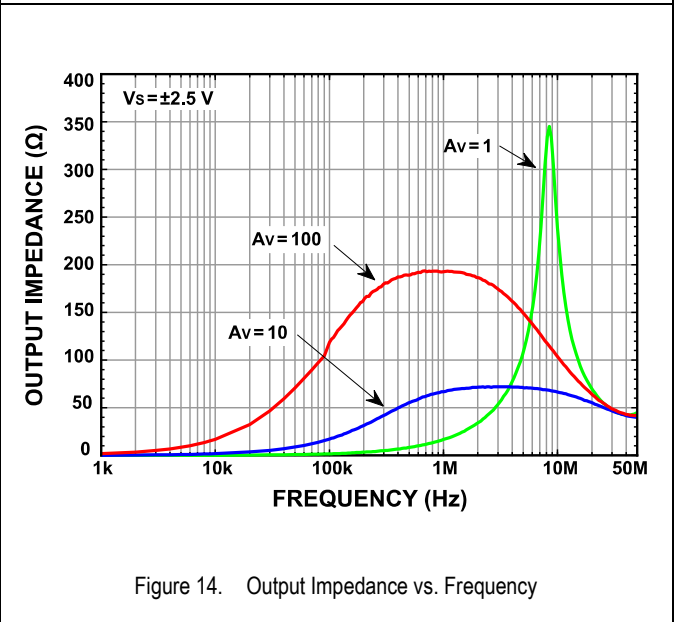
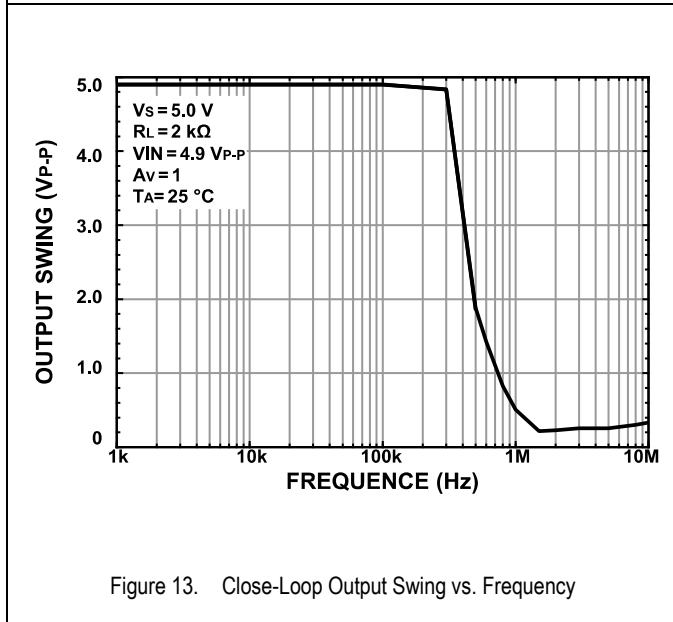
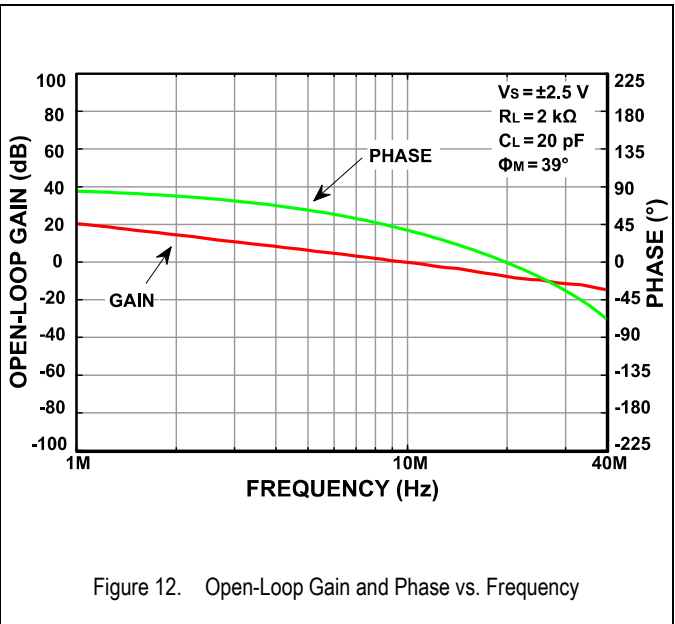
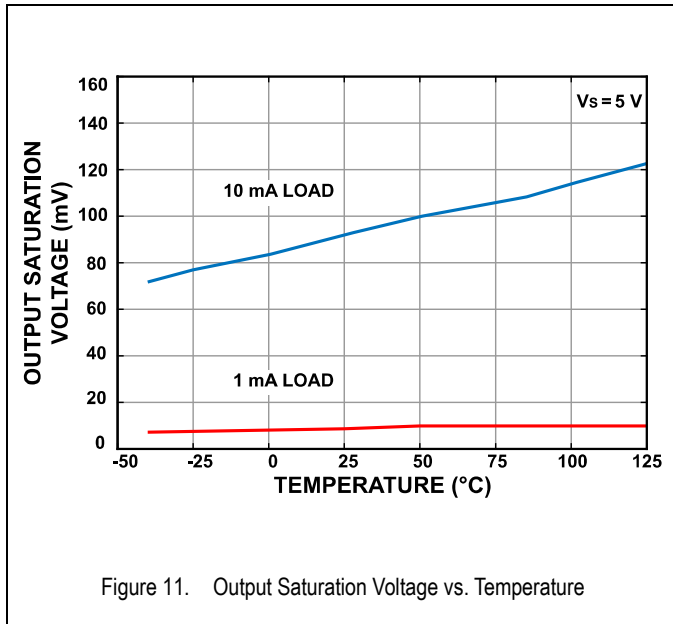


Figure 10. Output Voltage to Supply Rail vs. Load Current



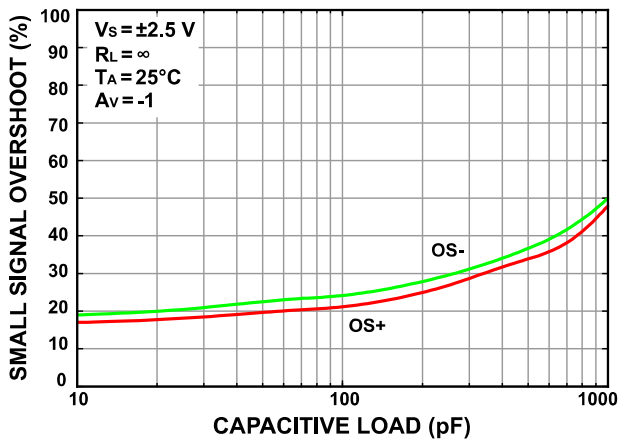


Figure 17. Small-Signal Overshoot vs. Load Capacitance

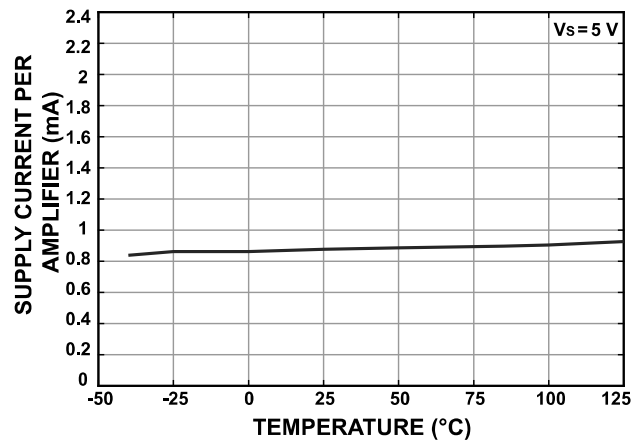


Figure 18. Supply Current vs. Temperature

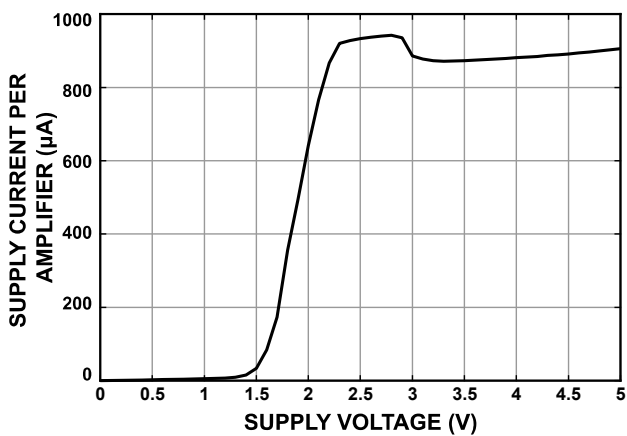


Figure 19. Supply Current per Amplifier vs. Supply Voltage

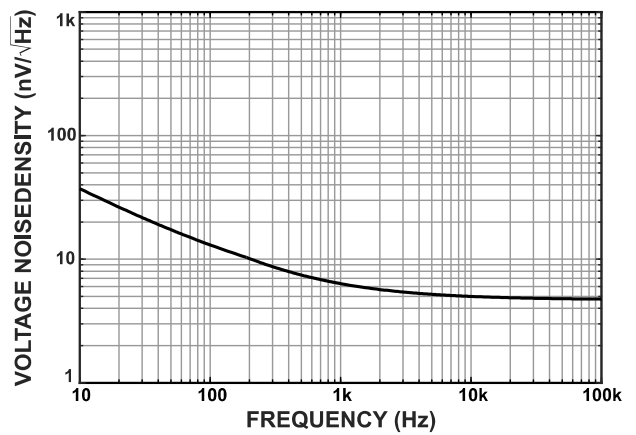


Figure 20. Voltage Noise Density vs. Frequency

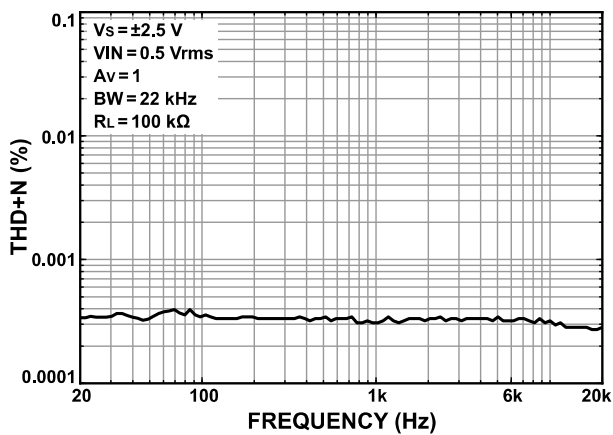


Figure 21. THD+Noise vs. Frequency

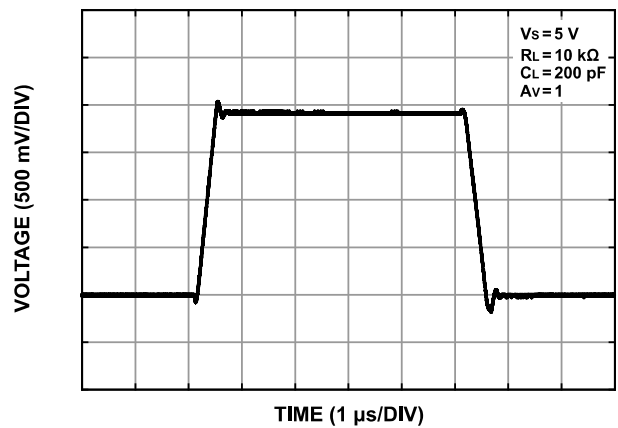
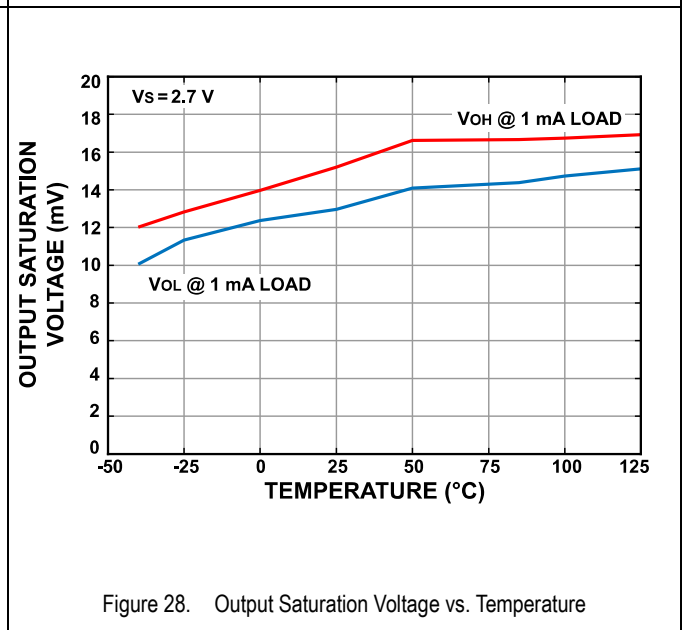
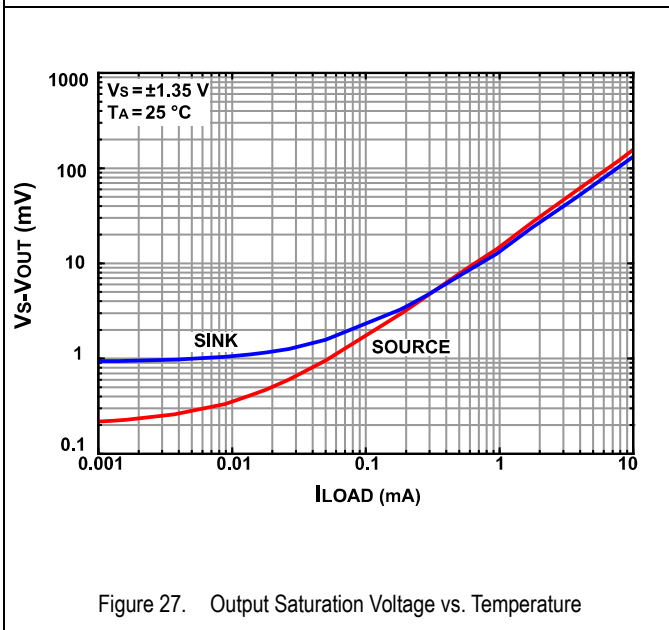
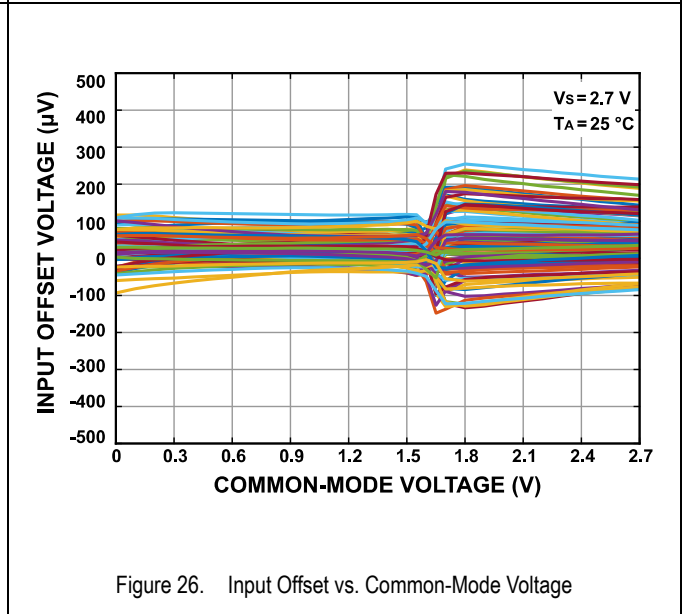
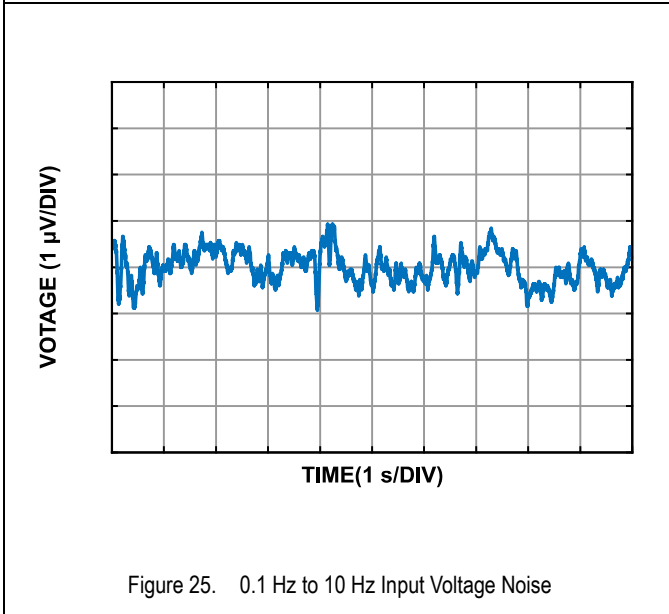
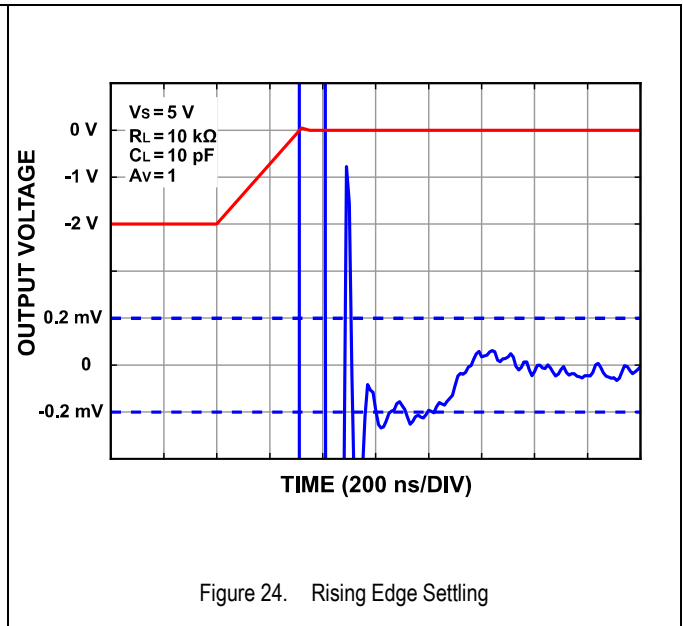
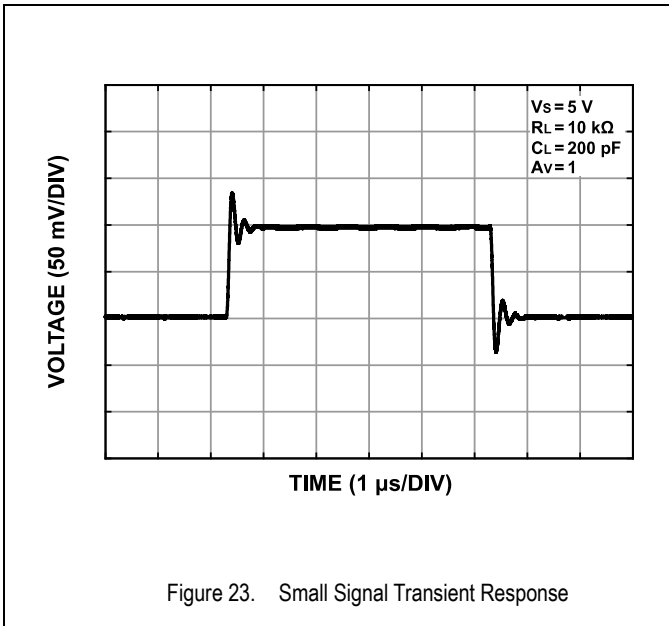
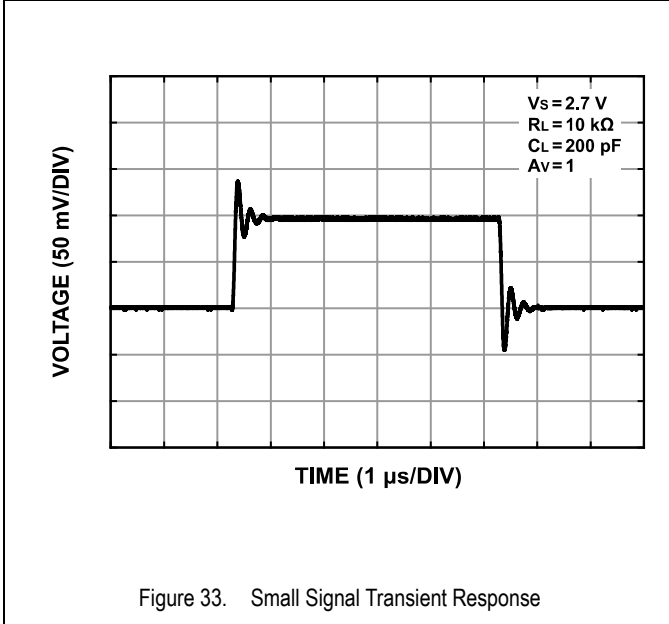
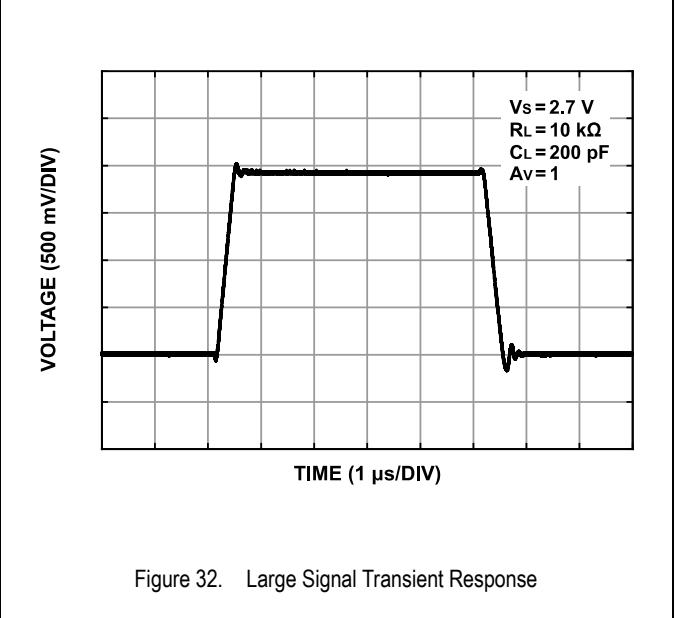
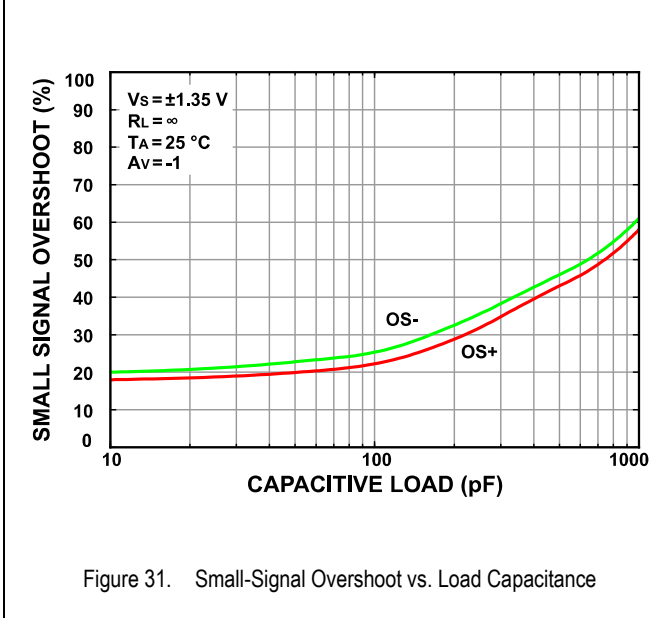
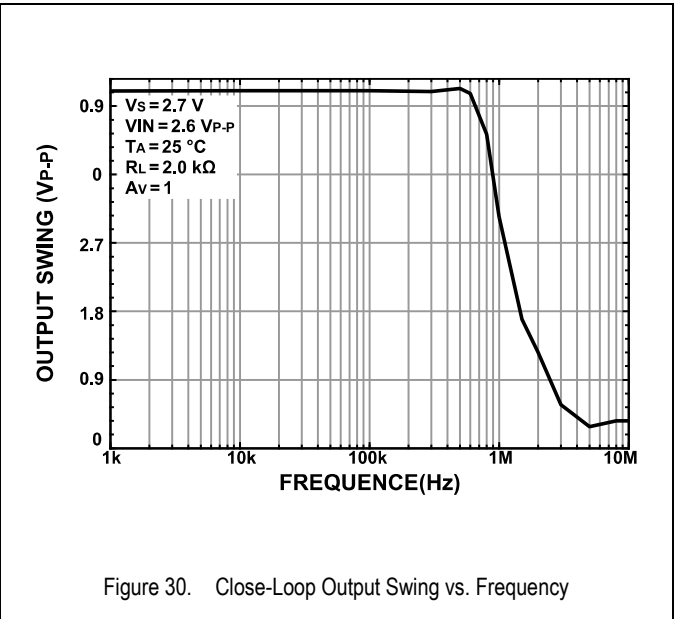
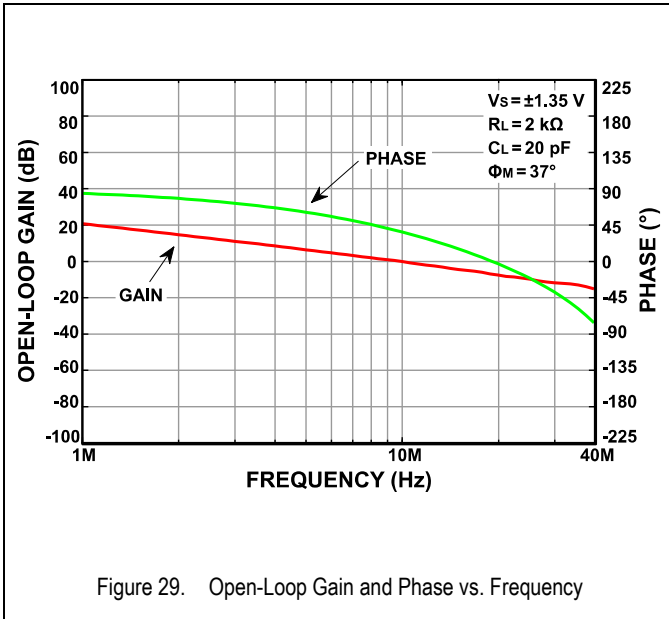


Figure 22. Large Signal Transient Response





## General Application Information

### Output Phase Reversal

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of an amplifier exceeds the maximum common-mode voltage. Phase reversal can cause permanent damage to the device and may result in system lockups. The ZJA3206-1, ZJA3206-2 and ZJA3206-4 and ZJA3207 do not exhibit phase reversal when input voltages are beyond the supplies.

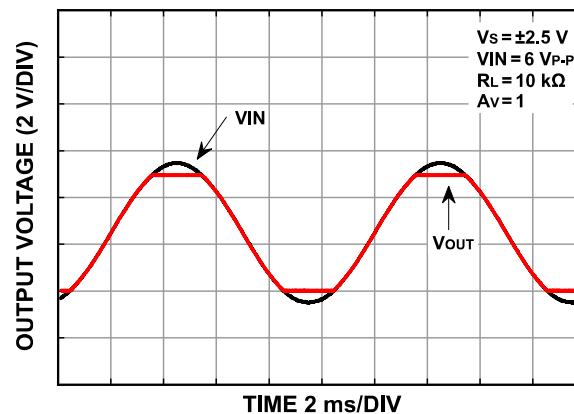


Figure 34. No Phase Reversal

### THD+Noise

ZJA3206/7 features low total harmonic distortion (THD) and excellent gain linearity, making these amplifiers a great choice for precision circuits with high closed-loop gain and for audio application circuits. Figure 35 demonstrates that when configured with positive unity gain (the worst case) and driving a 100 kΩ load, the total distortion and noise of ZJA3206/7 is approximately 0.0004%.

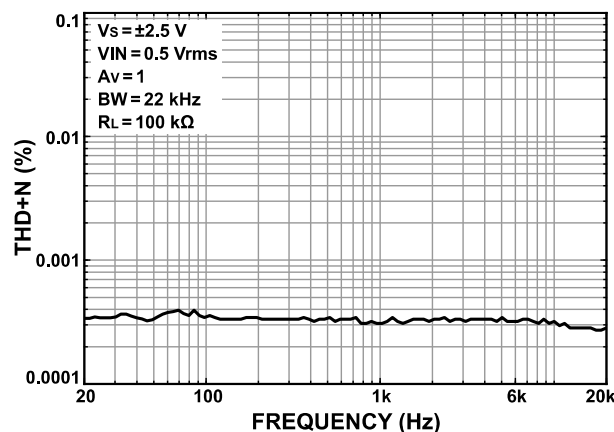


Figure 35. THD+N vs. Frequency

### Total Noise Including Source Resistors

The low input current noise and input bias current of the ZJA3206/7 make it the ideal amplifier for circuits with substantial input source resistance. Input offset voltage increases by less than 15 nV per 500 Ω of source resistance at room temperature. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_s)^2 + 4kTR_s}$$

Where:

- $e_n$  is the input voltage noise density of the parts.
- $i_n$  is the input current noise density of the parts.
- $R_S$  is the source resistance at the noninverting terminal.
- $K$  is Boltzman's constant ( $1.38 \times 10^{-23}$  J/K).
- $T$  is the ambient temperature in Kelvin ( $T = 273 + \text{°C}$ ).

For  $R_S < 3.9 \text{ k}\Omega$ ,  $e_n$  dominates and  $e_{nTOTAL} \approx e_n$ .

The current noise of the ZJA3206/7 is so low that its contribution does not become a significant term unless  $R_S$  is greater than  $165 \text{ M}\Omega$ , an impractical value for most applications.

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{nRMS} = e_{nTOTAL} \sqrt{BW}$$

Where BW is the bandwidth in Hertz.

Note that the above analysis is valid for frequencies larger than 300 Hz and assumes flat noise above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

### Settling Time

Settling time is the time required for the amplifier output to reach a stable state and remain within a percentage of its step value. The pulse has been applied to the input terminal. Thanks to its high slew rate of  $5.1 \text{ V}/\mu\text{s}$  and  $11.6 \text{ MHz}$  bandwidth, ZJA3206/7 settles to within 0.01% in less than 810 ns, for a 2 V step in positive unity gain. This makes it an excellent choice as a buffer at the output of DACs whose settling time is typically less than  $1 \mu\text{s}$ .

In addition to fast settling time and fast slew rate, the low offset voltage drift and input offset current of ZJA3206/7 allows full accuracy of a 16-bit converter over the entire operating temperature range.

### Overload Recovery Time

Overload recovery, also known as overspeed recovery, refers to the time it takes the output of an amplifier to recover from a saturated condition to its linear region. This recovery time is particularly long, which is crucial for the application of amplifiers that must promptly response to small signal in the presence of excessive large transient. Figure 36 shows the positive overload recovery of ZJA3206/7. The output recovers from saturation within approximately  $1.2 \mu\text{s}$ .

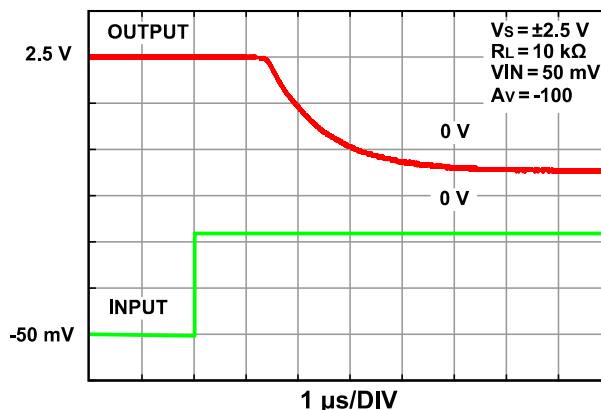


Figure 36. Positive Overload Recovery



The negative overdrive recovery time is also approximately 1.2  $\mu\text{s}$  as shown in Figure 37. In addition to the fast recovery time, ZJA3206/7 show excellent positive and negative recovery time symmetry. This is an important feature of transient signal rectification, as the output signal is kept equally undistorted throughout any given period.

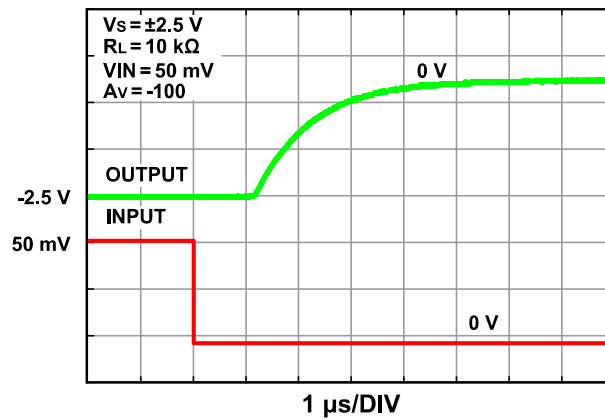


Figure 37. Negative Overload Recovery

### Capacitive Load Drive

ZJA3206/7 is unconditionally stable under all gains in both inverted and non-inverting configurations. It is capable of directly driving up to 10 nF capacitive load, without oscillation under positive unity gain configuration (worst case configuration). However, as with most amplifiers, driving larger capacitive loads in a unity gain configuration may cause excessive overshoot and/or ringing, or even oscillation. A simple snubber network reduces the amount of overshoot and ringing significantly. The advantage of this configuration is that the output swing of the amplifier will not decrease, as  $R_S$  is located outside the feedback loop.

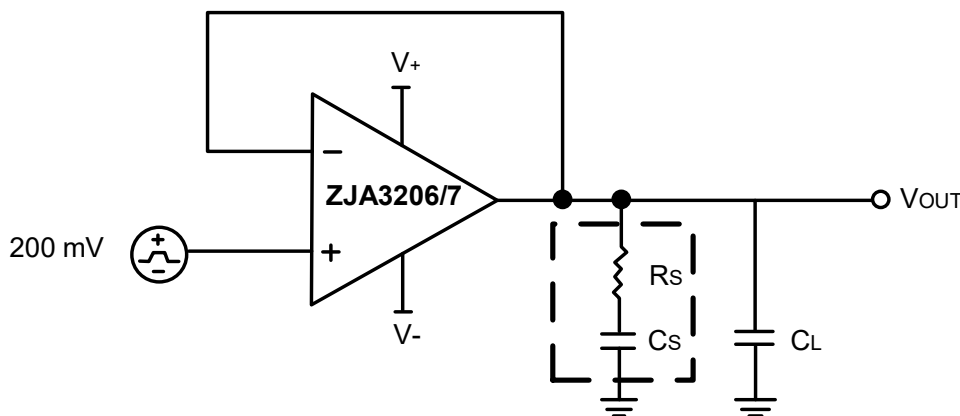


Figure 38. Snubber Network Configuration

Figure 39 shows a scope plot of the output of ZJA3206/7 in response to a 100 mV pulse. The circuit is configured as unity gain (worst case), with a load capacitance of 200 pF, and no ringing is observed at the output.

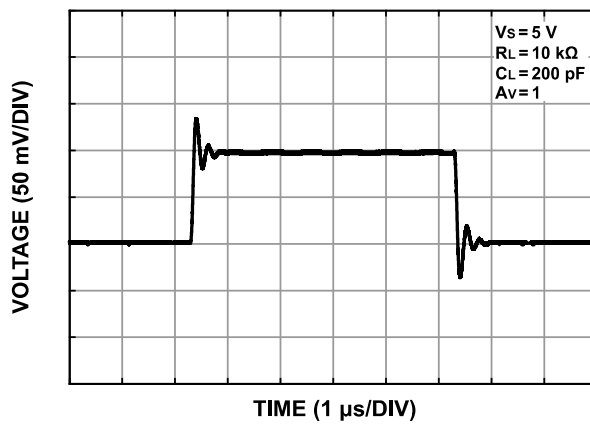


Figure 39. ZJA3206/7 Directly Drive Large Capacitive Load

However, further increase of capacitive load eventually undermines stability and leads to ringing as shown in Figure 40 for Load of 10 nF. By adding a simple snubber network, it is able to eliminate the ringing as displayed in Figure 41.

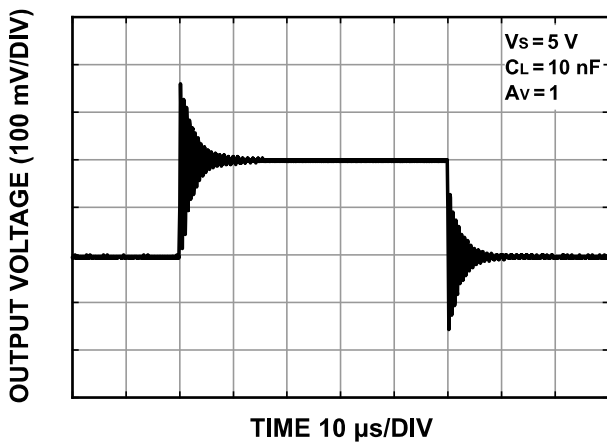


Figure 40. Direct Capacitive Load Drive of 10 nF

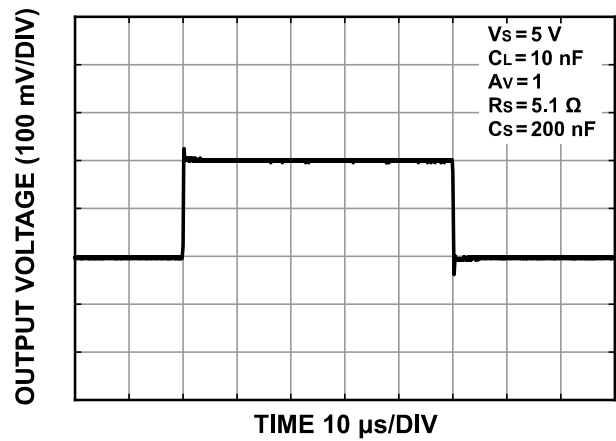


Figure 41. Capacitive Load Drive of 10 nF with Snubber

The optimal values of  $R_s$  and  $C_s$  depend on the load capacitance and input capacitance of ZJA3206/7, which is summarized in Table 1.

$C_L$	$R_s$ ( $\Omega$ )	$C_s$
1 nF	100	10 nF
2 nF	50	10 nF
5 nF	20	10 nF

Table 1. Optimum Values for Capacitive Loads

### Open-Loop Gain and Phase Response

In addition to impressive low noise, low offset voltage and offset current, ZJA3206/7 has excellent loop gain and phase response even when driving heavy resistive or capacitive load. When the output is loaded with 2.5 k $\Omega$  resistor, ZJA3206/7 has unity gain frequency of 11.6 MHz and a phase margin of 39°. Comparing to amplifiers with similar bandwidth, ZJA3206/7 is much more stable, showing much less peaking in transient response and thus much faster settling time.

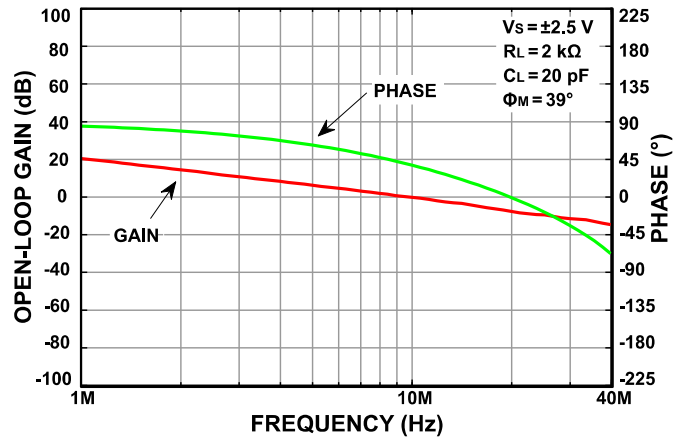


Figure 42. Frequency Response of ZJA3206/7

### Photodiode Circuits

Common applications for I-V conversion include photodiode circuits, where the amplifier is used to convert a current, generated by a photo diode placed at the inverting input terminal, into an output voltage.

ZJA3206/7's low input bias current, wide bandwidth, and low noise make it an excellent choice for various photodiode applications, including fiber optic controls, motion sensors, and bar code readers.

The circuit shown in Figure 43 uses a silicon diode with zero bias voltage. This is known as a Photovoltaic Mode; this configuration limits the overall noise and is suitable for instrumentation applications.

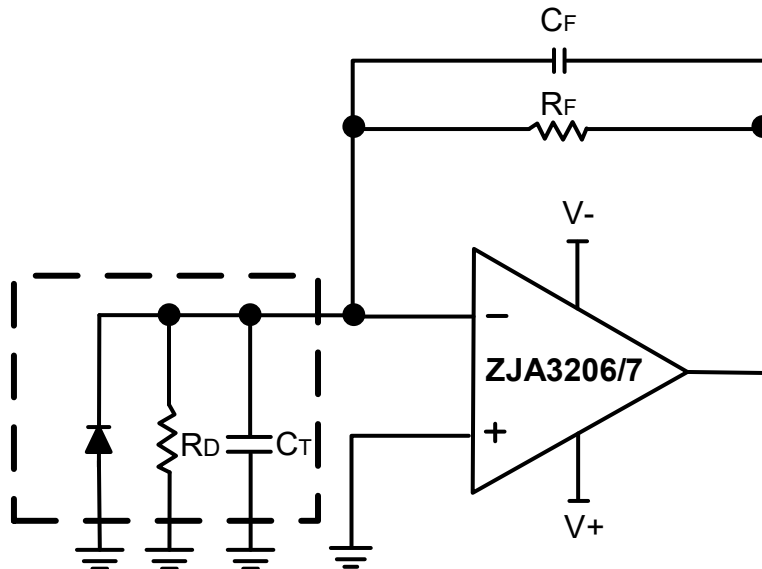


Figure 43. Equivalent Preamplifier Photodiode Circuit

A larger signal bandwidth can be attained at the expense of additional output noise. The total input capacitance ( $C_T$ ) consists of the sum of the diode capacitance (typically 3 pF to 4 pF) and the amplifier's input capacitance (12 pF), which includes external parasitic capacitance.  $C_T$  creates a pole in the frequency response, which may lead to an unstable system. To ensure stability and optimize the bandwidth of the signal, a capacitor is placed in the feedback loop of the circuit shown in Figure 43. It creates a zero and yields a bandwidth whose corner frequency is  $1 / (2\pi (R_F C_F))$ .

The value of  $R_F$  can be determined by the ratio  $V/I_D$ , where  $V$  is the desired output voltage of the op amp and  $I_D$  is the diode current.

For example, if  $I_D$  is 100  $\mu\text{A}$  and a 10 V output voltage is desired,  $R_F$  should be 100 k $\Omega$ .  $R_D$  is a junction resistance that drops typically by a factor of 2 for every 10  $^{\circ}\text{C}$  increase in temperature. A typical value for  $R_D$  is 1000 M $\Omega$ . Since  $R_D \gg R_F$ , the circuit behavior is not impacted by the effect of the junction resistance. The maximum signal bandwidth is

$$f_{MAX} = \sqrt{\frac{f_T}{2\pi R_F C_T}}$$

where  $f_T$  is the unity gain frequency of the amplifier.

Using the parameters above,  $C_F \approx 1$  pF, which yields a signal bandwidth of about 2.6 MHz.

$$C_F = \sqrt{\frac{C_T}{2\pi R_F f_T}}$$

where  $f_T$  is the unity gain frequency of the op amp, achieves a phase margin,  $\Phi_m$ , of approximately 45 $^{\circ}$ .

A higher phase margin can be obtained by increasing the value of  $C_F$ . Setting  $C_F$  to twice the previous value yields approximately  $\Phi_m = 65^{\circ}$  and a maximally flat frequency response, but reduces the maximum signal bandwidth by 50%.

Outline Information

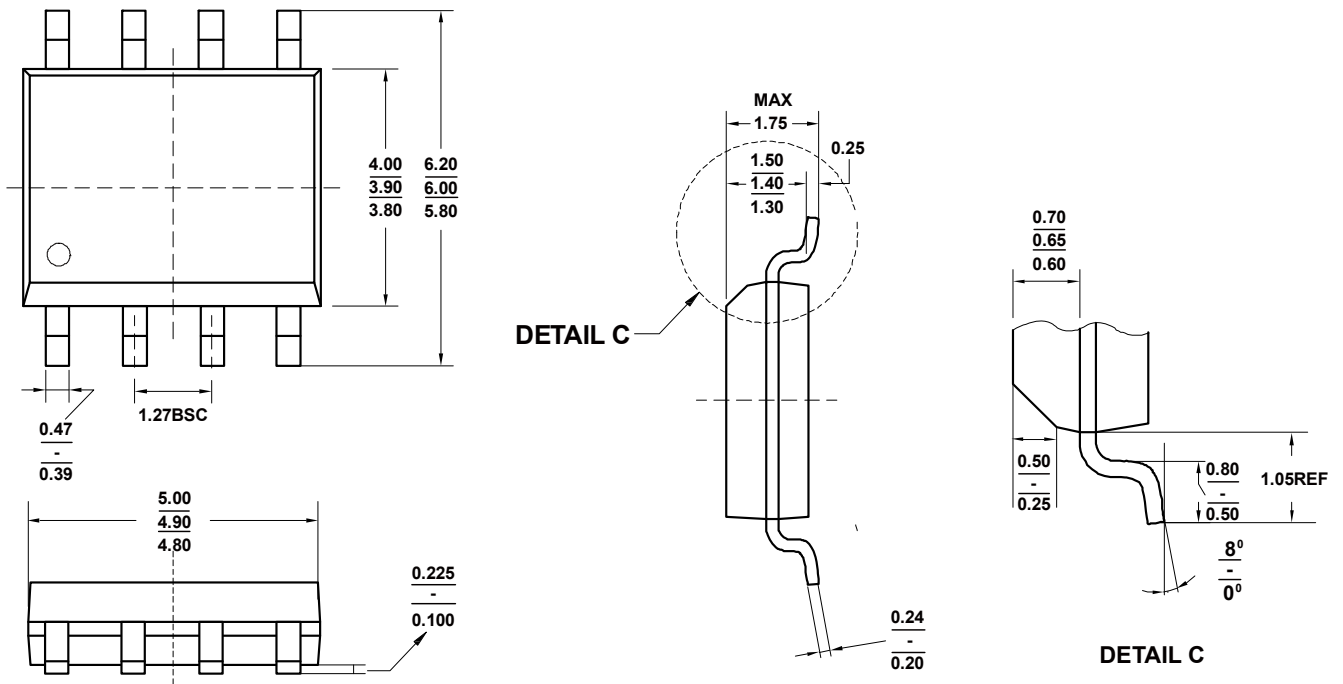


Figure 44. 8-Lead SOIC Package Dimensions shown in millimeters

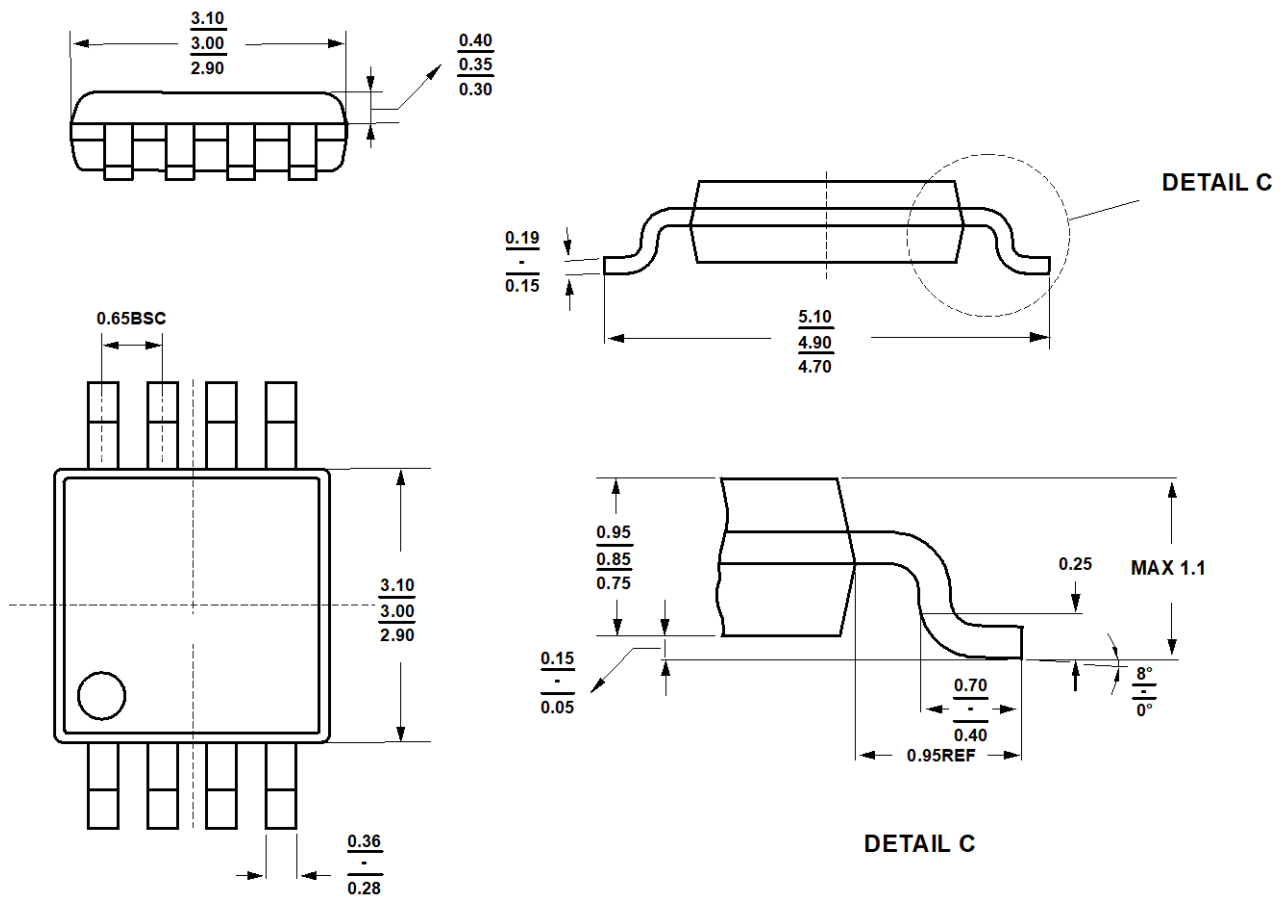


Figure 45. 8-Lead MSOP Package Dimensions shown in millimeters

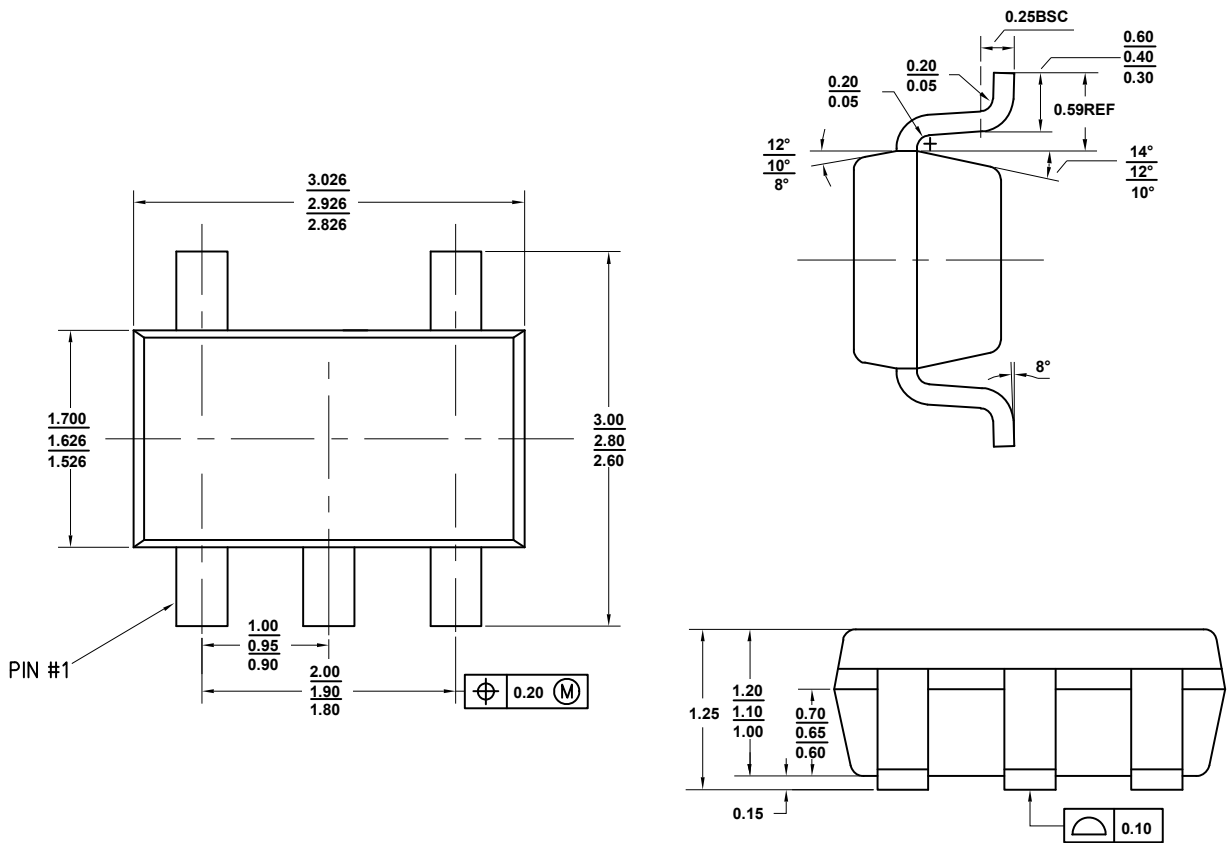


Figure 46. 5-Lead SOT23 Package Dimensions shown in millimeters

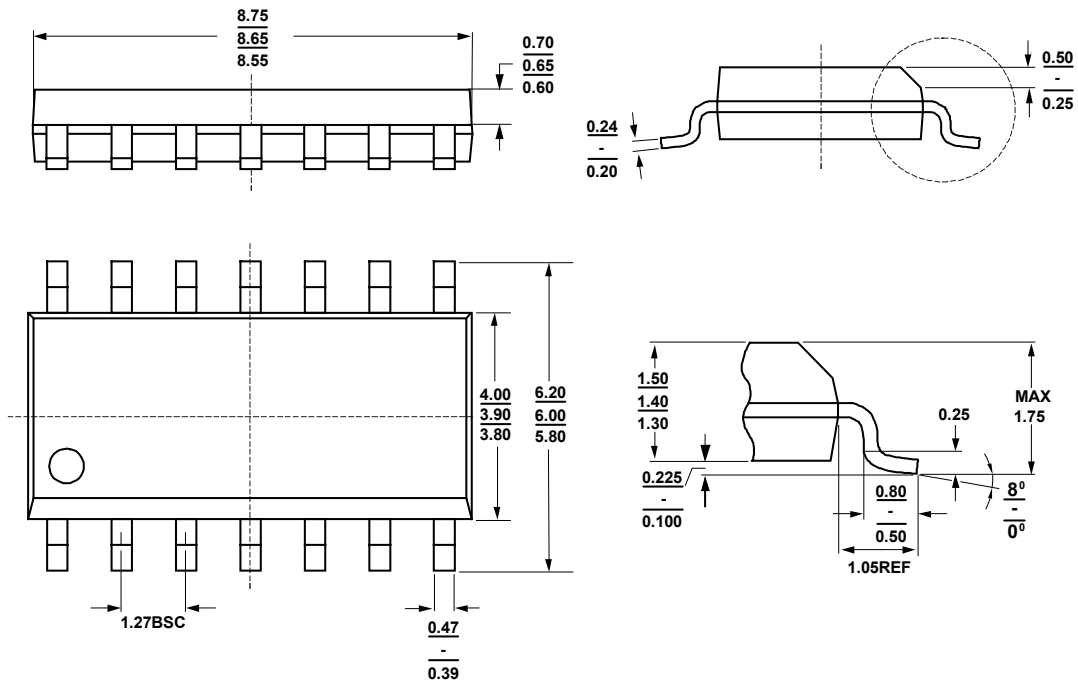


Figure 47. 14-Lead SOIC Package Dimensions shown in millimeters

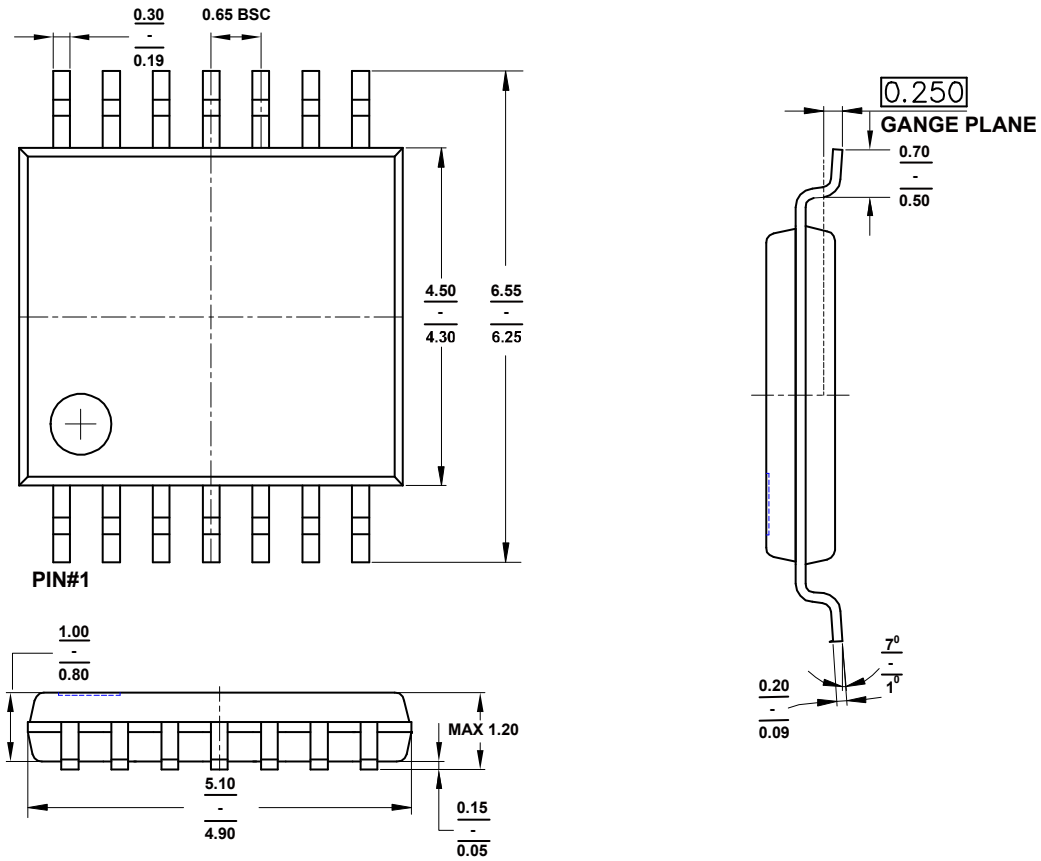


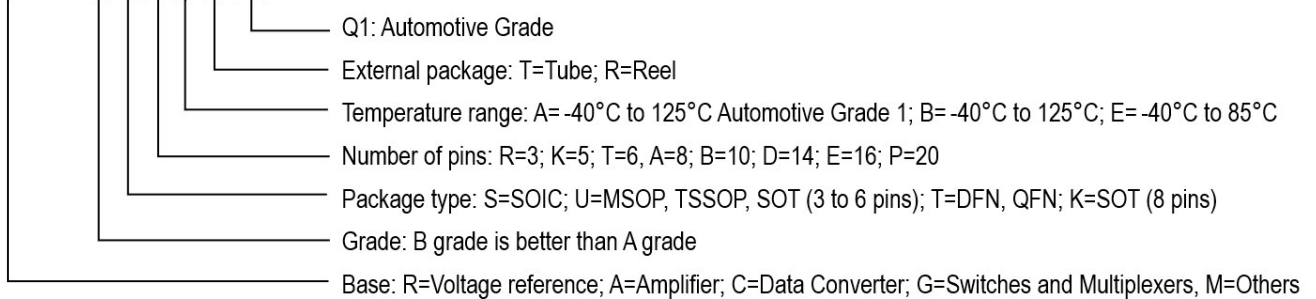
Figure 48. 14-Lead TSSOP Package Dimensions shown in millimeters

Ordering Guide

Model	Orderable Device	Status <sup>1</sup>	Channels	Package	Temperature Range (°C)	External Package
ZJA3206-1	ZJA3206-1AUKBR	ACTIVE	1	SOT23-5	-40 to +125	7" Reel
ZJA3206-2	ZJA3206-2ASABT	ACTIVE	2	SOIC-8	-40 to +125	Tube
	ZJA3206-2ASABR	ACTIVE				13" Reel
	ZJA3206-2AUABT	ACTIVE		MSOP-8		Tube
	ZJA3206-2AUABR	ACTIVE				13" Reel
ZJA3206-4	ZJA3206-4ASDBT	PREVIEW	4	SOIC-14	-40 to +125	Tube
	ZJA3206-4ASDBR	PREVIEW				13" Reel
	ZJA3206-4AUDBT	PREVIEW		TSSOP-14		Tube
	ZJA3206-4AUDBR	PREVIEW				13" Reel
ZJA3207	ZJA3207AUKBR	PREVIEW	1	SOT23-5	-40 to +125	7" Reel

Product Order Model

ZJXXXXX X X X X X Q1



<sup>1</sup> The marketing status values are defined as follows:

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**ACTIVE:** Product device recommended for new designs.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but ZJW does not recommend using this part in a new design.

**LIFEBUY:** ZJW has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**OBSOLETE:** ZJW has discontinued the production of the device.



## Related Parts

Part Number	Description	Comments
<b>ADC</b>		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2003/2013		Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2005/2015		Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB
ZJC2008/2018		Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB	
ZJC2100/1-16	16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2102/3-16	16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
ZJC2102/3-14	14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB	
ZJC2104/5-16	16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
<b>DAC</b>		
ZJC2541-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or $V_{REF}/2$ (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2543-18/16/14		
ZJC2542-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or $V_{REF}/2$ (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
ZJC2544-18/16/14		
<b>Amplifier</b>		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 $\mu$ V max Vos, 0.5 $\mu$ V/ $^{\circ}$ C max TCvos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3001-1/2/4		
ZJA3018-2	OVP $\pm$ 75 V, 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 $\mu$ V max Vos, 0.5 $\mu$ V/ $^{\circ}$ C max TCvos, 25 pA max Ibias, 0.5 mA/ch, OVP $\pm$ 75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3008-2		
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/ $\mu$ S, 50 $\mu$ V max Vos, 1 $\mu$ V/ $^{\circ}$ C max TCvos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 $\mu$ V max Vos, 1 $\mu$ V/ $^{\circ}$ C max TCvos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G=1), 25 pA max Ib, 25 $\mu$ V max Vosi, $\pm$ 2.4 V to $\pm$ 18 V, -40 $^{\circ}$ C to 125 $^{\circ}$ C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G $\geq$ 10)	CMRR 120 dB min (G=10), 25 pA max Ibias, 25 $\mu$ V max Vosi, 1.2 MHz BW (G=10)
ZJA3676/7	Low power, G=1 Single/Dual 36 V difference amplifier	Input protection to $\pm$ 65 V, CMRR 104 dB min (G=1), Vos 100 $\mu$ V max, gain error 15 ppm max, 500 kHz BW (G=1), 330 $\mu$ A/channel, 2.7 V to 36 V
ZJA3678/9		
ZJA3669	High Common-Mode Voltage Difference Amplifier	$\pm$ 270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/ $\mu$ S, 50 nS to 16-bit, 50 $\mu$ V max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 $\mu$ V/ $^{\circ}$ C max TCvos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 $\mu$ V max Vosi, 625 kHz BW (G=10), 3.3 mA Iq, $\pm$ 2.4 V to $\pm$ 18 V
<b>Voltage Reference</b>		
ZJR1004	40 V supply precision voltage reference	$V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10$ V, 5 ppm/ $^{\circ}$ C max drift -40 $^{\circ}$ C to 125 $^{\circ}$ C
ZJR1001/2	5.5 V low power voltage reference (ZJR1001 with noise filter option)	$V_{OUT} = 2.048/2.5/3/3.3/4.096/5$ V, 5 ppm/ $^{\circ}$ C max drift -40 $^{\circ}$ C to 125 $^{\circ}$ C, $\pm$ 0.05% initial error, 130 $\mu$ A, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1003		
<b>Switches and Multiplexers</b>		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to $\pm$ 50 V power on & off, latch-up immune, Ron 270 $\Omega$ , 14.8 pC, $t_{ON}$ 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 $\Omega$ , 14.8 pC charge injection, $t_{ON}$ 166 nS
<b>Quad Matching Resistor</b>		
ZJM5400	$\pm$ 75 V precision match resistors	Mismatch <100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV