

Features

- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
- Supports the requirements of Telcordia GR-1244 Stratum 3 and GR-253, ITU-T G.812, G.813
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces
- Meets the SONET/SDH jitter generation requirements up to OC-48/STM-16
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
- Programmable output synthesizer generates telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
- Generates several styles of telecom frame pulses with selectable pulse width, polarity and frequency
- Internal state machine automatically controls mode of operation (free-run, locked, holdover)

Ordering Information

ZL30142GGG 64 Pin CABGA Trays
 ZL30142GGG2 64 Pin CABGA* Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
- Provides automatic reference switching and holdover during loss of reference input
- Supports master/slave configuration and dynamic input to output delay compensation for AdvancedTCA™
- Configurable input to output delay and output to output phase alignment

Applications

- ITU-T G.8262 System Timing Cards which support 1 GbE interfaces
- Telcordia GR-253 Carrier Grade SONET/SDH Stratum 3 System Timing Cards
- Controllable DCO for IEEE1588v2 ToP (Timing over Packet) Client Applications.

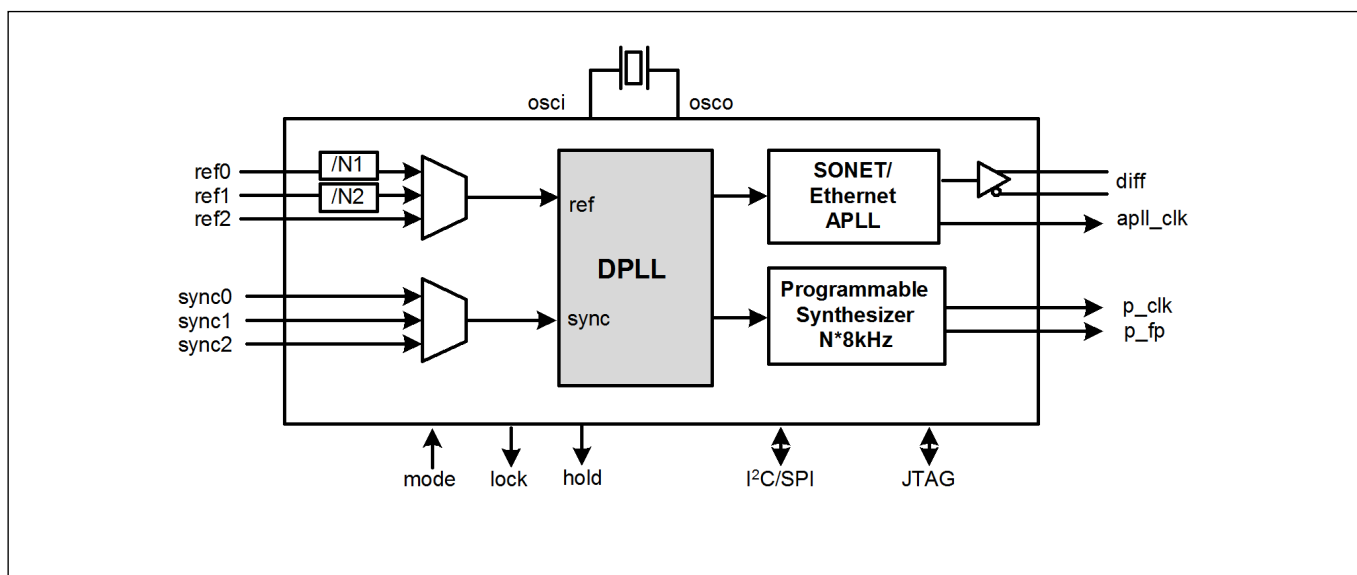


Figure 1 - Functional Block Diagram

Table of Contents

1.0 Pin Diagram	11
2.0 High Level Overview	12
2.1 DPLL Features	13
2.2 DPLL Mode Control	14
2.2.1 DPLL Mode Of Operation	15
2.2.1.1 ToP (Timing over Packet) Client Mode	15
2.3 Loop Bandwidth	15
2.4 Pull-in/hold-in Range	16
2.5 Phase Slope Limiting	16
2.6 Hitless Reference Switching	16
2.7 Free-run Frequency Offset	16
2.8 Holdover	17
2.9 Reference and Sync Inputs	17
2.10 Reference Input Selection	19
2.11 Reference Monitoring	19
2.12 Sync Monitoring	22
2.13 Reference Monitoring for Custom Configurations	23
2.14 Output Clocks and Frame Pulses	25
2.14.1 Output Clock and Frame Pulse Squelching	27
2.14.2 Disabling Output Clocks and Frame Pulses	27
2.14.3 Disabling Output Synthesizers	27
2.15 Configurable Input-to-Output and Output-to-Output Delays	28
2.16 Master/Slave Configuration	29
2.17 Master Clock Interface	30
2.18 Clock Oscillator	30
2.19 Power Up/Down Sequence	30
2.20 Power Supply Filtering	30
2.21 Reset Circuit	31
2.22 APLL Filter Components and Recommended Layout	31
2.23 Serial Interface	33
2.23.1 Serial Peripheral Interface	33
2.23.2 SPI Functional Waveforms	34
2.23.3 I2C Interface	35
3.0 Software Configuration	37
3.1 Interrupts	37
3.2 Extended Page Registers	37
3.3 Multi-byte Register Values	38
4.0 Detailed Register Map	46
5.0 AC and DC Electrical Characteristics	91
6.0 Thermal Characteristics	103

List of Figures

Figure 1 - Functional Block Diagram	1
Figure 2 - Typical Application of the ZL30142	12
Figure 3 - Automatic Mode State Machine	14
Figure 4 - Reference and Sync Inputs	17
Figure 5 - Output Frame Pulse Alignment	18
Figure 6 - Behaviour of the Guard Soak Timer during CFM or SCM Failures	20
Figure 7 - Stratum 3/G.813 Option I Frequency Acceptance and Rejection Ranges	21
Figure 8 - Reference Monitoring Block Diagram	22
Figure 9 - Sync Monitoring	22
Figure 10 - Defining SCM Limits for Custom Configurations	23
Figure 11 - Custom CFM Configuration for 50 MHz	24
Figure 12 - Output Clock Configuration	25
Figure 13 - Phase Delay Adjustments	28
Figure 14 - Typical Master/Slave Configuration	29
Figure 15 - Clock Oscillator Circuit	30
Figure 16 - Typical Power-Up Reset Circuit	31
Figure 17 - APLL Filter Component Values	31
Figure 18 - Recommended APLL Filter Layout	32
Figure 19 - Serial Interface Configuration	33
Figure 20 - LSB First Mode - One Byte Transfer	34
Figure 21 - MSB First Mode - One Byte Transfer	34
Figure 22 - Example of a Burst Mode Operation	35
Figure 23 - I2C Data Write Protocol	35
Figure 24 - I2C Data Write Protocol	35
Figure 25 - ZL30142 I2C 7-bit Slave Address	36
Figure 26 - I2C Data Write Burst Mode	36
Figure 27 - I2C Data Read Burst Mode	36
Figure 28 - Memory Map Organization	37
Figure 29 - Accessing Multi-byte Register Values	38
Figure 30 - Sync Input Timing	93
Figure 31 - Input To Output Timing	94
Figure 32 - Output Duty Cycle	95
Figure 33 - Output Clock Fall and Rise Times	96
Figure 34 - E1 Output Frame Pulse Timing	97
Figure 35 - Serial Peripheral Interface Timing - LSB First Mode	98
Figure 36 - Serial Peripheral Interface Timing - MSB First Mode	98
Figure 37 - I2C Serial Microport Timing	99

List of Tables

Table 1 - DPLL Features	13
Table 2 - DPLL Default Mode Selection	15
Table 3 - DPLL Loop Bandwidth	15
Table 4 - DPLL Pull-in Range	16
Table 5 - DPLL Phase Slope Limiting	16
Table 6 - Set of Pre-Defined Auto-Detect Clock Frequencies	17
Table 7 - Set of Pre-Defined Auto-Detect Sync Frequencies	19
Table 8 - Frequency Out of Range Limits	21
Table 9 - APLL LVCMOS Output Clock Frequencies	25
Table 10 - APLL Differential Output Clock Frequencies	26
Table 11 - Output Frame Pulse Frequencies	26
Table 12 - Programmable Synthesizer Frame Pulse Widths	27
Table 13 - Master Oscillator Frequency Accuracy	30
Table 14 - Register Map	39
Table 15 - Serial Peripheral Interface Timing	98
Table 16 - I2C Serial Microport Timing	99
Table 17 - Thermal Data	103

Change Summary

The following table captures changes from January 2011 issue to March 2013 issue.

Page	Item	Change
Multiple	Zarlink logo and name reference	Updated to Microsemi® logo and name.

Below are the changes from the April 2010 issue to the January 2011 issue.

Page	Item	Change
19	Table 7	Added 1 Hz to auto-detect sync frequencies.
52	Register "detected_sync_0" (0x14)	Bit(2:0) and (6:4), added 1 Hz.
53	Register "detected_sync_1" (0x15)	Bit(2:0), added 1 Hz.
70	Register "Page Pointer" (0x64)	Added register description.
85	Register "1Hz_enable (08_0x71)"	Added register description.
104	Package Drawing	Added package drawing.
105	Disclaimer	Added disclaimer.

Below are the changes from the July 2009 issue to the April 2010 issue.

Page	Item	Change
83	Page_Address: 01_0x75 to Page_Address: 01_0x7C	Added Registers.
86	Page_Address: 0A_0x72	Replaced table.
86	Page_Address: 0A_0x76 to Page_Address: 0A_0x7D	Added Registers.

Below are the changes from the February 2009 issue to the July 2009 issue.

Page	Item	Change
13	Table 1 -, "DPLL Features"	Updated lock times and added ToP client mode.
15	Section 2.2.1.1, "ToP (Timing over Packet) Client Mode"	Added section to describe ToP Client Mode
23	2.13, "Reference Monitoring for Custom Configurations"	Added instructions for SCM and CFM limits when using low frequency customs frequencies.
25	2.14, "Output Clocks and Frame Pulses"	Added reference to ZLAN-254.
26	Table 11 -, "Output Frame Pulse Frequencies"	Added 1 Hz output option.
56, 57	Register Address: 0x1D, Register Address: 0x1E	Included register default values.
58	Register Address: 0x1F	Added ToP Client Mode
65	Register Address: 0x3E	Added 1 Hz

Page	Item	Change
65	Register Address: 0x3F	Updated descriptions for 1Hz operation.
79	Register Address: 01_0x65, Register Address: 01_0x66, Register Address: 01_0x67 and Register Address: 01_0x68	Corrected description.
80	Register Addresses 01_0x69 to 01_0x70	Added DCO_Phase_0 to DCO_Phase_7 registers
82	Register Addresses: 01_0x71 to 01_0x74	Added Local_Time_0 to Local_Time_4 registers
85	Register Address: 0A_0x6C	Added DCO_Update register
86	Register Address: 0A_0x71	Added DCO_update_interval register
83	Register Address: 0A_0x72	Added ToP_1Hz_Alignment register
88	Register Address: 0F_0x6E	Added ToP_isr register
89	Register Address: 0F_0x6F	Added ToP_isr_mask register
90	Register Address: 0F_0x7D	Added isr0_reg
90	Register Address: 0F_0x7E	Added Register.

Pin Description

Pin #	Name	I/O Type	Description
Input Reference			
B1 A3 B4	ref0 ref1 ref2	I _u	Input References 2:0 (LVCMOS, Schmitt Trigger). These input references are available to the DPLL for synchronizing output clocks. All three input references can lock to any multiple of 8 kHz up to 77.76 MHz including 25 MHz and 50 MHz. Input ref0 and ref1 have additional configurable pre-dividers allowing input frequencies of 62.5 MHz and 125 MHz. These pins are internally pulled up to V _{dd} .
A1 A2 A4	sync0 sync1 sync2	I _u	Frame Pulse Synchronization References 2:0 (LVCMOS, Schmitt Trigger). These are optional frame pulse synchronization inputs associated with input references 0, 1 and 2. These inputs accept frame pulses in a clock format (50% duty cycle) or a basic frame pulse format with minimum pulse width of 5 ns. These pins are internally pulled up to V _{dd} .
Output Clocks and Frame Pulses			
A7 B8	diff_p diff_n	O	Differential Output Clock 0 (LVPECL). When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See "Output Clocks and Frame Pulses" on page 25 for more details on clock frequency settings.
D8	apll_clk	O	APLL Output Clock (LVCMOS). When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks up to 77.76 MHz. When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks up to 125 MHz. See "Output Clocks and Frame Pulses" on page 25 for more details on clock frequency settings. The default frequency for this output is 77.76 MHz.
G8	p_clk	O	Programmable Synthesizer - Output Clock (LVCMOS). This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz in addition to 2 kHz. The default frequency for this output is 2.048 MHz.
G7	p_fp	O	Programmable Synthesizer - Output Frame Pulse (LVCMOS). This output can be configured to provide virtually any style of output frame pulse. The default frequency for this frame pulse output is 8 kHz.
Control			
G5	rst_b	I	Reset (LVCMOS, Schmitt Trigger). A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
B2	mode	I _u	DPLL Mode Select (LVCMOS, Schmitt Trigger). During reset, the level on this pin determines the default mode of operation for DPLL (Normal=0 or Freerun=1). After reset, the mode of operation can be controlled directly with this pin, or by accessing the dpll_modesel register (0x1F) through the serial interface. This pin is internally pulled up to V _{dd} .

Pin #	Name	I/O Type	Description
B3	diff_en	I _u	Differential Output Enable (LVCMOS, Schmitt Trigger). When set high, the differential LVPECL output driver is enabled. When set low, the differential driver is tristated reducing power consumption. This pin is internally pulled up to Vdd.
Status			
E1	lock	O	Lock Indicator (LVCMOS). This is the lock indicator pin for DPLL. This output goes high when the DPLL's output is frequency and phase locked to the input reference.
H1	hold	O	Holdover Indicator (LVCMOS). This pin goes high when the DPLL enters the holdover mode.
Serial Interface			
C1	sck_scl	I/B	Clock for Serial Interface (LVCMOS). Serial interface clock. When i2c_en = 0, this pin acts as the sck pin for the serial interface. When i2c_en = 1, this pin acts as the scl pin (bidirectional) for the I ² C interface.
D2	si_sda	I/B	Serial Interface Input (LVCMOS). Serial interface data pin. When i2c_en = 0, this pin acts as the si pin for the serial interface. When i2c_en = 1, this pin acts as the sda pin (bidirectional) for the I ² C interface.
D1	so	O	Serial Interface Output (LVCMOS). Serial interface data output. When i2c_en = 0, this pin acts as the so pin for the serial interface. When i2c_en = 1, this pin is unused and should be left unconnected.
C2	cs_b_ase10	I _u	Chip Select for SPI/Address Select 0 for I²C (LVCMOS). When i2c_en = 0, this pin acts as the chip select pin (active low) for the serial interface. When i2c_en = 1, this pin acts as the ase10 pin for the I ² C interface.
E2	int_b	O	Interrupt Pin (LVCMOS). Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled-up to Vdd.
H2	i2c_en	I _u	I²C Interface Enable (LVCMOS). If set high, the I ² C interface is enabled, if set low, the SPI interface is enabled. Internally pull-up to Vdd.
APLL Loop Filter			
A5	apll_filter	A	External Analog PLL Loop Filter terminal.
B5	filter_ref0	A	Analog PLL External Loop Filter Reference.
C5	filter_ref1	A	Analog PLL External Loop Filter Reference.
JTAG and Test			
G4	tdo	O	Test Serial Data Out (Output). JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G2	tdi	I _u	Test Serial Data In (Input). JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.

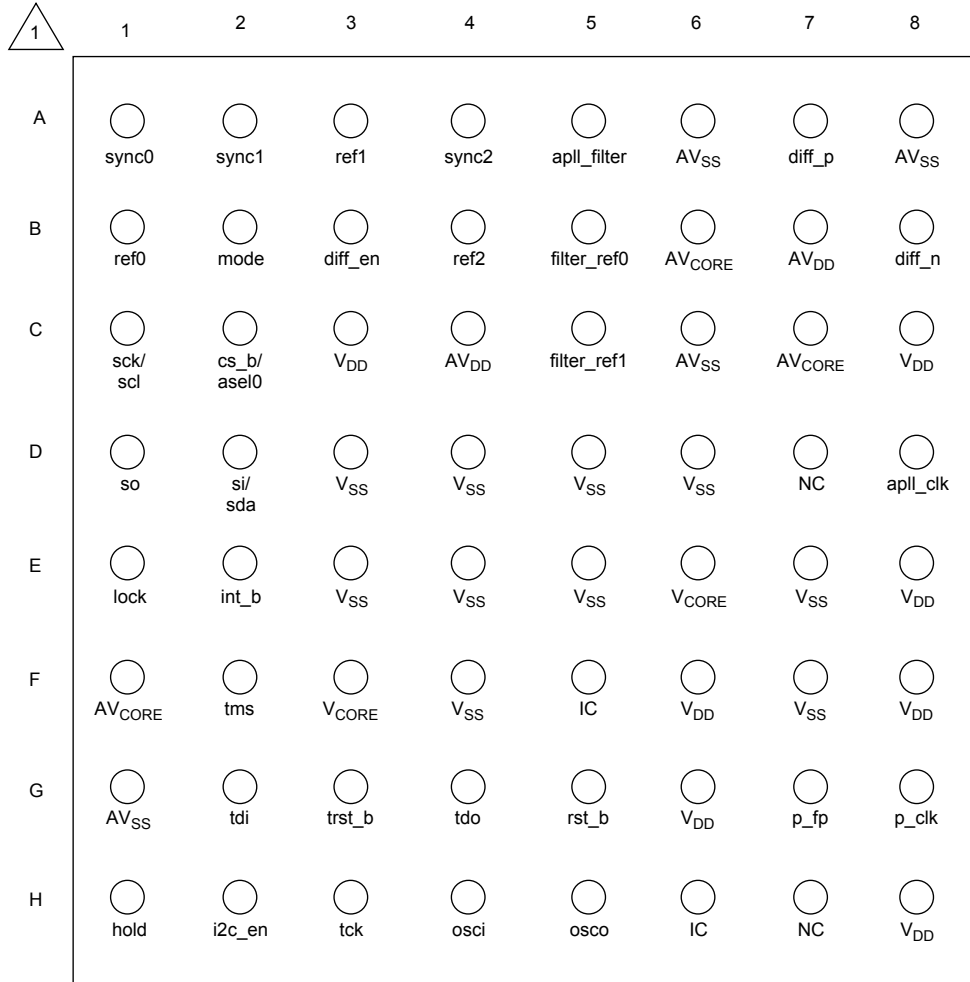
Pin #	Name	I/O Type	Description
G3	trst_b	I _u	Test Reset (LVCMOS). Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to V _{DD} . If this pin is not used then it should be connected to GND.
H3	tck	I	Test Clock (LVCMOS): Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
F2	tms	I _u	Test Mode Select (LVCMOS). JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V _{DD} . If this pin is not used then it should be left unconnected.
Master Clock			
H4	osci	I	Oscillator Master Clock Input (LVCMOS). This input accepts a 20 MHz reference from a clock oscillator (XO) or crystal XTAL. The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
H5	osco	O	Oscillator Master Clock Output (LVCMOS). This pin must be left unconnected when the osci pin is connected to a clock oscillator.
Miscellaneous			
F5	IC		Internal Connection. Leave unconnected.
H6	IC		Internal Connection. Connect to ground.
H7 D7	NC		No Connection. Leave unconnected.
Power and Ground			
C3 C8 E8 F6 F8 G6 H8	V _{DD}	P P P P P P P	Positive Supply Voltage. +3.3V _{DC} nominal.
E6 F3	V _{CORE}	P P	Positive Supply Voltage. +1.8V _{DC} nominal.
B7 C4	AV _{DD}	P P	Positive Analog Supply Voltage. +3.3V _{DC} nominal.
B6 C7 F1	AV _{CORE}	P P P	Positive Analog Supply Voltage. +1.8V _{DC} nominal.


Pin #	Name	I/O Type	Description
D3 D4 D5 D6 E3 E4 E5 E7 F4 F7	V _{SS}	G G G G G G G G G G	Ground. 0 Volts.
A6 A8 C6 G1	AV _{SS}	G G G G	Analog Ground. 0 Volts.

- I - Input
- I_d - Input, Internally pulled down
- I_u - Input, Internally pulled up
- O - Output
- A - Analog
- P - Power
- G - Ground

1.0 Pin Diagram

TOP VIEW



 1 - A1 corner is identified with a dot.

2.0 High Level Overview

The ZL30142 SONET/SDH/GbE Stratum 3 System Synchronizer and SETS device is a highly integrated device that provides all of the functionality that is required for a central timing card in carrier grade network equipment. The basic functions of a central timing card include:

- Input reference monitoring for both frequency accuracy and phase irregularities
- Automatic input reference selection
- Support of both external timing and line timing modes
- Hitless reference switching
- Wander and jitter filtering
- Master/slave crossover for minimizing phase alignment between redundant timing cards
- Independent derived output timing path for support of the SETS functionality

In a typical application, the main timing path uses the DPLL to synchronize to either an external BITS source or to a recovered line timed source. The DPLL monitors the references and automatically selects the best available reference based on configurable priority and revertive properties. The DPLL provides the wander filtering function and the P0 synthesizer generates a jitter filtered clock and frame pulse for the system timing bus which supplies all line cards with a common timing reference.

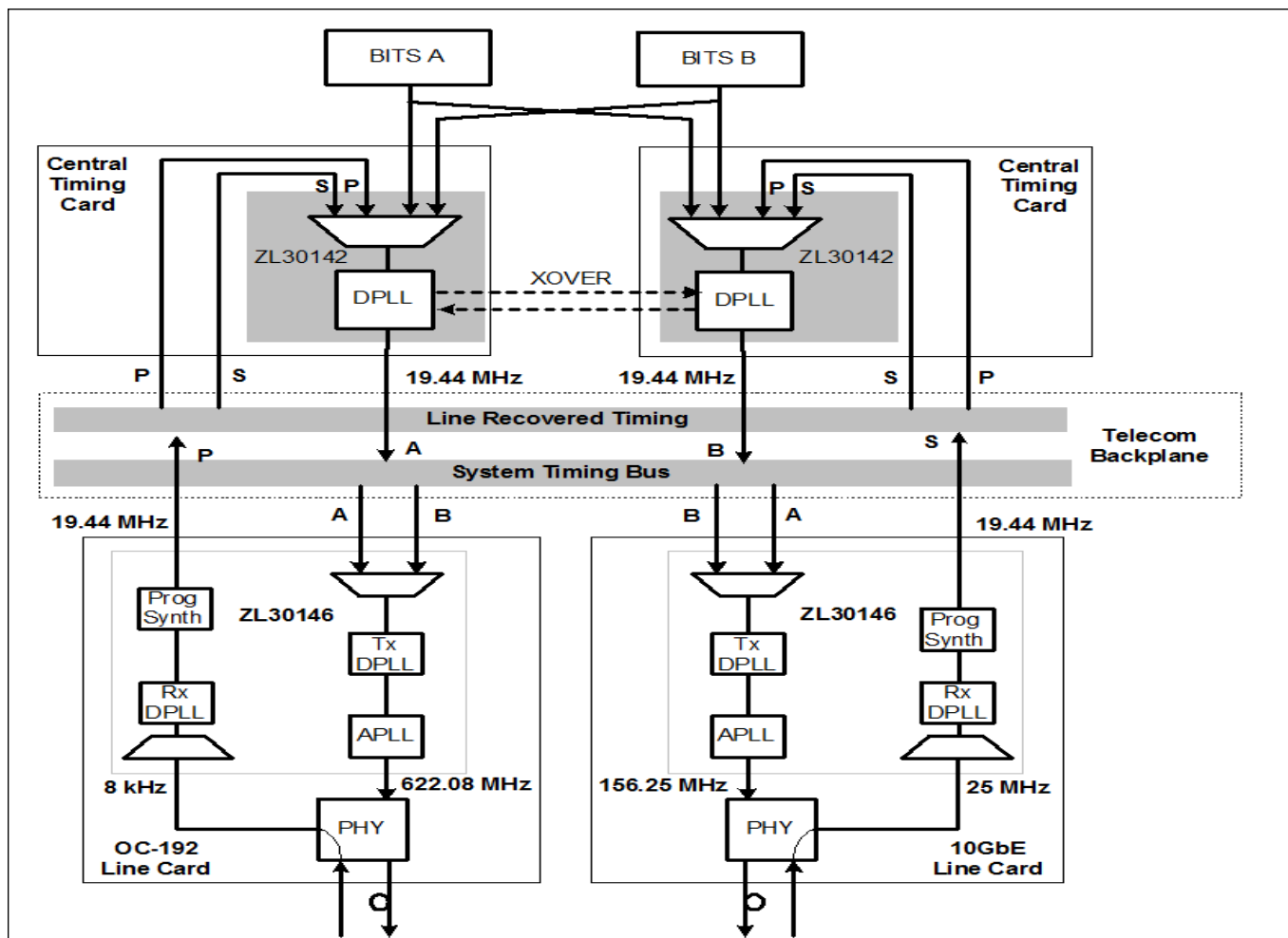


Figure 2 - Typical Application of the ZL30142

2.1 DPLL Features

The ZL30142 provides Digital Phase-Locked Loops (DPLL) for clock and/or frame pulse synchronization. Table 1 shows a feature summary for both DPLL.

Feature	DPLL
Modes of Operation	Free-run, Normal (locked), Holdover, Timing over Packet (ToP) Client Mode.
Loop Bandwidth (BW)	User selectable: 0.1 Hz, 1.7 Hz, 3.5 Hz, fast lock (7 Hz), 14 Hz, 28 Hz ¹ , or wideband ^{1,2} (890 Hz / 56 Hz / 14 Hz)
Lock Time	< 60 s for 0.1 Hz, 1.7 Hz, 3.5 Hz BW < 10 s for all other BW (PSL = 885ns/s) < 1 s for all other BW (PSL = 7.5 μs/s, 61 μs/s, or unlimited)
Phase Slope Limiting	User selectable: 885 ns/s, 7.5 μs/s, 61 μs/s, or unlimited
Pull-in Range	User selectable: 12 ppm, 52 ppm, 83 ppm, 130 ppm
Holdover Parameters	Selectable Update Times: 26 ms, 1 s, 10 s, 60 s, and Selectable Holdover Post Filter BW: 18 mHz, 0.6 Hz, 10 Hz.
Holdover Frequency Accuracy	Better than 1 ppb (Stratum 3E) initial frequency offset. Frequency drift depends on the 20 MHz external oscillator (OCXO or TCXO).
Reference Inputs	Ref0 to Ref2
Sync Inputs	Sync0, Sync1, Sync2
Input Reference Selection/Switching	Automatic (based on programmable priority and reversioness), or manual
Hitless Ref Switching	Can be enabled or disabled
External Status Pin Indicators	Lock, Holdover

Table 1 - DPLL Features

1. Limited to 0.1 Hz or 14 Hz for 2 kHz references

2. In the wideband mode, the loop bandwidth depends on the frequency of the reference input. For reference frequencies greater than 8 kHz, the loop bandwidth = 890 Hz. For reference frequencies equal to 8 kHz, the loop bandwidth = 56 Hz. The loop bandwidth is equal to 14 Hz for reference frequencies of 2 kHz.

2.2 DPLL Mode Control

The DPLL supports three modes of operation - free-run, normal, and holdover. The mode of operation can be manually set or controlled by an automatic state machine as shown in Figure 3.

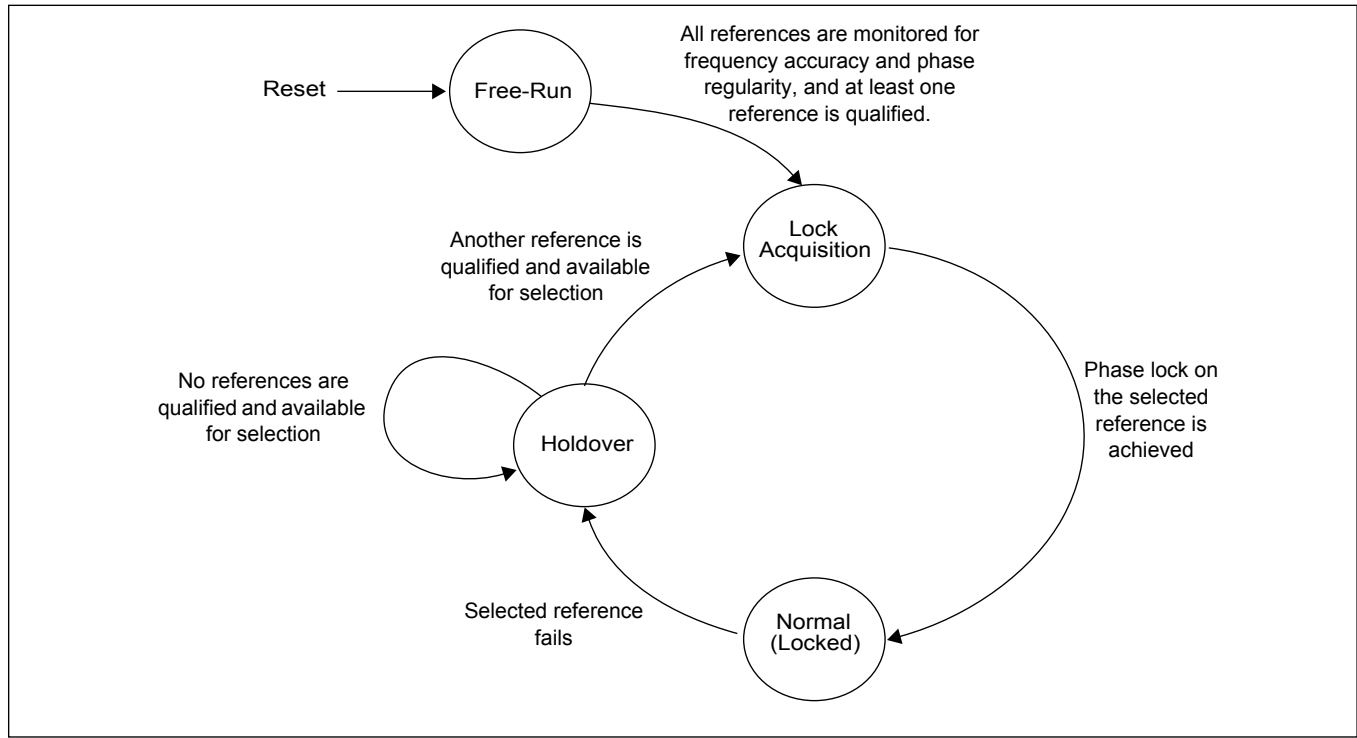


Figure 3 - Automatic Mode State Machine

Free-run

The free-run mode occurs immediately after a reset cycle or when the DPLL has never been synchronized to a reference input. In this mode, the frequency accuracy of the output clocks is equal to the frequency accuracy of the external master oscillator.

Lock Acquisition

The input references are continuously monitored for frequency accuracy and phase regularity. If at least one of the input references is qualified by the reference monitors, then the DPLL will begin lock acquisition on that input. Given a stable reference input, the ZL30142 will enter in the Normal (locked) mode.

Normal (locked)

The usual mode of operation for the DPLL is the normal mode where the DPLL phase locks to a selected qualified reference input and generates output clocks and frame pulses with a frequency accuracy equal to the frequency accuracy of the reference input. While in the normal mode, the DPLL's clock and frame pulse outputs comply with the MTIE and TDEV wander generation specifications as described in Telcordia and ITU-T telecommunication standards.

Holdover

When the DPLL operating in the normal mode loses its reference input, and no other qualified references are available, it will enter the holdover mode and continue to generate output clocks based on historical frequency data collected while the DPLL was synchronized. The transition between normal and holdover modes is controlled by the DPLL so that its initial frequency offset is better than 1 ppb which meets the requirement of Stratum 3E. The frequency drift after this transition period is dependant on the frequency drift of the external master oscillator.

2.2.1 DPLL Mode Of Operation

During reset, the level on the **mode** pin determine the default start-up mode of operation for DPLL. Table 2 shows the settings for this pin. When left unconnected, the default mode of operation will be set to manual free-run mode. The selected value is reflected in the *dpll_modesel* register (0x1F).

After reset, the mode of operation can be controlled by software using the *dpll_modesel* register (0x1F), or it can be controlled using the **mode** pin by setting the *dpll_mode_hsw* bit of the *use_hw_ctrl* register (0x01) to 1.

mode	Function
0	Set the default mode of operation to Manual Normal Mode . In this mode, automatic reference switching is disabled and the selected reference is determined by the <i>dpll_refsel</i> register (0x20). If the selected reference fails, the device automatically enters the holdover mode.
1	Set the default state to Manual Freerun Mode . In this mode, automatic reference switching is disabled and the DPLL stays in the free-run mode.

Table 2 - DPLL Default Mode Selection

2.2.1.1 ToP (Timing over Packet) Client Mode

In software control mode the ZL30142 can also be set in Timing over Packet (ToP) Client Mode using the *dpll1_modesel* register (0x1F).

ToP Client mode allows external software to control DCO frequency offset of the DPLL using the 28 bit 2's complement value in the *DCO_freq_offset* registers (page 1, addresses 0x65 to 0x68). The offset is programmed in steps according to the following equation.

$$\text{LSB} = 2^{-40} * (80\text{MHz}/65,536\text{MHz}) * 10^9 \text{ppb}$$

In ToP client mode, the zl30143 also samples the DCO Phase Word and Local System time to be read by the ToP clock recovery algorithm software.

The 64 bit DCO phase Word is available in the *DCO_Phase* registers (page 1, address 0x69 to 0x70). The 32 bit Local System Time is available in the *Local Time* registers (page 1, address 0x71 to 0x74)

For more details contact your local Microsemi FAE.

2.3 Loop Bandwidth

The loop bandwidth determines the amount of wander and jitter filtering that is provided by the DPLL. The loop bandwidth for DPLL is programmable using the *bandwidth* field of the *dpll_control_register_0* register (0x1D). The bandwidth should be set according to the application. Table 3 gives examples of typical applications and their bandwidth settings.

bandwith[3:1]	BW (Hz)	Application
000	0.1	GR-253 SONET Stratum 3, SMC, G.813 option 2, G.8262 EEC 2
001	1.7	GR-1244 Stratum 3, G.813 option 1
010	3.5	G.813 option 1, G.8262 EEC option 1
101	14/56/890	Wide Band Mode. BW depends on input frequency.
110	7	Fast Lock

Table 3 - DPLL Loop Bandwidth

2.4 Pull-in/hold-in Range

The **pull-in range** defines the maximum input frequency range that the DPLL can lock to. The pull-in range for DPLL is programmable using the *dplldpll_pull_in_range* register (0x29). The pull-in range should be set according to the application as shown in Table 4. The **hold-in range**, which defines the range of input frequencies that the PLL will continue to lock to, is equal to the pull-in range.

pull_in_range[1:0]	+/- ppm	Application
00	12	Stratum 3, G.813 option 1, G.8262 EEC 1 & 2
01	52	SONET Minimum Clock, G.813 option 2
10	130	ITU-T G.703, ETSI ETS 300 011
11	83	ANSI T1.403, Stratum 4

Table 4 - DPLL Pull-in Range

2.5 Phase Slope Limiting

The DPLL offers a phase slope limit feature which can be used to limit the rate of output phase movement of the output clocks and frame pulses during an input transient. This feature is used for meeting the phase slope requirements of Telcordia and ITU-T standards. The level of phase slope limiting depends on the application. The *dpll_ph_slopelim* field of the *dpll_ctrl_0* register (0x1D) allows four levels of phase slope limiting as shown in Table 5. By default.

dpll_ph_slopelim[1:0]	Phase Slope Limiting	Application
00	885 ns/s	GR-1244 Stratum 3 (objective)
01	7.5 μ s/s	G.813 option 1 and G.8262
10	61 μ s/s	GR-1244 Stratum 3
11	Unrestricted (default)	

Table 5 - DPLL Phase Slope Limiting

2.6 Hitless Reference Switching

With hitless reference switching enabled, the phase difference between the originally selected reference and the newly selected reference is absorbed by the DPLL preventing a possible non-compliant phase transient at its output. The *hs_en* bit of the *dpll_ctrl_0* register (0x1D) allows this feature to be enabled or disabled. When disabled, the DPLL will align its output to the new reference at a rate of alignment which is dependant on the phase slope limit set in the *dpll_ph_slopelim* field of the *dpll_ctrl_0* register (0x1D).

2.7 Free-run Frequency Offset

When operating in Free Run mode, the accuracy of the output clocks is equal to that of the oscillator connected to the Master Clock Input (OSC_i). The ZL30142 allows the user to offset this frequency by +/-149 ppm by using the 28 bit 2's complement value in the *DCO_freq_offset* registers (page 1, addresses 0x65, 0x66, 0x67, and 0x68). The offset is programmed in steps according to the following equation.

$$\text{LSB} = 2^{-40} * (80\text{MHz}/65,536\text{MHz}) * 10^9 \text{ppb}$$

To enable the free run frequency offset, set the *freq_offset_en* bit of the *dpll_ctrl_1* register (page 0, address 0x1E, bit 1).

2.8 Holdover

The DPLL continuously collect phase data while synchronized to a valid reference. These data samples are accumulated and averaged to determine a stable holdover frequency in the event that all of the valid references are lost. To prevent reference input jitter from corrupting the final holdover value, samples are taken on phase data filtered by the DPLL's loop bandwidth. The DPLL offers an additional stage of filtering that can be enabled if the DPLL's loop bandwidth does not provide adequate filtering. This allows the DPLL to operate in a wide bandwidth mode and still provide an accurate holdover value. This is useful when the DPLL is used in a slave mode. The holdover filter bandwidth is programmable using the *hold_filt_bw* field of the *dll_ctrl_1* register (0x1E).

The holdover performance of the output clocks will depend on two factors. One is the initial offset of the DPLL, and the other is the frequency drift (or stability) of the external oscillator. The initial offset of the DPLL meets Stratum 3/G.813 leaving the overall holdover performance dependant on the frequency drift of the external oscillator. An OCXO or TCXO is recommended for Stratum 3/G.813.

2.9 Reference and Sync Inputs

There are three reference clock inputs (**ref0** to **ref2**) available to the DPLL. The selected reference input is used to synchronize the output clocks. Reference selection can be controlled using the built-in state machine or set in a manual mode.

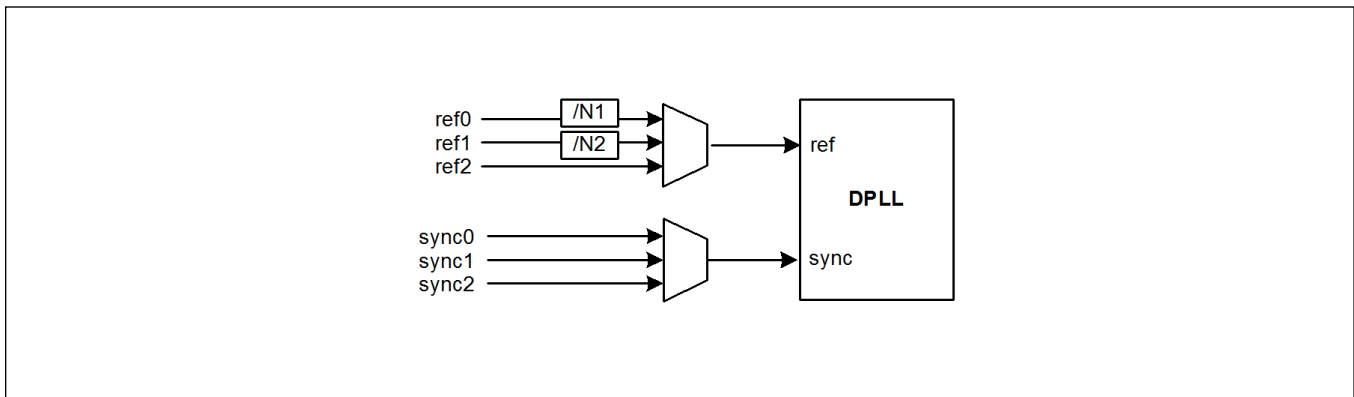


Figure 4 - Reference and Sync Inputs

Each of the **ref** inputs accept a single-ended LVCMOS clock with a frequency ranging from 2 kHz to 77.76 MHz. Built-in frequency detection circuitry automatically determines the frequency of the reference if its frequency is within the set of pre-defined frequencies as shown in Table 6. Once detected, the resulting frequency of the reference can be read from the *detected_ref[0:1]* registers (0x10 - 0x11).

2 kHz	16.384 MHz
8 kHz	19.44 MHz
64 kHz	38.88 MHz
1.544 MHz	77.76 MHz
2.048 MHz	
6.48 MHz	
8.192 MHz	

Table 6 - Set of Pre-Defined Auto-Detect Clock Frequencies

Two additional custom reference frequencies (Custom A and Custom B) are also programmable using the *custA_mult[1:0]* and *custB_mult[1:0]* registers (0x67, 0x68, 0x71, 0x72). These custom frequencies are programmable as 8 kHz * N up to 77.76 MHz (where N = 1 to 9720), or 2 kHz (when N = 0). The *ref_freq_mode_0* register (0x65) are used to configure each of the reference inputs as auto-detect, custom A, or custom B.

The first two reference inputs (**ref0** and **ref1**) have programmable pre-dividers which allows them to lock to frequencies higher than 77.76 MHz or to non-standard frequencies. By default the pre-dividers divide by 1, but they can be programmed to divide by 1.5, 2, 2.5, 3, 4, 5, 6, 7, and 8 using the *ref0_div* and *ref1_div* bits of the *predivider_ctrl* register (0x7E). For example, an input frequency of 125 MHz can be divided down by 5 using the pre-dividers to create a 25 MHz input reference. The 25 MHz can then be programmed as a custom input frequency. Similarly, a 62.5 MHz input clock can be divided by 2.5 to create 25 MHz. **Note that division by non-integer values (e.g., 1.5, 2.5) is achieved by using both the rising and falling edges of the input reference. This may cause higher jitter levels at the output clocks when the reference input does not have a 50% duty cycle.**

In addition to the reference inputs, the DPLL has three optional frame pulse synchronization inputs (**sync0** to **sync2**) used to align the output frame pulses. The *sync_n* input is selected with its corresponding *ref_n* input, where *n* = 0, 1, 2. Note that the sync input cannot be used to synchronize the DPLL, it only determines the alignment of the frame pulse outputs. An description of output frame pulse alignment is shown in Figure 5.

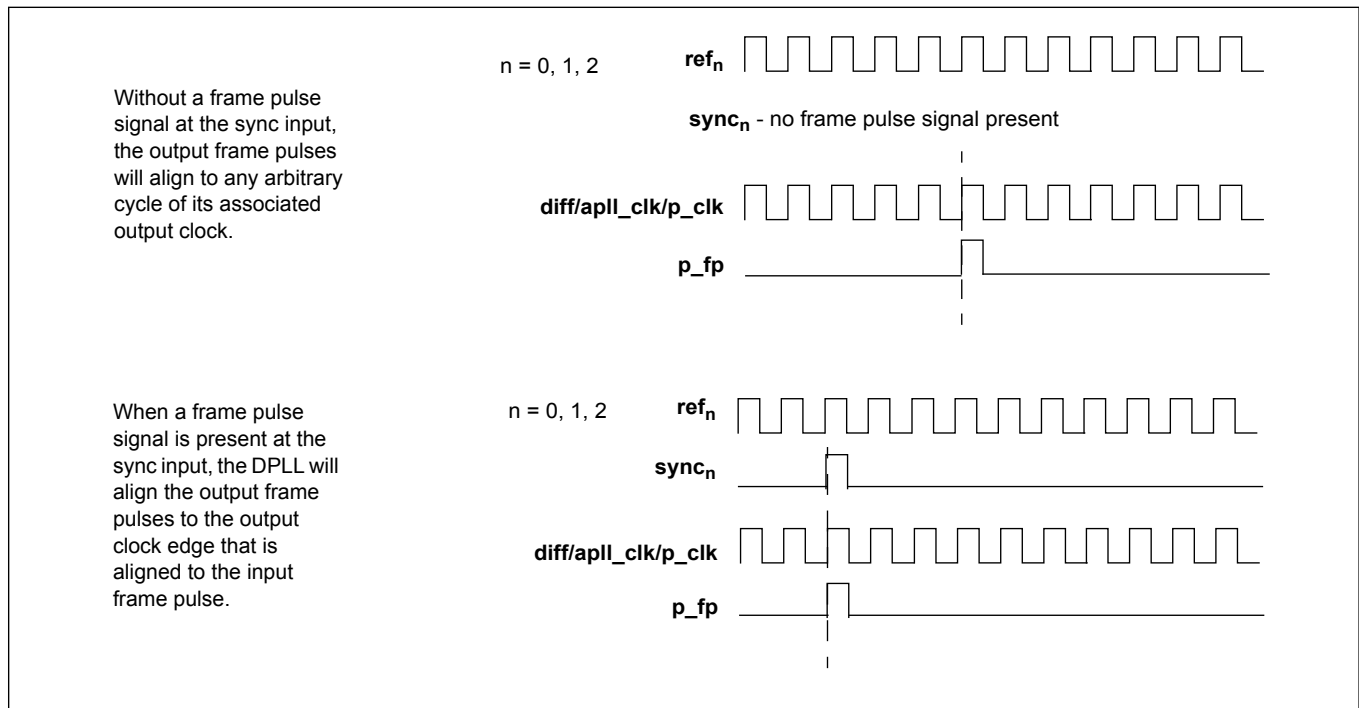


Figure 5 - Output Frame Pulse Alignment

Each of the **sync** inputs accept a single-ended LVCMOS frame pulse. Since alignment is determined from the rising edge of the frame pulse, there is no duty cycle restriction on this input, but there is a minimum pulse width requirement of 5 ns. Frequency detection for the sync inputs is automatic for the supported frame pulse frequencies shown in Table 7.

1 Hz ¹
166.67 Hz (48x 125 μ s frames)
400 Hz
1 kHz
2 kHz
8 kHz
64 kHz

1. Bit 0 of 1Hz_Enable Register (08_0x71) must be set to 1 for 1Hz detection

Table 7 - Set of Pre-Defined Auto-Detect Sync Frequencies

2.10 Reference Input Selection

The DPLL can independently select any of the qualified input references for synchronization. Reference selection can be automatic or manual depending on the *dppl_modesel* register (0x1F). For automatic reference selection, the mode selection register must be set to the "Automatic Normal Mode" setting. For manual reference selection, set the mode selection registers to the "Manual Normal Mode".

In the case of automatic reference selection, the selection criteria is based on reference qualification, input priority, and the revertive setting. Only references that are valid can be selected by the automatic state machine. If there are no valid references available, then the DPLL will automatically enter the holdover mode. Each of the references has an assignable priority using *dppl_ref_pri_ctrl* registers (0x24 to 0x25). Any of the references can be prevented from being selected by setting their priority to "1111".

The *revert_en* bit of the *dppl_ctrl_1* register (0x1E) controls the revertive switching option for the DPLL. With revertive switching enabled, the highest priority reference input with a valid reference is always selected. If a reference with a higher priority becomes valid, then a reference switchover to that reference will be initiated. With non-revertive switching, the active reference will always remain selected while it is valid. If this reference becomes invalid, a reference switchover to a valid reference with the highest priority will be initiated. Note that if two or more references have been assigned the same priority, then priority will be given to the lowest reference number (e.g., if ref1 and ref2 have the same assigned priority, then ref1 will have higher priority over ref2). The revertive feature can also be applied to individual references using the *dppl_ref_rev_ctrl* register (0x23).

When the *dppl_modesel* register (0x1F) is set to the "Manual Normal Mode", the active reference is selected using the *dppl_refsel* register (0x20). If the defined reference is not valid, then the DPLL will automatically enter the holdover mode.

2.11 Reference Monitoring

All input references (**ref0** to **ref2**) are monitored for frequency accuracy and phase regularity. New references are qualified before they can be selected as a synchronization source, and qualified references are continuously monitored to ensure that they are suitable for synchronization. The process of qualifying a reference depends on four levels of monitoring.

Single Cycle Monitor (SCM)

The SCM block measures the period of each reference clock cycle to detect phase irregularities or a missing clock edge. In general, if the measured period deviates by more than 50% from the nominal period, then an SCM failure (scm_fail) is declared.

Coarse Frequency Monitor (CFM)

The CFM block monitors the reference frequency over a measurement period of 30 μ s so that it can quickly detect large changes in frequency. A CFM failure (cfm_fail) is triggered when the frequency has changed by more than 3% or approximately 30000 ppm.

Guard Soak Timer (GST)

The SCM and the CFM are used to quickly detect failures of the reference clocks. To prevent intermittent failures from triggering a false reference failure, the SCM and the CFM failure indicators are processed by the Guard Soak Timer. The GST block mimics the operation of an analog integrator by accumulating failure events from the CFM and the SCM blocks and applying a selectable rate of decay when no failures are detected. A GST failure (gst_fail) is triggered when the accumulated failures have reached the upper threshold during the disqualification observation window. When there are no CFM or SCM failures, the accumulator decrements until it reaches its lower threshold during the qualification window.

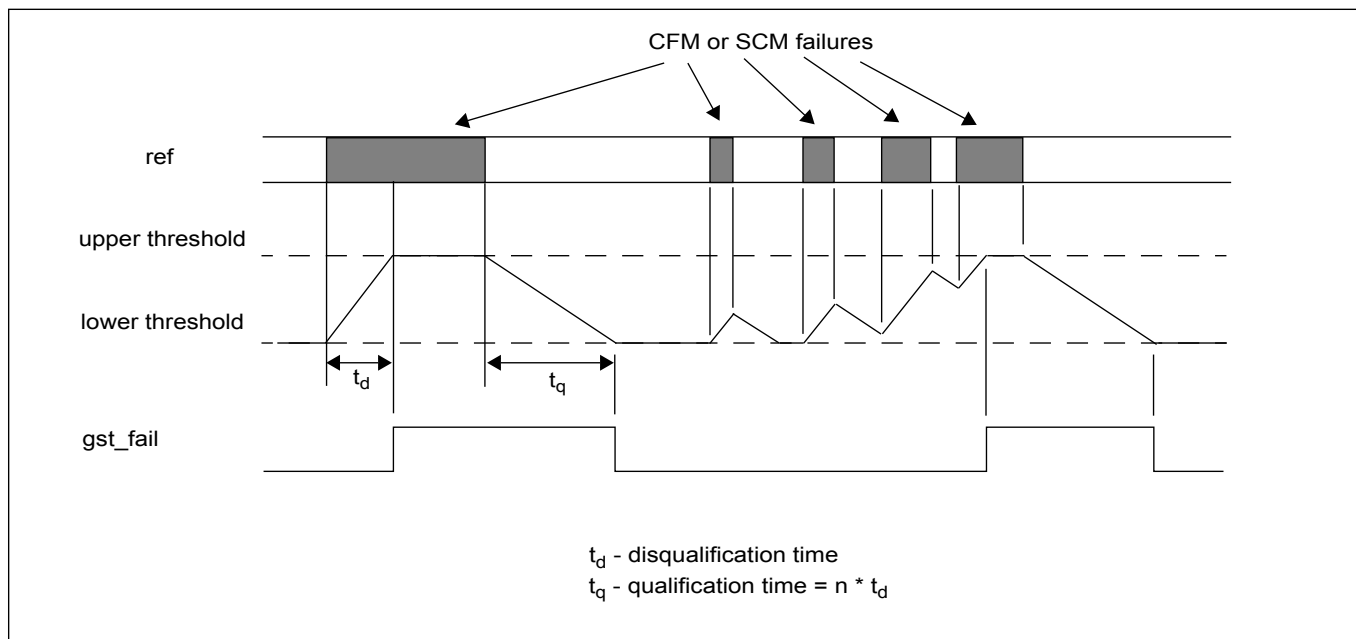


Figure 6 - Behaviour of the Guard Soak Timer during CFM or SCM Failures

Precise Frequency Monitor (PFM)

The PFM is used to keep track of the frequency of the reference clock. It measures its frequency over a 10 second period and indicates a failure when the measured frequency exceeds the out-of-range (OOR) limits configured in the `oor_ctrl[0:3]` registers (0x16, 0x17). The OOR should be set according to the application as shown in Table 8.

oor_ctrl[0:3]	Acceptance Range	Rejection Range	Typical Application
000	+/- 9.2 ppm	+/- 12 ppm	Stratum 3, G.813 option 1, G.8262 EEC 1 & 2
100	+/- 13.8 ppm	+/- 18 ppm	
101	+/- 24.6 ppm	+/- 32 ppm	
110	+/- 36.6 ppm	+/- 47.5 ppm	
001	+/- 40 ppm	+/- 52 ppm	SONET Minimum Clock, G.813 option 2
111	+/- 52 ppm	+/- 67.5 ppm	
011	+/- 64 ppm	+/- 83 ppm	ANSI T1.403, Stratum 4
010	+/- 100 ppm	+/- 130 ppm	ITU-T G.703, ETSI ETS 300 011

Table 8 - Frequency Out of Range Limits

To ensure an accurate frequency measurement, the PFM measurement interval is re-initiated if phase or frequency irregularities are detected by the SCM or CFM. The PFM provides a level of hysteresis between the acceptance range and the rejection range to prevent a failure indication from toggling between valid and invalid for references that are on the edge of the acceptance range.

When determining the frequency accuracy of the reference input, the PFM uses the external oscillator's output frequency (f_{ocsi}) as its point of reference. As a result, the actual acceptance and rejection frequencies can be offset with respect to the external oscillator's output frequency. This is accounted for in the acceptance and rejection requirements as described in Telcordia GR-1244 section 3.4.1. An example of the acceptance and rejection ranges for Stratum 3 application (acceptance in the range of +/- 9.2 ppm, rejection at +/- 12 ppm) given a +/- 4.6 ppm free-run frequency accuracy of a Stratum 3 reference oscillator is shown in Figure 7.

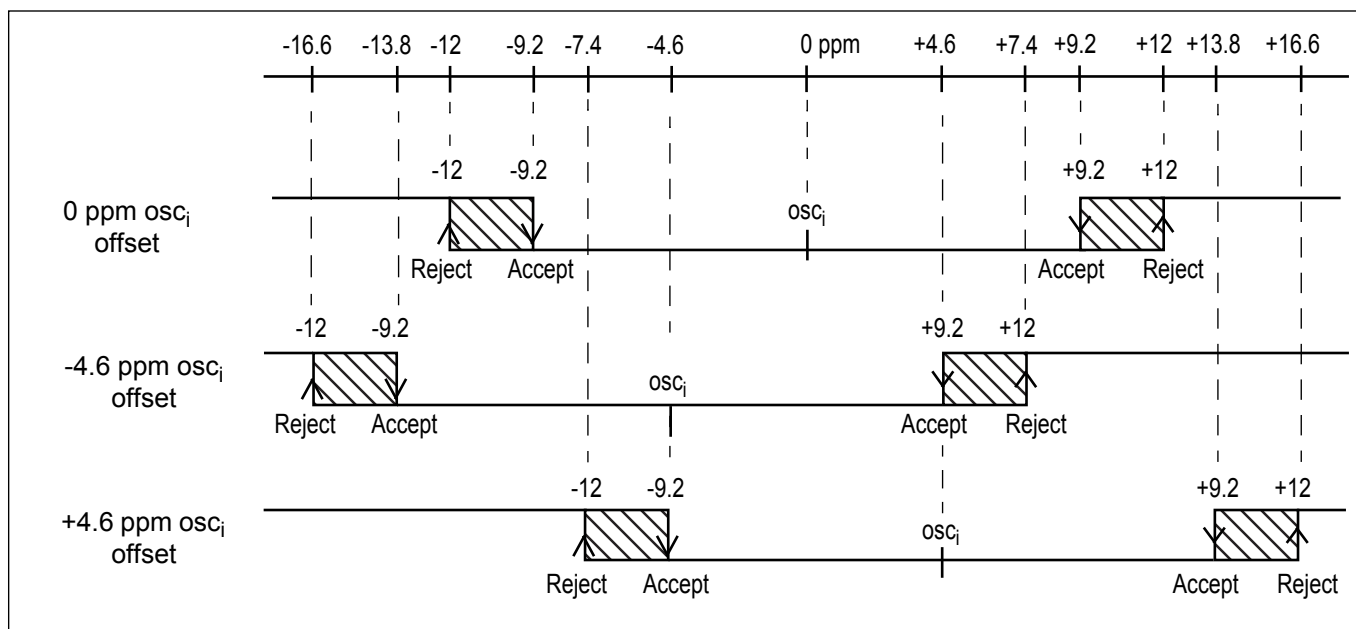


Figure 7 - Stratum 3/G.813 Option 1 Frequency Acceptance and Rejection Ranges

SCM, CFM, PFM, and GST failures are indicated in the *ref_mon_fail*[0:1] registers (0x05, 0x06). As shown in Figure 8, the SCM, CFM, PFM, and GST indicators are logically ORed together to form a reference failure indicator. An interrupt is triggered when the failure indicator is triggered. The status of the failure indicators can be read in the *ref_fail_isr* interrupt service register (0x02). A change in the bit status of this register will cause the interrupt pin (*int_b*) to go low. It is possible to mask this interrupt with the *ref_fail_isr_mask* register (0x09) which is represented as "mask_isr_n".

It is possible to mask an individual reference monitor from triggering a reference failure by setting the *ref_mon_fail_mask*[3:0] registers (0x0C, 0x0D). These are represented by mask_scm_n, mask_cfm_n, mask_gst_n, and mask_pfm_n in Figure 8. In addition, the CFM and SCM reference monitor indicators can be masked from indicating failures to the GST reference monitor using the *gst_mask* register (0x1A). These are represented as mask_cfm_gst_n and mask_scm_gst_n.

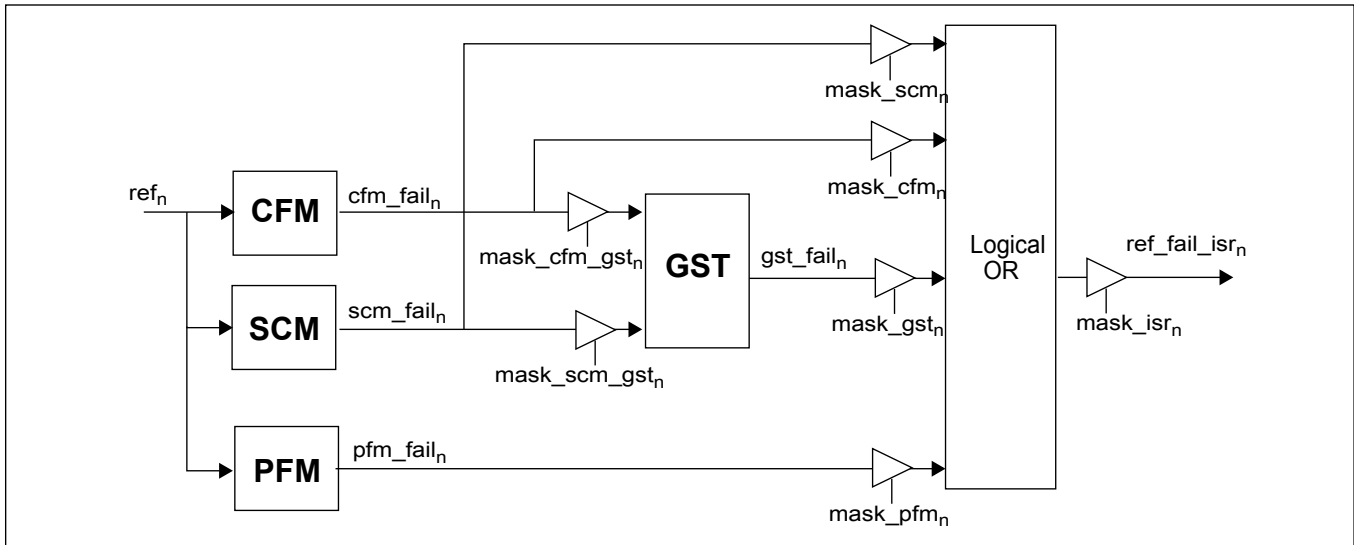


Figure 8 - Reference Monitoring Block Diagram

2.12 Sync Monitoring

Sync inputs (**sync0 to sync2**) are continuously monitored by the Sync Ratio Monitor (SRM). The SRM ensures that the sync inputs are valid by verifying that there is a correct number of reference cycles within the sync period. The status of this monitor is reported in the *sync_fail* bits of the *detected_sync*[0:1] registers (0x14, 0x15).

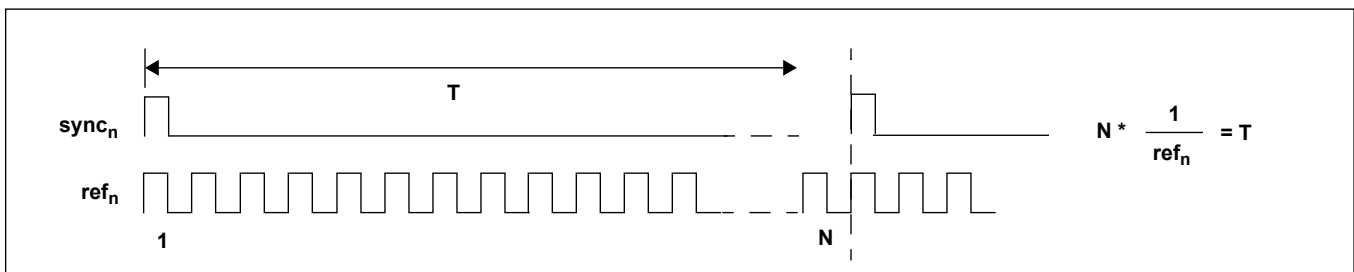


Figure 9 - Sync Monitoring

2.13 Reference Monitoring for Custom Configurations

As described in section 2.9, “Reference and Sync Inputs“, two additional custom reference input frequencies (Custom A, Custom B) are definable allowing a reference input to accept any multiple of 8 kHz up to 77.76 MHz.

Each of the custom configurations also have definable SCM and CFM limits. The SCM limits are programmable using the *custA_scm_low*, *custA_scm_high_lim*, *custB_scm_low*, *custB_scm_high* registers (0x69, 0x6A, 0x73, 0x74). The SCM low and high limits determine the acceptance window for the clock period as shown in Figure 10. Any clock edge that does not fall into the acceptance window will trigger an SCM failure. High and low limits are programmed as multiples of a 300 MHz cycle (3.33 ns).

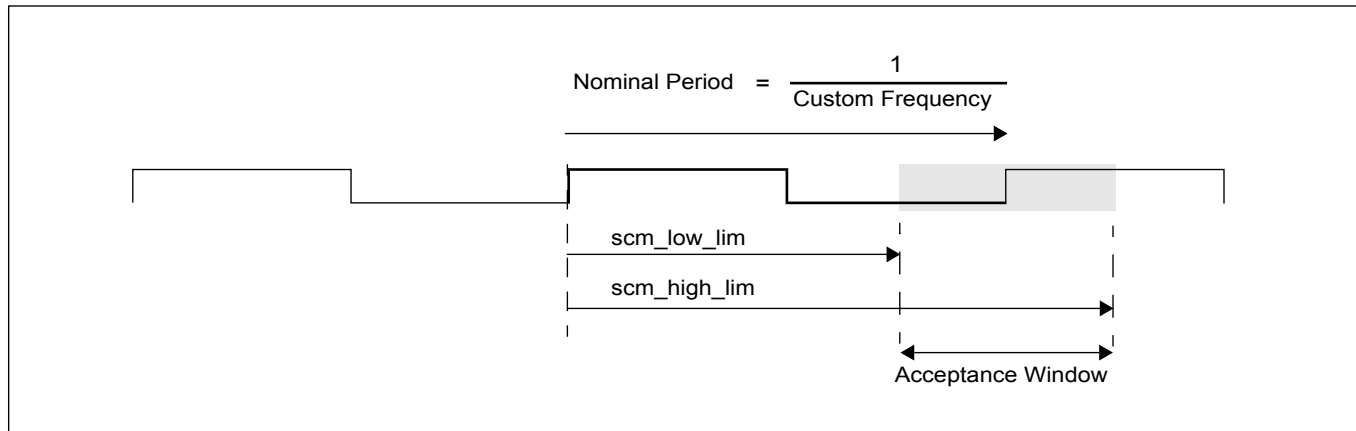


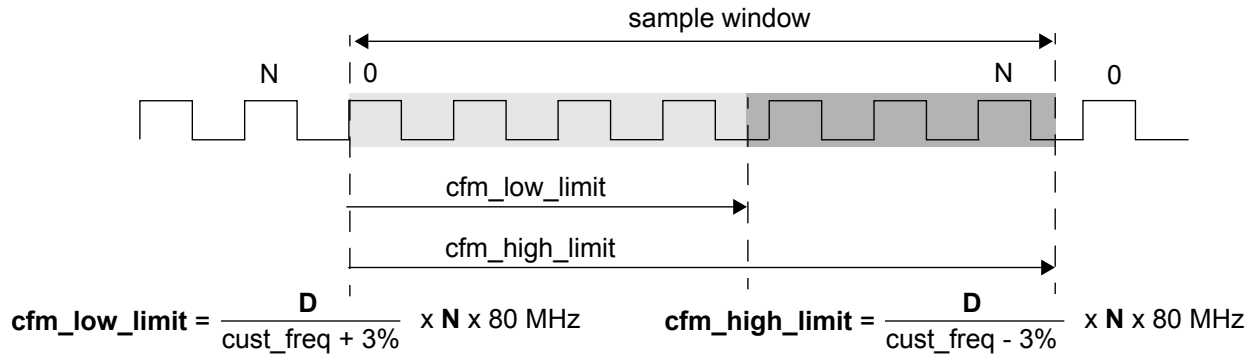
Figure 10 - Defining SCM Limits for Custom Configurations

Since the SCM is used to identify a missing clock edge, the acceptance window should be set to approximately +/-50% of the nominal period. Using a smaller window may trigger unwanted SCM failures.

For example, if the Custom A frequency was defined as 50 MHz (using registers 0x67, 0x68), its nominal period is 20 ns. To fail the input reference when its period falls below 10 ns (-50% of the nominal period), the *custA_scm_low* register is programmed to 0x03 (3 x 1/300MHz = 10 ns). To fail the input reference if its period exceeds 30 ns (+50% of the nominal period), the *custA_scm_high* register is programmed with 0x09 (9 x 1/300MHz = 30 ns).

For low speed input references less than 1.8 MHz, the SCM counter does not provide enough range to reliably perform its function. Therefore for custom inputs of less than 1.8 MHz the device should set the *scm_low_lim* and *scm_high_lim* to 0 and the CFM should be used as the single cycle monitor.

The CFM quickly determines large changes in frequency by verifying that there are N amount of input reference clock cycles within a programmable sample window. The value of N is programmable in the *custA_cfm_cycle* and the *custB_cfm_cycle* registers (0x6F, 0x79). The size of the sample window is defined in terms of high and low limits and are programmed as multiples of 80 MHz cycles. These are defined using the *custA_cfm_low_0*, *custA_cfm_low_1*, *custA_cfm_high_0*, *custA_cfm_high_1*, *custB_cfm_low_0*, *custB_cfm_low_1*, *custB_cfm_high_0*, *custB_cfm_high_1* registers (0x6B-0x6E, 0x75-0x78). A divide-by-4 circuit can be enabled to increase the resolution of the sample window. This is recommended when the input reference frequency exceeds 19.44 MHz. The divide-by-4 is enabled using the *custA_div* and *custB_div* registers (0x70, 0x7A). Equations for calculating the high and low limits are shown in Figure 11.



For low speed Custom Input Frequencies (<1.8 MHz) the following equations should be used instead:

$$\text{cfm_low_limit} = \frac{0.5}{\text{cust_freq}} \times 80 \text{ MHz}$$

$$\text{cfm_high_limit} = \frac{1.5}{\text{cust_freq}} \times 80 \text{ MHz}$$

where **N** and **D** are dependant on the setting of the custom frequency. Recommended values are shown in the following table:

Input Frequency Range	D (Divider)	N (Number of cycles)
38.88 MHz < freq ≤ 77.76 MHz	4	256
19.44 MHz < freq ≤ 38.88 MHz	4	128
8.192 MHz < freq ≤ 19.44 MHz	1	256
2.048 MHz < freq ≤ 8.192 MHz	1	128
1.8 MHz < freq ≤ 2.048 MHz	1	32
2 kHz < freq ≤ 1.8 MHz (Recommended CFM limits = +/- 50%)	1	1

Example: Custom configuration A is set for 50 MHz (**custA_mult13_8 = 0x18**, **custA_mult13_8 = 0x6A**)

The values for D and N are determined using the table above with respect to a 50 MHz input reference.

D = 4 (**custA_div = 0x01**)
 N = 256 (**custA_cfm_cycle = 0xFF**)

The CFM low and high values are calculated using the equations above:

$$\text{cfm_low_limit} = \frac{4}{51.5 \text{ MHz}} \times 256 \times 80 \text{ MHz} = 1591_{\text{dec}} = 0637_{\text{hex}} \quad (\text{custA_cfm_low15_8} = \text{0x06})$$

$$\quad \quad \quad (\text{custA_cfm_low7_0} = \text{0x37})$$

$$\text{cfm_high_limit} = \frac{4}{48.5 \text{ MHz}} \times 256 \times 80 \text{ MHz} = 1689_{\text{dec}} = 0699_{\text{hex}} \quad (\text{custA_cfm_high15_8} = \text{0x06})$$

$$\quad \quad \quad (\text{custA_cfm_high7_0} = \text{0x99})$$

Figure 11 - Custom CFM Configuration for 50 MHz

2.14 Output Clocks and Frame Pulses

The ZL30142 offers a wide variety of outputs including one low-jitter differential LVPECL clock (**diff**), one APLL LVCMOS (**apll_clk**) output clock, and one programmable LVCMOS (**p_clk**) output clock. In addition to the clock outputs, one LVCMOS programmable frame pulse (**p_fp**) is also available.

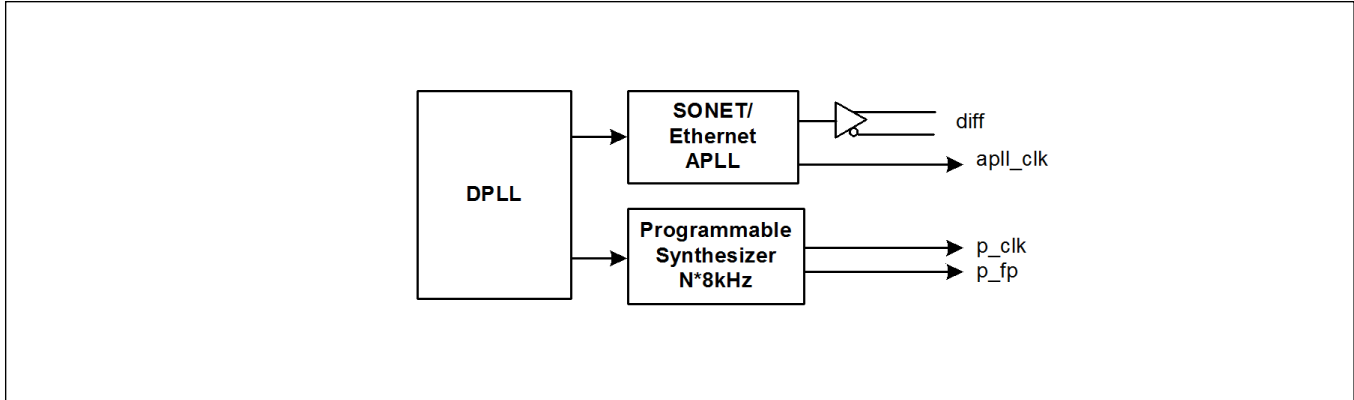


Figure 12 - Output Clock Configuration

The single ended APLL LVCMOS output clock (**apll_clk**) frequency is programmable using the *apll_clk_freq* register (0x52). Valid frequencies are listed in Table 9. The *eth_en* and the *f_sel* bits are set using the *apll_run* register (0x51).

apll_clk_freq bit settings	apll_clk Output Frequency	
	SONET/SDH Mode	Ethernet Mode - Low Speed
	eth_en = 0 f_sel = 0	eth_en = 1 f_sel = 1
0001	Reserved	125 MHz
0010	77.76 MHz	62.5 MHz
0011	38.88 MHz	Reserved
0100	19.44 MHz	Reserved
0101	9.72 MHz	50 MHz
0110	Reserved	25 MHz
0111	Reserved	12.5 MHz
1010	51.84 MHz	Reserved
1011	25.92 MHz	Reserved
1100	12.96 MHz	Reserved
1101	6.48 MHz	Reserved

Table 9 - APLL LVCMOS Output Clock Frequencies

The differential output clock (**diff**) frequency is programmable using the *diff_sel* bit of the *diff_sel* register (0x61). When in SONET/SDH mode (*eth_en* = 0, *f_sel_diff* = 0), any of the valid SONET/SDH clock frequencies shown in Table 10 can be selected. When in Ethernet mode (*eth_en* = 1), the APLL can generate two groups of frequencies - low speed (*f_sel_diff* = 1) or high speed (*f_sel_diff* = 0). Valid frequencies are listed in Table 10. The frequency group selector (*f_sel_diff*) is programmable using the *apl_run* register (0x51). When low speed ethernet mode and high speed ethernet modes are enabled at the same time (i.e., (*eth_en* = 1, *fsel* = 1 and *f_sel_diff* = 0), please refer to Application Note ZLAN-254 for details on the appropriate device configuration settings.

diff_clk_sel bit settings	diff Output Frequency		
	SONET/SDH Mode	Ethernet Mode - Low Speed	Ethernet Mode - High Speed
	eth_en = 0 f_sel_diff = 0	eth_en = 1 f_sel_diff = 1	eth_en = 1 f_sel_diff = 0
000	19.44 MHz	Reserved	Reserved
001	38.88 MHz	125 MHz	Reserved
010	77.76 MHz	62.5 MHz	Reserved
011	155.52 MHz	Reserved	156.25 MHz
100	311.04 MHz	Reserved	312.5 MHz
101	622.08 MHz	50 MHz	Reserved
110	6.48 MHz	25 MHz	Reserved
111	51.84 MHz	12.5 MHz	Reserved

Table 10 - APLL Differential Output Clock Frequencies

The frequency of the **p_clk** output is programmable from 2 kHz up to 100 MHz where,

$$f_{p_clk} = N \times 8 \text{ kHz}$$

The value of N is a 16-bit word which is programmable using the *p_freq_0* and *p_freq_1* registers (0x38, 0x39). For an output frequency of 2 kHz, let N = 0.

The frequency of the frame pulses generated from the programmable synthesizer (**p_fp**) is configurable using the *p_fp_freq* register (0x3E). Valid frequencies are listed in Table 11.

p_fp_freq bit settings	p_fp Frequency
0000	166.6667 Hz (48x 125 μs frames)
0001	400 Hz
0010	1 kHz
0011	2 kHz
0100	4 kHz
0101	8 kHz
0110	32 kHz
0111	64 kHz
1000	1 Hz

Table 11 - Output Frame Pulse Frequencies

The pulse width of the frame pulse is programmable using the *p_fp_type* bits of the *p_fp_type* register (0x3F). Valid pulse widths are shown in Table 12.

p_fp_type bit settings	p_fp Pulse Width	Comment
000	One period of a 4.096 MHz clock	These are pre-defined pulse widths that are usable when p_clk is set to a frequency that is a multiple of the E1 rate (2.048 MHz). When p_clk is not an E1 multiple, the p_fp_type must be set to '111'
001	One period of a 8.192 MHz clock	
010	One period of a 16.384 MHz clock	
011	One period of a 32.768 MHz clock	
100	One period of a 65.536 MHz clock	
101	Reserved	
110	Reserved	
111	One period of p_clk	The frame pulse width is equal to one period of the p_clk. This setting must be used when the p_clk is not an E1 multiple.

Table 12 - Programmable Synthesizer Frame Pulse Widths

The style (frame pulse or 50% duty cycle clock), alignment (rising or falling edge of its associated clock), and its polarity (positive or negative) is programmable using the *p_fp_type* register (0x3F).

2.14.1 Output Clock and Frame Pulse Squelching

A clock squelching feature is available which allows forcing an output clock to a specific logic level. The *apll_clk_run* of the *apll_run_register* (0x51) control the ethernet single ended output (**apll_clk**). The programmable clock output can also be forced to a logic low level using the *p_clk_run* bit of the *p_run* register (0x37).

2.14.2 Disabling Output Clocks and Frame Pulses

Unused outputs can be set to a high impedance state to reduce power consumption. The differential outputs can be disabled using the *diff_en* bit of the *diff_ctrl* register (0x60). The ethernet output can be disabled using the *apll_clk_en* of the *apll_enable* register (0x50). The programmable clock can be disabled using the *p_clk_en* bit of the *p_enable* register (0x36). When not in use, the frame pulse output (**p_fp**) can be disabled using the *p_fp_en* bit of the *p_enable* register (0x36).

2.14.3 Disabling Output Synthesizers

In applications where none of the Ethernet APLL clocks are used, the entire APLL can be disabled to conserve power using the *apll_en* bit of the *apll_enable* register (0x50). The programmable synthesizer can also be disabled by using the *p_en* bit of the *p_enable* register (0x36).

2.15 Configurable Input-to-Output and Output-to-Output Delays

The ZL30142 allows programmable static delay compensation for controlling input-to-output and output-to-output delays of its clocks and frame pulses.

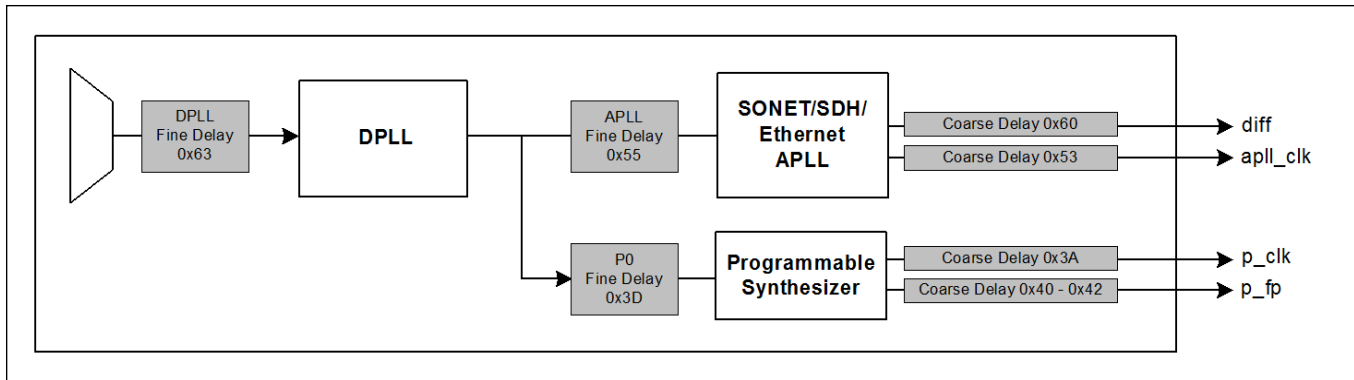


Figure 13 - Phase Delay Adjustments

Both of the SONET/SDH/Ethernet APLL and the Programmable Synthesizer can be configured to lead or lag the selected input reference clock using the DPLL Fine Delay register (0x63). This allows delay adjustments in steps of 119.2 ps definable as an 8-bit two's complement value in the range of -128 to +127. Negative values delay the output clock, positive values advance the output clock. This gives a total delay adjustment in the range of -15.26 ns to +15.14 ns.

In addition to the delay introduced by the DPLL Fine Delay, the SONET/SDH/Ethernet APLL and programmable synthesizer have the ability to add their own fine delay adjustments by programming registers 0x3D and 0x55. These registers are programmed as 8-bit two's complement values representing delays defined in steps of 119.2 ps with a range of -15.26 ns to +15.14 ns.

The single-ended output clocks (**apll_clk**, **p_clk**) can be independently offset by 90, 180, and 270 degrees using the coarse delay registers (0x3A, 0x53).

The differential clock output (**diff**) can be delayed by -1.6 ns, 0 ns, +1.6 ns, or +3.2 ns. This delay is programmable using the *diff_adjust* bit of the *diff_ctrl* register (0x60).

The output frame pulse (**p_fp**) can be offset using the frame pulse delay registers (0x40 - 0x42). Frame pulses generated from the programmable synthesizer (**p_fp**) associated with programmable synthesizer clock (**p_clk**) that are multiples of 2.048 MHz (E1) can be delayed in steps of 1/262.144 MHz (or approx. 3.81 ns). The delay value is programmed as a 16-bit value defined in registers 0x40/0x41. The maximum amount of delay is 125 μ s (= 32767 * 1/262.14 MHz). In addition, the frame pulses can be delayed in steps of 125 μ s (up to $2^6 * 125 \mu$ s = 8 ms) using the 0x42 register.

2.16 Master/Slave Configuration

In systems that provide redundant timing sources, it is desirable to minimize the output skew between the master and the slave's output clocks. This can be achieved by synchronizing the slave to one of the master's output clocks instead of synchronizing the slave to an external reference. If frame pulse alignment between the timing sources is required, then the crossover link should consist of a clk/fp pair.

One method of connecting two ZL30142 devices in a master/slave configuration is shown in Figure 14 where there is a dedicated crossover link between timing cards.

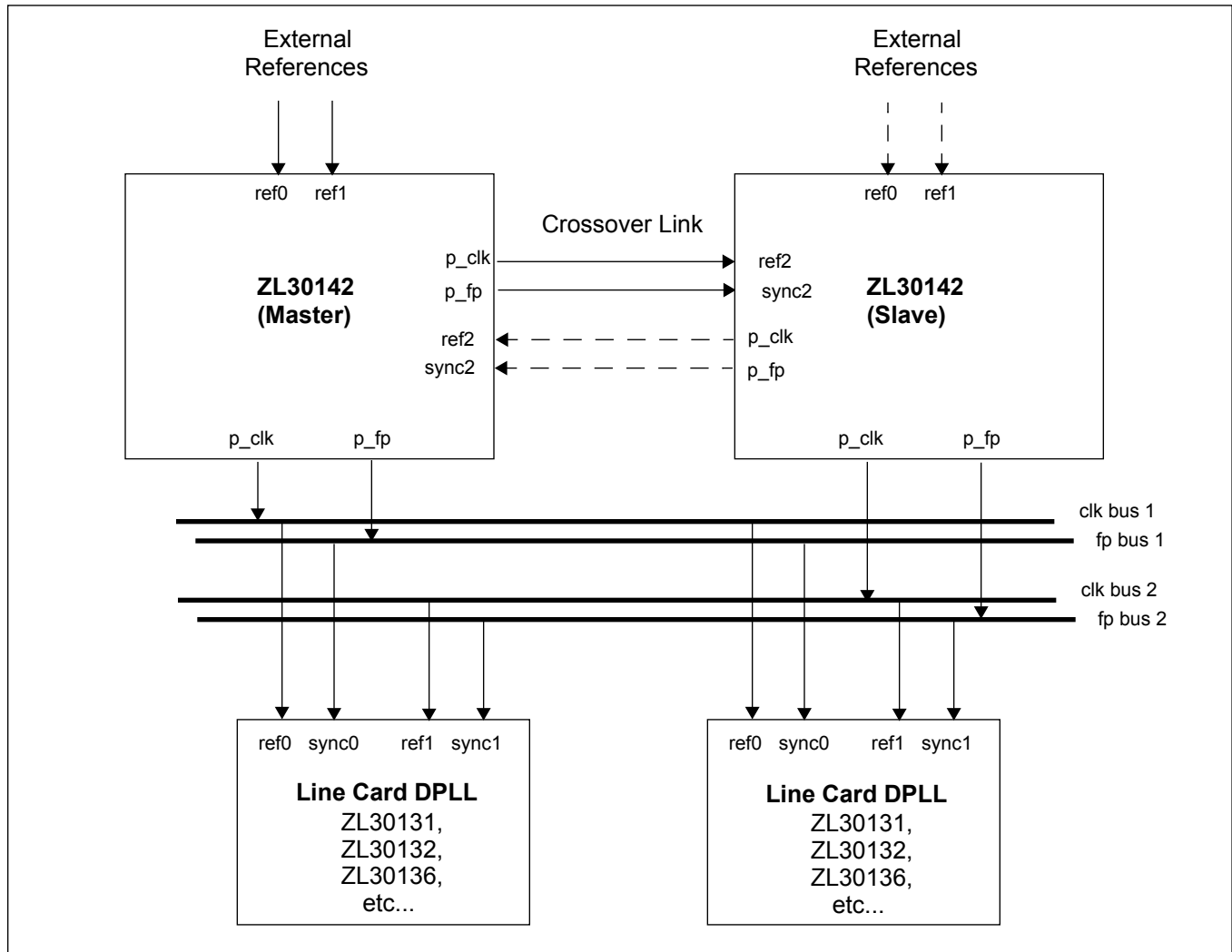


Figure 14 - Typical Master/Slave Configuration

2.17 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. It is important to select a master oscillator with the appropriate frequency accuracy and stability for the given application. Table 13 lists typical applications. Refer to application note ZLAN-68 for a list of recommended clock oscillators.

Master Oscillator Frequency Accuracy (+/- ppm)	Application
4.6	SONET Stratum 3, G.813 option 1 SEC, G.8262 EEC 1 & 2
20	SONET Minimum Clock, G.813 option 2 SEC
32	ANSI T1.403, Stratum 4
50	ITU-T G.703, ETSI ETS 300 011

Table 13 - Master Oscillator Frequency Accuracy

2.18 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 15. The connection to **osci** should be direct and not AC coupled. The **osco** pin must be left unconnected.

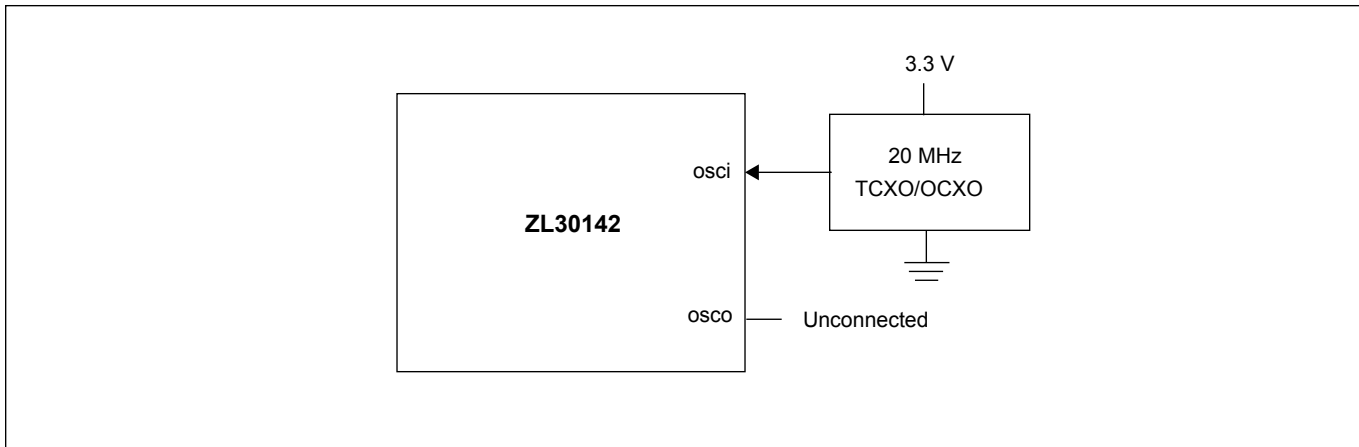


Figure 15 - Clock Oscillator Circuit

2.19 Power Up/Down Sequence

The 3.3 V power rail should be powered before or simultaneously with the 1.8 V power rail to prevent the risk of latch-up. The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

2.20 Power Supply Filtering

Jitter levels on the ZL30142 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30142 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Microsemi Application Note ZLAN-212.

2.21 Reset Circuit

To ensure proper operation, the device must be reset by holding the `rst_b` pin low for at least 300 ns after power-up. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 16. This circuit provides approximately 60 μ s of reset low time. The `rst_b` input has schmitt trigger properties to prevent level bouncing.

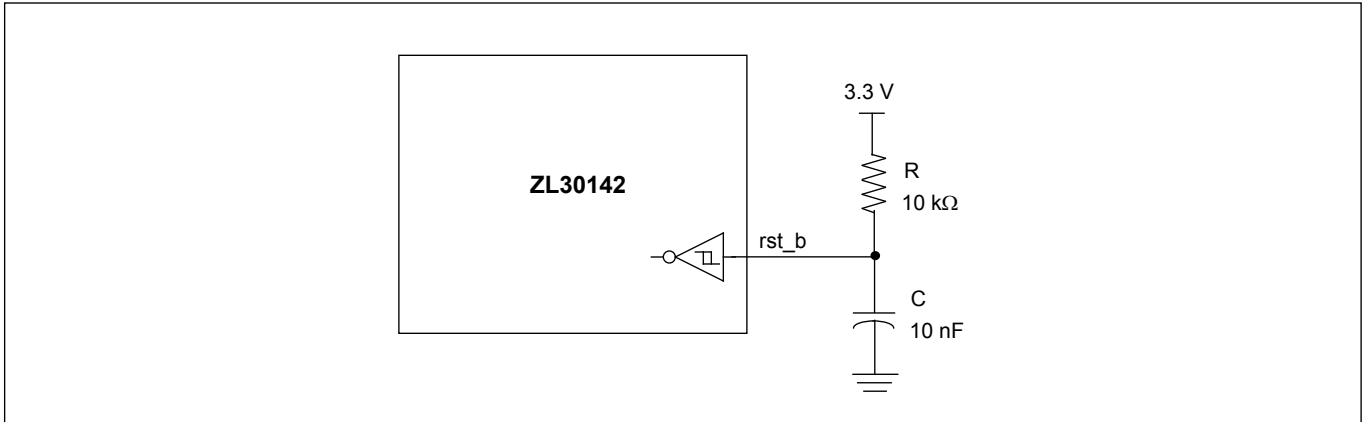


Figure 16 - Typical Power-Up Reset Circuit

2.22 APLL Filter Components and Recommended Layout

The low jitter APLL in the ZL30142 uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

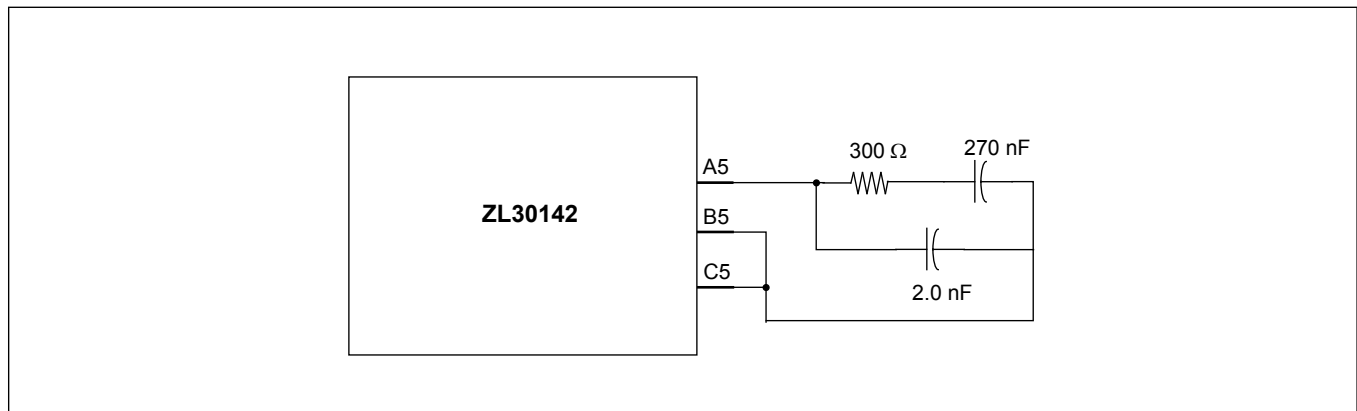


Figure 17 - APLL Filter Component Values

The recommended PCB layout for the external filter components is shown in Figure 18.

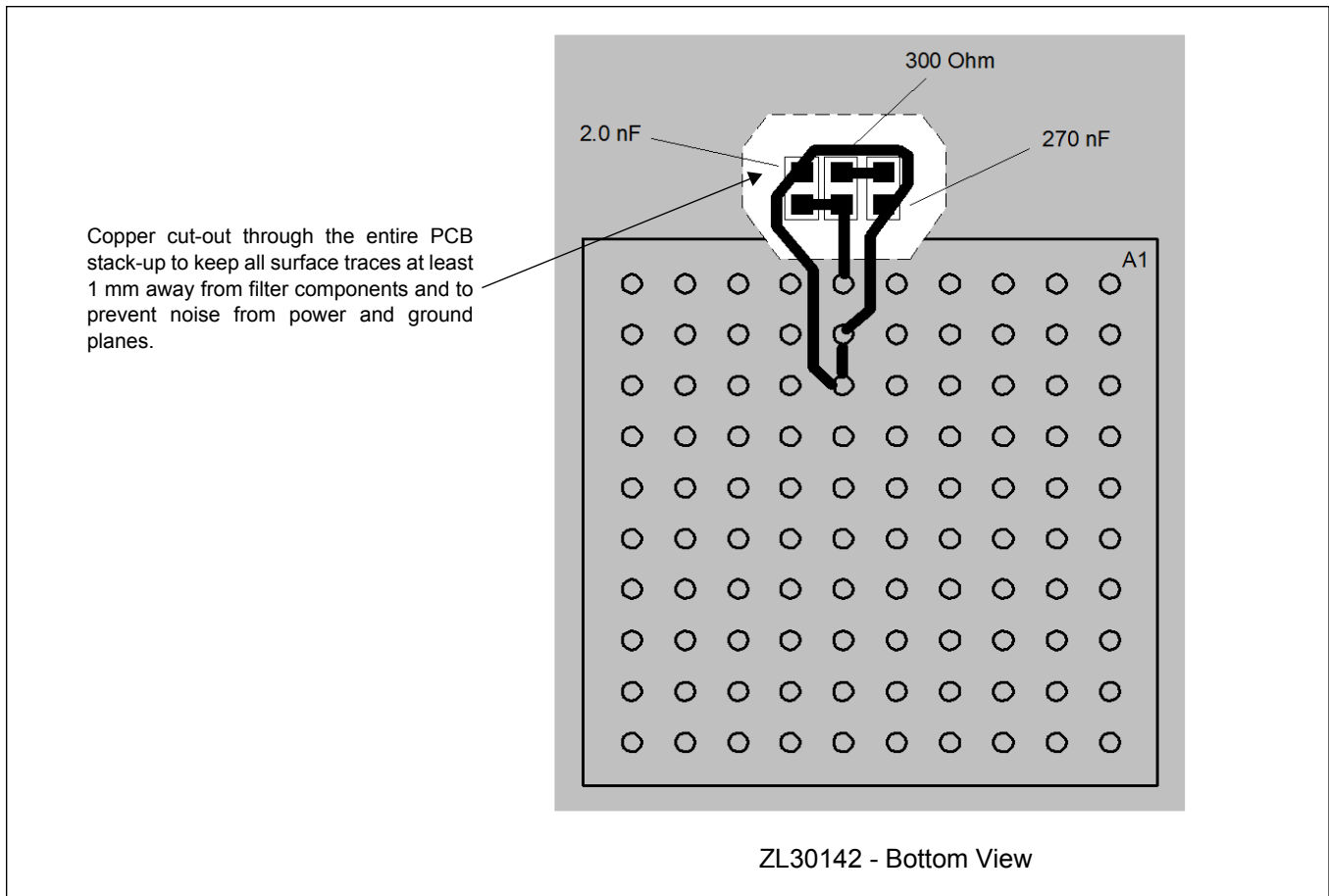


Figure 18 - Recommended APLL Filter Layout

2.23 Serial Interface

A host processor controls and receives status from the ZL30142 using either a SPI or an I²C interface. The type of interface is selected using the **i2c_en** pin. As shown in Figure 19, when **i2c_en** is set high (or left unconnected) the serial interface is compatible with an I²C bus and is compatible with SPI when set low.

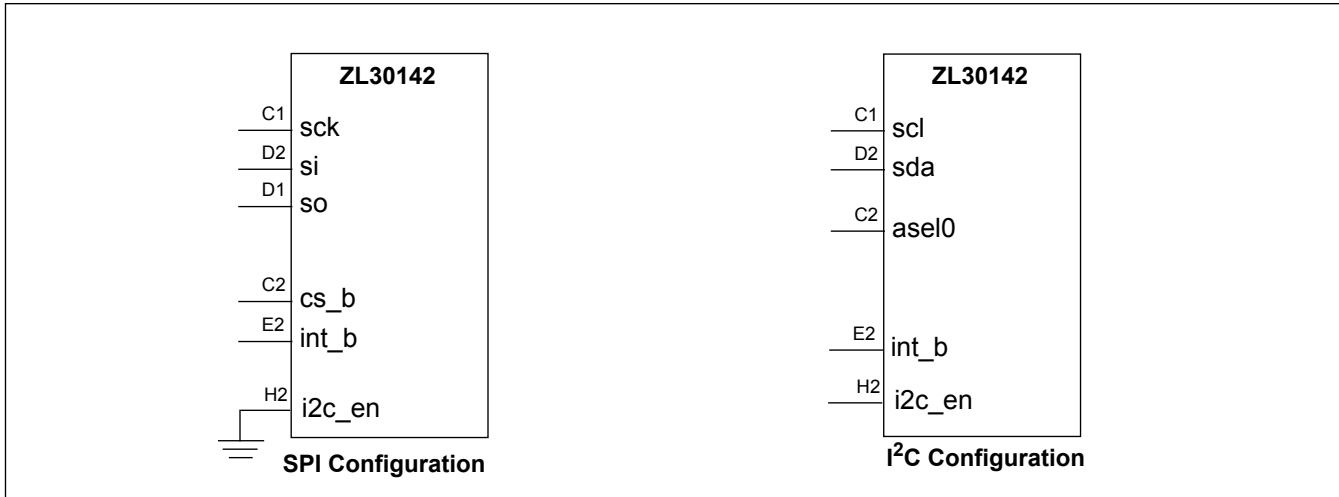


Figure 19 - Serial Interface Configuration

2.23.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **sck_scl** pin when the **cs_b_asel0** pin is active. If the **sck_scl** pin is low during **cs_b_asel0** activation, then MSB first timing is selected. If the **sck_scl** pin is high during **cs_b_asel0** activation, then LSB first timing is assumed.

The SPI port expects 7-bit addressing and 8-bit data transmission, and is reset when the chip select pin **cs_b_asel0** is high. During SPI access, the **cs_b_asel0** pin must be held low until the operation is complete. The first bit transmitted during the address phase of a transfer indicates whether a read (1) or a write (0) is being performed. Burst read/write mode is also supported by leaving the chip select signal **cs_b_asel0** low after a read or a write. The address will be automatically incremented after each data byte is read or written.

The SPI supports half-duplex processor mode which means that during a write cycle to the ZL30142, output data from the **so** pin must be ignored. Similarly, the input data on the **si_sda** pin is ignored by the device during a read cycle from the ZL30142.

Functional waveforms for the LSB and MSB first mode, and burst mode are shown in Figure 20, Figure 21 and Figure 22. Timing characteristics are shown in Table 15, Figure 35, and Figure 36.

2.23.2 SPI Functional Waveforms

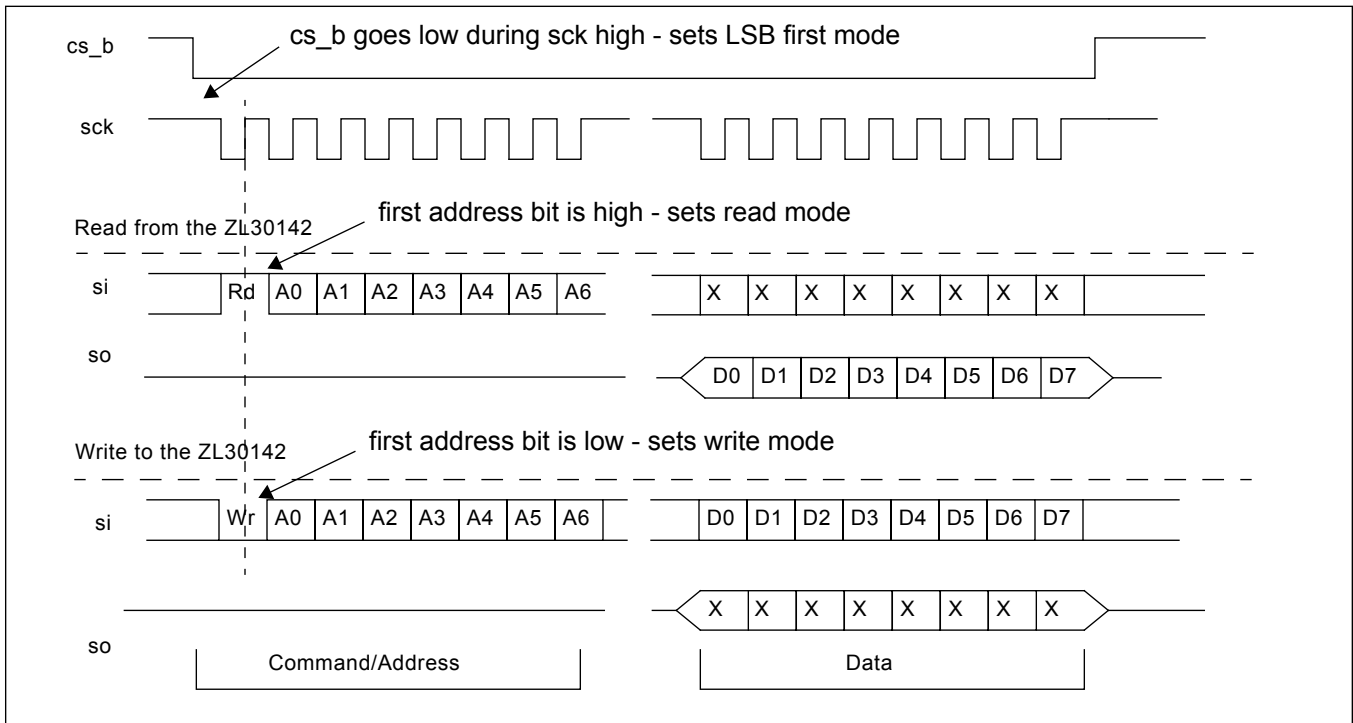


Figure 20 - LSB First Mode - One Byte Transfer

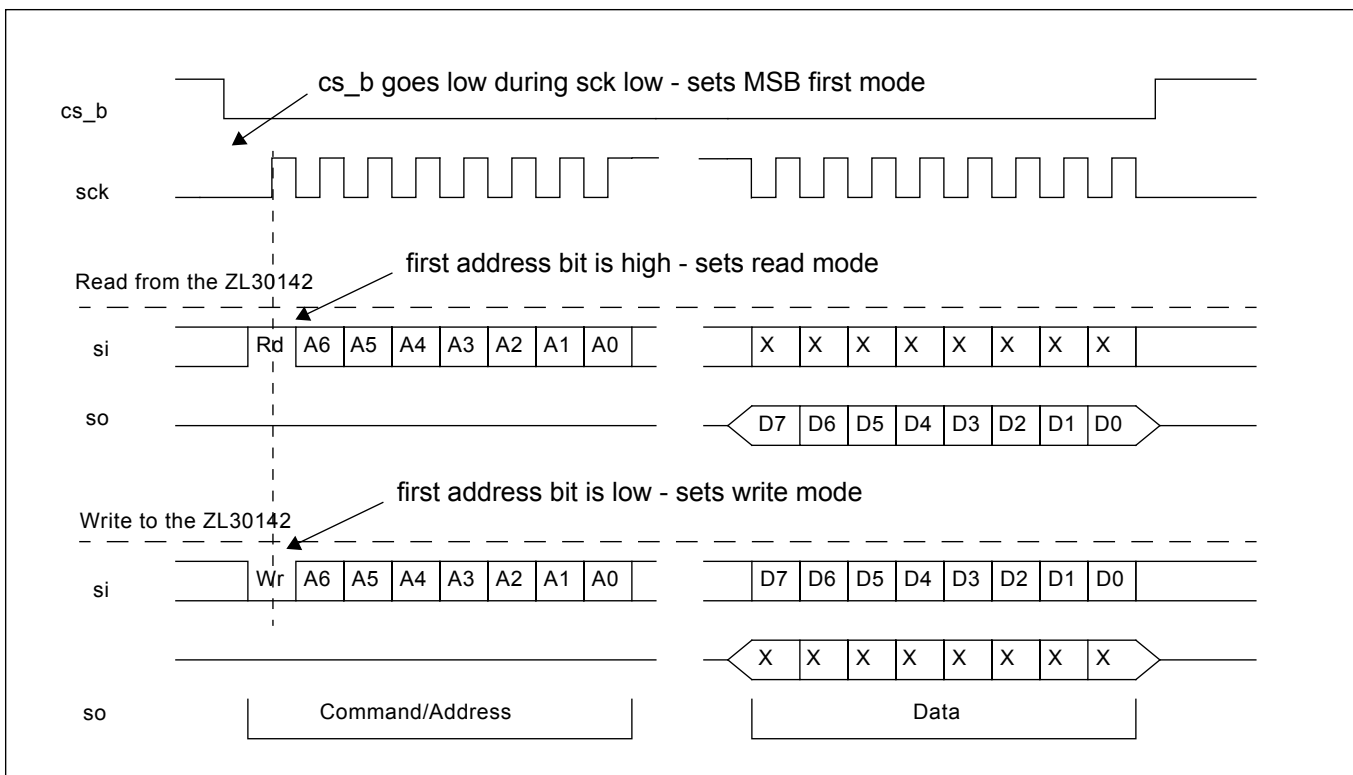


Figure 21 - MSB First Mode - One Byte Transfer

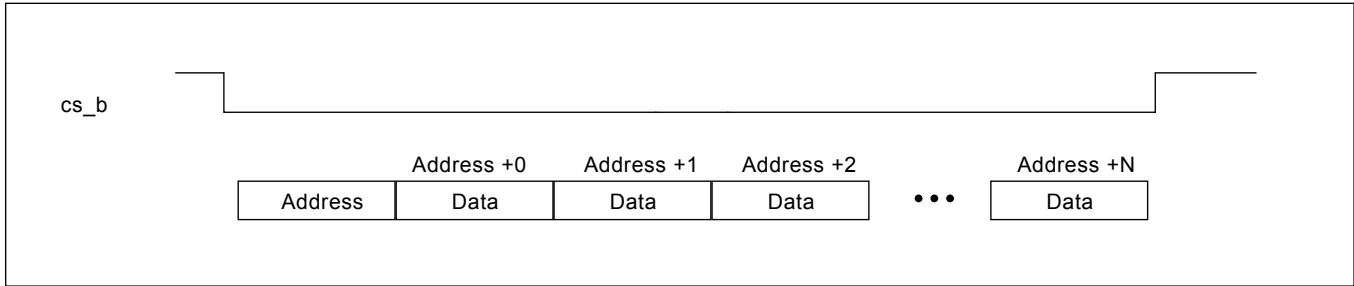


Figure 22 - Example of a Burst Mode Operation

2.23.3 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSB first and occurs in 1 byte blocks. As shown in Figure 23, a **write** command consists of a 7-bit device (slave) address, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

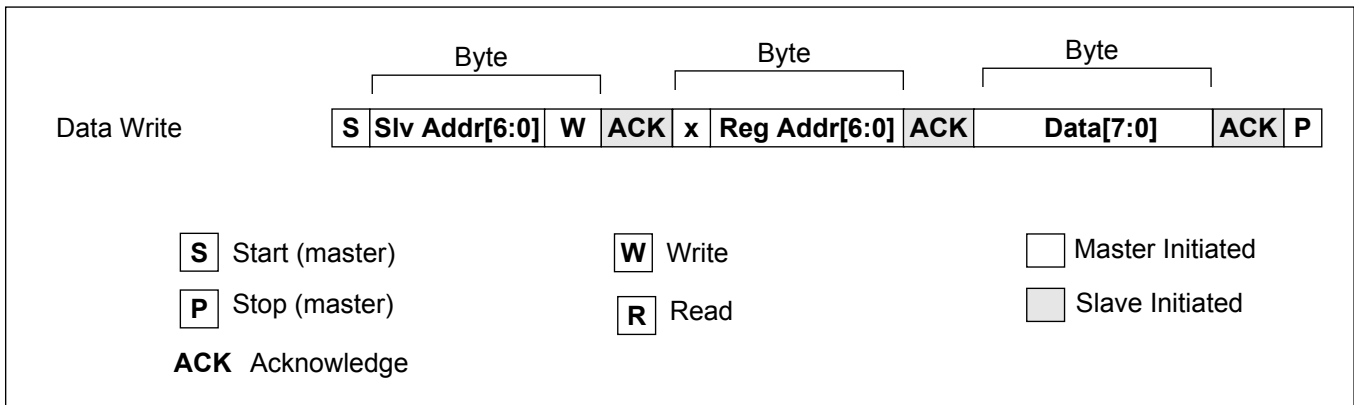


Figure 23 - I²C Data Write Protocol

A **read** is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 24.

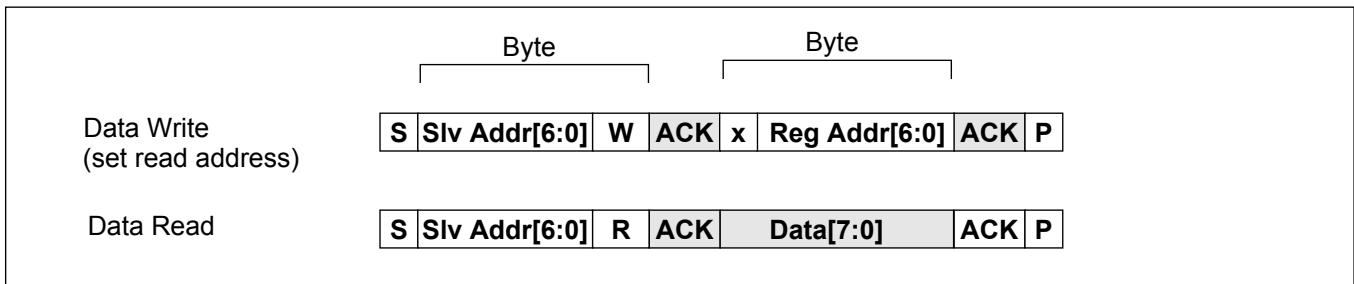


Figure 24 - I²C Data Write Protocol

The **7-bit device (slave) address** of the ZL30142 contains a 6 bit fixed address plus a variable bit which is set with the **asel0** pin. This allows two ZL30142s to share the same I²C bus. The address configuration is shown in Figure 25.

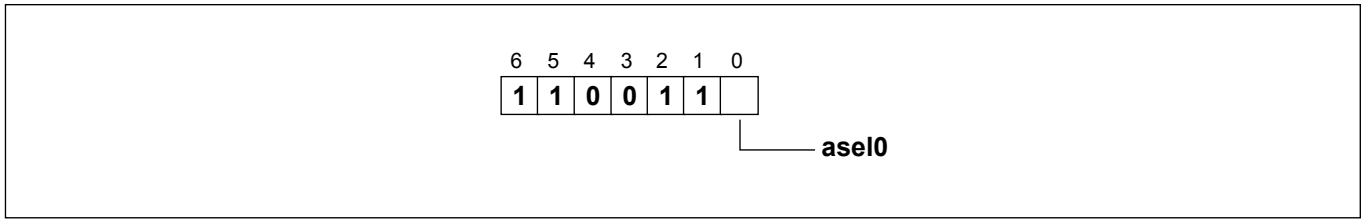


Figure 25 - ZL30142 I²C 7-bit Slave Address

The ZL30142 also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 26 (write) and Figure 27 (read). The first data byte is written/read from the specified address, and subsequent data bytes are written/read using an automatically incremented address. The maximum auto incremented address of a burst operation is 0x7F. Any operations beyond this limit will be ignored. In other words, the auto incremented address does not wrap around to 0x00 after reaching 0x7F.

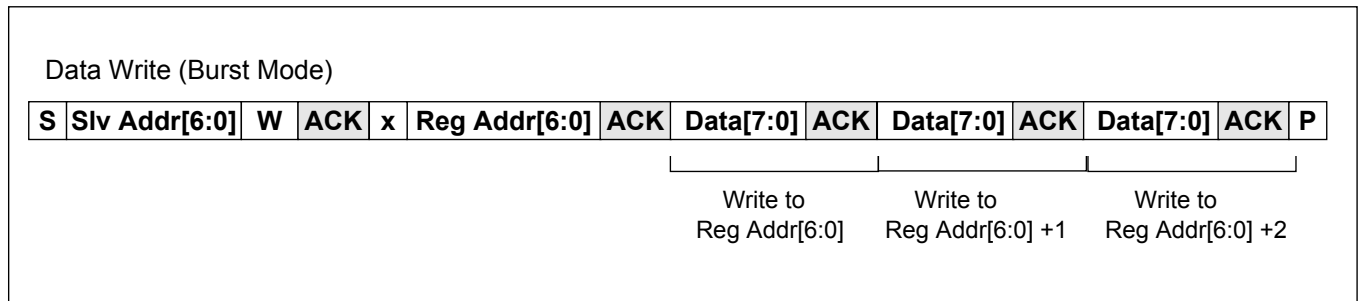


Figure 26 - I²C Data Write Burst Mode

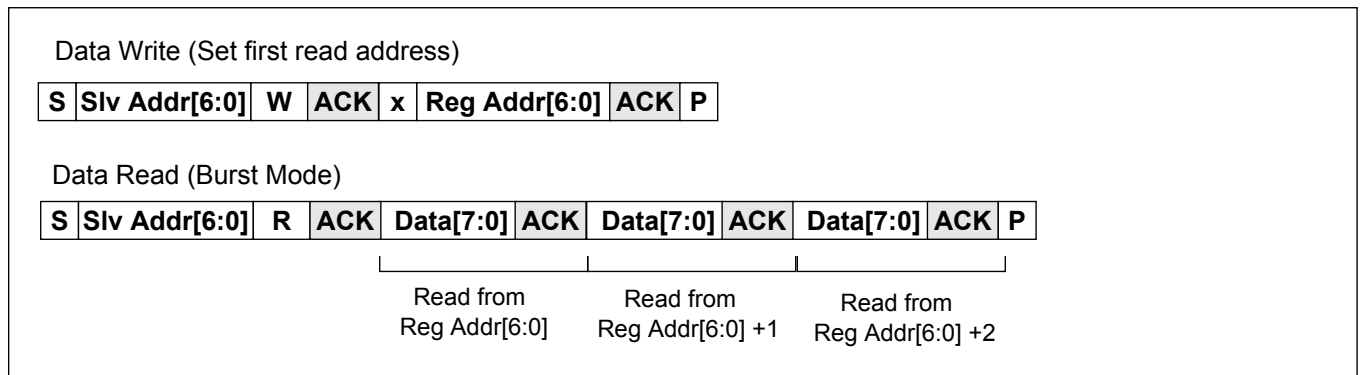


Figure 27 - I²C Data Read Burst Mode

The timing specification for the I²C interface is shown in Figure 37 and Table 16.

3.0 Software Configuration

The ZL30142 is mainly controlled by accessing software registers through the serial interface (SPI or I²C). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

3.1 Interrupts

The device has several status registers to indicate its current state of operation. The interrupt pin (**int_b**) becomes active (low) when a critical change in status occurs. Examples of critical events that would trigger an interrupt are:

- Reference or sync input failures
- Changes in mode of operation (lock, holdover)
- Reference input switchovers

Most of the interrupt register bits behave like "sticky bits" which means that once they are triggered, they will stay triggered even if the condition that caused the interrupt is removed. When a register containing sticky bits is read, the sticky bits are automatically cleared.

3.2 Extended Page Registers

The memory map is organized over 16 pages. Addressable locations as shown in Figure 28. Most of the general configuration and status registers are located in page 0, but some are located in the extended page area of the memory map. Extended page register addresses are identified with a two digit prefix in this document (e.g., **08_0x6E**). Register addresses with no prefix (e.g., 0x6F) are located in page zero.

The page location is defined in the *page_pointer* register (0x64). By default this register is set to 00 so that access to page zero registers can easily be made. To access extended pages of the memory map, the page pointer must be first set to the desired page location. For example, to access register 08_0x6E, write 0x08 to register 0x64, then read or write to register 0x6E. It is recommended that the page pointer is set back to 0x00 once access to an extended page location is complete.

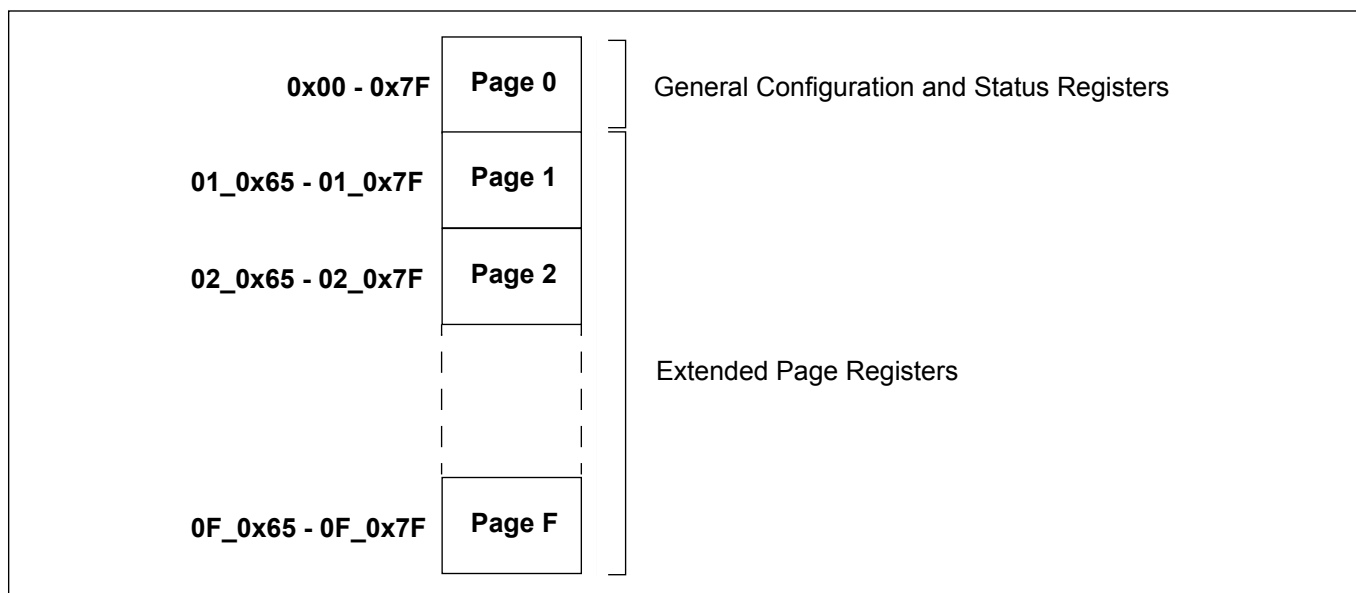


Figure 28 - Memory Map Organization

3.3 Multi-byte Register Values

The ZL30142 register map is based on 8-bit register access, so register values that require more than 8 bits must be spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the least significant byte (LSB) must be accessed first, and the register containing the most significant byte (MSB) must be accessed last. An example of a multi-byte register is shown in Figure 29. When reading a multi-byte value, the value across all of its registers remains stable until the MSB is read. When writing a multi-byte value, the value is latched when the MSB is written.

Example:

The programmable frame pulse phase offset for p_fp is programmed using a 22-bit value which is spread over three 8-bit registers. The LSB is contained in address 0x40, the middle byte in 0x41, and the MSB in 0x42. When reading or writing this multi-byte value, the LSB must be accessed first, followed by the middle byte, and the MSB last.

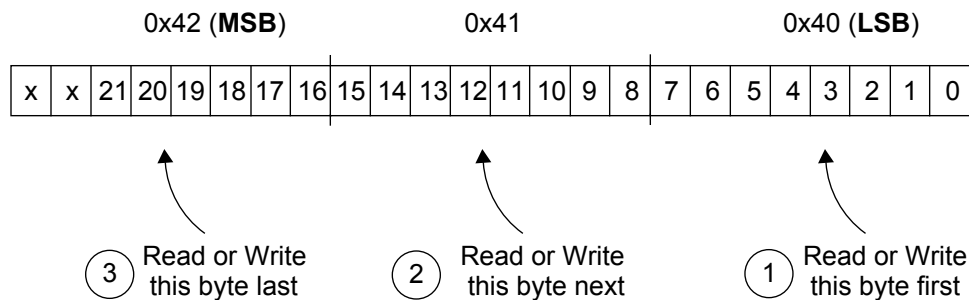


Figure 29 - Accessing Multi-byte Register Values

The following table provides a summary of the registers available for status updates and configuration of the device.

Page_Addr (Hex)	Register Name	Description	Type
Miscellaneous Registers			
0x00	id_reg	Chip and version identification	R
0x01	use_hw_ctrl	Allows some functions of the device to be controlled by hardware pins	R/W
Interrupts			
0x02	ref_fail_isr	Reference failure interrupt service register	R
0x03	dpll_isr	DPLL interrupt service register	StickyR
0x04	Reserved		
0x05	ref_mon_fail_0	Ref0 and ref1 failure indications	Sticky R
0x06	ref_mon_fail_1	Ref2 failure indications	Sticky R
0x07 - 0x08	Reserved		
0x09	ref_fail_isr_mask	Reference failure interrupt service register mask	R/W
0x0A	dpll_isr_mask	DPLL interrupt service register mask	R/W
0x0B	Reserved		
0x0C	ref_mon_fail_mask_0	Control register to mask each failure indicator for ref0 and ref1	R/W
0x0D	ref_mon_fail_mask_1	Control register to mask each failure indicator for ref2	R/W
0x0E - 0x0F	Reserved		
Reference Monitor Setup			
0x10	detected_ref_0	Ref0 and ref1 auto-detected frequency value status register	R
0x11	detected_ref_1	Ref2 auto-detected frequency value status register	R
0x12 - 0x13	Reserved		
0x14	detected_sync_0	Sync0 and sync1 auto-detected frequency value and sync failure status register	R
0x15	detected_sync_1	Sync2 auto-detected frequency value and sync failure status register	R

Table 14 - Register Map

Page_Addr (Hex)	Register Name	Description	Type
0x16	oor_ctrl_0	Control register for the ref0 and ref1 out of range limit	R/W
0x17	oor_ctrl_1	Control register for the ref2 out of range limit	R/W
0x18 - 0x19	Reserved		
0x1A	gst_mask_0	Control register to mask the inputs to the guard soak timer for ref0 to ref2	R/W
0x1B	Reserved		
0x1C	gst_qualif_time	Control register for the guard soak timer qualification time and disqualification time for the references	R/W
DPLL Control Registers			
0x1D	dpll_ctrl_0	Control register for the DPLL filter control; phase slope limit, bandwidth and hitless switching	R/W
0x1E	dpll_ctrl_1	Holdover update time, filter_out_en, freq_offset_en, revert enable	R/W
0x1F	dpll_modesel	Control register for the DPLL mode of operation	R/W
0x20	dpll_refsel	DPLL reference selection or reference selection status	R/W
0x21	dpll_ref_fail_mask	Control register to mask each failure indicator (SCM, CFM, PFM and GST) used for automatic reference switching and automatic holdover	R/W
0x22	dpll_wait_to_restore	Control register to indicate the time to restore a previous failed reference	R/W
0x23	dpll_ref_rev_ctrl	Control register for the ref0 and ref1 enable revertive signals	R/W
0x24	dpll_ref_pri_ctrl_0	Control register for the ref0 and ref1 priority values	R/W
0x25	dpll_ref_pri_ctrl_1	Control register for the ref2 priority values	R/W
0x26 - 0x27	Reserved		
0x28	dpll_hold_lock_fail	DPLL lock and holdover status register	R
0x29	dpll_pullinrange	DPLL Pull-in range	R/W

Table 14 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x2A - 0x35	Reserved		
Programmable Synthesizer Configuration Registers			
0x36	p_enable	Control register to enable the p_clk and p_fp outputs of the programmable synthesizer	R/W
0x37	p_run	Control register to enable/disable p_clk, p_fp	R/W
0x38	p_clk_freq_0	Configuration bits 7:0 used to set the frequency for p_clk	R/W
0x39	p_clk_freq_1	Configuration bits 13:8 used to set the frequency for p_clk	R/W
0x3A	p_clk_offset90	Control register for the p_clk phase position coarse tuning	R/W
0x3B - 0x3C	Reserved		
0x3D	p_offset_fine	Control register for the output/output phase alignment fine tuning for the p_clk path	R/W
0x3E	p_fp_freq	Control register to select the p_fp frame pulse frequency	R/W
0x3F	p_fp_type	Control register to select p_fp type	R/W
0x40	p_fp_offset_0	Bits [7:0] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	0x40
0x41	p_fp_offset_1	Bits [15:8] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	0x41
0x42	p_fp_offset_2	Bits [21:16] of the programmable frame pulse phase offset in multiples of 8 kHz cycles	0x42
0x43 - 0x4F	Reserved		
0x50	apll_enable	Control register to enable eth_clk and the APLL block	R/W
0x51	apll_run	Control register to generate apll_clk. Also used for enabling ethernet output clocks.	R/W
0x52	apll_clk_freq	Control register for the apll_clk frequency selection	R/W
0x53	apll_clk_offset90	Control register for the apll_clk phase position coarse tuning	R/W

Table 14 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x54	Reserved		
0x55	apll_offset_fine	Control register for the apll path	R/W
0x56 - 0x5F	Reserved		
Differential Output Configuration			
0x60	diff_clk_ctrl	Control register to enable diff_clk	R/W
0x61	diff_clk_sel	Control register to select the diff_clk frequency	R/W
0x62	Reserved		
0x63	dpll_offset	Control register for the input/output phase alignment fine tuning for the DPLL	R/W
0x64	Page pointer	Use to access extended page addresses	
Custom Input Frequency Configuration			
0x65	ref_freq_mode_0	Control register to set whether to use auto detect, CustomA or CustomB for ref0, ref1, ref2	R/W
0x66	Reserved		
0x67	custA_mult_0	Control register for the [7:0] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
0x68	custA_mult_1	Control register for the [13:8] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
0x69	custA_scm_low	Control register for the custom configuration A: single cycle SCM low limiter	R/W
0x6A	custA_scm_high	Control register for the custom configuration A: single cycle SCM high limiter	R/W
0x6B	custA_cfm_low_0	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM low limit	R/W
0x6C	custA_cfm_low_1	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM low limit	R/W
0x6D	custA_cfm_hi_0	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM high limit	R/W

Table 14 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x6E	custA_cfm_hi_1	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM high limiter	R/W
0x6F	custA_cfm_cycle	Control register for the custom configuration A: CFM reference monitoring cycles - 1	R/W
0x70	custA_div	Control register for the custom configuration A: enable the use of ref_div4 for the CFM and PFM inputs	R/W
0x71	custB_mult_0	Control register for the [7:0] bits of the custom configuration B. This is the 8 k integer for the N*8kHz reference monitoring.	R/W
0x72	custB_mult_1	Control register for the [13:8] bits of the custom configuration B. This is the 8 k integer for the N*8kHz reference monitoring.	R/W
0x73	custB_scm_low	Control register for the custom configuration B: single cycle SCM low limiter	R/W
0x74	custB_scm_high	Control register for the custom configuration B: single cycle SCM high limiter	R/W
0x75	custB_cfm_low_0	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM low limiter.	R/W
0x76	custB_cfm_low_1	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM low limiter.	R/W
0x77	custB_cfm_hi_0	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM high limiter.	R/W
0x78	custB_cfm_hi_1	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM high limiter.	R/W
0x79	custB_cfm_cycle	Control register for the custom configuration B: CFM reference monitoring cycles - 1	R/W
0x7A	custB_div	Control register for the custom configuration B: enable the use of ref_div4 for the CFM and PFM inputs	R/W
0x7B to 0x7D	Reserved		

Table 14 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
Input Reference Pre-Divider Control			
0x7E	predivider_control	Controls pre-dividers for ref0 and ref1	R/W
0x7F	Reserved		
Extended Page Area			
Free Run Frequency Offset			
01_0x65	DCO_freq_offset_0	Set programmable DCO frequency offset	R/W
01_0x66	DCO_freq_offset_1	Set programmable DCO frequency offset	R/W
01_0x67	DCO_freq_offset_2	Set programmable DCO frequency offset	R/W
01_0x68	DCO_freq_offset_3	Set programmable DCO frequency offset	R/W
01_0x69	DCO_phase_0	Bits [7:0] of the 64 bit DCO Phase Word	R
01_0x6A	DCO_phase_1	Bits [15:8] of the 64 bit DCO Phase Word	R
01_0x6B	DCO_phase_2	Bits [23:16] of the 64 bit DCO Phase Word	R
01_0x6C	DCO_phase_3	Bits [31:24] of the 64 bit DCO Phase Word	R
01_0x6D	DCO_phase_4	Bits [39:32] of the 64 bit DCO Phase Word	R
01_0x6E	DCO_phase_5	Bits [47:40] of the 64 bit DCO Phase Word	R
01_0x6F	DCO_phase_6	Bits [55:48] of the 64 bit DCO Phase Word	R
01_0x70	DCO_phase_7	Bits [63:56] of the 64 bit DCO Phase Word	R
01_0x71	Local_Time_0	Bits [7:0] of the 32 bit Local System Time	R
01_0x72	Local_Time_1	Bits [15:8] of the 32 bit Local System Time	R
01_0x73	Local_Time_2	Bits [23:16] of the 32 bit Local System Time	R
01_0x74	Local_Time_3	Bits [31:24] of the 32 bit Local System Time	R
01_0x75	ToD_update_0	Bits[7:0] of the 64 bit ToD update register	R
01_0x76	ToD_update_1	Bits[15:8] of the 64 bit ToD update register	R
01_0x77	ToD_update_2	Bits[23:16] of the 64 bit ToD update register	R
01_0x78	ToD_update_3	Bits[31:24] of the 64 bit ToD update register	R
01_0x79	ToD_update_4	Bits[39:32] of the 64 bit ToD update register	R
01_0x7A	ToD_update_5	Bits[47:40] of the 64 bit ToD update register	R
01_0x7B	ToD_update_6	Bits[55:48] of the 64 bit ToD update register	R
01_0x7C	ToD_update_7	Bits[63:56] of the 64 bit ToD update register	R
Extended Page Area			

Table 14 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
01_0x7D to 08_0x70	Reserved		
1Hz Sync enable Register			
08_0x71	1Hz_enable	Enables 1Hz sync detection	R/W
08_0x72 to 0A_0x6B	Reserved		
DCO update configuration Registers (ToP Client Mode)			
0A_0x6C	DCO_update	Enables DCO updates	R/W
0A_0x6D to 0A_0x70	Reserved		
0A_0x71	DCO_Update_Interval	Configures DCO update Interval	R/W
0A_0x72	ToP_1Hz_Alignment	Enables 1 Hz alignment in ToP Client Mode	R/W
Extended Page Area			
0A_0x73 to 0A_0x75	Reserved		
0A_0x76	Time_of_Day_0	Bits[7:0] of the 64 bit Time of Day register	R/W
0A_0x77	Time_of_Day_1	Bits[15:8] of the 64 bit Time of Day register	R/W
0A_0x78	Time_of_Day_2	Bits[23:16] of the 64 bit Time of Day register	R/W
0A_0x79	Time_of_Day_3	Bits[31:24] of the 64 bit Time of Day register	R/W
0A_0x7A	Time_of_Day_4	Bits[39:32] of the 64 bit Time of Day register	R/W
0A_0x7B	Time_of_Day_5	Bits[47:40] of the 64 bit Time of Day register	R/W
0A_0x7C	Time_of_Day_6	Bits[55:48] of the 64 bit Time of Day register	R/W
0A_0x7D	Time_of_Day_7	Bits[63:56] of the 64 bit Time of Day register	R/W
0A_7E to 0Fx6D	Reserved		
Timing over Packet (ToP) Interrupt Service Registers			
0F_0x6E	ToP_isr	Indicates ToP interrupt	Sticky R
0F_0x6F	ToP_isr_mask	ToP interrupt mask	R/W

Table 14 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0F_0x6B to 0F_0x7C	Reserved		
Interrupt Service Registers			
0F_0x7D	isr0_reg	Indicates Interrupt Source	R/W
0F_0x7E	isr0_mask	Masks Interrupt sources	R/W
0F_0x7F	Reserved		

Table 14 - Register Map (continued)

4.0 Detailed Register Map

Page_Address: 0x00 Register Name: id_reg Default Value: See description Type: R/W		
Bit Field	Function Name	Description
4:0	chip_id	Chip Identification = 11100
6:5	chip_revision	Chip revision number.
7	reset_ready	Reset ready indication. When this bit is set to 1 the reset cycle has completed. Note that it is recommended not to read or write to any other registers until this bit is set to 1. It takes 5 ms after the reset for this bit to go high.

Page_Address: 0x01 Register Name: use_hw_ctrl Default Value: 0x00 Type: R/W		
Bit Field	Function Name	Description
0	reserved	Leave as default
1	dpll_mode_hsw	This bit determines how the mode selection for DPLL is controlled. When set to 0, the mode selection is s/w controlled using the modesel bits of the dpll_modesel register (0x1F). When set to 1, the mode selection is h/w controlled using the mode pin.

Page_Address: **0x01**
 Register Name: **use_hw_ctrl**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:2	reserved	Leave as default

Address: **0x02**
 Register Name: **ref_fail_isr**
 Default Value: 0xFF
 Type: R

Bit Field	Function Name	Description
0	ref0_fail	This bit is set to 1 when ref0 has a failure
1	ref1_fail	This bit is set to 1 when ref1 has a failure
2	ref2_fail	This bit is set to 1 when ref2 has a failure
7:3	Reserved	Leave as default

Address: **0x03**
 Register Name: **dppll_isr**
 Default Value: **See description**
 Type: R Sticky

Bit Field	Function Name	Description
0	locked	This bit is set to high when DPLL achieves lock. The bit is cleared automatically when this register is read.
1	lost_lock	This bit is set to high when DPLL loses lock. The bit is cleared automatically when this register is read.
2	holdover	This bit is set to high when DPLL enters holdover. The bit is cleared automatically when this register is read.
3	ref_changed	This bit is set to high when DPLL makes a reference switch. The bit is cleared automatically when this register is read.
6:4	sync_fail[2:0]	This bit is set to high when a failure of the sync[i] is detected. The bit is cleared automatically when this register is read.
7	reserved	Leave as default

Address: **0x05**
 Register Name: **ref_mon_fail_0**
 Default Value: **See description**
 Type: Sticky R

Bit Field	Function Name	Description
0	ref0_scm_failed	SCM failure indication
1	ref0_cfm_failed	CFM failure indication
2	ref0_gst_failed	GST failure indication
3	ref0_pfm_failed	PFM failure indication
4	ref1_scm_failed	SCM failure indication
5	ref1_cfm_failed	CFM failure indication
6	ref1_gst_failed	GST failure indication
7	ref1_pfm_failed	PFM failure indication

Address: **0x06**
 Register Name: **ref_mon_fail_1**
 Default Value: **See description**
 Type: R Sticky

Bit Field	Function Name	Description
0	ref2_scm_failed	SCM failure indication (1 indicates a failure)
1	ref2_cfm_failed	CFM failure indication (1 indicates a failure)
2	ref2_gst_failed	GST failure indication (1 indicates a failure)
3	ref2_pfm_failed	PFM failure indication (1 indicates a failure)
7:4	Reserved	Leave as default

Address: **0x09**Register Name: **ref_fail_isr_mask**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	ref_fail_isr_mask	Reference failure interrupt service register mask.Masking a bit to zero will disable interrupt generation. xxxxxxx0: masks ref0 failure xxxxxx0x: masks ref1 failure xxxxx0xx: masks ref2 failure

Address: **0x0A**Register Name: **dpll_isr_mask**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
6:0	dpll_isr_mask	DPLL interrupt service register mask. Enabling a mask bit to one will allow interrupt generation xxxxxxx0: masks locked condition xxxxxx0x: masks lost_lock condition xxxxx0xx: masks holdover condition xxxx0xxx: masks ref_changed condition x000xxxx: masks sync_fail[1:0] failure
7	Reserved	Leave as default

Address: **0x0C**
 Register Name: **ref_mon_fail_mask_0**
 Default Value: 0xFF
 Type: R/W

Bit Field	Function Name	Description
3:0	ref0_mon_fail_mask	Control register to mask each failure indicator for ref0 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure
7:4	ref1_mon_fail_mask	Control register to mask each failure indicator for ref1 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure

Address: **0x0D**
 Register Name: **ref_mon_fail_mask_1**
 Default Value: 0xFF
 Type: R/W

Bit Field	Function Name	Description
3:0	ref2_mon_fail_mask	Control register to mask each failure indicator for ref2 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure
7:4	Reserved	Leave as default

Address: **0x10**Register Name: **detected_ref_0**Default Value: **See description**

Type: R

Bit Field	Function Name	Description
3:0	ref0_frq_detected	ref0 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected
7:4	ref1_frq_detected	ref1 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected

Address: **0x11**Register Name: **detected_ref_1**Default Value: **See description**

Type: R

Bit Field	Function Name	Description
3:0	ref2_frq_detected	ref2 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected
7:4	Reserved	Leave as default

Address: **0x14**Register Name: **detected_sync_0**Default Value: **See description**

Type: R

Bit Field	Function Name	Description
2:0	sync0_frq_detected	sync0 frequency value 000 -> 166.67 Hz 001 -> 400 Hz 010 -> 1 kHz 011 -> 2 kHz 100 -> 1 Hz 101 -> 8 kHz 111 -> 64 kHz Otherwise: not yet detected
3	sync0_fail	sync0 fail status. A value of 1 indicates a failure.

Address: **0x14**
 Register Name: **detected_sync_0**
 Default Value: **See description**
 Type: R

Bit Field	Function Name	Description
6:4	sync1_frq_detected	sync1 frequency value 000 -> 166.67 Hz 001 -> 400 Hz 010-> 1 kHz 011 -> 2 kHz 100 -> 1 Hz 101 -> 8 kHz 111 -> 64 kHz Otherwise: not yet detected
7	sync1_fail	sync1 valid status. A value of 1 indicates a failure

Address: **0x15**
 Register Name: **detected_sync_1**
 Default Value: **See description**
 Type: R

Bit Field	Function Name	Description
2:0	sync2_frq_detected	sync2 frequency value 000 -> 166.67 Hz 001 -> 400 Hz 010 -> 1 kHz 011 -> 2 kHz 100 -> 1 Hz 101 -> 8 kHz 111 -> 64 kHz Otherwise: not yet detected
3	sync2_fail	sync2 fail status. A value of 1 indicates a failure.
7:4	Reserved	Leave as default

Address: **0x16**Register Name: **oor_ctrl_0**

Default Value:0x33

Type: R/W

Bit Field	Function Name	Description
2:0	ref0_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
3	Reserved	Leave as default
6:4	ref1_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
7	Reserved	Leave as default

Address: **0x17**
 Register Name: **oor_ctrl_1**
 Default Value: 0x33
 Type: R/W

Bit Field	Function Name	Description
2:0	ref2_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
7:3	Reserved	Leave as default

Address: **0x1A**
 Register Name: **gst_mask_0**
 Default Value: 0xFF
 Type: R/W

Bit Field	Function Name	Description
1:0	ref0_gst_mask	ref0 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
3:2	ref1_gst_mask	ref1 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
5:4	ref2_gst_mask	ref2 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
7:6	Reserved	Leave as default

Address: 0x1C Register Name: gst_qualif_time Default Value: 0x1A Type: R/W		
Bit Field	Function Name	Description
3:0	time_to_disqualify	Guard_soak_timer control bits to disqualify the reference 0000: -> minimum delay possible 0001: -> 0.5 ms 0010: -> 1 ms 0011: -> 5 ms 0100: -> 10 ms 0101: -> 50 ms 0110: -> 100 ms 0111: -> 500 ms 1000: -> 1 s 1001: -> 2 s 1010: -> 2.5 s 1011: -> 4 s 1100: -> 8 s 1101: -> 16 s 1110: -> 32 s 1111: -> 64 s
5:4	time_to_qualify	Timer control bits to qualify the reference. 00: -> 2 times the time to disqualify 01: -> 4 times the time to disqualify 10: -> 16 times the time to disqualify 11: -> 32 times the time to disqualify
7:6	Reserved	Leave as default

Address: 0x1D Register Name: dpll_ctrl_0 Default Value: See description Type: R/W		
Bit Field	Function Name	Description
0	$\overline{\text{hs_en}}$	Controls hitless reference switching. When set to 0 (default), DPLL builds-out the phase difference between the current and the new reference to minimize the phase transient at the output. When set to 1, the output realigns itself with the new input phase. Hitless switching is enabled by default.

Address: 0x1D Register Name: dpll_ctrl_0 Default Value: See description Type: R/W		
Bit Field	Function Name	Description
3:1	bandwidth	000: 0.1 Hz 001: 1.7 Hz 010: 3.5 Hz 011: 14 Hz 100: 28 Hz (limited to 14 Hz for 2 kHz references) 101: 890 Hz (limited to 14 Hz and 56 Hz for 2 kHz and 8 kHz references respectively) 110: fast lock (7 Hz) (default) 111: Reserved
5:4	dpll_ph_slopelim	available phase slope limits 00: 885 ns/s 01: 7.5 μ s/s 10: 61 μ s/s 11: unlimited (default)
7:6	reserved	Leave as default

Address: 0x1E Register Name: dpll_ctrl_1 Default Value: See description Type: R/W		
Bit Field	Function Name	Description
0	revert_en	This signal enables revertive reference switching: 0: non-revertive (default) 1: revertive
1	freq_offset_en	Enables the Free-run frequency offset for DPLL1 (see Page 1, Address 0x65-0x68 to program offset value) 0: Free Run frequency offset disabled (default) 1: Free Run frequency offset enabled (only use in Free Run Mode)
3:2	reserved	Leave as default = '01'
5:4	hold_update	Holdover update time 00: 26 ms (default) 01: 1 s 10: 10 s 11: 60 s

Address: 0x1E Register Name: dp1l_ctrl_1 Default Value: See description Type: R/W		
Bit Field	Function Name	Description
7:6	hold_filt_bw	DPLL holdover post filtering bandwidth selection 00: bypass, no filtering 01: 18 mHz 10: 0.6 Hz 11: 10 Hz

Address: 0x1F Register Name: dp1l_modesel Default Value: See description Type: R/W		
Bit Field	Function Name	Description
2:0	modesel	DPLL mode of operation 000: Manual Normal Mode . In this mode, automatic reference switching is disabled and the selected reference is determined by the dp1l_refsel register (0x20). If the selected reference fails, the device enters holdover mode. 001: Manual Holdover Mode . In this mode, automatic reference switching is disabled and DPLL stays in the holdover mode. 010: Manual Freerun Mode . In this mode, automatic reference switching is disabled and DPLL stays in the free-run mode. 011: Automatic Normal Mode . In this mode, automatic reference switching is enabled so that DPLL automatically selects the highest priority qualified reference. If that reference fails, an automatic reference switchover to the next highest priority qualified reference is initiated. If there are no suitable references for selection, DPLL will enter the holdover mode. 100: Timing over Packet (ToP) Client Mode . In this mode, The DCO is controlled externally via software. The default value of this register depends on the mode pin.
7:3	reserved	Leave as default ([7:2] = 00000)

Address: **0x20**
 Register Name: **dpll_refsel**
 Default Value: 0x00
 Type: R in Automatic Normal Mode, R/W in Manual Normal Mode

Bit Field	Function Name	Description
3:0	refsel	In Automatic Normal Mode (see register 0x1F), this register indicates the currently selected reference. In Manual Normal Mode (see register 0x1F), this register is used to manually select the active reference. 0000: ref 0 0001: ref 1 0010: ref 2 0011 to 1111: reserved
7:4	reserved	Leave as default

Address: **0x21**
 Register Name: **dpll_ref_fail_mask**
 Default Values: 0x3C
 Type: R/W

Bit Field	Function Name	Description
3:0	ref_sw_mask	Mask for failure indicators (SCM, CFM, PFM and GST) used for automatic reference switching bit 0: SCM bit 1: CFM bit 2: GST bit 3: PFM 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled)
7:4	ref_hold_mask	Mask for failure indicators (SCM, CFM, GST and PFM) used for automatic holdover. bit 4: SCM bit 5: CFM bit 6: GST bit 7: PFM 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled)

Address: **0x22**Register Name: **dpll_wait_to_restore**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
3:0	wait_to_restore	Defines how long a previous failed reference must be fault free before it is considered as available for synchronization: 0000: 0 min 0001: 1 min 0010: 2 min 0011: 3 min 0100: 4 min 0101: 5 min 0110: 6 min 0111: 7 min 1000: 8 min 1001: 9 min 1010: 10 min 1011: 11 min 1100: 12 min 1101: 13 min 1110: 14 min 1111: 15 min
7:4	Reserved	Leave as default

Address: **0x23**Register Name: **dpll_ref_rev_ctrl**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
2:0	ref_rev_ctrl	Revertive enable bits for ref0 to ref2. Bit 0 is used for ref0, bit 1 is used for ref1, etc 0: non-revertive 1: revertive
7:3	Reserved	Leave as default

Address: **0x24**
 Register Name: **dp11_ref_pri_ctrl_0**
 Default Value: 0x10
 Type: R/W

Bit Field	Function Name	Description
3:0	ref0_priority	This selects the ref0 priority when in Automatic Normal Mode. 0000: ref0 has the highest priority 0001: ref0 has the 2nd highest priority 0010: ref0 has the 3rd highest priority 0011 - 1110: do not use 1111: ref0 is disabled
7:4	ref1_priority	This selects the ref1 priority when in Automatic Normal Mode. 0000: ref1 has the highest priority 0001: ref1 has the 2nd highest priority 0010: ref1 has the 3rd highest priority 0011 - 1110: do not use 1111: ref1 is disabled

Address: **0x25**
 Register Name: **dp11_ref_pri_ctrl_1**
 Default Value: 0x32
 Type: R/W

Bit Field	Function Name	Description
3:0	ref2_priority	This selects the ref2 priority when in Automatic Normal Mode. 0000: ref2 has the highest priority 0001: ref2 has the 2nd highest priority 0010: ref2 has the 3rd highest priority 0011 - 1110 do not use 1111: ref2 is disabled
7:4	Reserved	Leave as default

Address: **0x28**Register Name: **dp11_hold_lock_fail**Default Value: **See description**

Type: R

Bit Field	Function Name	Description
0	holdover	This bit goes high whenever the PLL goes into holdover mode
1	lock	This bit goes high when the PLL is locked to the input reference
2	cur_ref_fail	This bit goes high when the currently selected reference (see refsels register) has a failure.
7:3	Reserved	Leave as default

Address: **0x29**Register Name: **dp11_pull_in_range**Default Value: **0x03**Type: **R/W**

Bit Field	Function Name	Description
1:0	pull_in_range	DPLL pull-in range 00: ± 12 ppm 01: ± 52 ppm 10: ± 130 ppm 11: ± 83 ppm (default)
7:2	Reserved	Leave as default

Address: **0x36**Register Name: **p_enable**Default Value: **0x8F**

Type: R/W

Bit Field	Function Name	Description
0	p_clk_en	1: enable p_clk 0: p_clk is set to HiZ
1	Reserved	Leave as default

Address: **0x36**Register Name: **p_enable**

Default Value: 0x8F

Type: R/W

Bit Field	Function Name	Description
2	p_fp_en	1: enable p_fp 0: p_fp is set to HiZ
6:3	Reserved	Leave as default
7	p_en	1: enable the programmable synthesizer 0: disable the programmable synthesizer

Address: **0x37**Register Name: **p_run**

Default Value: 0x0F

Type: R/W

Bit Field	Function Name	Description
0	p_clk_run	1: generate p_clk 0: p_clk is set low
1	Reserved	Leave as default
2	p_fp_run	1: generate p_fp 0: p_fp is set low
7:3	Reserved	Leave as default

Address: **0x38**Register Name: **p_clk_freq_0**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	p_clk_freq7_0	Sets the frequency of the p_clk output programmed as N*8kHz. N is defined as a 14-bit value. This register defines bits 7:0.

Address: **0x39**Register Name: **p_clk_freq_1**

Default Value: 0x01

Type: R/W

Bit Field	Function Name	Description
5:0	p_clk_freq13_8	Sets the frequency of the p_clk output programmed as N*8kHz. N is defined as a 14-bit value. This register defines bits 13:8.
7:6	Reserved	Leave as default

Address: **0x3A**Register Name: **p_clk_offset90**Default Value: **0x00**Type: **R/W**

Bit Field	Function Name	Description
1:0	p_clk_offset90	p_clk phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees
7:2	Reserved	Not used

Address: **0x3D**Register Name: **p_offset_fine**Default Value: **0x00**Type: **R/W**

Bit Field	Function Name	Description
7:0	p_offset_fine	Phase alignment fine tuning for the programmable synthesizer. Defined as an 8-bit two's complement value in 119.2 ps steps.

Address: **0x3E**
 Register Name: **p_fp_freq**
 Default Value: 0x05
 Type: R/W

Bit Field	Function Name	Description
3:0	p_fp_freq	These signals select p_fp frame pulse frequency 0000: 166.67 Hz 0001: 400 Hz 0010: 1 kHz 0011: 2 kHz 0100: 4 kHz 0101: 8 kHz 0110: 32 kHz 0111: 64 kHz 1000: 1Hz
7:4	Reserved	Leave as default

Address: **0x3F**
 Register Name: **p_fp_type**
 Default Value: 0x83
 Type: R/W

Bit Field	Function Name	Description
0	p_fp_style	0: Clock style (50% duty cycle, for 1 Hz, pulse width is equal to 4 msec) 1: frame pulse synchronizes to any of the available E1 family of output frequencies
1	p_fp_sync_edge	0: pulsed on rising edge of synchronization clock 1: pulsed on falling edge of synchronization clock (Not applicable for 1 Hz)
3:2	Reserved	Leave as default
6:4	p_fp_type	Determines the pulse width of p_fp 000 -> pulse = one period of a 4.096 MHz clock 001 -> pulse = one period of a 8.192 MHz clock 010 -> pulse = one period of a 16.384 MHz clock 011 -> pulse = one period of a 32.768 MHz clock 100 -> pulse = one period of a 65.536 MHz clock 101 -> reserved 110 -> reserved 111 -> frame pulse width is one cycle of p_clk Note: the settings from 000 to 100 are pre-defined pulse widths when the p_clk frequency is a multiple of the E1 rate (2.048 MHz). When p_clk is not a multiple of E1, the 111 setting must be selected.

Address: **0x3F**
 Register Name: **p_fp_type**
 Default Value: 0x83
 Type: R/W

7	p_fp_polarity	0: positive polarity 1: negative polarity
---	---------------	--

Address: **0x40**
 Register Name: **p_fp_offset_0**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
7:0	p_fp_fine_offset7_0	Bits [7:0] of the programmable frame pulse phase offset. When the p_clk clock is an E1 multiple, the offset is defined in multiples of a 262.144 MHz period. This register is part of a 22-bit multi-byte register.

Address: **0x41**
 Register Name: **p_fp_offset_1**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
7:0	p_fp_fine_offset15_8	Bits [15:8] of the programmable frame pulse phase offset. When the p_clk clock is an E1 multiple, the offset is defined in multiples of a 262.144 MHz period. This register is part of a 22-bit multi-byte register.

Address: **0x42**
 Register Name: **p_fp_offset_2**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
5:0	p_fp_coarse_offset21_16	Bits [21:16] of the programmable frame pulse phase offset. This bit field programs the offset in multiples of 8 kHz cycles. This register is part of a 22-bit multi-byte register.

Address: **0x42**
 Register Name: **p_fp_offset_2**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
7:6	Reserved	Leave as default

Address: **0x50**
 Register Name: **apll_enable**
 Default Value: **0x8F**
 Type: **R/W**

Bit Field	Function Name	Description
0	apll_clk_en	1: enable apll_clk 0: apll_clk is set to HiZ
6:1	Reserved	Leave as default
7	apll_en	1: enable the APLL 0: disable the APLL

Address: **0x51**
 Register Name: **apll_run**
 Default Value: **0x0F**
 Type: **R/W**

Bit Field	Function Name	Description
0	apll_clk_run	1: generate apll_clk 0: apll_clk is set low
3:1	Reserved	Leave as default
4	f_sel	Along with eth_en bit selects if the APLL generates SONET/SDH or Ethernet frequencies 0: SONET/SDH clocks 1: Ethernet clocks

Address: 0x51 Register Name: apll_run Default Value: 0x0F Type: R/W		
Bit Field	Function Name	Description
5	f_sel_diff	Selects low-speed or high-speed frequency group for diff output 0: Selects the high-speed frequency group 1: Selects the low-speed frequency group
6	eth_en	Select if the APLL generates SONET/SDH or Ethernet frequencies 0: SONET/SDH clocks 1: Ethernet clocks
7	Reserved	Leave as default

Address: 0x52 Register Name: apll_clk_freq Default Value: 0x42 Type: R/W		
Bit Field	Function Name	Description
3:0	apll_clk_freq	Sets the frequency of the apll_clk clock output. Refer to Table 9, "APLL LVCMOS Output Clock Frequencies" on page 25 for list of available frequencies
7:4	Reserved	Leave as default

Address: 0x53 Register Name: apll_clk_offset90 Default Value: 0x00 Type: R/W		
Bit Field	Function Name	Description
1:0	apll_clk_offset90	apll_clk phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees
7:2	Reserved	Leave as default

Address: **0x55**Register Name: **apll_offset_fine**Default Value: **0x00**Type: **R/W**

Bit Field	Function Name	Description
7:0	apll_offset_fine	Phase alignment fine tuning for the APLL clock path. The delay is defined as an 8-bit two's complement value in 119.2 ps steps.

Address: **0x60**Register Name: **diff_clk_ctrl**Default Value: **0xA3**Type: **R/W**

Bit Field	Function Name	Description
0	Reserved	Leave as default
1	diff_en	1: enable diff 0: diff is set to HiZ
5:2	Reserved	Leave as default
7:6	diff_clk_adjust	Adjusts alignment of differential output to the CMOS outputs in steps of 1.6 ns. A lower value advances the differential output, a higher value delays it. The default value aligns for conditions as specified in the data sheet

Address: **0x61**Register Name: **diff_clk_sel**Default Value: **0x55**Type: **R/W**

Bit Field	Function Name	Description
3:0	Reserved	Leave as default
6:4	diff_sel	Selects the output frequency for diff. Refer to Table 10, "APLL Differential Output Clock Frequencies" on page 26 for specific frequency settings.

Address: **0x61**
 Register Name: **diff_clk_sel**
 Default Value: 0x55
 Type: R/W

Bit Field	Function Name	Description
7	Reserved	Leave as default

Address: **0x63**
 Register Name: **dpll_offset_fine**
 Default Value: **0xFF**
 Type: **R/W**

Bit Field	Function Name	Description
7:0	dpll_offset_fine	Phase alignment fine tuning for both the APLL and Programmable Synthesizers in steps of 119.2 ps. Programmed as an 8-bit two's complement value.

Address: **0x64**
 Register Name: **Page_Pointer**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
7:0	page_pointer	Use to access extended page addresses 00 - General registers 01 - DCO registers 08 - 1Hz sync enable 0A -Time of Day and ToP client mode registers 0F -ISR registers All other pages are reserved.

Address: **0x65**Register Name: **ref_freq_mode_0**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
1:0	ref0_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
3:2	ref1_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
5:4	ref2_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
7:6	Reserved	Leave as default

Address: **0x67**Register Name: **custA_mult_0**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custA_mult7_0	Bits 7:0 of a 14-bit value that defines the input reference Custom A frequency. This defined as a multiple of 8 kHz. See section 2.9, "Reference and Sync Inputs" for detail on this register settings.

Address: **0x68**Register Name: **custA_mult_1**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
5:0	custA_mult13_8	Bits 13:8 of a 14-bit value that defines the input reference Custom A frequency. This defined as a multiple of 8 kHz. See section 2.9, "Reference and Sync Inputs" for detail on this register settings.

Address: **0x68**
 Register Name: **custA_mult_1**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:6	Reserved	Leave as default

Address: **0x69**
 Register Name: **custA_scm_low**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custA_scm_low_lim	Defines the SCM low limit for the Custom A frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x6A**
 Register Name: **custA_scm_high**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custA_scm_high_lim	Defines the SCM high limit for the Custom A frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x6B**
 Register Name: **custA_cfm_low_0**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_low7_0	Bits 7:0 of a 16-bit value that defines the CFM low limit for the Custom A frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x6C**Register Name: **custA_cfm_low_1**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_low15_8	Bits 15:8 of a 16-bit value that defines the CFM low limit for the Custom A frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x6D**Register Name: **custA_cfm_hi_0**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_hi7_0	Bits 7:0 of a 16-bit value that defines the CFM high limit for the Custom A frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x6E**Register Name: **custA_cfm_hi_1**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_hi15_8	Bits 15:8 of a 16-bit value that defines the CFM high limit for the Custom A frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x6F**
 Register Name: **custA_cfm_cycle**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_cycle	Defines the number of cycles that are monitored in the given sample window for custom configuration A. Set as CFM reference monitoring cycles - 1. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x70**
 Register Name: **custA_div**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
0	custA_div	When enabled (set to 1) the CFM divides the reference input frequency by 4 to increase the measurement window. This is recommended when the reference frequency is greater than 19.44 MHz. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.
7:1	Reserved	Leave as default

Address: **0x71**
 Register Name: **custB_mult_0**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custB_mult7_0	Bits 7:0 of a 14-bit value that defines the input reference Custom B frequency. This defined as a multiple of 8 kHz. See section 2.9, "Reference and Sync Inputs" for detail on this register settings.

Address: **0x72**Register Name: **custB_mult_1**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
5:0	custB_mult13_8	Bits 13:8 of a 14-bit value that defines the input reference Custom B frequency. This defined as a multiple of 8 kHz. See section 2.9, "Reference and Sync Inputs" for detail on this register settings.
7:6	Reserved	Leave as default

Address: **0x73**Register Name: **custB_scm_low**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custB_scm_low_lim	Defines the SCM low limit for the Custom B frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x74**Register Name: **custB_scm_high**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custB_scm_high_lim	Defines the SCM high limit for the Custom B frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x75**
 Register Name: **custB_cfm_low_0**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_low7_0	Bits 7:0 of a 16-bit value that defines the CFM low limit for the Custom B frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x76**
 Register Name: **custB_cfm_low_1**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_low15_8	Bits 15:8 of a 16-bit value that defines the CFM low limit for the Custom B frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x77**
 Register Name: **custB_cfm_hi_0**
 Default Value: 0x00
 Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_hi7_0	Bits 7:0 of a 16-bit value that defines the CFM high limit for the Custom B frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x78**Register Name: **custB_cfm_hi_1**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_hi15_8	Bits 15:8 of a 16-bit value that defines the CFM high limit for the Custom B frequency. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x79**Register Name: **custB_cfm_cycle**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_cycle	Defines the number of cycles that are monitored in the given sample window for custom configuration B. Set as CFM reference monitoring cycles - 1. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.

Address: **0x7A**Register Name: **custB_div**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
0	custB_div	When enabled (set to 1) the CFM divides the reference input frequency by 4 to increase the measurement window. This is recommended when the reference frequency is greater than 19.44 MHz. See section 2.13, "Reference Monitoring for Custom Configurations" for more details.
7:1	Reserved	Leave as default

Address: **0x7E**Register Name: **predivider_ctrl**

Default Value: 0x00

Type: R/W

Bit Field	Function Name	Description
3:0	ref0_div	<p>Reference 0 frequency divide ratio</p> <p>0000: Divide by 1 0001: Divide by 2 0010: Divide by 3 0011: Divide by 4 0100: Divide by 5 0101: Divide by 6 0110: Divide by 7 0111: Divide by 8 1010: Divide by 1.5. 1100: Divide by 2.5. 1101 - 1111: reserved</p> <p>Note: Output jitter generation may be higher when using divide by 1.5 and 2.5 ratios</p>
7:4	ref1_div	<p>Reference 1 frequency divide ratio</p> <p>0000: Divide by 1 0001: Divide by 2 0010: Divide by 3 0011: Divide by 4 0100: Divide by 5 0101: Divide by 6 0110: Divide by 7 0111: Divide by 8 1010: Divide by 1.5. 1100: Divide by 2.5. 1101 - 1111: reserved</p> <p>Note: Output jitter generation may be higher when using divide by 1.5 and 2.5 ratios</p>

Address: **01_0x65**
 Register Name: **DCO_freq_offset_0**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
7:0	DCO_freq_offset_0	Bits[7:0] of the 28 bit DCO frequency offset value. Programmable in steps of $(2^{-40} * 80\text{MHz}/65.536\text{MHz} * 10^9)\text{ppb}$.

Address: **01_0x66**
 Register Name: **DCO_freq_offset_1**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
7:0	DCO_freq_offset_1	Bits[15:8] of the 28 bit DCO frequency offset value. Programmable in steps of $(2^{-40} * 80\text{MHz}/65.536\text{MHz} * 10^9)\text{ppb}$.

Address: **01_0x67**
 Register Name: **DCO_freq_offset_2**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
7:0	DCO_freq_offset_2	Bits[23:16] of the 28 bit DCO frequency offset value. Programmable in steps of $(2^{-40} * 80\text{MHz}/65.536\text{MHz} * 10^9)\text{ppb}$.

Address: **01_0x68**
 Register Name: **DCO_freq_offset_3**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
3:0	DCO_freq_offset_3	Bits[27:24] of the 28 bit DCO frequency offset value. Programmable in steps of $(2^{-40} * 80\text{MHz}/65.536\text{MHz} * 10^9)\text{ppb}$.
7:4	Reserved	Leave as default

Address: **01_0x69**
 Register Name: **DCO_Phase_0**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_0	Bits[7:0] of the 64 bit DCO Phase Word.

Address: **01_0x6A**
 Register Name: **DCO_Phase_1**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_1	Bits[15:8] of the 64 bit DCO Phase Word.

Address: **01_0x6B**
 Register Name: **DCO_Phase_2**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_2	Bits[23:16] of the 64 bit DCO Phase Word.

Address: **01_0x6C**
 Register Name: **DCO_Phase_3**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_3	Bits[31:24] of the 64 bit DCO Phase Word.

Address: **01_0x6D**
 Register Name: **DCO_Phase_4**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_4	Bits[39:32] of the 64 bit DCO Phase Word.

Address: **01_0x6E**
 Register Name: **DCO_Phase_5**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_5	Bits[47:40] of the 64 bit DCO Phase Word.

Address: **01_0x6F**
 Register Name: **DCO_Phase_6**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_6	Bits[55:48] of the 64 bit DCO Phase Word.

Address: **01_0x70**
 Register Name: **DCO_Phase_7**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	DCO_Phase_7	Bits[63:56] of the 64 bit DCO Phase Word.

Address: **01_0x71**
 Register Name: **Local_Time_0**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	Local_Time_0	Bits[7:0] of the 32 bit Local System Time.

Address: **01_0x72**
 Register Name: **Local_Time_1**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	Local_Time_1	Bits[15:8] of the 32 bit Local System Time.

Address: **01_0x73**
 Register Name: **Local_Time_2**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	Local_Time_2	Bits[23:16] of the 32 bit Local System Time.

Address: **01_0x74**
 Register Name: **Local_Time_3**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
7:0	Local_Time_3	Bits[31:24] of the 32 bit Local System Time.

Page_Address: **01_0x75**
 Register Name: **ToD_update_0**
 Default Value:**0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_0	Bits[7:0] of the 64 bit ToD update register

Page_Address: **01_0x76**
 Register Name: **ToD_update_1**
 Default Value:**0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_1	Bits[15:8] of the 64 bit ToD update register

Page_Address: **01_0x77**
 Register Name: **ToD_update_2**
 Default Value:**0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_2	Bits[23:16] of the 64 bit ToD update register

Page_Address: **01_0x78**
 Register Name: **ToD_update_3**
 Default Value:**0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_3	Bits[31:24] of the 64 bit ToD update register

Page_Address: **01_0x79**
 Register Name: **ToD_update_4**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_4	Bits[39:32] of the 64 bit ToD update register

Page_Address: **01_0x7A**
 Register Name: **ToD_update_5**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_5	Bits[47:40] of the 64 bit ToD update register

Page_Address: **01_0x7B**
 Register Name: **ToD_update_6**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_6	Bits[55:48] of the 64 bit ToD update register

Page_Address: **01_0x7C**
 Register Name: **ToD_update_7**
 Default Value: **0x00**
 Type: **R**

Bit Field	Function Name	Description
4:0	ToD_update_7	Bits[63:56] of the 64 bit ToD update register

Address: **08_0x71**
 Register Name: **1Hz_enable**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
0	1Hz_enable	1: enables 1Hz sync auto-detection and qualification 0: disables 1Hz sync auto-detection and qualification
7:1	Reserved	Leave as Default

Address: **0A_0x6C**
 Register Name: **DCO_update**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
1:0	Reserved	Leave as Default.
3:2	DCO_Freq_update_en	00: Default mode, to be used in all modes except ToP Client Mode 01:Reserved 10:Reserved 11: ToP Client Mode (Enables the DCO updates and samples the DCO Phase Word and Local System Time and a ToP interrupt is generated at an interval specified in the DCO_update_interval register (0A_0x71),
7:4	Reserved	Leave as Default

Address: **0A_0x71**
 Register Name: **DCO_update_interval**
 Default Value: **0x07**
 Type: **R/W**

Bit Field	Function Name	Description
3:0	DCO_update_interval	Sets the interval between DCO frequency updates. Interval Time = $2^{(\text{DCO_update_interval} + 17)} \times 12.5\text{nsec}$
7:4	Reserved	Leave as Default

Page_Address: **0A_0x72**
 Register Name: **ToP_1Hz_Alignment**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
1:0	Reserved	Reserved for ToP Client Mode
3:2	ToD_sync_ctrl	Used to latch the ToD into the ToD_update registers
5:4	1Hz_sync_ctrl	Used to align internal 1 Hz to external 1 Hz sync pulse
7:6	Reserved	Reserved for ToP Client Mode

Page_Address: **0A_0x76**
 Register Name: **Time_of_Day_0**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_0	Bits[7:0] of the 64 bit Time of Day register

Page_Address: **0A_0x77**
 Register Name: **Time_of_Day_1**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_1	Bits[15:8] of the 64 bit Time of Day register

Page_Address: **0A_0x78**
 Register Name: **Time_of_Day_2**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_2	Bits[23:16] of the 64 bit Time of Day register

Page_Address: **0A_0x79**
 Register Name: **Time_of_Day_3**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_3	Bits[31:24] of the 64 bit Time of Day register

Page_Address: **0A_0x7A**
 Register Name: **Time_of_Day_4**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_4	Bits[39:32] of the 64 bit Time of Day register

Page_Address: **0A_0x7B**
 Register Name: **Time_of_Day_5**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_5	Bits[47:40] of the 64 bit Time of Day register

Page_Address: **0A_0x7C**
 Register Name: **Time_of_Day_6**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_6	Bits[55:48] of the 64 bit Time of Day register

Page_Address: **0A_0x7D**
 Register Name: **Time_of_Day_7**
 Default Value: **0x00**
 Type: **R/W**

Bit Field	Function Name	Description
4:0	Time_of_Day_7	Bits[63:56] of the 64 bit Time of Day register

Address: **0F_0x6E**
 Register Name: **ToP_isr**
 Default Value: **0x10**
 Type: **Sticky R**

Bit Field	Function Name	Description
0	Reserved	Reserved

Address: **0F_0x6E**
 Register Name: **ToP_isr**
 Default Value: **0x10**
 Type: **Sticky R**

Bit Field	Function Name	Description
1	ToP_isr	This bit is asserted when the DCO Phase Word and Local System Time have been sampled
7:2	Reserved	Reserved

Address: **0F_0x6F**
 Register Name: **ToP_isr_mask**
 Default Value: **0x1F**
 Type: **R/W**

Bit Field	Function Name	Description
0	Reserved	Leave as Default
1	ToP_isr_mask	A 0 in this bit masks the ToP_isr
7:2	Reserved	Leave as Default

Address: 0F_0x7D Register Name: isr0_reg Default Value: 0x48 Type: R		
Bit Field	Function Name	Description
0	ref0_2_int	1: interrupt from ref_fail_isr_0 @0x02
1	dpll1_int	1: interrupt from dpll1_isr @0x03
5:2	Reserved	
6	ToP_int	1: interrupt from ToP_isr @0F_ 0x6E
7	Reserved	Reserved

Address: 0F_0x7E Register Name: isr0_mask Default Value: 0x07 Type: R/W		
Bit Field	Function Name	Description
7:0	isr0_mask	Enabling a mask bit will allow interrupt generation. xxxxxx0: masks ref0_2_int xxxxxx0x: masks dpll1_int x0xxxxxx: masks ToP_isr

5.0 AC and DC Electrical Characteristics

DC Electrical Characteristics - Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	-0.5	4.6	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	$V_{DD} + 0.3$	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

* Voltages are with respect to ground (GND) unless otherwise stated.

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	3.1	3.3	3.5	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	1.7	1.8	1.9	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	1.8 V Core Supply Current	$I_{1.8_CORE}$		121	159	mA	osci = 20 MHz, All outputs disabled.
2	I/O Supply Current (Differential Outputs)	I_{DIFF}		37	46	mA	All differential outputs operating at max frequency and biased with a 200 Ohm resistor to ground
3	I/O Supply Current (CMOS Outputs)	I_{CMOS}		51	72	mA	All CMOS outputs operating at max frequency and loaded with 15 pF
4	Total Power Dissipation	P_{T_D}		508	715	mW	All outputs operating at max frequency and loaded with 15 pF
5	CMOS high-level input voltage	V_{IH}	$0.7 \cdot V_{DD}$			V	Applies to osci pin
6	CMOS low-level input voltage	V_{IL}			$0.3 \cdot V_{DD}$	V	
7	Input leakage current	I_{IL}	-15		15	μA	$V_I = V_{DD}$ or 0 V
8	Input leakage current low for pull-up pads	I_{IL_PU}	-121		-23	μA	$V_I = 0$ V
9	Input leakage current high for pull-down pads	I_{IL_PD}	23		121	μA	$V_I = V_{DD}$
10	Schmitt trigger Low to High threshold point	V_{t+}	1.35		1.85	V	All CMOS inputs are schmitt level triggered
11	Schmitt trigger High to Low threshold point	V_{t-}	0.80		1.15	V	
12	CMOS high-level output voltage	V_{OH}	2.4			V	$I_{OH} = 8mA$ on clk & fp output. $I_{OH} = 4mA$ other outputs
13	CMOS low-level output voltage	V_{OL}			0.4	V	$I_{OL} = 8mA$ on clk & fp output. $I_{OL} = 4mA$ other outputs
14	LVPECL: High-level output voltage	$V_{OH_LVPE_CL}$	V_{DD-} 1.08	V_{DD-} 0.96	V_{DD-} 0.88	V	
15	LVPECL: Low-level output voltage	$V_{OL_LVPE_CL}$	V_{DD-} 1.81	V_{DD-} 1.71	V_{DD-} 1.62	V	
16	LVPECL: Differential output voltage	$V_{OD_LVPE_CL}$	0.6	0.8	0.93	V	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

* Voltages are with respect to ground (GND) unless otherwise stated.

AC Electrical Characteristics* - Input Timing For Sync References (See Figure 30).

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	sync0/1/2 lead time	$t_{\text{SYNC_LD}}$		0	ns	
2	sync0/1/2 lag time	$t_{\text{SYNC_LG}}$	0	$t_{\text{REFP}} - 4$	ns	t_{REFP} = minimum period of ref0/1/2 clock
3	sync0/1/2 pulse width high or low	$t_{\text{SYNC_W}}$	5		ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

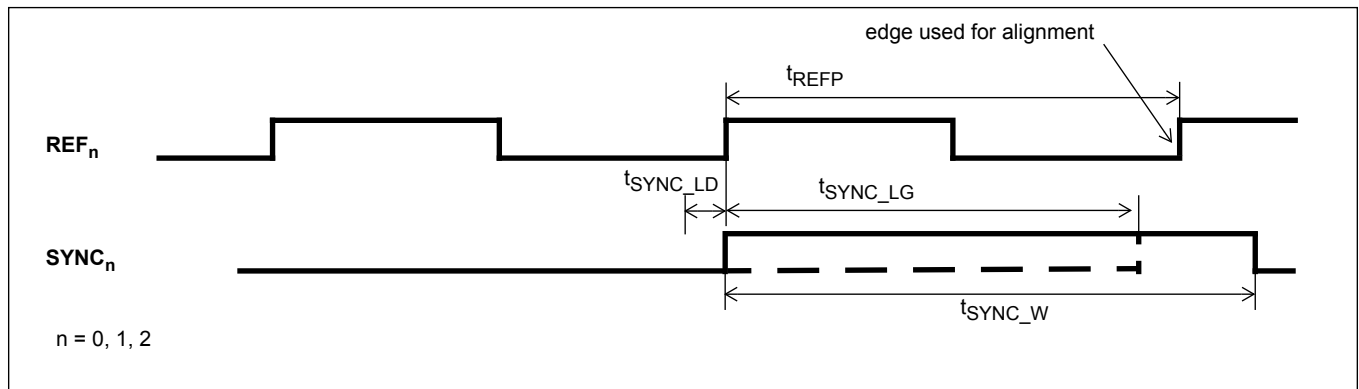


Figure 30 - Sync Input Timing

AC Electrical Characteristics* - Input To Output Timing For Ref<2:0> References (See Figure 31).

	Characteristics	Symbol	Min.	Max.	Units
1	LVC MOS Clock Output (p_clk, ap11_clk)	t_D	-1.0	+4.0	ns
2	LVPECL Differential Clock Output (diff)	t_D	-0.5	+5.5	ns

* Input to output timing is measured over the specified operating voltage and temperature ranges using the same input and output spot frequencies of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 6.48 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz, 38.88 MHz, and 77.76 MHz.

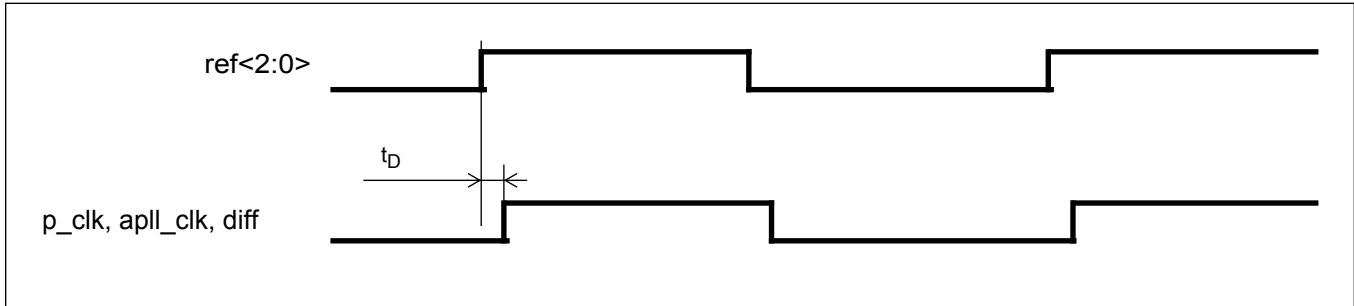


Figure 31 - Input To Output Timing

AC Electrical Characteristics - Output Clock Duty Cycle¹ (See Figure 32).

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	LVCMOS Output Duty Cycle ²	t_{SYM}	45	55	%	$2\text{ kHz} < f_{clk} \leq 125\text{ MHz}$
			40	60	%	50 MHz
2	LVPECL Output Duty Cycle ³	t_{SYM}	45	55	%	$2\text{ kHz} < f_{clk} \leq 622\text{ MHz}$
			40	60	%	50 MHz

- Duty cycle is measured over the specified operating voltage and temperature ranges at specified spot frequencies.
- Measured on spot frequencies of 1.544 MHz, 2.048 MHz, 3.088 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz, 8.448 MHz, 16.384 MHz, 25 MHz, 32.768 MHz, 34.368 MHz, 44.736 MHz, 65.536 MHz, 125 MHz.
- Measured on spot frequencies of 6.48 MHz, 19.44 MHz, 25 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz.

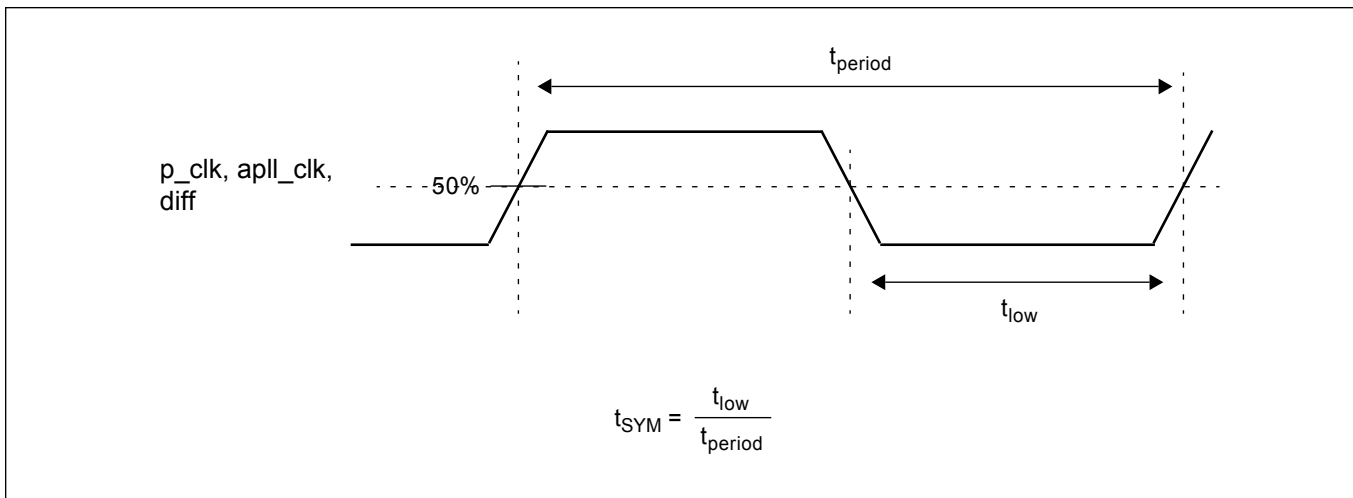


Figure 32 - Output Duty Cycle

AC Electrical Characteristics* - Output Clock and Frame Pulse Fall and Rise Times¹ (See Figure 33).

	Characteristics	Symbol	Min.	Max.	Units	C _{LOAD}
1	Output Rise Time	t_{rise}	2.3	4.5	ns	30 pF
2	Output Rise Time	t_{rise}	2.0	3.9	ns	25 pF
3	Output Rise Time	t_{rise}	1.6	3.2	ns	20 pF
4	Output Rise Time	t_{rise}	1.3	2.6	ns	15 pF
5	Output Rise Time	t_{rise}	1.0	1.9	ns	10 pF
6	Output Rise Time	t_{rise}	0.6	1.3	ns	5 pF
7	Output Fall Time	t_{fall}	2.1	5.2	ns	30 pF
8	Output Fall Time	t_{fall}	1.8	4.5	ns	25 pF
9	Output Fall Time	t_{fall}	1.5	3.7	ns	20 pF
10	Output Fall Time	t_{fall}	1.2	3.0	ns	15 pF
11	Output Fall Time	t_{fall}	0.9	2.3	ns	10 pF
12	Output Fall Time	t_{fall}	0.6	1.5	ns	5 pF

1. Output fall and rise times are specified over the operating voltage and temperature ranges at 10 MHz.

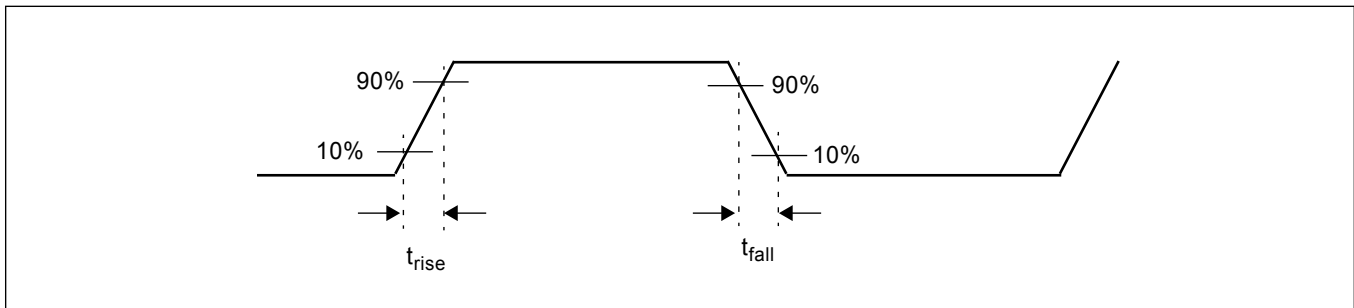


Figure 33 - Output Clock Fall and Rise Times

AC Electrical Characteristics* - E1 Output Frame Pulse Timing (See Figure 34).

	Pulse Width Setting	f _{pulse_width}		t _{delay}		t _{delay_inv}		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
1	One period of a 4.096 MHz clock	242	246	-2	2	120	124	ns
2	One period of a 8.192 MHz clock	120	124	-2	2	59	63	ns
3	One period of a 16.384 MHz clock	59	62	-2	2	29	33	ns
4	One period of a 32.768 MHz clock	29	32	-2	2	13	17	ns
5	One period of a 65.536 MHz clock	13.3	17.3	-2	2	5.6	9.6	ns

* All measurements taken over the specified operating voltage and temperature range.

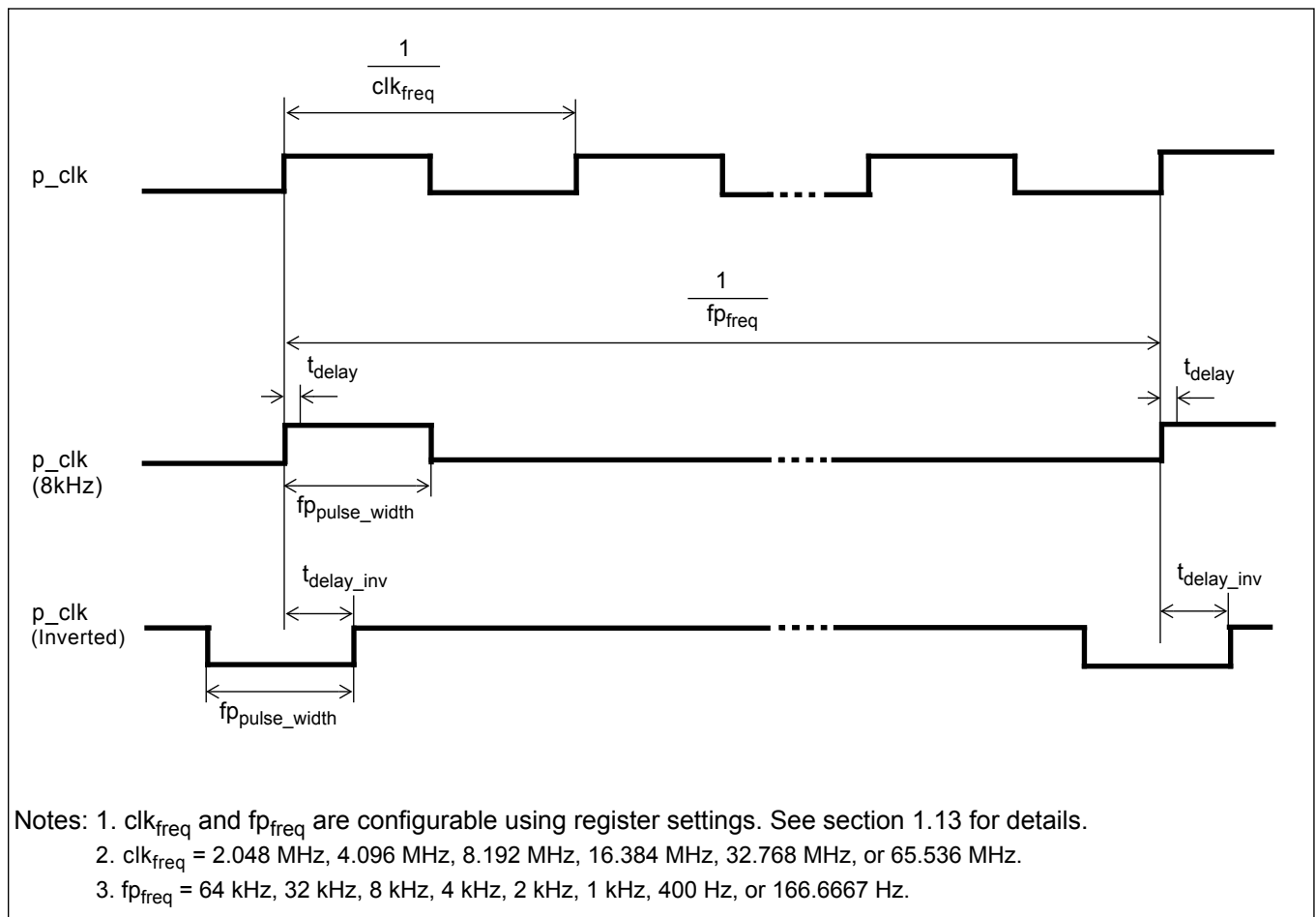


Figure 34 - E1 Output Frame Pulse Timing

AC Electrical Characteristics - Serial Peripheral Interface Timing

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclk _l	62		ns
sck pulse width high	tclk _h	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 15 - Serial Peripheral Interface Timing

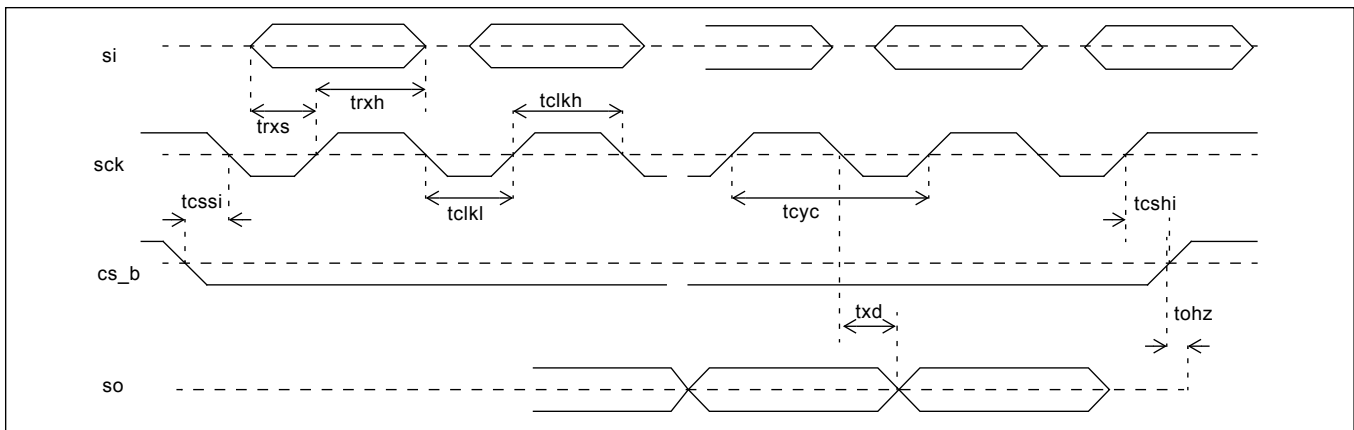


Figure 35 - Serial Peripheral Interface Timing - LSB First Mode

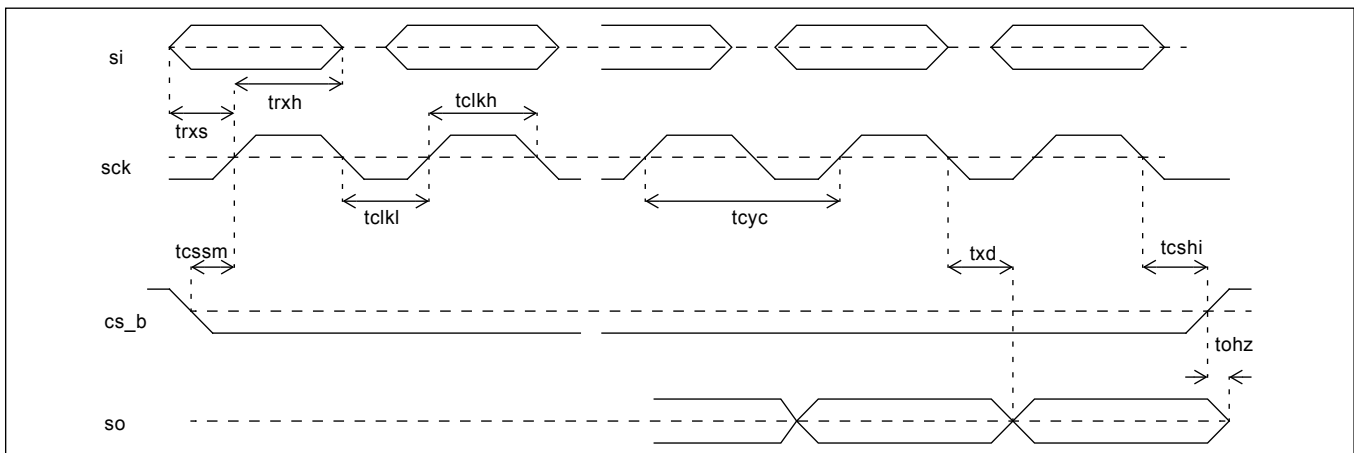


Figure 36 - Serial Peripheral Interface Timing - MSB First Mode

AC Electrical Characteristics - I²C Timing

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f _{SCL}	0		400	kHz	
Hold time START condition	t _{HD:STA}	0.6			us	
Low period SCL	t _{LOW}	1.3			us	
Hi period SCL	t _{HIGH}	0.6			us	
Setup time START condition	t _{SU:STA}	0.6			us	
Data hold time	t _{HD:DAT}	0		0.9	us	
Data setup time	t _{SU:DAT}	100			ns	
Rise time	t _r				ns	Determined by pull-up resistor
Fall time	t _f	20 + 0.1C _b		250	ns	
Setup time STOP condition	t _{SU:STO}	0.6			us	
Bus free time between STOP/START	t _{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t _{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 16 - I²C Serial Microport Timing

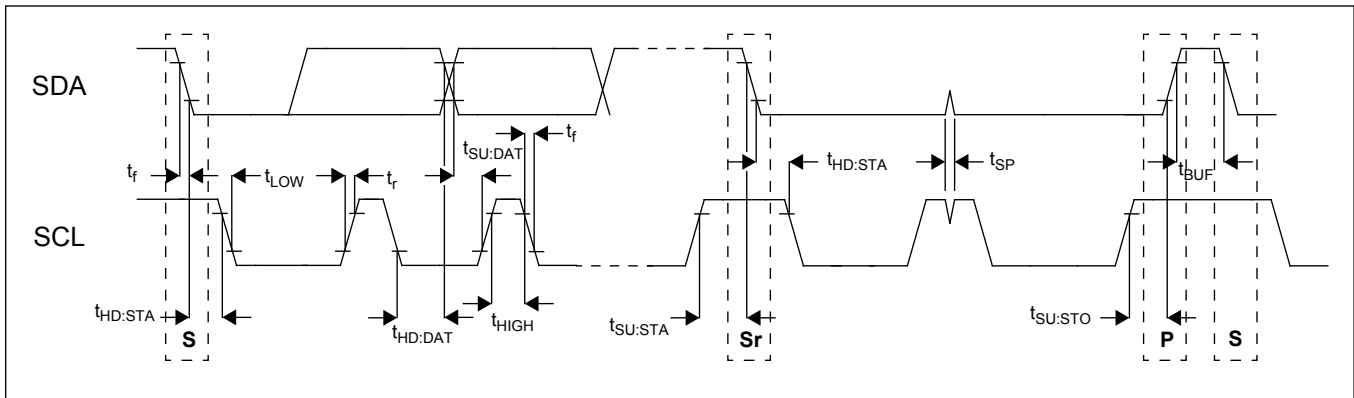


Figure 37 - I²C Serial Microport Timing

Performance Characteristics - Output Jitter Generation On Differential LVPECL Output (diff). All other outputs disabled.

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement		Jitter Generation			
					Typ ¹	Max ²	Units	
OC-3	19.44 MHz	12 kHz to 1.3 MHz	0.01 UI _{RMS}	64.30	1.3	1.7	ps _{RMS}	
			0.1 UI _{P-P}	643.00	14.6	17.5	ps _{P-P}	
	77.76 MHz	12 kHz to 1.3 MHz	0.01 UI _{RMS}	64.30	0.7	0.9	ps _{RMS}	
			0.1 UI _{P-P}	643.00	8.7	10.7	ps _{P-P}	
	155.52 MHz	12 kHz to 1.3 MHz	0.01 UI _{RMS}	64.30	0.7	0.9	ps _{RMS}	
			0.1 UI _{P-P}	643.00	8.8	10.9	ps _{P-P}	
OC-12	77.76 MHz	12 kHz to 5 MHz	0.01 UI _{RMS}	16.08	0.7	1.1	ps _{RMS}	
			0.1 UI _{P-P}	160.80	9.0	11.0	ps _{P-P}	
	155.52 MHz	12 kHz to 5 MHz	0.01 UI _{RMS}	16.08	0.7	0.9	ps _{RMS}	
			0.1 UI _{P-P}	160.80	9.0	11.1	ps _{P-P}	
	622.08 MHz	12 kHz to 5 MHz	0.01 UI _{RMS}	4.020	0.7	0.9	ps _{RMS}	
			0.1 UI _{P-P}	40.20	8.5	10.6	ps _{P-P}	
	OC-48	155.52 MHz	12 kHz to 20 MHz	0.01 UI _{RMS}	4.020	0.8	1.0	ps _{RMS}
				0.1 UI _{P-P}	40.20	9.5	11.6	ps _{P-P}
622.08 MHz		12 kHz to 20 MHz	0.01 UI _{RMS}	4.020	0.7	0.9	ps _{RMS}	
			0.1 UI _{P-P}	40.20	8.6	10.7	ps _{P-P}	

Interface	Output Frequency	Jitter Measurement Filter	Jitter Generation		
			Typ ¹	Max ²	Units
Ethernet Clock Rates	25 MHz	12 kHz to 10 MHz	1.3	1.8	ps _{RMS}
			12.6	16.4	ps _{P-P}
	125 MHz	12 kHz to 20 MHz	0.8	1.0	ps _{RMS}
			9.4	11.7	ps _{P-P}
	156.25 MHz	12 kHz to 20 MHz	0.8	1.0	ps _{RMS}
			9.5	11.6	ps _{P-P}

¹ Typical jitter specifications are measured when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

² Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with the differential outputs enabled and all other outputs disabled.

Performance Characteristics - Output Jitter Generation On Differential LVPECL Outputs (diff). All other outputs enabled.

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement		Jitter Generation		
					Typ ¹	Max ²	Units
OC-3	19.44 MHz	12 kHz to 1.3 MHz	0.01 UI _{RMS}	64.30	1.6	2.3	ps _{RMS}
			0.1 UI _{P-P}	643.00	15.4	19.7	ps _{P-P}
	77.76 MHz	12 kHz to 1.3 MHz	0.01 UI _{RMS}	64.30	0.8	1.3	ps _{RMS}
			0.1 UI _{P-P}	643.00	9.2	12.4	ps _{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.01 UI _{RMS}	64.30	0.8	1.3	ps _{RMS}
			0.1 UI _{P-P}	643.00	9.3	12.7	ps _{P-P}
OC-12	77.76 MHz	12 kHz to 5 MHz	0.01 UI _{RMS}	16.08	0.9	1.5	ps _{RMS}
			0.1 UI _{P-P}	160.80	9.6	13.3	ps _{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.01 UI _{RMS}	16.08	0.9	1.4	ps _{RMS}
			0.1 UI _{P-P}	160.80	9.6	13.3	ps _{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.01 UI _{rms}	4.020	0.8	1.4	ps _{RMS}
			0.1 UI _{P-P}	40.20	9.1	12.9	ps _{P-P}
OC-48	155.52 MHz	12 kHz to 20 MHz	0.01 UI _{rms}	4.020	1.0	1.5	ps _{RMS}
			0.1 UI _{P-P}	40.20	10.1	13.7	ps _{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.01 UI _{rms}	4.020	0.8	1.4	ps _{RMS}
			0.1 UI _{P-P}	40.20	9.2	13.0	ps _{P-P}

Interface	Output Frequency	Jitter Measurement Filter	Jitter Generation		
			Typ ¹	Max ²	Units
Ethernet Clock Rates	25 MHz	12 kHz to 20 MHz	1.4	1.9	ps _{RMS}
			13.0	16.7	ps _{P-P}
	125 MHz	12 kHz to 20 MHz	0.8	1.0	ps _{RMS}
			9.5	11.7	ps _{P-P}
	156.25 MHz	12 kHz to 20 MHz	0.9	1.1	ps _{RMS}
			9.7	11.8	ps _{P-P}

¹ Typical jitter specifications are measured under the power-up default configuration when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

² Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with all other outputs enabled while generating any of the frequencies available from the SONET/SDH/Ethernet synthesizer and any of the programmable frequencies on the programmable outputs up to 65.536 MHz.

Performance Characteristics - Output Jitter Generation On Differential LVPECL Outputs (diff). All other outputs enabled.

Interface	Output Frequency	Jitter Measurement Filter	G.813 Jitter Requirement		Jitter Generation		
					Typ ¹	Max ²	Units
Option 1							
STM-1	19.44 MHz	65 kHz to 1.3 MHz	0.1 UI _{P-P}	643	13.9	17.8	ps _{P-P}
		500 Hz to 1.3 MHz	0.5 UI _{P-P}	3215	16.3	20.6	ps _{P-P}
	77.76 MHz	65 kHz to 1.3 MHz	0.1 UI _{P-P}	643	6.8	9.7	ps _{P-P}
		500 Hz to 1.3 MHz	0.5 UI _{P-P}	3215	10.3	13.6	ps _{P-P}
	155.52 MHz	65 kHz to 1.3 MHz	0.1 UI _{P-P}	643	6.8	9.8	ps _{P-P}
		500 Hz to 1.3 MHz	0.5 UI _{P-P}	3215	10.5	13.9	ps _{P-P}
STM-4	77.76 MHz	250 kHz to 5 MHz	0.1 UI _{P-P}	161	4.8	8.4	ps _{P-P}
		1 kHz to 5 MHz	0.5 UI _{P-P}	804	10.5	14.2	ps _{P-P}
	155.52 MHz	250 kHz to 5 MHz	0.1 UI _{P-P}	161	4.4	5.6	ps _{P-P}
		1 kHz to 5 MHz	0.5 UI _{P-P}	804	10.5	14.3	ps _{P-P}
	622.08 MHz	250 kHz to 5 MHz	0.1 UI _{P-P}	161	3.9	5.0	ps _{P-P}
		1 kHz to 5 MHz	0.5 UI _{P-P}	804	10.0	13.9	ps _{P-P}
STM-16	155.52 MHz	1 MHz to 20 MHz	0.1 UI _{P-P}	40.2	4.0	5.4	ps _{P-P}
		5 kHz to 20 MHz	0.5 UI _{P-P}	201	10.6	14.3	ps _{P-P}
	622.08 MHz	1 MHz to 20 MHz	0.1 UI _{P-P}	40.2	2.4	4.4	ps _{P-P}
		5 kHz to 20 MHz	0.5 UI _{P-P}	201	9.7	13.6	ps _{P-P}
Option 2							
STM-1	77.76 MHz	12 kHz to 1.3 MHz	0.1 UI _{P-P}	643	9.1	12.4	ps _{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.1 UI _{P-P}	643	9.3	12.7	ps _{P-P}
STM-4	77.76 MHz	12 kHz to 5 MHz	0.1 UI _{P-P}	161	9.6	13.3	ps _{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.1 UI _{P-P}	161	9.6	13.3	ps _{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.1 UI _{P-P}	161	9.1	12.9	ps _{P-P}
STM-16	155.52 MHz	12 kHz to 20 MHz	0.1 UI _{P-P}	40.2	10.1	13.7	ps _{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.1 UI _{P-P}	40.2	9.2	13.0	ps _{P-P}

¹ Typical jitter specifications are measured under the power-up default configuration when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

² Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with all outputs enabled while generating any of the frequencies available from the SONET/SDH/Ethernet synthesizer and any of the programmable frequencies on the programmable outputs up to 65.536 MHz.

Performance Characteristics - Measured Output Jitter On APLL CMOS Output (apll_clk). All other outputs enabled.

Output Frequency	Jitter Measurement Filter	Jitter Generation		
		Typ ¹	Max ²	Units
SONET/SDH 6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz	12 kHz to 5 MHz	2.3	3.1	ps _{RMS}
		22.8	28.7	ps _{P-P}
	unfiltered	3.2	4.3	ps _{RMS}
		33.1	42.0	ps _{P-P}
Ethernet 25 MHz	637 kHz to Nyquist	1.7	2.9	ps _{RMS}
		11.8	19.6	ps _{P-P}
	12 kHz to 10 MHz	1.8	2.9	ps _{RMS}
		15.2	22.8	ps _{P-P}
Ethernet 125 MHz	637 kHz to Nyquist	0.6	1.0	ps _{RMS}
		5.0	8.9	ps _{P-P}
	12 kHz to 20 MHz	0.9	1.4	ps _{RMS}
		10.4	14.2	ps _{P-P}

¹ Typical jitter specifications are measured when operating at nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

² Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with all outputs enabled.

Performance Characteristics - Measured Output Jitter On Programmable CMOS Output (p_clk).

Output Frequency	Jitter Measurement Filter	Jitter Generation		
		Typ ¹	Max ²	Units
8 kHz to 100 MHz	unfiltered	18.0	24.0	ps _{RMS}

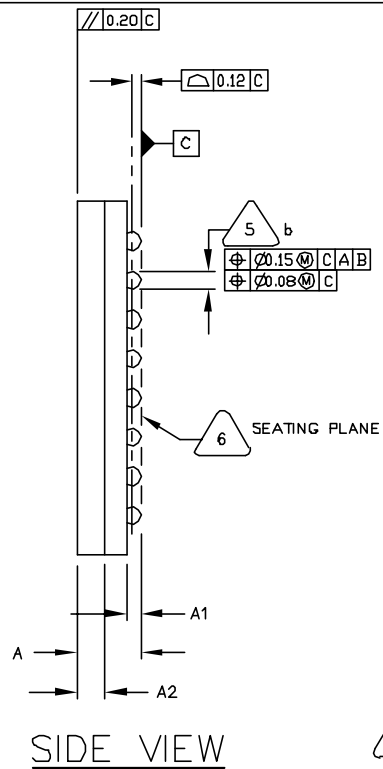
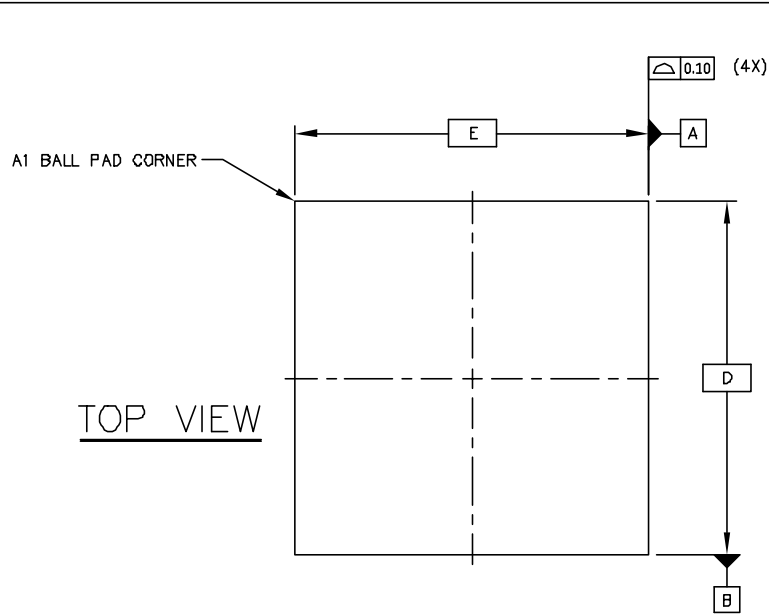
¹ Typical jitter specifications are measured when operating at nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

² Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with all outputs enabled.

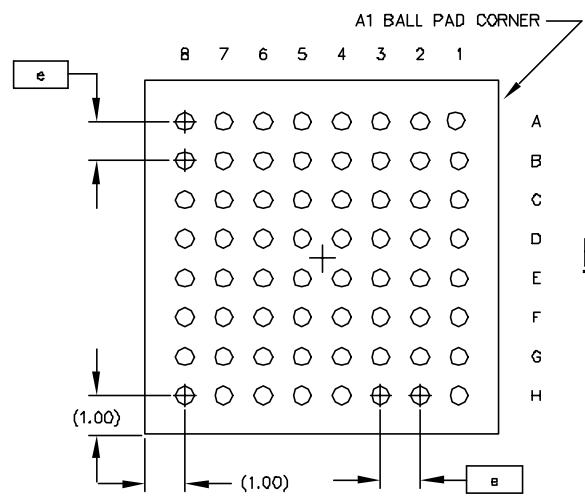
6.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{ja}	Still Air	31.6	°C/W
Junction to Case Thermal Resistance	θ_{jc}	Still Air	10.3	°C/W

Table 17 - Thermal Data



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46 Typ.		
D	9.00 REF.		
E	9.00 Ref.		
e	1.0 Ref		
n	64		



BOTTOM VIEW
64 SOLDER BALLS



6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.



5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

© Copyright 2013, Microsemi Corporation. All Rights Reserved.				
ISSUE	1			
ACN	CDCA			
DATE	15April05			
APPRD.				



	Package Code	GG
Previous package codes	Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA	
	N/A	
	111039	

Information relating to products and services furnished herein by Microsemi Corporation or its subsidiaries (collectively "Microsemi") is believed to be reliable. However, Microsemi assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Microsemi or licensed from third parties by Microsemi, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Microsemi, or non-Microsemi furnished goods or services may infringe patents or other intellectual property rights owned by Microsemi.

This publication is issued to provide information only and (unless agreed by Microsemi in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Microsemi without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical and other products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Microsemi's conditions of sale which are available on request.

**For more information about all Microsemi products
visit our website at
www.microsemi.com**

TECHNICAL DOCUMENTATION – NOT FOR RESALE



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at www.microsemi.com.

© 2013 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.