ZL30168

Enhanced Quad Clock Translator

Data Sheet

March 2015

Features

- Four independent clock channels
- Programmable synthesizers generate any clock-rate from 1 Hz to 750 MHz
- Four precision synthesizers generate clocks with maximum jitter below 0.63 ps RMS
- Four programmable digital PLLs/Numerically Controlled Oscillators (NCOs)/OTN clock generators based on buffer-fill levels
  - Programmable digital PLLs synchronize to any clock rate from 1 kHz to 750 MHz
  - Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
  - Digital PLLs filter jitter with bandwidths from 5 to 896 Hz
  - Automatic hitless reference switching and digital holdover on reference fail
- Eight reference inputs configurable as single ended or differential

Ordering Information

ZL30168GDG2 144 Pin LBGA Trays
Pb Free Tin/Silver/Copper
-40°C to +85°C
Package size: 13 x 13 mm

- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Configurable via four selectable default configurations or field programmable via SPI/I2C interface

Applications

- OTN muxponders and transponders
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI

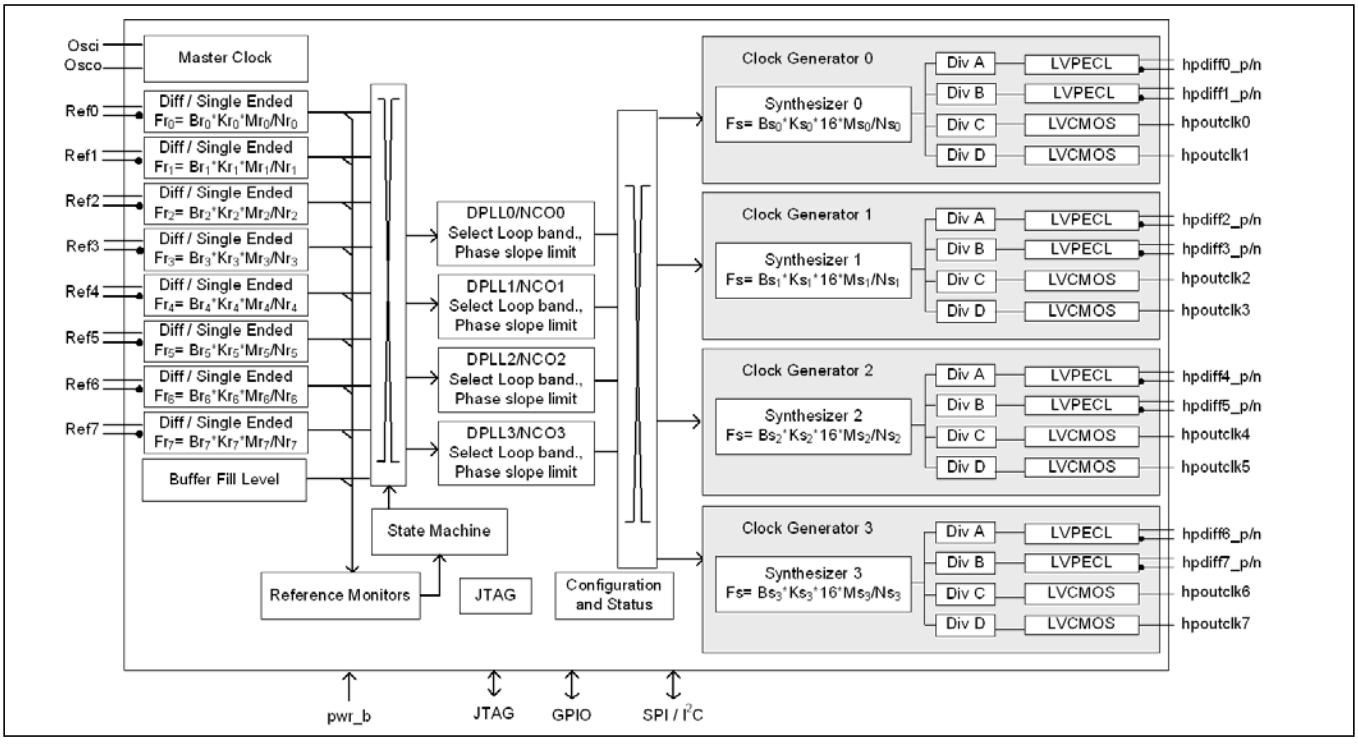

Figure 1 - Functional Block Diagram

Change History

Below are the changes from the February 2014 issue to the March 2015 issue:

Page	Item	Change
10	GPIO pin description	Updated GPIO[5:6] power-up settings
16	Precise Frequency Monitor (PFM)	Clarified the PFM measurement interval
17	Guard Soak Timer (GST)	Corrected the GST description
29	Figure 14 "Typical Power-Up Reset and Configuration Circuit"	Updated GPIO[5:6] power-up settings
31	5.1, “ZL30168 Configuration programming“	Added section 5.1
87	Register Name: phasemem_limit_ref0	Corrected the 1ms phase memory limit example in the register description
127	Register Name: dpll0_df_offset	Corrected the f_out equation in the register description
187	13.0, “Package Markings“	Added section 13.0 for package markings

Below are the changes from the January 2014 issue to the February 2014 issue:

Page	Item	Change
16	Precise Frequency Monitor (PFM)	Added description for supported PFM frequencies
18	DPLL Phase Slope Limiting	Added note to Table 3
19	DPLL States	Added more descriptive text for different DPLL modes
21	Frequency Synthesizer	Added paragraph to match note 2 from 0x1BA:0x1BB register description
48	Register Map	Added Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers when using an Interrupt Handler (event or polling)
85	Register 0x060	Added note to the description of Ref1 PFM Limit
100	Register 0x100	Added note to the description of phase_slope_limit
129	Register 0x1B6	Added text to description of Synth3 APLL syncfailFlag status
131	Register 0x1BA:0x1BB	Updated note2 in the description of Synth0 base frequency multiple Ks0
146	Quadrature Phase Shift	Added a note in the register description for the quadrature phase shift
179	Input to Output Timing	removed parameter T_{REFD}

Page	Item	Change
179	Input to Output Timing	added parameter $T_{HP\_DIFF\_REFD}$
179	Input to Output Timing	updated figure 27 and figure 28 to show ref<7:0> instead of ref<3:0>

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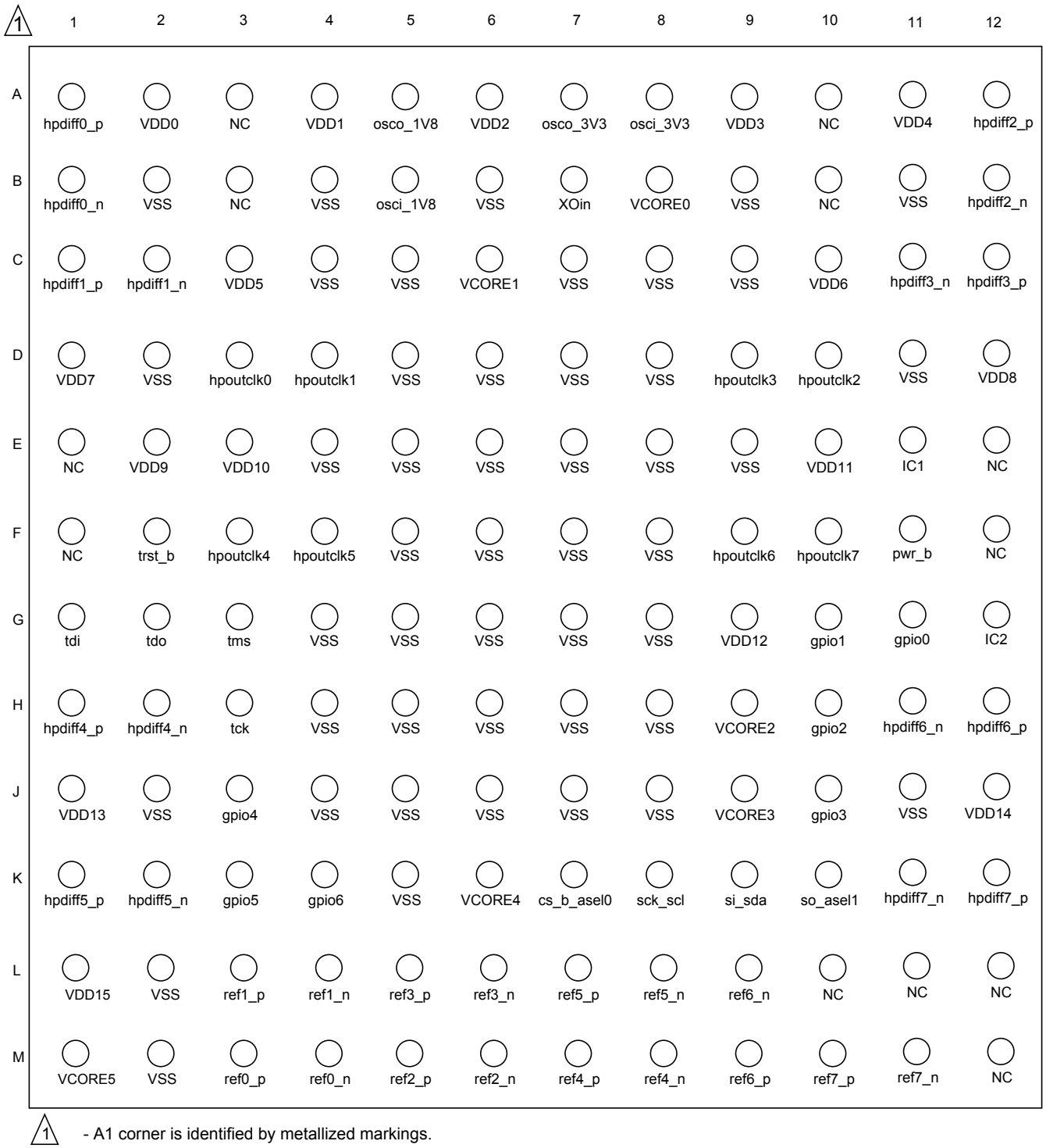
1.0 Pin Diagram

TOP VIEW



1 - A1 corner is identified by metallized markings.

Figure 2 - Package Description

2.0 Pin Description

All device inputs and outputs are LVCMOS unless specifically stated to be differential.For the I/O column, there are digital inputs (I), digital outputs (O), analog inputs (A-I) and analog outputs (A-O).

Ball #	Name	I/O	Description
Input Reference			
M3 M4 L3 L4 M5 M6 L5 L6 M7 M8 L7 L8 M9 L9 M10 M11	ref0_p ref0_n ref1_p ref1_n ref2_p ref2_n ref3_p ref3_n ref4_p ref4_n ref5_p ref5_n ref6_p ref6_n ref7_p ref7_n	I	**Input Reference 0 to 7.** Input reference sources used for synchronization. The positive and negative pair of these inputs accepts a differential input signal. The refx_p input terminal accept a CMOS input reference. These inputs can be used as an external feedback input. Maximum frequency limit on single ended inputs is 177.5 MHz, and 750 MHz on differential inputs.
Output Clocks			
D3 D4 D10 D9 F3 F4 F9 F10	hpoutclk0 hpoutclk1 hpoutclk2 hpoutclk3 hpoutclk4 hpoutclk5 hpoutclk6 hpoutclk7	O	**High Performance Output Clock 0 to 7.** Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz
A1 B1 C1 C2 A12 B12 C12 C11 H1 H2 K1 K2 H12 H11 K12 K11	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdiff3_n hpdiff4_p hpdiff4_n hpdiff5_p hpdiff5_n hpdiff6_p hpdiff6_n hpdiff7_p hpdiff7_n	O	**High Performance Differential Output Clock 0 to 7 (LVPECL).** Maximum frequency limit on differential outputs is 750 MHz

Table 1 - Pin Description

Ball #	Name	I/O	Description
Control and Status			
F11	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The **pwr_b** pin should be held low for 2 ms after all power supplies are stabilized. This pin is internally pulled-up to V_{DD}. User can access device registers either 125 ms after **pwr_b** goes high, or after bit 7 in register at address 0x000 goes high (which can be determined by polling).
G11 G10 H10 J10 J3 K3 K4	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6	I/O	**General Purpose Input and Output pins.** These are general purpose I/O pins. Available GPIO functions include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • Differential output clock enable • High performance LVCMOS outputs enable • Host Interrupt Output to flag status changes. Pins 5:0 are internally pulled down to GND and pins 6 is internally pulled up to V_{DD}. Unused GPIO pins can be left unconnected. After power on reset, device GPIO[0,1,3] configure basic device function. GPIO3 sets I^2C or SPI control mode, GPIO[1,0] sets master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1 kΩ resistor for their assigned functions at reset; or they must be driven low or high for 125 ms after reset, and released and then used for normal GPIO functions. The GPIO4 pin must be either pulled low with an external 1 kΩ resistor; or it must be driven low for 125 ms after reset, and then released and used for normal GPIO functions. GPIO[5,6] are not used during power up for generic devices. For custom configured devices they select one of the four OTP configurations stored in the device and must be either pulled low or high with an external 1kohm resistor; or driven low or high for 125ms after reset, then released and used for normal GPIO functions.
Host Interface			
K8	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I^2C mode. As an input, this pin is internally pulled up to V_{DD}.
K9	si_sda	I/O	**Serial Interface Input.** The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I^2C mode. This pin is internally pulled up to V_{DD}.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
K10	so_asel1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I^2C address select when host interface is configured for I^2C mode.
K7	cs_b_asel0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I^2C address select when host interface is configured for I^2C mode.This pin is internally pulled up to V_{DD}.
JTAG (IEEE 1149.1) and Test			
G12	IC2	I	**Internal Connection**. Connect this pin to GND.
E11	IC1	A-I/O	**Internal Connection.** Leave unconnected.
G2	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G1	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
F2	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be held low or pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
H3	tck	I	**Test Clock.** Provides the clock for the JTAG test logic. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
G3	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock Note: The **osci_1V8/osco_1V8** pins are preferred to connect a crystal to the device. The **XOin** pin is preferred to connect a crystal oscillator (XO) to the device.			
A7	osco_3V3	A-O	**3.3V Crystal Master Clock Output.** For the alternative connection method for a crystal, the crystal is connected from this pin to **osci_3V3**. Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between **osci_1V8** and **osco_1V8**, this pin should be left unconnected.
A8	osci_3V3	I	**3.3V Crystal Master Clock Input.** For the alternative connection method for a crystal, the crystal is connected from this pin to **osco_3V3**. For clock oscillator operation or the use of a crystal between **osci_1V8** and **osco_1V8**, this pin should be grounded.
A5	osco_1V8	A-O	**1.8V Crystal Master Clock Output.** For the primary connection method for a crystal, the crystal is connected from this pin to **osci_1V8**. Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between **osci_3V3** and **osco_3V3**, this pin should be left unconnected.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B5	osci_1V8	I	**1.8V Crystal Master Clock Input.** For the primary connection method for a crystal, the crystal is connected from this pin to **osco_1V8.** For clock oscillator operation or the use of a crystal between **osci_3V3** and **osco_3V3**, this pin should be grounded.
B7	XOin	I	**XO Master Clock Output.** For clock oscillator operation, this pin is connected to the output of the oscillator. For crystal operation using either method, this pin should be grounded.
Power and Ground			
B8 C6 H9 J9 K6 M1	V_{CORE0} V_{CORE1} V_{CORE2} V_{CORE3} V_{CORE4} V_{CORE5}		**Positive Supply Voltage.** +1.8V_{DC} nominal. These pins should not be connected together on the board. Please see application note for recommendations
A2 A4 A6 A9 A11 C3 C10 D1 D12 E2 E3 E10 G9 J1 J12 L1	V_{DD0} V_{DD1} V_{DD2} V_{DD3} V_{DD4} V_{DD5} V_{DD6} V_{DD7} V_{DD8} V_{DD9} V_{DD10} V_{DD11} V_{DD12} V_{DD13} V_{DD14} V_{DD15}		**Positive Supply Voltage.** +3.3V_{DC} nominal. These pins should not be connected together on the board. Please refer to ZLAN-327 for recommendations

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B2 B4 B6 B9 B11 C4 C5 C7 C8 C9 D2 D11 E4 E9 G4 H4 H5 H6 H7 H8 J2 J4 J5 J6 J7 J8 J11 K5 L2 M2 D5 D6 D7 D8 E5 E6 E7 E8 F5 F6 F7 F8 G5 G6 G7 G8	V_{SS}		**Ground.** 0 Volts.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
No connection			
A3 A10 B3 B10 E1 E12 F1 F12 L10 L11 L12 M12	NC		**No Connection.** These pins should be left open.

Table 1 - Pin Description (continued)

3.0 Application Example

Optical Transport Network (OTN) Transponders and Muxponders require de-synchronizers (PLLs) to filter gapped clock jitter introduced in demapping process. Figure 1 shows a typical OTN Muxponder with four different clients: SONET/SDH, Ethernet, Fiber Channel and Digital Video. ZL30168 has four independent de-synchronizers capable of locking and generating any frequency between 1 kHz and 750 MHz. Hence, ZL30168 can handle any OTN client rate. In addition, an additional ZL30168 could be used to generate a free-running master clock for the OTN Transmit line.

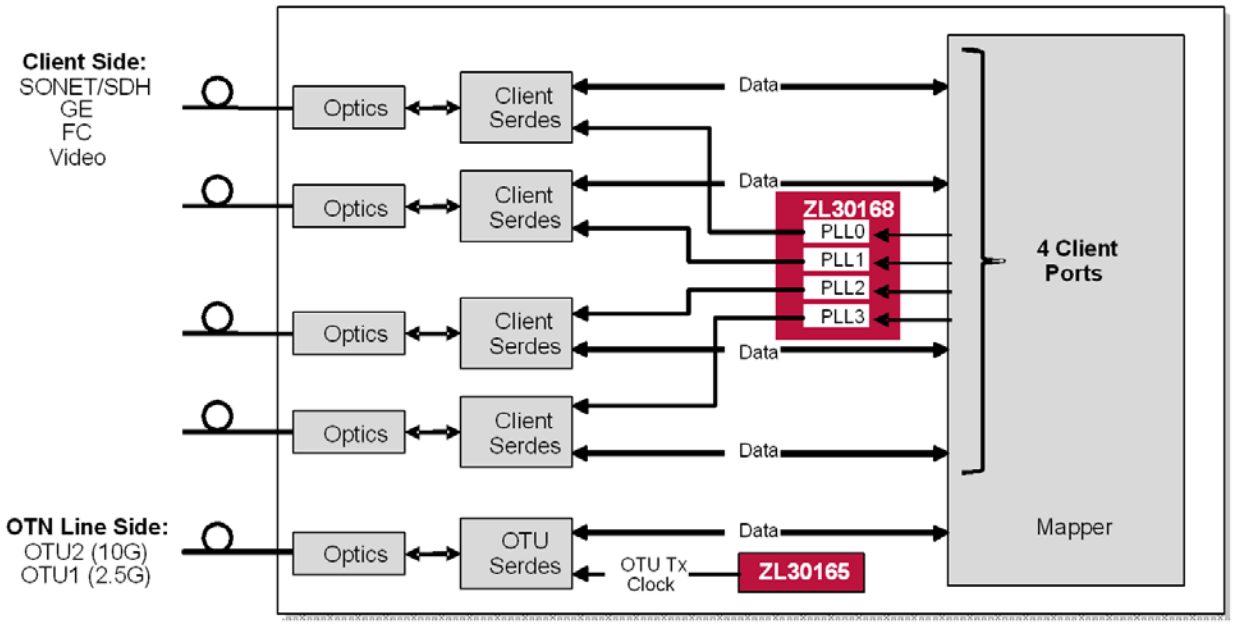


Figure 3 - Application Diagram: Frequency Generation for OTN Client Clock Generation

4.0 Functional Description

The functional block diagram of the device is shown in Figure 1. It's detailed operation is described in the following sections.

4.1 Input Sources

The device has nine input sources: eight input references (single ended or differential) and one oscillator clock source (oscillator or xtal).

The device master clock frequency is configured on reset via external voltage levels on GPIO[1:0] pins. The recommended frequency of the master clock is 49.152 MHz.

The device synchronizes (locks) to any input reference which is a 1 kHz multiple, or it synchronizes (locks) to any input reference which is an M/N x 1 kHz multiple (FEC rate) where M and N are 16 bits wide.

The device input reference frequency is programmed during initialization, which can be changed during operation by setting the DPLL into the holdover mode before a frequency change.

The device accepts an input reference with a maximum frequency of 177.5 MHz through single ended LVCMOS input or 750 MHz frequency through differential inputs.

If the frequency of an input reference exceeds 400 MHz, the reference must be divided by 2 before being fed to DPLL (Refer to **ref_pre_divide** registers).

4.2 Input Reference Monitoring

The input references are monitored by reference monitor indicators which are independent for each reference. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

Loss of Signal Monitor (LOS)

LOS is an external signal, fed to one of ZL30168 GPIO pins. LOS is typically generated by a PHY device whose recovered clock is fed to one of the reference inputs. The PHY device will generate a LOS signal when it cannot reliably extract the clock from the line. The user can set one of GPIO pins as a LOS input by programming corresponding GPIO register.

Coarse Frequency Monitor (CFM)

The CFM monitors the input reference frequency for 1.25 ms so that it can quickly detect large changes in frequency. CFM limit for each input reference can be selected in corresponding **scm_cfm_limit_ref** registers with range from 0.1% to 50%. If the CFM limit is exceeded, then CFM failure is declared for corresponding reference.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same values for proper operation.

Precise Frequency Monitor (PFM)

The PFM block measures the frequency accuracy of the reference over a 10 second interval, the indicator bit is updated every second. The PFM provides a level of hysteresis to prevent a failure indication from toggling between valid and invalid for input references that are on the edge of the acceptance range. PFM limit for each reference can be selected in the **pfm_limit_ref** registers. When determining the frequency accuracy of the reference input, the PFM uses the external master clock oscillator's frequency as its reference.

PFM supports any reference (input) frequency from 1 Hz to 750 MHz except for non integer (in Hz) frequencies below 5,000,000 Hz. For example 1 Hz, 8 kHz, 2.048 MHz, 156.25*66/64 MHz are supported frequencies but 0.5 Hz and 1.5 Hz are not supported.

PFM limit should be set based on the following table in **pfm_limit_ref** registers:

Value	Acceptance Range	Rejection Range	Typical Application
000	+/- 9.2 ppm	+/- 12 ppm	Stratum 3, G.813 option 1, G.8262 EEC 1 & 2
100	+/- 13.8 ppm	+/- 18 ppm	
101	+/- 24.6 ppm	+/- 32 ppm	
110	+/- 36.6 ppm	+/- 47.5 ppm	
001	+/- 40 ppm	+/- 52 ppm	SONET Minimum Clock, G.813 option 2
111	+/- 52 ppm	+/- 67.5 ppm	
010	+/- 64 ppm	+/- 83 ppm	Stratum 4, G.824
011	+/- 100 ppm	+/- 130 ppm	G.823

Table 2 - Frequency Out of Range Limits

Single Cycle Monitor (SCM)

This detector measures the rising to rising edge and falling to falling edge periods of the input reference. If either exceeds the predefined SCM limit then a SCM failure is declared. The SCM limit for each input reference can be selected in the corresponding **scm_cfm_limit_ref** registers with range from 0.1% to 50%. The limits are input frequency dependent. Please refer to the description in **scm_cfm_limit_ref** registers.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same values for proper operation.

For frequencies above 400 MHz, SCM (and the GST) should not be used.

Guard Soak Timer (GST)

When selected, the guard soak timer adds extra time to qualify and disqualify a reference. The default time to wait to disqualify a reference is 50 ms after a CFM and SCM failure is detected. When qualifying a reference, the time starts when the CFM or SCM failure is cleared. The default qualification time is 4 times the disqualification time.

A PFM failure does not effect this timer.

For frequencies above 400 MHz, the GST should not be used because the single cycle monitor (SCM) will never be valid.

Holdover and Reference Switching Masks

These bit fields control which of the reference monitoring signals on the selected reference are used to trigger a reference switch or transition to holdover. The **dplln_ref_fail_mask** and **dplln_pfm_fail_mask** fields control the action taken when any of the reference monitoring signals is triggered. Please note that the GST mask bit should not be enabled without either the SCM or the CFM bit for either reference switching or holdover. Also, the holdover mask has higher priority than the reference switching mask when both have the same signal unmasked.

For return from holdover, the mask refers to the highest priority reference and will prevent the start of transition to lock mode if the indicated conditions are active.

4.3 Digital Phase Locked Loop (DPLL)

The device supports four independent digital PLL modules. All four DPLLs are enabled by default. Each DPLL can be enabled/disabled through the host registers via I^2C or SPI.

With four DPLLs, the device can synchronize to four independent reference clocks.

4.3.1 DPLL General Characteristics

Pull-in Hold-in range

The DPLL supports pull-in/hold-in of +/-12 ppm, +/-52 ppm, +/-83 ppm,+/-130 ppm, +/-400 ppm or unlimited.

The pull-in/hold-in range is selected per DPLL and prevents the DPLL from locking to a reference that is off-frequency. The PFM (and CFM) also measure the frequency of an input and are provisioned on a per input basis. Both mechanisms work together to control the reference selection and DPLL state based on the input frequency. If the PFM out of range limit is set to allow a wide range of frequencies while the pull-in is set to be narrow, the reference will be qualified but the DPLL will never lock to the reference. For a certain application, it is important to set the PFM and pull-in ranges correctly for proper operation.

DPLL bandwidth (jitter/wander transfer)

The DPLL supports the following first order filtering cut-off frequencies: 5.2 Hz,14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz and 896 Hz. The DPLL bandwidth is typically determined during the initialization. When changing the bandwidth dynamically, it is recommended to put the DPLL to Holdover mode first and then change the bandwidth. After the bandwidth has been changed, the DPLL is then set back to the Normal mode.

For line card bandwidths in the ZL30168 (5.2 Hz and above), it is recommended that the fast lock mode be enabled when phase slope limiting is used. The fast lock mode should be disabled with an unlimited PSL. This can be done in the **dpll*n*_fast_lock_ctrl** register.

The DPLL locks to an input reference and provides a stable low jitter output clock when the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a 19.44 MHz reference could use a bandwidth up to 896 Hz, and a 1 kHz input reference could be used a loop bandwidth of up to 14 Hz. For 8 kHz reference the recommended maximum loop bandwidth is 56 Hz.

Jitter/Wander Generation

Jitter and wander generation performances are provided in section 10.0, “Performance Characterization“.

Phase Transients

When a reference switch occurs with phase tracking active (i.e., TIE clear disabled or hitless reference switching), the DPLL transitions the phase of the output smoothly, limited by the selected loop bandwidth and by the selected phase slope limit.

The device offers the following selectable phase slope limiting options: 61 usec/sec, 7.5 usec/sec, 0.885 usec/sec or unlimited. If the required phase slope limit is 0.885 usec/sec or 7.5 usec/sec, the user should first set the device to unlimited phase slope and wait for PLL to achieve lock before changing it to desired phase slope limit The phase slope limit is set in register **dpllX_ctrl** as shown in Table 3.

dpll_phase_slope_limit	Phase Slope Limiting	Application
00	61 μs/s	GR-1244 Stratum 3
01	7.5 μs/s	G.813 option 1
10	885 ns/s	GR-1244 Stratum 2, 3E, 3 (objective)

Table 3 - DPLL Phase Slope Limiting

dpll_phase_slope_limit	Phase Slope Limiting	Application
11	Unlimited	Default setting

Table 3 - DPLL Phase Slope Limiting

Note: Under certain configurations, the output of the DPLL may exceed these phase slope limit values. This depends on the input transient (phase or frequency) and the bandwidth of the DPLL.

Holdover Stability

DPLL initial holdover accuracy is better than 50 ppb for a jittered input and better than 10 ppb for a jitter-free input.

Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, reference switching or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with input reference type.

DPLL Monitoring

The DPLL provides lock and holdover indicators using the default lock indicator conditions.

The lock time is dependent on employed loop bandwidth. The device has a lock time of less than 1 sec for all available DPLL loop bandwidth selections with phase slope limit set to unlimited. For the other phase slope limits please refer to Section 10.2.

4.3.2 DPLL States

The DPLL in the device support five modes: free-run, forced holdover, automatic, forced reference lock and numerically controlled oscillator (NCO). To lock the DPLL to a reference, automatic or forced reference mode should be used. In each of the locked modes, there are three states: acquiring, normal (locked) and holdover. (The acquiring state is temporary between the availability of a reference and the completion of the locking process.) In the automatic mode, the DPLL may go between the states depending on the availability of all the references (with a priority above “never lock”). In forced reference mode, the device will go into holdover if the reference selected is unavailable even if other references are available. The availability of a reference is determined by the reference qualification process. In the holdover state, the device provides output clocks which are not locked to an external reference signal, but are based on an estimate of the frequency during the previous time in the locked state. To force the DPLL into the holdover state even with good references present, the forced holdover mode is used.

In addition, the DPLL can be put into the free-run mode. This is used when the synchronization to a reference is not required or is not possible. Typically, this is used immediately following system power-up. In the free-run mode, the device provides timing and synchronization signals which are based on the master clock frequency only, and are not synchronized to the reference input signals. The free-run accuracy of the output clock is equal to the accuracy of the master clock. So if a ±20 ppm free-run output clock is required, the master clock must also be ±20 ppm.

The freerun mode:

- The DPLL has to generate all its output clocks based only on the device master clock input.
- The DPLL will not lock or switch to a reference or go into holdover.
- The reference switch mask and the reference holdover mask are ignored.

The forced holdover mode:

- All references are ignored and the DPLL has to go to holdover (based on last selected reference)
- The reference switch mask and the reference holdover mask are ignored.

The forced reference lock mode:

- The DPLL will try to lock to the host-specified reference.
- The reference switch mask is ignored. No reference switching will be performed.
- If the holdover mask is set, then the device will switch to holdover if the selected reference fails.
- If the holdover mask is not set, then the device will attempt to lock to the selected reference, even if it is failing one of the reference monitors.

The automatic mode:

- Reference selection and holdover is automatically handled by the device, based on the holdover and reference switch masks, and the reference priority.
- If the reference switch mask is set, then reference will be selected based on availability and priority. If all enabled references are bad, then the device will enter holdover.
- If holdover mask is set (and ref. switch mask cleared), then device switches to holdover on ref failure.
- If neither ref switch nor holdover mask are set, then device will keep trying to lock to a failed ref.

The NCO mode:

The DPLL is run in free-run mode. The output clock is the requested synthesizer frequency with an offset specified by the **deployments** register. This write-only register will change the output frequency of the DPLL.

Finally, a **buffer-fill** mode is also available.

4.3.3 DPLL Rate Conversion Function and FEC Support

The DPLL provides up scaling and down scaling functions. It has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports:

- **Simple rate conversion** (i.e., take in 19.44 MHz and create 255/238 FEC SONET/SDH clock of 666.51 MHz),
- **Double rate conversion** (i.e., take in 19.44 MHz, create FEC 10 GbE clock of 644.5313, which is 66/64 rate converted 625 MHz, or create 690.5692 which is 255/238 x 66/64 rate converted 625 MHz)

The following is just an example of the frequencies that can be supported at the input and output independently (many more frequencies can be supported):

- **GbE:**
  - 25 MHz
  - 125 MHz
- **XAUI (chip to chip interface, which is a common chassis to chassis interface)**:
  - 156.25 MHz or x2 or x4 version
- **OC-192/STM-64:**
  - 155.52 MHz or x2 or x4 version
  - 155.52 MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
  - 155.52 MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version
- **10 GbE:**
  - 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
  - 155.52 MHz x 66/64 or x2 or x4 version

- Long reach 10 GE might require the following frequencies with simple rate conversion: (156.25 MHz x 255/237) and (156.25 MHz x 255/238).
- The following frequencies with double rate conversion: (155.52 MHz x 66/64 x 255/237) or (155.52 MHz x 66/64 x 255/238) and (156.25 MHz x 66/64 x 255/238) or (156.25 MHz x 66/64 x 255/238). Also, user can use x2 or x4 version of the listed frequencies.

Application Note ZLAN-447 explains how to generate the most common frequencies.

4.3.4 DPLL Input to Output and Output to Output Phase Alignment

Techniques offered for Phase Alignment

When the output clock is locked to a jitter free and wander free input clock, input to output latency is expected to have a typical error of 0 nsec.

The coarse and fine phase adjustments allow for input to output and output to output latency corrections to compensate for PCB load delay, as detailed in 4.5, “Dividers and Skew Management“.

The PLL architecture allows for implementation of an external feedback (external output clock phase sense) of the PLL path that is fed through one of the available references (REF 0 to 7). Such external feedback would allow for dynamic changes of PCB routing and external buffer delay caused by changes in temperature.

It is recommended that the DPLLs be fully configured before enabling external feedback. If a synthesizer or DPLL in the external feedback path need to be reconfigured, disable external feedback before changing the parameters and then enable external feedback.

4.4 Frequency Synthesizer

The device frequency synthesizers can generate output clocks which meet the jitter generation requirements for various timing requirements detailed in section 10.0, “Performance Characterization“.

The frequency synthesis engines can generate any clock frequency between 1 GHz and 1.5 GHz. The frequency for each synthesizer is programmed as 16 * B * K * M/N Hz where B, K, M and N are 16 bits wide registers.

For proper operation of the synthesizer, Bs x Ks x Ms / Ns must not be a multiple any of the following frequencies: 65,536,000; 69,632,000; 73,728,000; 77,824,000; 81,920,000; 86,016,000 or 90,112,000.

4.5 Dividers and Skew Management

Each frequency synthesizer has four independent output dividers. Two dividers are associated with differential LVPECL outputs that can generate clocks from 1 Hz to 750 MHz and the other two dividers are associated with single ended LCVCMOS outputs that can generate clocks between 1 Hz and 177.5 MHz.

Each synthesizer with associated dividers supports fine and coarse phase (skew) adjustment of output clocks. The fine phase adjustment affects equally all four outputs driven by a particular synthesizer, while the coarse phase affects independently each LVCMOS output.

The fine phase adjustment allows the user to advance simultaneously all four outputs of each synthesizer in 256 steps where each step is 1/256 of the Synthesizer clock period. For example if the synthesizer is programmed to generate 1.5GHz clock, the maximum fine advancement is 666.6 ps with the step size of only 2.6 ps.

The coarse phase adjustment allows the user to advance or delay each LVCMOS output in steps equal to the period of the synthesizer clock frequency with the maximum range equal to +/-4096 synthesizers clock periods. For example, if the synthesizer is programmed to generate 1.5 GHz clock, the step size will be 1/1.5GHz = 666.6ps and the maximum range will be +/-4096 * 666.6 ps.

4.6 Output Clocks Configuration

Figure 4 shows relationship between synthesizers, dividers and output dividers.

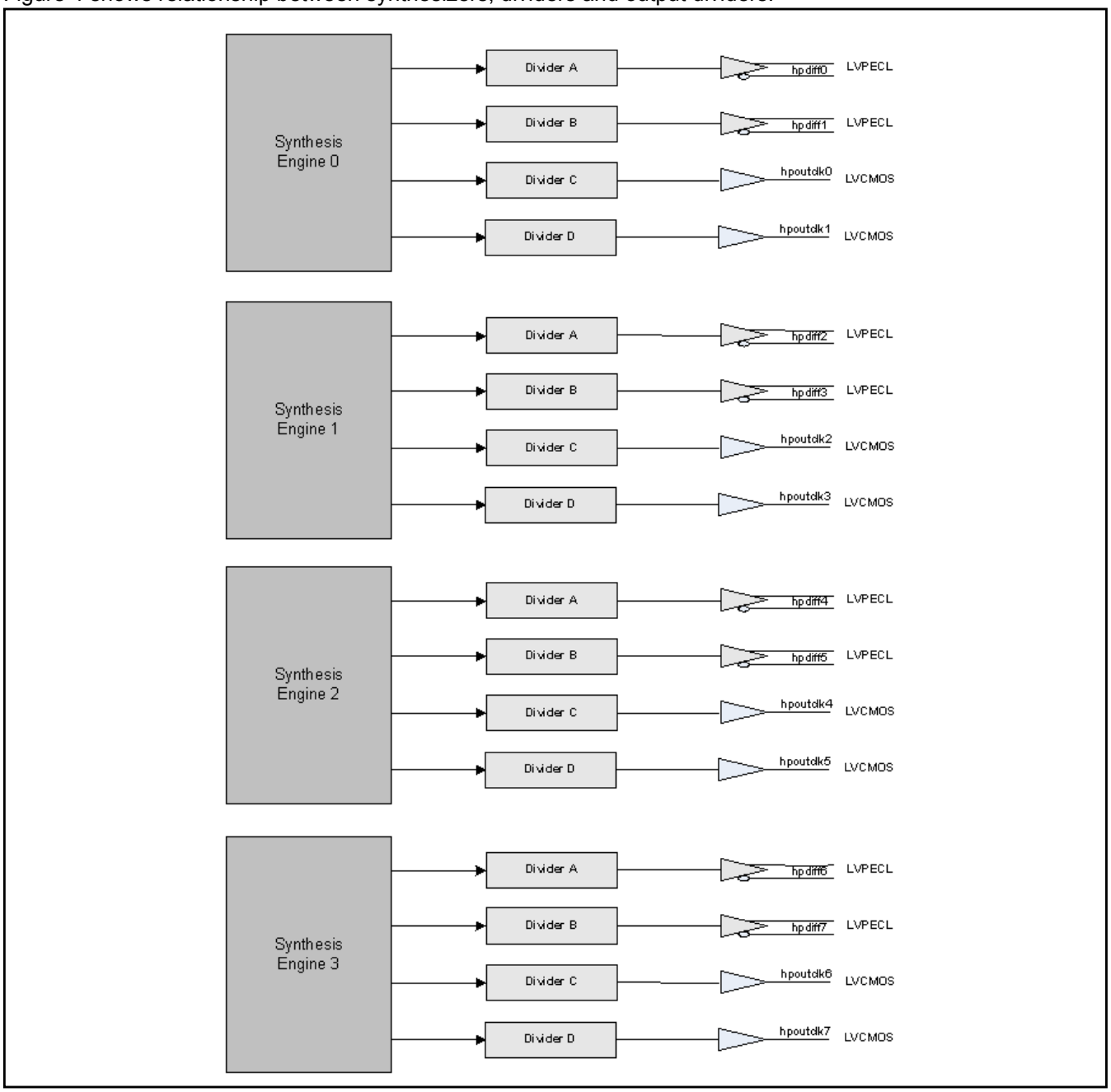


Figure 4 - Output Clocks Configuration

4.7 Output Drivers

The device has eight high performance (HP) differential (LVPECL) outputs. and eight high performance (HP) single ended outputs.

High Performance (HP) single ended driver (LVCMOS) supports a maximum clock frequency of 177.5 MH and the high performance (HP) differential driver (LVPECL) supports a maximum clock frequency of 750 MHz, the jitter performance is detailed in section 10.0, “Performance Characterization“.

The LVPECL outputs should be terminated as shown in Figure 5. Terminating resistors provide 50 Ω equivalent Thevenin termination as well as biasing for the output LVPECL driver. Terminating resistors should be placed as close as possible to input pins of the LVPECL receiver. If the LVPECL receiver has internal biasing then AC coupling capacitors should be added.

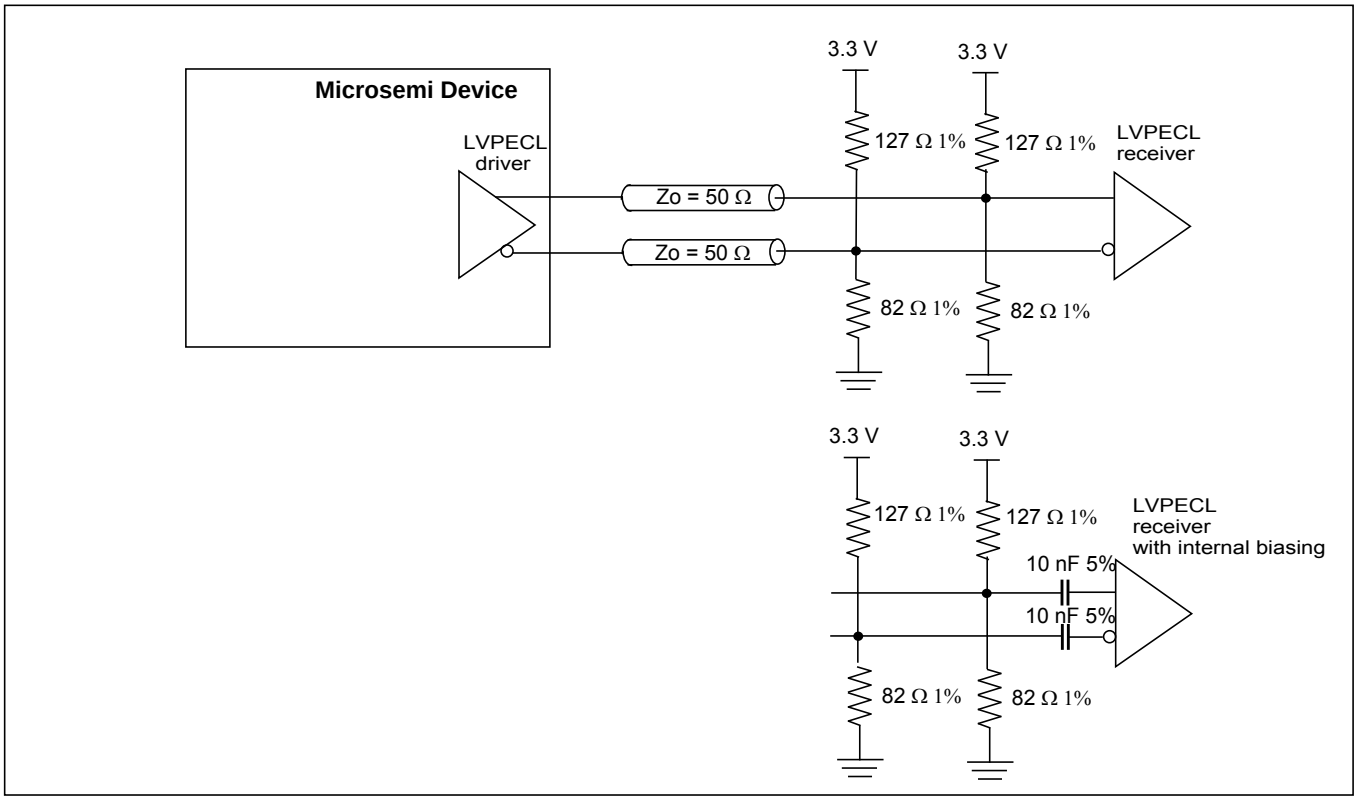


Figure 5 - Terminating LVPECL Outputs

If the transmission line is required to be AC coupled then the termination shown in Figure 6 should be implemented. 200 Ω resistors are used to provide DC biasing for LVPECL driver. Both AC coupling capacitor and biasing resistors should be placed as close as possible to output pins.

Thevenin termination (127 Ω and 82 Ω resistor) provide 50 Ω termination as well as biasing of the input LVPECL receiver. If the LVPECL receiver has internal DC biasing then the line should be terminated with 100 Ω termination resistor between positive and negative input. In both cases termination resistors should be places as close as possible to the LVPECL receiver pins. Some LVPECL receivers have internal biasing and termination. In this case no external termination should be present.

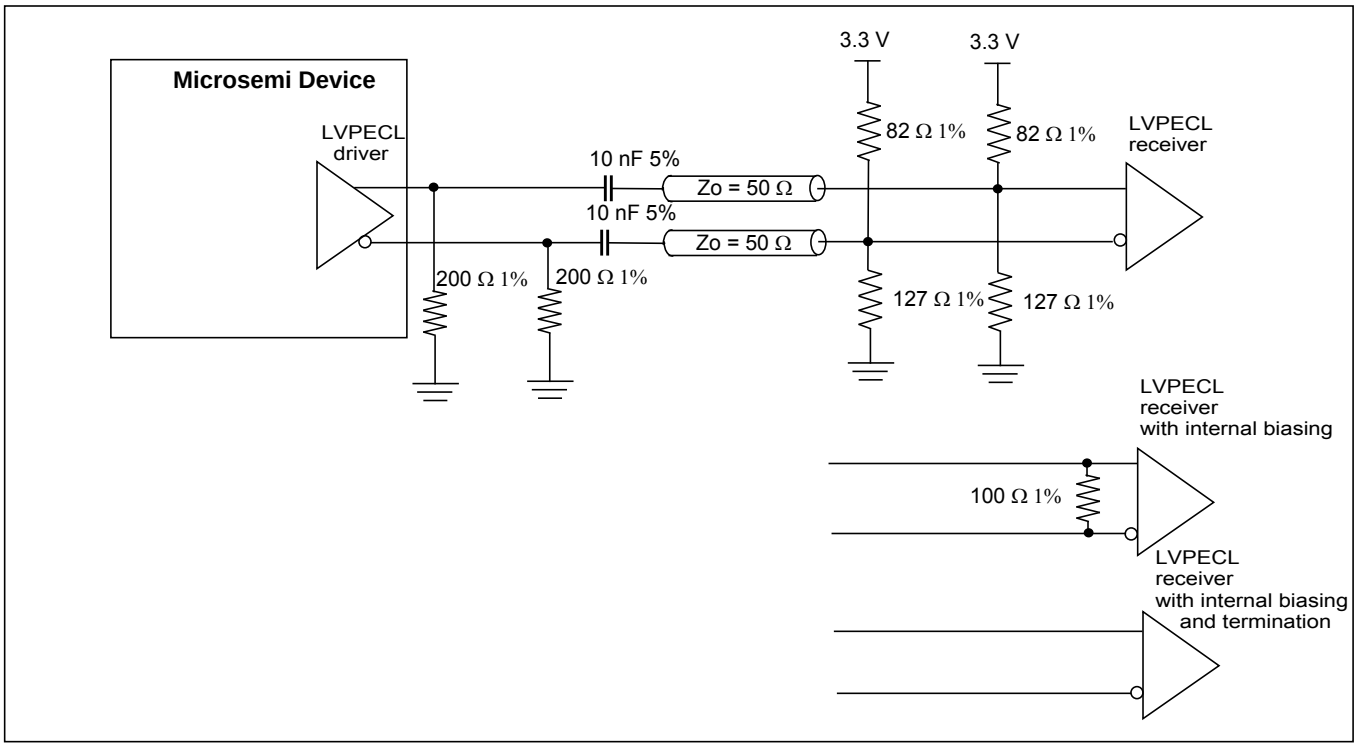


Figure 6 - Terminating AC coupled LVPECL outputs

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 7.

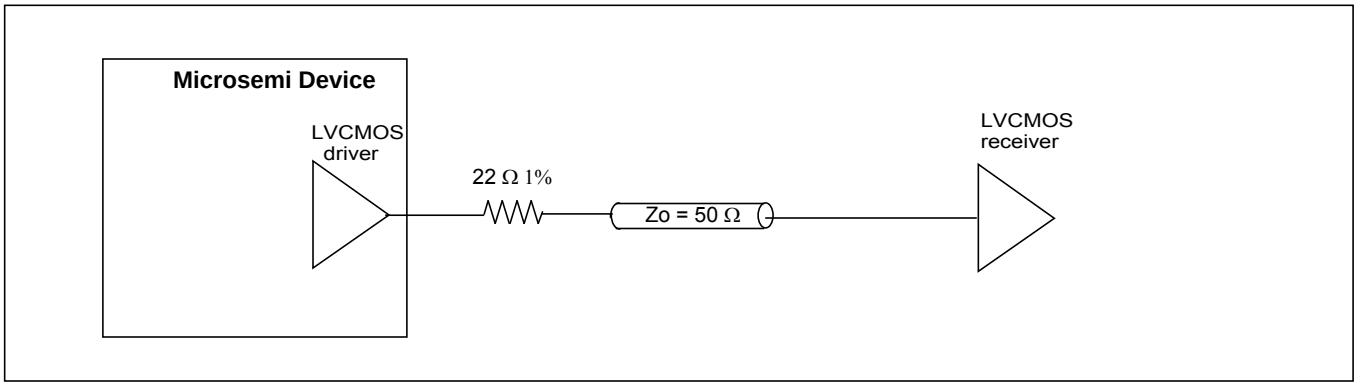


Figure 7 - Terminating LVCMOS outputs

4.8 Input Buffers

The ZL30168 has eight reference inputs ref[7:0]_p/ref[7:0]_n that can work as either single ended or differential. By default all reference inputs are single ended. This can be changed by programming **ref_config** register.

The Input frequency range for differential inputs is: 1 kHz to 750 MHz; for single ended inputs is: 1 kHz to 177.5 MHz.

Differential reference inputs need to be properly terminated and biased as shown in Figure 8 and Figure 9 for LVPECL and Figure 10 and Figure 11 for LVDS drivers. When terminating LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC couple the LVPECL driver because ZL30168 differential inputs have different common mode (bias) voltage than LVPECL receivers. Thevenin termination (182 Ω and 68 Ω resistors) provide 50 ohm equivalent termination as well as biasing of the input buffer for DC coupled line. For AC coupled line, Thevenin termination with 127 Ω and 82 Ω resistors should be used as shown in Figure 9. The value of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10 nF is good for input clock frequencies above 100 MHz. For lower clock frequencies capacitor values will have to be increased accordingly.

Terminations for DC and AC coupled LVDS line are shown in Figure 10 and Figure 11 respectively. Differential input biasing is provided by LVDS driver in case of DC coupling (Figure 10), whereas for AC coupling (Figure 11) biasing is generated by 12 kΩ and 8.2 kΩ resistors. In both cases, the line is terminated with 100 Ω resistor.

For single ended CMOS inputs, refx_n input needs to be connected to the ground as shown in Figure 12. The value of series termination resistor will depend on CMOS output driver but the most common values are 33 Ω and 22 Ω.

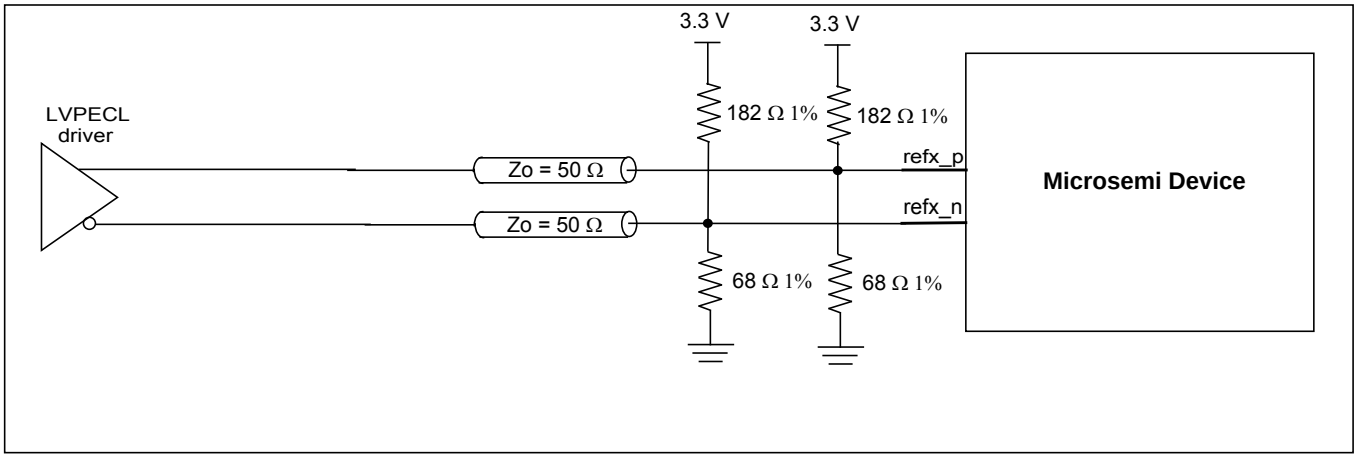


Figure 8 - Differential DC Coupled LVPECL Termination

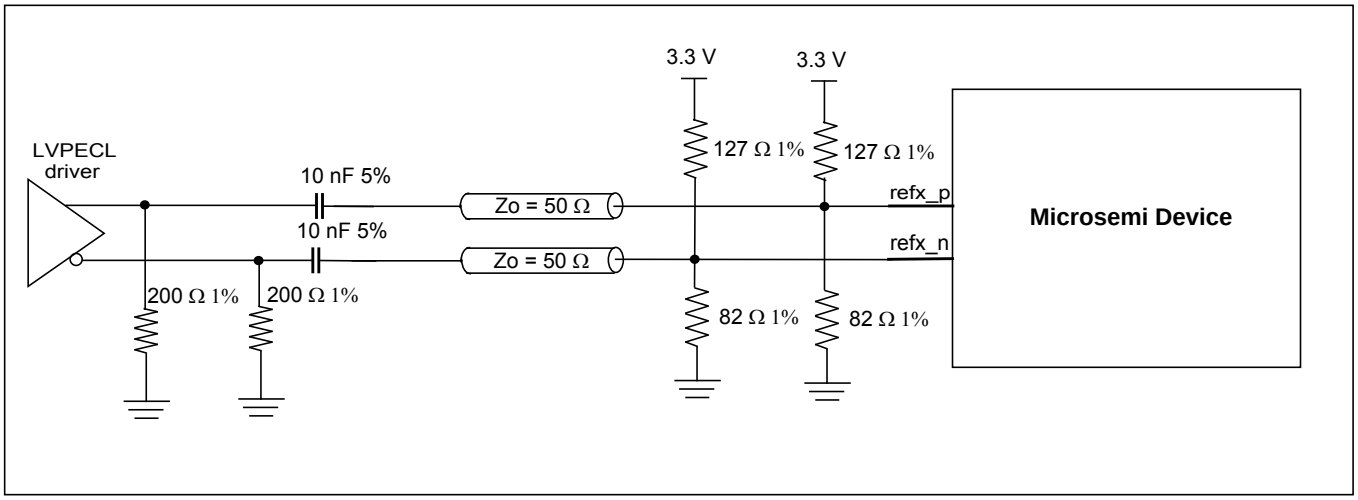


Figure 9 - Differential AC Coupled LVPECL Termination

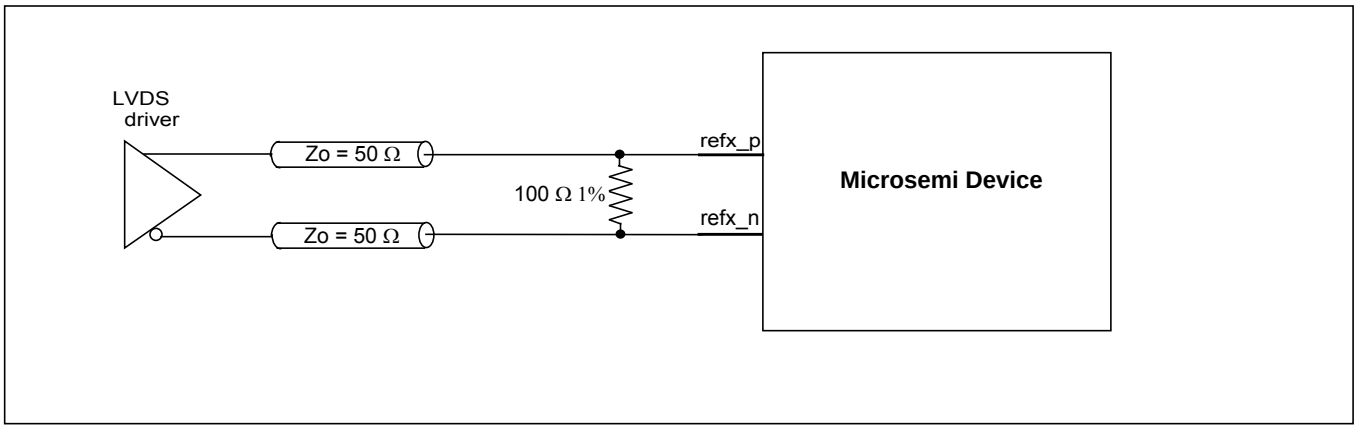


Figure 10 - Differential DC Coupled LVDS Termination

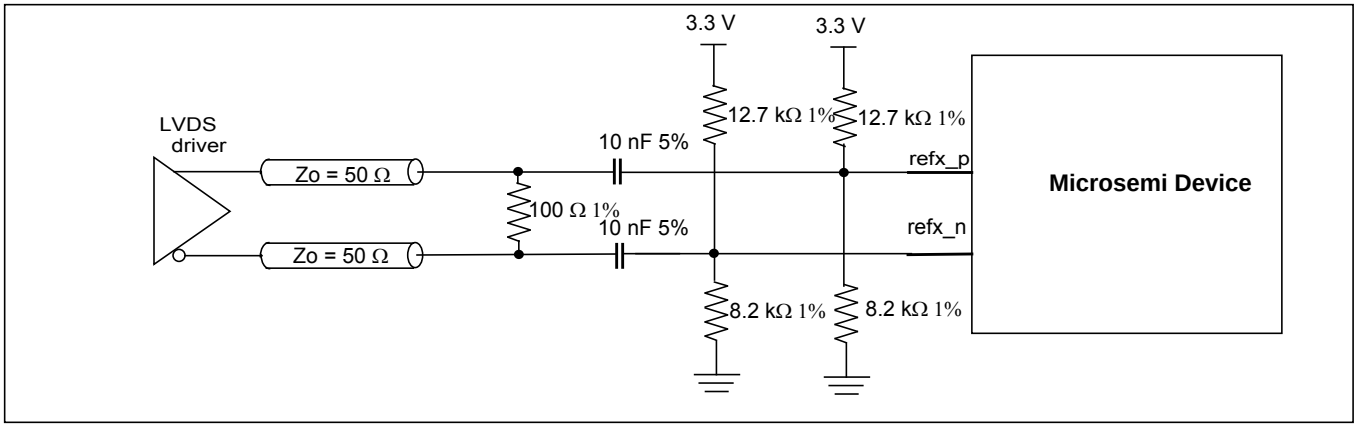


Figure 11 - Differential AC Coupled LVDS Termination

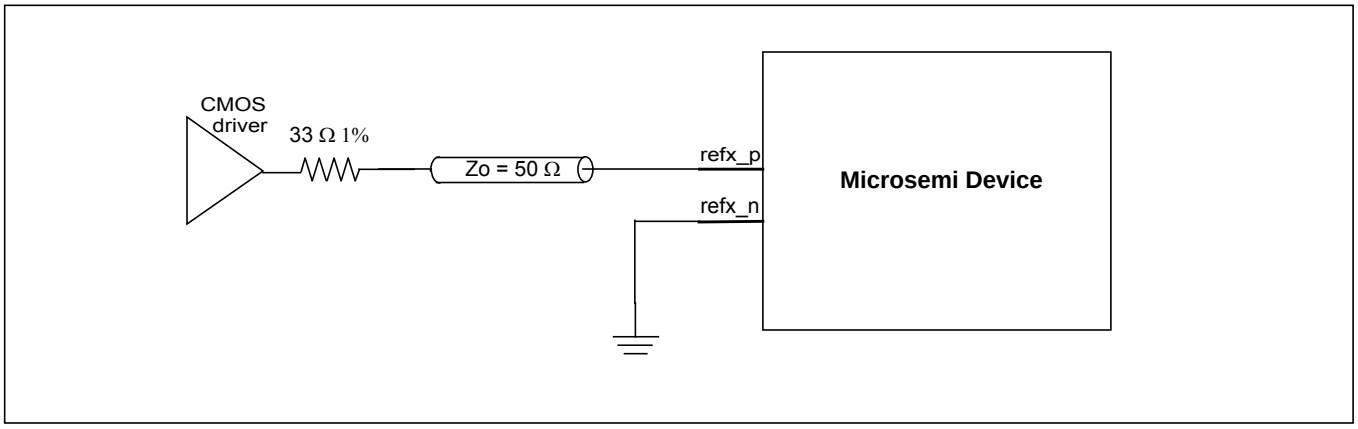


Figure 12 - Single Ended CMOS Termination

4.9 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to the Application Note for a list of recommended clock oscillators.

4.9.1 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **XOin** pin as shown in Figure 13. The connection to **XOin** should be direct and not AC coupled. The **osci_1V8** and **osci_3V3** pins must be grounded. The **osco_1V8** and **osco_3V3** pins must be left unconnected.

When using crystal resonator as the master timing source, connect the crystal between **osci_1V8** and **osco_1V8** pins as shown in Figure 13. (While it is not preferred, the crystal can also be connected between the **osci_3V3** and **osco_3V3** pins.) The crystal should have bias resistor of 1 MΩ and load capacitances C1 and C2. Value of the load capacitances is dependent on the crystal and should be per the crystal's datasheet. The crystal should be a fundamental mode type – not an overtone. When using 24.576 or 49.152 MHz oscillators, the user needs to use the default value of the **central_freq_offset** register (0x046AAAAB).

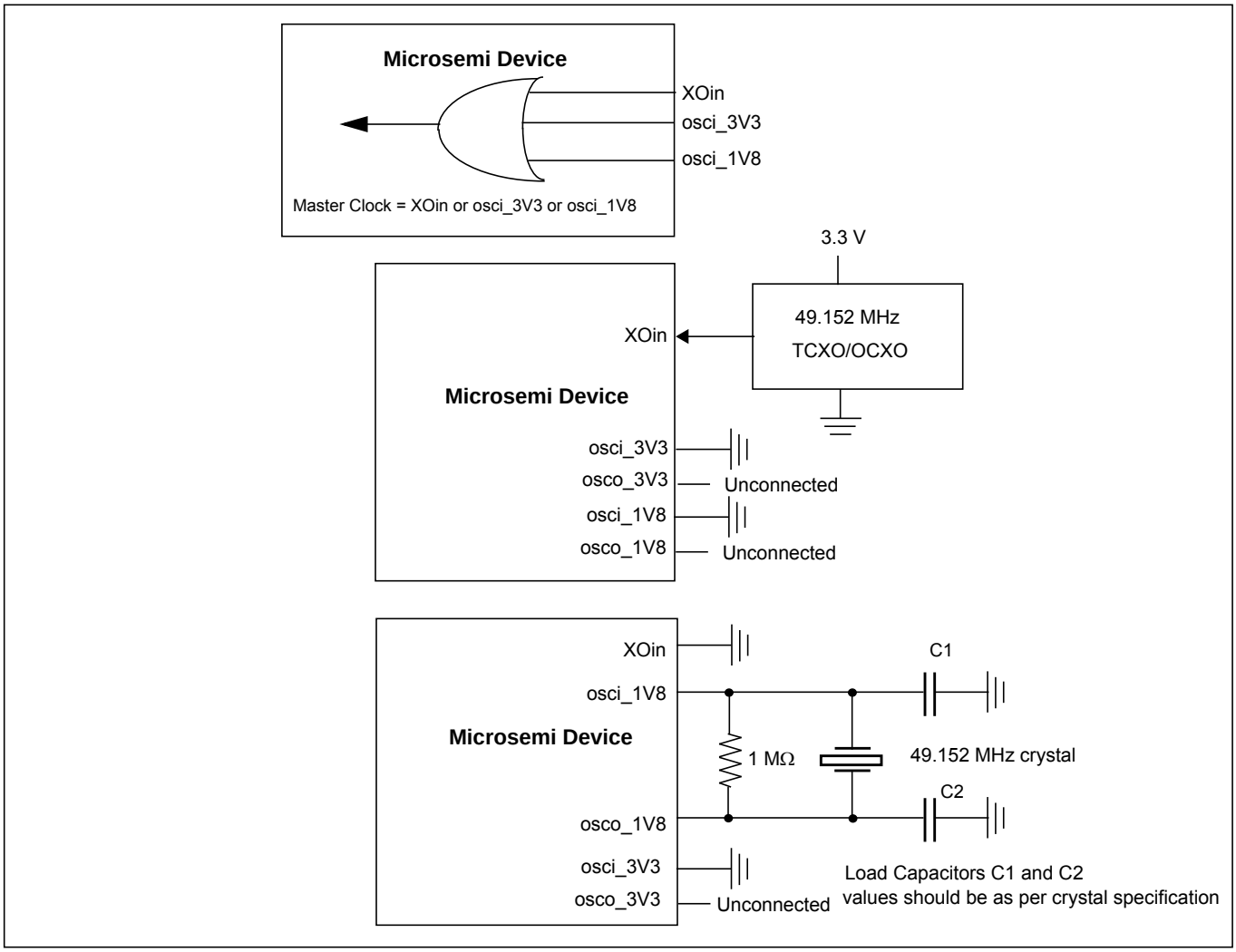


Figure 13 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (Oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the GPIO [1:0] pins, right after **pwr_b** gets de-asserted. The GPIO[1:0] pins are required to be in desired configuration (high or low) for 125 ms after the de-assertion of **pwr_b**, and then they can be released and used as regular GPIOs. Alternatively, these pins can be pulled high or low with 1 kΩ resistors.

GPIO [1:0]	Master Clock Frequency
00	24.576 MHz
01	49.152 MHz
10	20 MHz
11	reserved

Table 4 - Master Clock Frequency Selection

4.10 Power Up/Down Sequence

The 3.3 V supply should be powered before or simultaneously with the 1.8 V supply. The 1.8 V supply must never be greater than the 3.3 V supply by more than 0.3 V.

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.11 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Microsemi Application Note ZLAN-327 (Please contact Microsemi).

4.12 Reset and Configuration Circuit

To ensure proper operation, the device must be reset by holding the **pwr_b** pin low for at least 2 ms after power-up when 3.3V and 1.8V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 14. This circuit provides approximately 2 ms of reset low time. The **pwr_b** input has Schmidt trigger properties to prevent level bouncing.

Microsemi recommends that the power-on reset (**pwr_b**) signal be controlled by an on-board reset circuit or by a commercially available voltage supervisory device. It may also be possible to use a standalone power-up RC reset circuit. It is important to note that this circuit works reasonably well for power-up as long as the power supply rise time is fast with respect to the RC time constant, which may not always be the case. It is the board designer's responsibility to ensure that the circuit is properly tuned to each power supply's specific situation. As an example, for the capacitor C of 1 µF, the resistor should be 10 kΩ or higher.

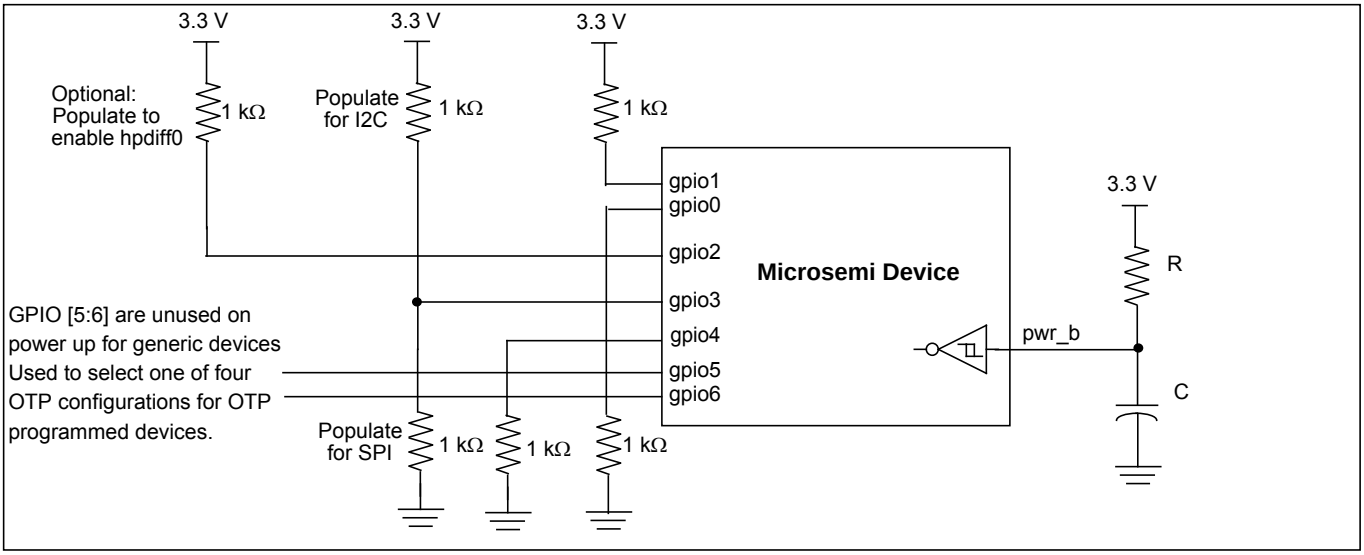


Figure 14 - Typical Power-Up Reset and Configuration Circuit

General purpose pins gpio[0,1,3,4,5,6] are used to configure device on power up. They have to be pulled up/down with 1 kΩ resistors as shown in Figure 14 or they can be held at the desired level for at least 125 ms after **pwr_b** goes high and then they can be released and used as general purpose I/O as described in Section 6.0.

By default all outputs are disabled to allow programing of required frequencies for different outputs and enabling corresponding outputs. During the prototype phase, hardware designer can verify if the device is working properly

even before software driver is implemented just by pulling up gpio2 pin which enables hpdiff0 output (generates 622.08 MHz by default).

4.13 OTN Demapper Clock Generation

The ZL30168 provides an extension of the DCO capabilities of the ClockCenter family of devices to allow an output clock to be controlled by the host processor based on the level of the buffer within an OTN demapper. The fill level of an internal buffer in the OTN demultiplexor will be communicated to the ZL30168 via SPI/I^2C. The DPLL will interpret these values as a stream of data similar to an input reference and filter the values with a selected bandwidth and other configured DPLL parameters.

5.0 Configuration and Control

5.1 ZL30168 Configuration programming

The ZL30168 configuration is composed of 768 x 8 bits. The configuration registers are assigned their values by any one of the following three methods:

1. Default Configuration
2. Custom OTP (One Time Programmable) configuration
3. SPI/I2C configuration

5.1.1 Default Configuration

At power-up the device sets its configuration registers to the default values.

5.1.2 Custom OTP Configuration

At power-up the device sets its configuration registers to the defined custom configuration values stored in its one time programmable memory. Custom configurations can be generated using Microsemi's ClockCenter+ GUI (ZLS30CCPLUS). Up to four unique custom configurations can be stored in the OTP memory and selected via GPIO pins 5,6 as follows:

GPIO 5	GPIO 6	Custom Configuration stored in slot
0	0	0
0	1	1
1	0	2
1	1	3

Table 5 - Custom Configuration power-up settings

For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.1.3 SPI/I2C Configuration

The SPI/I2C host interface allows field programmability of the device's configuration registers. As an example, the user might start the device at nominal SONET rate, then switch to an FEC rate once the link's FEC rate is negotiated. Configurations set via the SPI/I2C interface are volatile and will need to be re-written if the device is reset or powered down.

5.2 Registers Configuration

This section refers to configuration registers that are set by the user to control operation of the device.

5.2.1 Input Reference Configuration and Programmability

The following parameters can be configured for the reference input:

- Input reference frequency
- Default input reference selection

- Reference selection Priority
- Automatic or manual reference switching
- Glitch-less or hit-less reference switching
- Reference switch based on single cycle monitor, coarse frequency monitor, guard soak timer and precise frequency monitor.

5.2.2 DPLL Configuration and Programmability

The following parameters can be configured for each DPLL:

- Input reference
- Loop bandwidth
- Phase slope limiter
- Pull-in range

5.2.3 Output Multiplexer Configuration

The following parameter can be configured:

- Select which DPLL drives which Synthesizer

5.2.4 Synthesizer Configuration

The following parameters can be configured for each Synthesizer:

- Synthesizer can be configured to be locked to any DPLL, freerun or disabled
- Synthesizer frequency between 1 GHz and 1.5 GHz

5.2.5 Output Dividers and Output phase offset (skew) Configuration

The following parameters can be configured:

- Output divider enable/disable
- Divider ratio
- Output phase offset (fine and coarse)

5.2.6 Output Drivers Configuration

The following parameters can be configured:

- Output enable/disable
- Normal and low power mode

5.3 GPIO Configuration

The device GPIO is configured using the SPI/I^2C. The following is an example of control inputs and status reporting outputs that can be accomplished using the GPIOs:

Status Outputs

- DPLL lock indicators
- DPLL holdover indicators

- Reference 0 to 7 fail indicators
- Interrupt

Control Inputs

- Select DPLLs reference
- Reference 0 to 7 external Loss Of Signal (LOS) indication
- Enable/disable differential and single ended outputs
- Enable/disable TIE Clear
- Stop/start output clocks

The following table defines the functions of the GPIO pin when configured as a control input pin. Configuring the value in bit 6:0 in **gpio_function_pinX** register enables the desired function.

Value	Name	Description
Default		
0x00	Default	GPIO defined as an input. No function assigned.
Input References		
0x10	Ref0 external LOS signal	Ref0 external Loss Of Signal (LOS) - indicates to DPLLs that Ref0 has failed. This signal is used by DPLLs locked to Ref0 to do the reference switch or go to the holdover mode if another good reference is not available.
0x11	Ref1 external LOS signal	Same description as REF0 external LOS
0x12	Ref2 external LOS signal	Same description as REF0 external LOS
0x13	Ref3 external LOS signal	Same description as REF0 external LOS
0x14	Ref4 external LOS signal	Same description as REF0 external LOS
0x15	Ref5 external LOS signal	Same description as REF0 external LOS
0x16	Ref6 external LOS signal	Same description as REF0 external LOS
0x17	Ref7 external LOS signal	Same description as REF0 external LOS
DPLLs		
0x20	DPLL0 Time Interval Error (TIE) clear enable	This signal is OR-ed with the 'DPLL0 TIE clear enable' bit of the **dpllX_ctrl** register. The functionality of this signal is explained in the **dpllX_ctrl** register.
0x21	DPLL0 buffer-fill external LOS signal	When the GPIO is set and the DPLL is in buffer fill mode, the DPLL will go into holdover mode until this GPIO is reset.
0x28	DPLL1 Time Interval Error (TIE) clear enable	Same description as DPLL0 TIE clear enable
0x29	DPLL1 buffer-fill external LOS signal	Same description for DPLL1 external LOS signal
0x30	DPLL2 Time Interval Error (TIE) clear enable	Same description as DPLL0 TIE clear enable
0x31	DPLL2 buffer-fill external LOS signal	Same description for DPLL1 external LOS signal
0x38	DPLL3 Time Interval Error (TIE) clear enable	Same description as DPLL0 TIE clear enable

Value	Name	Description
0x39	DPLL3 buffer-fill external LOS signal	Same description for DPLL1 external LOS signal.
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer0 Post Divider C bit1	This signal is OR-ed with the 'Synthesizer0 Post Divider C stop clock' bit1 in the **synth1_0_stop_clk** register.
0x45	Stop output clock from Synthesizer0 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x46	Stop output clock from Synthesizer0 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x47	Stop output clock from Synthesizer0 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4C	Stop output clock from Synthesizer1 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4D	Stop output clock from Synthesizer1 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4E	Stop output clock from Synthesizer1 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x4F	Stop output clock from Synthesizer1 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x54	Stop output clock from Synthesizer2 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x55	Stop output clock from Synthesizer2 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x56	Stop output clock from Synthesizer2 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x57	Stop output clock from Synthesizer2 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5C	Stop output clock from Synthesizer3 Post Divider C bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5D	Stop output clock from Synthesizer3 Post Divider C bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1

Value	Name	Description
0x5E	Stop output clock from Synthesizer3 Post Divider D bit1	Same description as Stop output clock Synthesizer0 Post Divider C bit1
0x5F	Stop output clock from Synthesizer3 Post Divider D bit0	Same description as Stop output clock Synthesizer0 Post Divider C bit1
High Performance Differential Outputs		
0x60	Enable Differential output HPDIFF0	This signal is OR-ed with the 'Enable HPDIFF0' bit in the **hp_diff_en** register. Functionality of this signal is explained in **hp_diff_en** register.
0x62	Enable Differential output HPDIFF1	Same description as Enable Differential output HPDIFF0
0x64	Enable Differential output HPDIFF2	Same description as Enable Differential output HPDIFF0
0x66	Enable Differential output HPDIFF3	Same description as Enable Differential output HPDIFF0
0x68	Enable Differential output HPDIFF4	Same description as Enable Differential output HPDIFF0
0x6A	Enable Differential output HPDIFF5	Same description as Enable Differential output HPDIFF0
0x6C	Enable Differential output HPDIFF6	Same description as Enable Differential output HPDIFF0
0x6E	Enable Differential output HPDIFF7	Same description as Enable Differential output HPDIFF0
High Performance CMOS Outputs		
0x70	Enable HPOUTCLK0	This signal is OR-ed with the 'Enable HPOUTCLK0' bit in the **hp_cmos_en** register.
0x72	Enable HPOUTCLK1	Same description as Enable HPOUTCLK0
0x74	Enable HPOUTCLK2	Same description as Enable HPOUTCLK0
0x76	Enable HPOUTCLK3	Same description as Enable HPOUTCLK0
0x78	Enable HPOUTCLK4	Same description as Enable HPOUTCLK0
0x7A	Enable HPOUTCLK5	Same description as Enable HPOUTCLK0
0x7C	Enable HPOUTCLK6	Same description as Enable HPOUTCLK0
0x7E	Enable HPOUTCLK7	Same description as Enable HPOUTCLK0

The following table defines the function of the GPIO pin when configured as a status output pin. Configuring the value in bit 6:0 in **gpio_function_pinX** registers enables the stated function.

Value	Name	Description
Interrupt		
0x80	Interrupt output signal	This bit will be high if the interrupt has been asserted.
Input Reference Status Indicators		

Value	Name	Description
0x88	Ref0 - Precise Frequency Measurement (PFM) failure	This bit will be set if Ref0 PFM indicator is active (see **pfm_limit_refX** register for PFM limits).
0x89	Ref0 Single Cycle Measurement (SCM) failure	This bit will be set if Ref0 SCM indicator is active (see **scm_cfm_limit_refX** register for SCM limits).
0x8A	Ref0 Coarse Frequency Measurement (CFM) failure	This bit will be set if Ref0 CFM indicator is active (see **scm_cfm_limit_refX** register for CFM limits).
0x8B	Ref0 Guard Soak Timer (GST) indicator	Ref0 Guard Soak Timer (GST) indicator
0x8C	Ref0 failure indicator	This bit will be set if either Ref0 external LOS signal is high, or Ref0 SCM, CFM or GST indicator is high, and appropriate mask bit in the 'Ref0 and Ref1 failure mask' register is set to 1 (not masked).
0x8D	Ref1 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0x8E	Ref1 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x8F	Ref1 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x90	Ref1 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x91	Ref1 failure indicator	Same description as for Ref0
0x92	Ref0 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0x93	Ref2 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x94	Ref2 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x95	Ref2 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x96	Ref2 failure indicator	Same description as for Ref0
0x97	Ref3 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0x98	Ref3 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x99	Ref3 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x9A	Ref3 Guard Soak Timer (GST) indicator	Same description as for Ref0
0x9B	Ref3 failure indicator	Same description as for Ref0

Value	Name	Description
0x9C	Ref3 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0x9D	Ref4 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0x9E	Ref4 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0x9F	Ref4 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xA0	Ref4 failure indicator	Same description as for Ref0
0xA1	Ref5 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xA2	Ref5 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xA3	Ref5 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xA4	Ref5 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xA5	Ref5 failure indicator	Same description as for Ref0
0xA6	Ref6 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xA7	Ref6 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xA8	Ref6 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xA9	Ref6 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xAA	Ref6 failure indicator	Same description as for Ref0
0xAB	Ref7 - Precise Frequency Measurement (PFM) failure	Same description as for Ref0
0xAC	Ref7 Single Cycle Measurement (SCM) failure	Same description as for Ref0
0xAD	Ref7 Coarse Frequency Measurement (CFM) failure	Same description as for Ref0
0xAE	Ref7 Guard Soak Timer (GST) indicator	Same description as for Ref0
0xAF	Ref7 failure indicator	Same description as for Ref0

Value	Name	Description
DPLL Status Indicators		
0xC0	DPLL0 Normal mode indicator	This bit will be set when DPLL0 is in normal locking mode (not holdover, not freerun)
0xC1	DPLL0 holdover mode indicator	This bit will be set when DPLL0 is in holdover mode
0xC2	DPLL0 used reference bit3	This bit in combination with DPLL0 ref sel bit2, bit1 and bit0 represents DPLL0 selected reference. Selection: bit3 bit2 bit1 bit0 0 0 0 0 = Ref0 0 0 0 1 = Ref1 0 0 1 0 = Ref2 0 0 1 1 = Ref3 0 1 0 0 = Ref4 0 1 0 1 = Ref5 0 1 1 0 = Ref6 0 1 1 1 = Ref7
0xC3	DPLL0 used reference bit2	See bit3 description
0xC4	DPLL0 used reference bit1	See bit3 description
0xC5	DPLL0 used reference bit0	See bit3 description
0xC6	DPLL0 phase memory hit	This bit will be set when DPLL0 phase is beyond selected phase memory limit (specified in the **phasemem_limit_refX** register).
0xC7	DPLL0 frequency range hit	This bit will be set when DPLL0 frequency is beyond pull-in/hold-in range limit, specified in the **dpllX_pullin_holdin** register
0xC8	DPLL0 phase slope limit	This bit will be set when DPLL0 frequency is beyond phase slope limit, specified in the **dpllX_ctrl** register
0xC9	DPLL0 Lock Indication 0	This bit will be set when DPLL0 phase error is less than 36 us during 10 s period.This bit can be selected for DPLL0 lock indicator.
0xCA	DPLL0 Lock Indication 1	This bit will be set when DPLL0 phase error is less than 1us during 1s period.This bit can be selected for DPLL0 lock indicator.
0xCB	DPLL0 Lock Indication 2	This bit will be set when DPLL0 phase error is less than 10us during 1s period.This bit can be selected for DPLL0 lock indicator.
0xCC	DPLL0 Lock Indication 3	This bit will be set when DPLL0 phase error is less than 10us during 10s period. This bit can be selected for DPLL0 lock indicator.
0xCD	DPLL0 Buffer Fill input reference failure Indication	This bit should only be used when DPLL0 is programmed to be in buffer-fill mode. It will be set when the DPLL0 LOS signal is asserted forcing DPLL0 to be in holdover mode and when the buffer-fill input reference fails the output failure criteria in the buffer-fill output frequency register.

Value	Name	Description
0xCE	DPLL0 Buffer Fill output reference failure Indication	This bit should only be used when DPLL0 is programmed to be in buffer-fill mode.It will be set when the DPLL0 LOS signal is NOT asserted (allowing DPLL0 to be in locking mode) and the buffer full input reference fails the output failure criteria specified in the buffer-fill output frequency register
0xD0	DPLL1 Normal mode indicator	Same description as for DPLL0
0xD1	DPLL1 holdover mode indicator	Same description as for DPLL0
0xD2	DPLL1 used reference bit3	Same description as for DPLL0
0xD3	DPLL1 used reference bit2	Same description as for DPLL0
0xD4	DPLL1 used reference bit1	Same description as for DPLL0
0xD5	DPLL1 used reference bit0	Same description as for DPLL0
0xD6	DPLL1 phase memory hit	Same description as for DPLL0
0xD7	DPLL1 frequency range hit	Same description as for DPLL0
0xD8	DPLL1 phase slope limit	Same description as for DPLL0
0xD9	DPLL1 Lock Indication 0	Same description as for DPLL0
0xDA	DPLL1 Lock Indication 1	Same description as for DPLL0
0xDB	DPLL1 Lock Indication 2	Same description as for DPLL0
0xDC	DPLL1 Lock Indication 3	Same description as for DPLL0
0xDD	DPLL1 Buffer Fill input reference failure Indication	Same description as for DPLL0
0xDE	DPLL1 Buffer Fill output reference failure Indication	Same description as for DPLL0
0xE0	DPLL2 Normal mode indicator	Same description as for DPLL0
0xE1	DPLL2 holdover mode indicator	Same description as for DPLL0
0xE2	DPLL2 used reference bit3	Same description as for DPLL0
0xE3	DPLL2 used reference bit2	Same description as for DPLL0
0xE4	DPLL2 used reference bit1	Same description as for DPLL0
0xE5	DPLL2 used reference bit0	Same description as for DPLL0
0xE6	DPLL2 phase memory hit	Same description as for DPLL0
0xE7	DPLL2 frequency range hit	Same description as for DPLL0
0xE8	DPLL2 phase slope limit	Same description as for DPLL0
0xE9	DPLL2 Lock Indication 0	Same description as for DPLL0
0xEA	DPLL2 Lock Indication 1	Same description as for DPLL0
0xEB	DPLL2 Lock Indication 2	Same description as for DPLL0

Value	Name	Description
0xEC	DPLL2 Lock Indication 3	Same description as for DPLL0
0xED	DPLL2 Buffer Fill input reference failure Indication	Same description as for DPLL0
0xEE	DPLL2 Buffer Fill output reference failure Indication	Same description as for DPLL0
0xF0	DPLL3 Normal mode indicator	Same description as for DPLL0
0xF1	DPLL3 holdover mode indicator	Same description as for DPLL0
0xF2	DPLL3 used reference bit3	Same description as for DPLL0
0xF3	DPLL3 used reference bit2	Same description as for DPLL0
0xF4	DPLL3 used reference bit1	Same description as for DPLL0
0xF5	DPLL3 used reference bit0	Same description as for DPLL0
0xF6	DPLL3 phase memory hit	Same description as for DPLL0
0xF7	DPLL3 frequency range hit	Same description as for DPLL0
0xF8	DPLL3 phase slope limit	Same description as for DPLL0
0xF9	DPLL3 Lock Indication 0	Same description as for DPLL0
0xFA	DPLL3 Lock Indication 1	Same description as for DPLL0
0xFB	DPLL3 Lock Indication 2	Same description as for DPLL0
0xFC	DPLL3 Lock Indication 3	Same description as for DPLL0
0xFD	DPLL3 Buffer Fill input reference failure Indication	Same description as for DPLL0
0xFE	DPLL3 Buffer Fill output reference failure Indication	Same description as for DPLL0

5.3.1 GPIO Indication and Control Functionality

The devices includes registers to control the GPIO pins directly using **gpio_in_6_0**, **gpio_out_6_0** and **gpio_out_en_6_0**. These registers are used with the **gpio_function_pin*x*** registers.

To read a GPIO:

- Set the **gpio_function_pin*x*** to 0x00 (control, no function assigned)
- Set the bit for the pin in **gpio_out_en_6_0** to 0
- Read the current GPIO value in **gpio_in_6_0**

To set a GPIO:

- Set the **gpio_function_pin*x*** to 0x00 (control, no function assigned)
- Set the bit for the pin in **gpio_out_en_6_0** to 1

The value in **gpio_out_6_0** for the GPIO is driven on the GPIO pin

5.4 State Control and Reference Switch Modes

In un-managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is automatically set by the internal state machine of the device. It is based on availability of a valid reference and on the reference's selection priority.

In managed mode of operation, the DPLL state (normal, freerun and holdover) and the selected reference is manually set by the user.

The device allows for a smooth transition from in and out of the two modes of operation. Hence if the DPLL was in managed mode, for example locked to Ref2 reference and switched to un-managed mode of operation, then the state machine continues managing the DPLL, locked to the Ref2 and it will not force reference switching to any other reference unless a change in the Ref2 input conditions occurs that necessitate a change to an alternate input reference.

Each DPLL has its own independent state control and reference selection state machine.

5.4.1 Un-managed Mode

The un-managed mode combines the functionality of the normal state with automatic holdover and automatic reference switching. In this mode, transitioning from one mode to the other is controlled by the device internal state machine.

The on-chip state machine monitors the DPLL status bits, and based on the status information the state machine makes a decision to force holdover or to perform reference switch.

The reference switching state machine is based on the internal clock monitoring of each of the available input references and their priorities.

The state machine selects a reference source based on its priority value defined in a control register and the current availability of the reference. If all the references are available, the reference with the highest priority is selected; if this reference fails, the next highest priority reference is selected, and so on.

In un-managed mode, the state machine only reacts to reference failure indicators and performs reference switching anytime one of the following conditions takes place assuming they are not masked with their corresponding mask bits:

- LOS detected a failure and refswitch mask LOS is at logic “1”
- SCM detected a failure and refswitch mask SCM is at logic “1”
- CFM detected a failure and refswitch mask CFM is at logic “1"
- PFM detected a failure and refswitch mask PFM is at logic “1"
- GST is triggered and refswitch mask GST is at logic “1"

In un-managed mode, the device automatically selects a valid reference input. If the current reference used for synchronization fails, the state machine switches to another available reference. If all the available references fail, then the device enters the holdover mode under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"

In un-managed mode of operation, the state machine automatically recovers from holdover when the conditions to enter auto-holdover are not present.

The reference selection is based on reference priority. The current active reference for each DPLL can be read from DPLLx Reference Selection Status register.

Reference Priority

Every reference is assigned a priority value (0 to 7) to allow system designers to specify the priority of each input reference. The priorities are relative to each other, with lower value numbers being the higher priority. Value “1111" disables the ability to select the reference (i.e., don’t use for synchronization). If two or more inputs are given the same priority number, the input is selected based on the reference naming convention (i.e., ref0 is higher priority than ref1). The default reference selection priority is equal to its reference number (i.e., ref0 is highest priority and ref7 is the lowest priority).

When two references have the same priority they will not revert to each other (as reference availability change), but they will revert to a reference with a higher priority when it is available.

5.4.2 Managed (Manual) Mode

In managed mode, the device does not auto-select between different reference inputs. The user specifies which reference to use for synchronization and if it fails the DPLL enters the auto-holdover mode without switching to another reference.

The user (external uP) monitors the device status bits. Based on the status information, the user makes a decision to force holdover or to perform reference switch. In managed mode the active reference input is selected based on reference selection control bits. If the user sets the device to lock to a failed reference, the device stays in auto-holdover and only locks to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"

The state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

Time critical transitions for entry into auto-holdover and exit from auto-holdover are managed by the internal state machine. A change of the reference select bits triggers an internal state transition into auto-holdover and then an exit into Normal state and locking to the new reference.

6.0 Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or an I^2C interface.

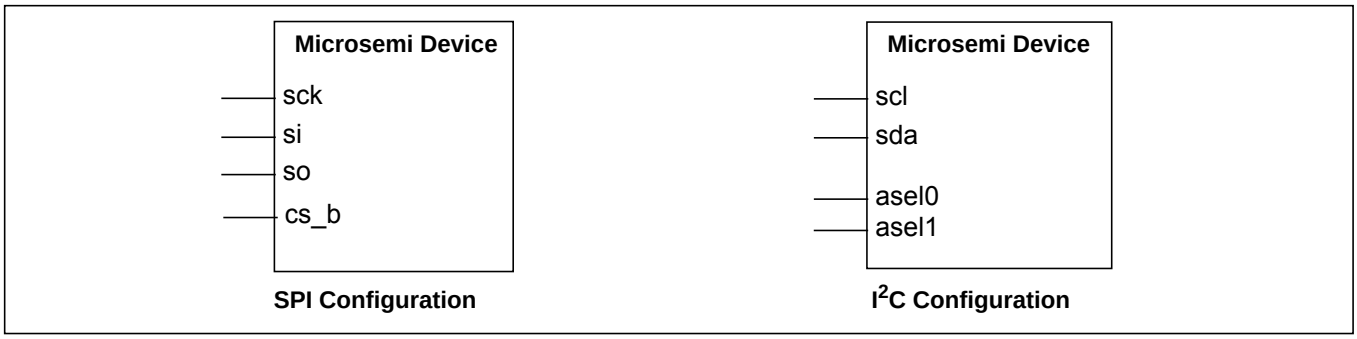


Figure 15 - Serial Interface Configuration

The selection between I^2C and SPI interfaces is performed at start-up using GPIO[3] pin, as **pwr_b** gets de-asserted. The GPIO[3] pin needs to be held at required level for 125 ms after the de-assertion of **pwr_b**, after which time they can be released and used as regular GPIO.

GPIO[3]	Serial Interface
0	SPI
1	I^2C

Table 6 - Serial Interface Selection

Both interfaces use seven bit address field and the device has eight bit address space. Hence, the device register space is divided in five pages of 127 registers each. Page 0 has addresses 0x000 to 0x07E and Page 1 with addresses 0x080 to 0x0FF and so on until page 5 which has addresses 0x200 to 0x27E. The host selects between the pages by writing to the Page Select register (address 0x7F or 0xFF on each page). e.g. writing a 0x03 to the page select register makes registers 0x180 to 0x1FF available through the host interface.

6.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the device internal registers that are used to configure, read status, and allow manual control of the device.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **so_asel1** pin must be ignored. Similarly, the input data on the **si_sda** pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **sck_scl** pin when the **cs_b_asel0** pin is active. If the **sck_scl** pin is low during **cs_b_asel0** activation, then MSb first timing is selected. If the **sck_scl** pin is high during **cs_b_asel0** activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **cs_b_asel0** pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **cs_b_asel0** is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 16, Figure 17 and Figure 18. Timing characteristics are shown in Table 8, Figure 30, and Figure 31.

6.1.1 Least Significant Bit (LSb) First Transmission Mode

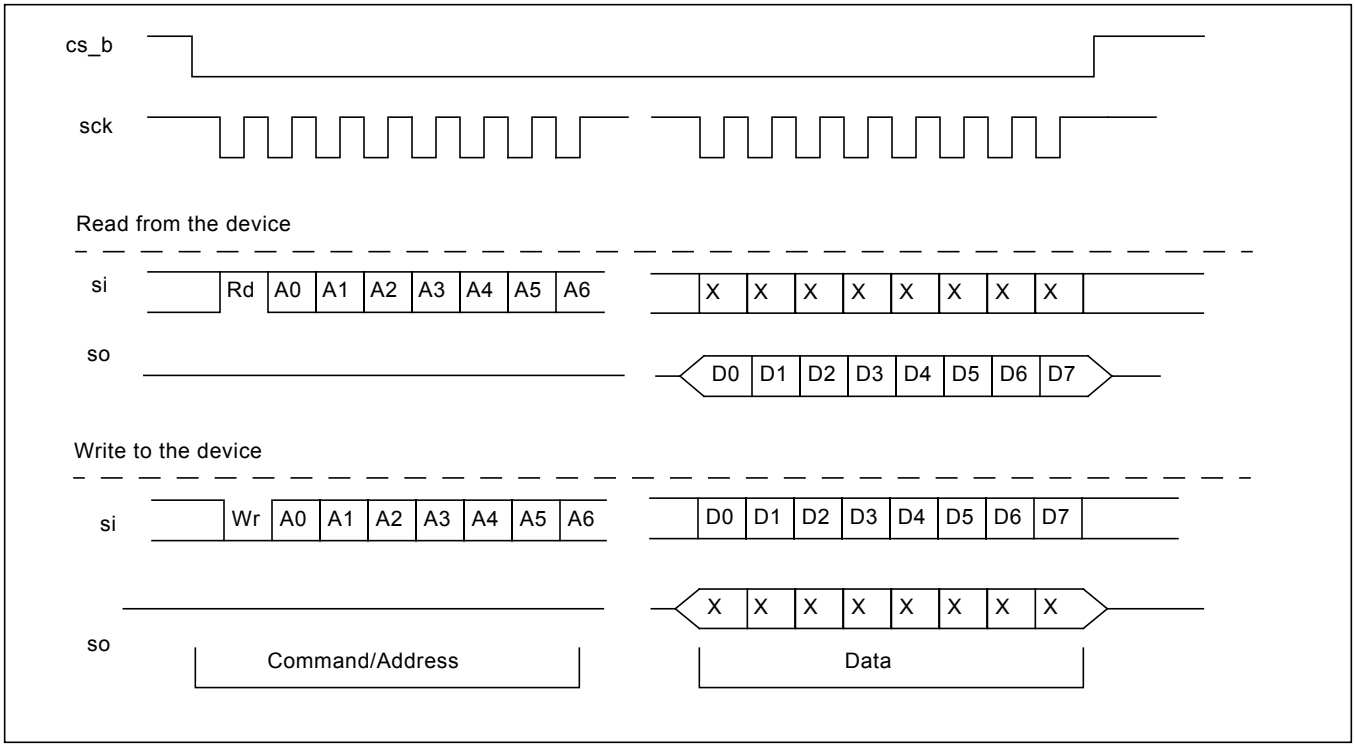


Figure 16 - Serial Peripheral Interface Functional Waveforms - LSb First Mode

6.1.2 Most Significant Bit (MSb) First Transmission Mode

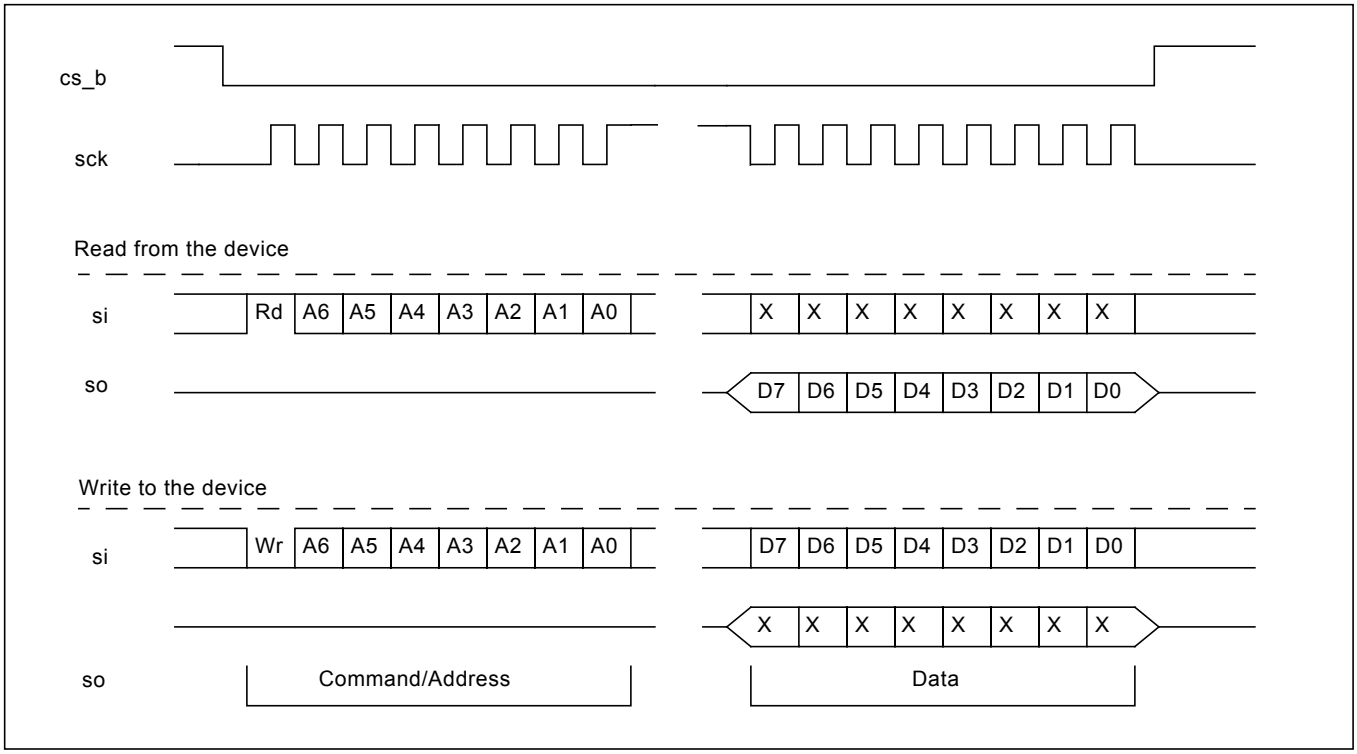


Figure 17 - Serial Peripheral Interface Functional Waveforms - MSb First Mode

6.1.3 SPI Burst Mode Operation

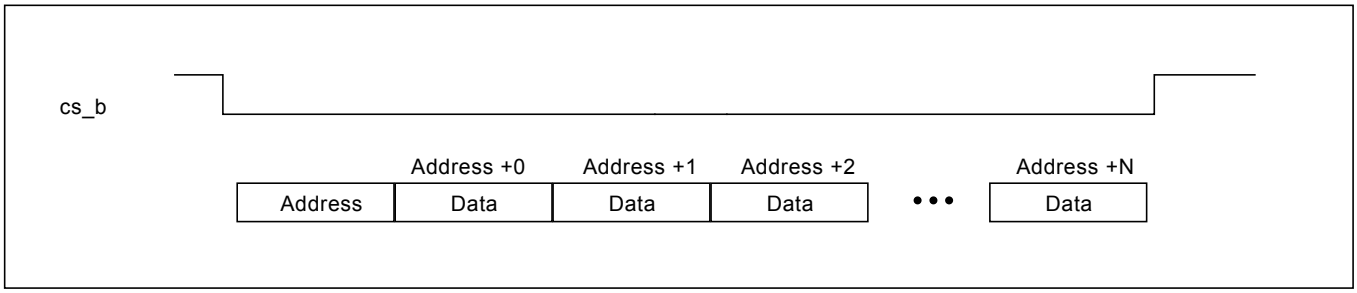


Figure 18 - Example of a Burst Mode Operation

6.2 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSb first and occurs in 1 byte blocks. As shown in Figure 19, a write command consists of a 7-bit device (slave) address, a R/W indicator bit, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

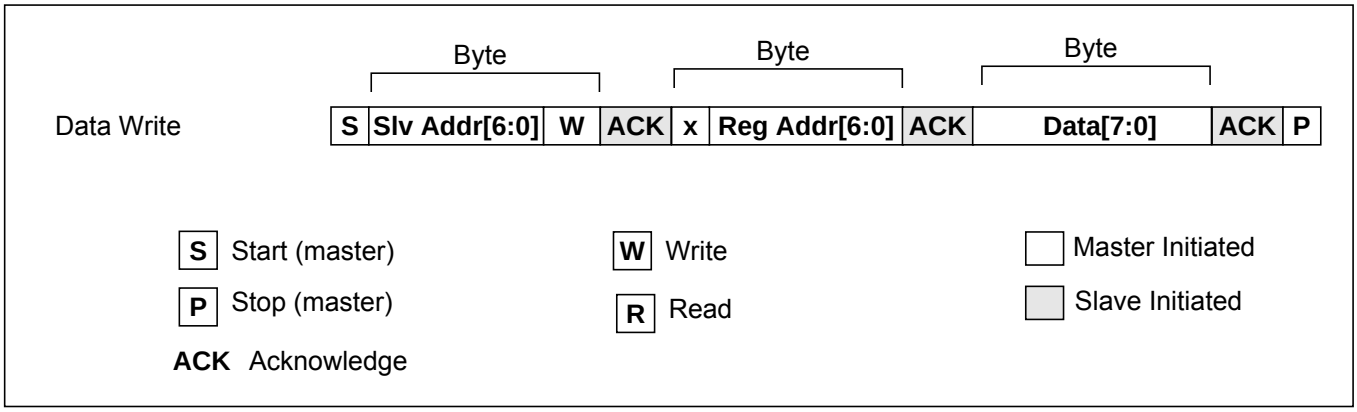


Figure 19 - I²C Data Write Protocol

A read is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 20.

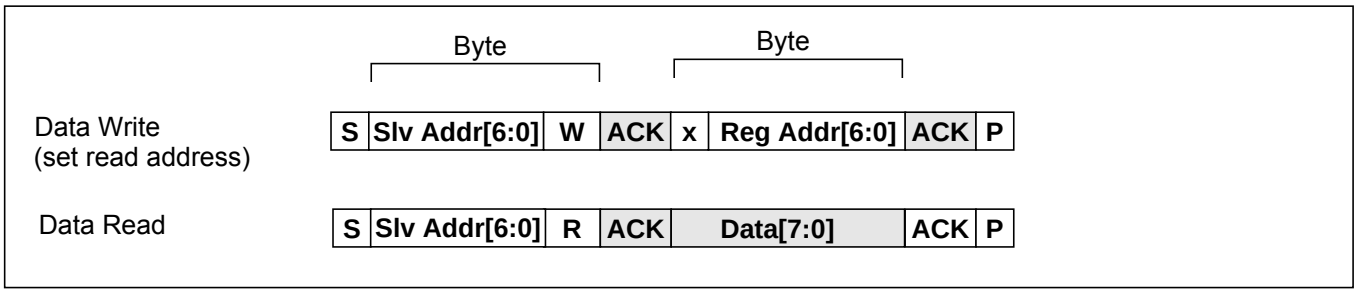


Figure 20 - I²C Data Read Protocol

The 7-bit device (slave) address contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple ZL30168s to share the same I^{2}C bus. The address configuration is shown in Figure 21.

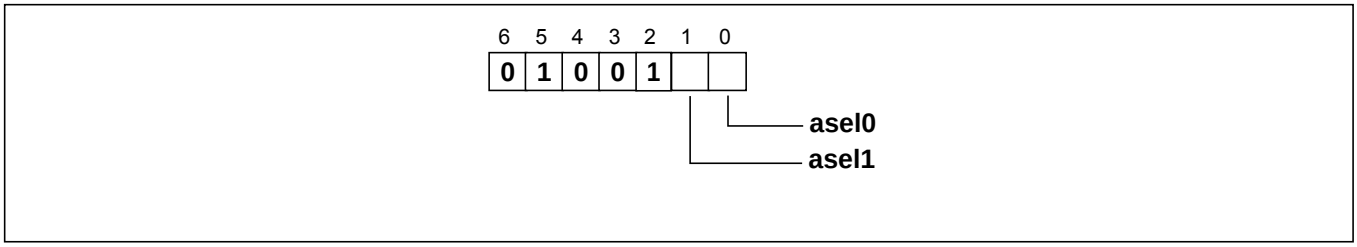


Figure 21 - I^{2}C 7-bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 22 (write) and Figure 23 (read). The first data byte is written/read to/from the specified address, and subsequent data bytes are written/read using an automatically increment address. The maximum auto increment address of a burst operation is 0x7F and operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

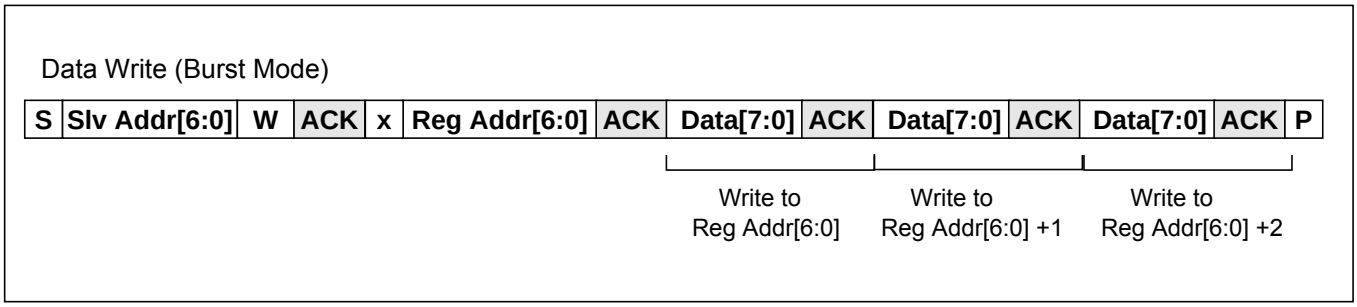


Figure 22 - I^{2}C Data Write Burst Mode

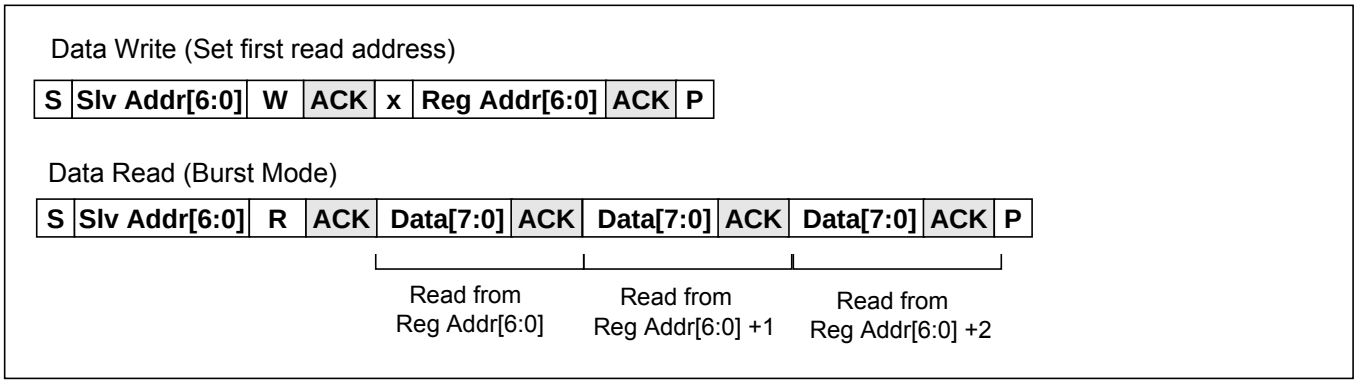


Figure 23 - I^{2}C Data Read Burst Mode

7.0 Register Map

The device is controlled by accessing registers through the serial interface (SPI or I^2C). The device can be configured to operate in un-managed (automatic) mode which minimizes its interaction with the system's processor, or it can operate in a managed (manual) mode where the system processor controls operation of the device.

A simple way to generate configuration for the device is to use the evaluation board GUI which can operate standalone (without the evaluation board). Through the GUI the user can quickly set all required parameters and save the configuration to a text file which can then be used by the system processor to load and configure the device.

Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits are spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 24. When writing a multi-byte value, the value is latched when the LSB is written.

Example:
The input reference M and N 16 are bit values defining the M/N ratio is programmed using a 32-bit value which is spread over four 8-bit registers. The MSB is contained in address 0x1BC and the LSB in 0x1BF When reading or writing this multi-byte value, the MSB must be accessed first, then the middle bytes, and the LSB last.

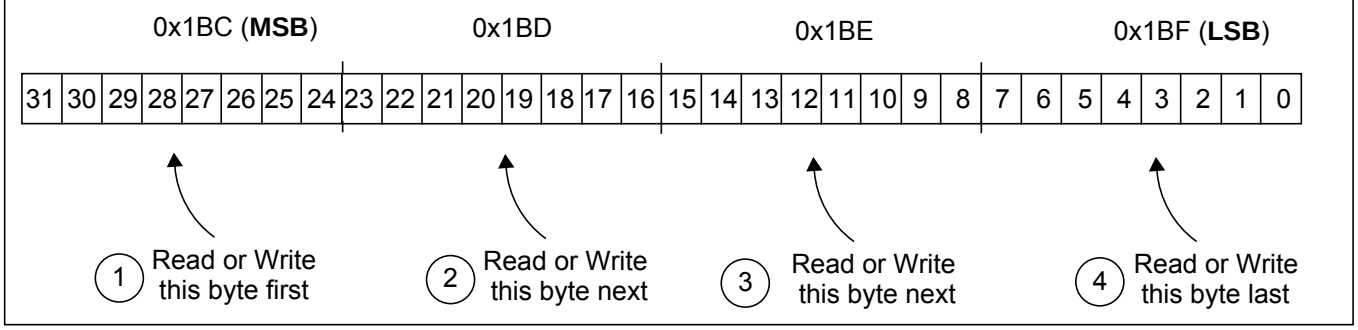


Figure 24 - Accessing Multi-byte Register Values

Time between two write accesses to the same register

- User should wait at least 25 ms between two write accesses to the same register
  - The **dpll*n*_df_offset** registers can be written with a minimum wait time of 300 microseconds between write accesses to the same register.
- For the page selection register (at addresses 0x07F, 0x0FF, 0x17F, 0x1FF, 0x27F and 0x2FF), there is no waiting time required between write accesses.

Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers without Interrupt Handler

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-write 0x01 to Sticky Lock Register at address 0x011

-clear status register(s) by writing 0x00 to it

-write 0x00 to StickyR Lock Register at address 0x011

-wait for 25 ms

-read the status register(s)

Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers when using an Interrupt Handler (event or polling)

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-host receives IRQ event or poll timer expiry

-disable the CPU IRQ

-write 0x01 to Sticky Lock Register at address 0x011

-read status register(s) (Sticky Status since the last IRQ)

-clear status register(s) by writing 0x00 to it

-write 0x00 to StickyR Lock Register at address 0x011

-exit IRQ handler or IRQ poll routine

-Re-enable the CPU IRQ

-next update to status will not occur for up to another 25 ms

-wait for IRQ event or poll timer expiry

The following table provides a summary of the registers available for status and configuration of the device. Devices with a custom OTP configuration will power-up with the custom configuration values instead of the default values.

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Miscellaneous Registers				
0x000	ready	0x1F	Ready Indicator register	R
0x001	id_reg	0x14	Chip ID Register	R
0x002	hw_rev_reg	0x04	Chip Hardware Revision register	R
0x00B:0x00E	central_freq_offset	0x046AAAAB	Central frequency offset	R/W
0x010	spurs supression	0x00	Spurs supression	R/W
0x011	sticky_lock	0x00	Sticky Lock Register	R/W
Input Reference Monitoring and DPLL Status				
0x020	ref_fail_isr_status_7_0	0x00	Reference failure interrupt status register for Ref 7:0	StickyR/W
0x022	dpll_isr_status	0x00	DPLL interrupt status register	StickyR/W
0x023	ref_fail_isr_mask_7_0	0x00	Reference failure interrupt mask register fro Ref 7:0	R/W
0x025	dpll_isr_mask	0x00	DPLL interrupt status register	R/W
0x026	ref_mon_fail_0	0x00	Reference 0 Failure Indicators	StickyR/W
0x027	ref_mon_fail_1	0x00	Reference 1 Failure Indicators	StickyR/W
0x028	ref_mon_fail_2	0x00	Reference 2 Failure Indicators	StickyR/W
0x029	ref_mon_fail_3	0x00	Reference 3 Failure Indicators	StickyR/W
0x02A	ref_mon_fail_4	0x00	Reference 4 Failure Indicators	StickyR/W
0x02B	ref_mon_fail_5	0x00	Reference 5 Failure Indicators	StickyR/W
0x02C	ref_mon_fail_6	0x00	Reference 6 Failure Indicators	StickyR/W
0x02D	ref_mon_fail_7	0x00	Reference 7 Failure Indicators	StickyR/W
0x036	ref_mon_fail_mask_0	0x16	Reference 0 Failure Masks	R/W
0x037	ref_mon_fail_mask_1	0x16	Reference 1 Failure Masks	R/W
0x038	ref_mon_fail_mask_2	0x16	Reference 2 Failure Masks	R/W
0x039	ref_mon_fail_mask_3	0x16	Reference 3 Failure Masks	R/W
0x03A	ref_mon_fail_mask_4	0x16	Reference 4 Failure Masks	R/W

Table 7 - Register Map

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x03B	ref_mon_fail_mask_5	0x16	Reference 5 Failure Masks	R/W
0x03C	ref_mon_fail_mask_6	0x16	Reference 6 Failure Masks	R/W
0x03D	ref_mon_fail_mask_7	0x16	Reference 7 Failure Masks	R/W
0x046	gst_disqualif_time_3_0	0xAA	Guard soak timer (GST) disqualify time selection for Ref3:0	R/W
0x047	gst_disqualif_time_7_4	0xAA	Guard soak timer (GST) disqualify time selection for Ref7:4	R/W
0x04A	gst_qualif_time_3_0	0x55	Guard soak timer (GST) qualify time selection for Ref 3:0	R/W
0x04B	gst_qualif_time_7_4	0x55	Guard soak timer (GST) qualify time selection for Ref 7:4	R/W
0x050	scm_cfm_limit_ref0	0x55	SCM and CFM limits for Reference 0	R/W
0x051	scm_cfm_limit_ref1	0x55	SCM and CFM limits for Reference 1	R/W
0x052	scm_cfm_limit_ref2	0x55	SCM and CFM limits for Reference 2	R/W
0x053	scm_cfm_limit_ref3	0x55	SCM and CFM limits for Reference 3	R/W
0x054	scm_cfm_limit_ref4	0x55	SCM and CFM limits for Reference 4	R/W
0x055	scm_cfm_limit_ref5	0x55	SCM and CFM limits for Reference 5	R/W
0x056	scm_cfm_limit_ref6	0x55	SCM and CFM limits for Reference 6	R/W
0x057	scm_cfm_limit_ref7	0x55	SCM and CFM limits for Reference 7	R/W
0x060	pfm_limit_ref1_0	0x33	PFM limits for References 1 and 0	R/W
0x061	pfm_limit_ref3_2	0x33	PFM limits for References 3 and 2	R/W
0x062	pfm_limit_ref5_4	0x33	PFM limits for References 5 and 4	R/W
0x063	pfm_limit_ref7_6	0x33	PFM limits for Reference 7 and 6	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x068	phase_acq_en_7_0	0xFF	Phase Acquisition enable for Acq7:0	R/W
0x06A	phasemem_limit_ref0	0x1B	Phase memory limit for Reference 0	R/W
0x06B	phasemem_limit_ref1	0x1B	Phase memory limit for Reference 1	R/W
0x06C	phasemem_limit_ref2	0x1B	Phase memory limit for Reference 2	R/W
0x06D	phasemem_limit_ref3	0x1B	Phase memory limit for Reference 3	R/W
0x06E	phasemem_limit_ref4	0x1B	Phase memory limit for Reference 4	R/W
0x06F	phasemem_limit_ref5	0x1B	Phase memory limit for Reference 5	R/W
0x070	phasemem_limit_ref6	0x1B	Phase memory limit for Reference 6	R/W
0x071	phasemem_limit_ref7	0x1B	Phase memory limit for Reference 7	R/W
0x07A	ref_config_7_0	0x00	Reference configuration register for References 7 to 0	R/W
0x07C	ref_pre_divide_7_0	0x00	Reference predivider control register for Ref7:0	R/W
Additional Miscellaneous Configuration				
0x07F	page_sel_register	0x00	SPI Page Selection Register	R/W
Input Frequency Configuration				
0x080:0x081	ref0_base_freq	0x9C40	Ref0 base frequency Br0	R/W
0x082:0x083	ref0_freq_multiple	0x0F30	Ref0 base frequency multiple Kr0	R/W
0x084:0x087	ref0_ratio_M_N	0x00010001	Ref0 Forward Error Correction (FEC) multiplication ratio Mr0 / Nr0 (numerator Mr0 and denominator Nr0 values)	R/W
0x088:0x089	ref1_base_freq	0x9C40	Ref1 base frequency Br1	R/W
0x08A:0x08B	ref1_freq_multiple	0x01E6	Ref1 base frequency multiple Kr1	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x08C:0x08F	ref1_ratio_M/N	0x00010001	Ref1 Forward Error Correction (FEC) multiplication ratio Mr1/ Nr1	R/W
0x090:0x091	ref2_base_freq	0x9C40	Ref2 base frequency Br2	R/W
0x092:0x093	ref2_freq_multiple	0x01E6	Ref2 base frequency multiple Kr2	R/W
0x094:0x097	ref2_ratio_M/N	0x00010001	Ref2 Forward Error Correction (FEC) multiplication ratio Mr2 / Nr2	R/W
0x098:0x099	ref3_base_freq	0x9C40	Ref3 base frequency Br3	R/W
0x09A:0x09B	ref3_freq_multiple	0x01E6	Ref3 base frequency multiple Kr3	R/W
0x09C:0x09F	ref3_ratio_M/N	0x00010001	Ref3 Forward Error Correction (FEC) multiplication ratio Mr3 / Nr3	R/W
0x0A0:0x0A1	ref4_base_freq	0x9C40	Ref4 base frequency Br4	R/W
0x0A2:0x0A3	ref4_freq_multiple	0x01E6	Ref4 base frequency multiple Kr4	R/W
0x0A4:0x0A7	ref4_ratio_M/N	0x00010001	Ref4 Forward Error Correction (FEC) multiplication ratio Mr4 / Nr4	R/W
0x0A8:0x0A9	ref5_base_freq	0x9C40	Ref5 base frequency Br5	R/W
0x0AA:0x0AB	ref5_freq_multiple	0x01E6	Ref5 base frequency multiple Kr5	R/W
0x0AC:0x0AF	ref5_ratio_M/N	0x00010001	Ref5 Forward Error Correction (FEC) multiplication ratio Mr5 / Nr5	R/W
0x0B0:0x0B1	ref6_base_freq	0x9C40	Ref6 base frequency Br6	R/W
0x0B2:0x0B3	ref6_freq_multiple	0x01E6	Ref6 base frequency multiple Kr6	R/W
0x0B4:0x0B7	ref6_ratio_M/N	0x00010001	Ref6 Forward Error Correction (FEC) multiplication ratio Mr6 / Nr6	R/W
0x0B8:0x0B9	ref7_base_freq	0x9C40	Ref7 base frequency Br7	R/W
0x0BA:0x0BB	ref7_freq_multiple	0x01E6	Ref7 base frequency multiple Kr7	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x0BC:0x0BF	ref7_ratio_M/N	0x00010001	Ref7 Forward Error Correction (FEC) multiplication ratio Mr7 / Nr7	R/W
0x0FF	page_sel_register	0x00	SPI Page Selection register	R/W
DPLL Configuration Registers				
0x100	dpll0_ctrl	0x0C	DPLL0 Control register	R/W
0x101	dpll0_var_bw_sel	0x00	DPLL0 variable bandwidth selection	R/W
0x102	dpll0_pull_in_hold_in	0x00	DPLL0 Pull-in Hold-in selection register	R/W
0x103	dpll0_mode_refsel	0x03	DPLL0 mode and reference selection	R/W
0x104	dpll0_refsel_stat	0x00	DPLL0 reference selection status	R
0x105	dpll0_ref_priority1_0	0x10	DPLL0 reference 1 and 0 selection priority	R/W
0x106	dpll0_ref_priority_3_2	0x32	DPLL0 reference 3 and 2 selection priority	R/W
0x107	dpll0_ref_priority_5_4	0x54	DPLL0 reference 5 and 4 selection priority	R/W
0x108	dpll0_ref_priority_7_6	0x76	DPLL0 reference 7 and 6 selection priority	R/W
0x10D	dpll0_ref_fail_mask	0x87	DPLL0 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x10E	dpll0_pfm_fail_mask	0x01	DPLL0 reference failure mask based on PFM failure indicator (used for automatic reference switching and automatic holdover)	R/W
0x10F	dpll0_ho_edge_sel	0x0B	DPLL0 Holdover Storage Delay and Reference Edge Selection register	R/W
0x119	dpll0_damping_ctrl	0x05	DPLL0 Damping Control	R/W
0x11B:0x11E	dpll0_buff_ptr_diff	0x00	DPLL0 Buffer Fill Level	R/W
0x120	dpll1_ctrl	0x0C	DPLL1 Control register	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x121	dpll1_var_bw_sel	0x00	DPLL1 variable bandwidth selection	R/W
0x122	dpll1_pull_in_hold_in	0x00	DPLL1 Pull-in Hold-in selection register	R/W
0x123	dpll1_mode_refsel	0x03	DPLL1 mode and reference selection	R/W
0x124	dpll1_refsel_stat	0x00	DPLL1 reference selection status	R
0x125	dpll1_ref_priority_1_0	0x10	DPLL1 reference 1 and 0 selection priority	R/W
0x126	dpll1_ref_priority_3_2	0x32	DPLL1 reference 3 and 2 selection priority	R/W
0x127	dpll1_ref_priority_5_4	0x54	DPLL1 reference 5 and 4 selection priority	R/W
0x128	dpll1_ref_priority_7_6	0x76	DPLL1 reference 7 and 6 selection priority	R/W
0x12D	dpll1_ref_fail_mask	0x87	DPLL1 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x12E	dpll1_pfm_fail_mask	0x01	DPLL1 reference failure mask based on PFM failure indicator (used for automatic reference switching and automatic holdover)	R/W
0x12F	dpll1_ho_edge_sel	0x0B	DPLL1 Holdover Storage Delay and Reference Edge Selection register	R/W
0x139	dpll1_damping_ctrl	0x05	DPLL1 Damping Control	R/W
0x13B:0x13E	dpll1_buff_ptr_diff	0x00	DPLL1 Buffer Fill Level	R/W
0x140	dpll2_ctrl	0x0C	DPLL2 Control register	R/W
0x141	dpll2_var_bw_sel	0x00	DPLL2 variable bandwidth selection	R/W
0x142	dpll2_pull_in_hold_in	0x00	DPLL2 Pull-in Hold-in selection register	R/W
0x143	dpll2_mode_refsel	0x03	DPLL2 mode and reference selection	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x144	dpll2_refsel_stat	0x00	DPLL2 reference selection status	R
0x145	dpll2_ref_priority_1_0	0x10	DPLL2 reference 1 and 0 selection priority	R/W
0x146	dpll2_ref_priority_3_2	0x32	DPLL2 reference 3 and 2 selection priority	R/W
0x147	dpll2_ref_priority_5_4	0x54	DPLL2 reference 5 and 4 selection priority	R/W
0x148	dpll2_ref_priority_7_6	0x76	DPLL2 reference 7 and 6 selection priority	R/W
0x14D	dpll2_ref_fail_mask	0x87	DPLL2 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x14E	dpll2_pfm_fail_mask	0x01	DPLL2 reference failure mask based on PFM failure indicator (used for automatic reference switching and automatic holdover)	R/W
0x14F	dpll2_ho_edge_sel	0x0B	DPLL2 Holdover Storage Delay and Reference Edge Selection register	R/W
0x159	dpll2_damping_ctrl	0x05	DPLL2 Damping Control	R/W
0x15B:0x15E	dpll2_buff_ptr_diff	0x00	DPLL2 Buffer Fill Level	R/W
0x160	dpll3_ctrl	0x0C	DPLL3 Control register	R/W
0x161	dpll3_var_bw_sel	0x00	DPLL3 variable bandwidth selection	R/W
0x162	dpll3_pull_in_hold_in	0x00	DPLL3 Pull-in Hold-in selection register	R/W
0x163	dpll3_mode_refsel	0x03	DPLL3 mode and reference selection	R/W
0x164	dpll3_refsel_stat	0x00	DPLL3 reference selection status	R
0x165	dpll3_ref_priority_1_0	0x10	DPLL3 reference 1 and 0 selection priority	R/W
0x166	dpll3_ref_priority_3_2	0x32	DPLL3 reference 3 and 2 selection priority	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x167	dpll3_ref_priority_5_4	0x54	DPLL3 reference 5 and 4 selection priority	R/W
0x168	dpll3_ref_priority_7_6	0x76	DPLL3 reference 7 and 6 selection priority	R/W
0x16D	dpll3_ref_fail_mask	0x87	DPLL3 reference failure mask (used for automatic reference switching and automatic holdover)	R/W
0x16E	dpll3_pfm_fail_mask	0x01	Enables phase build out for DPLL3, resets the build out occurrence counter, and resets total phase build out accumulated phase	R/W
0x16F	dpll3_ho_edge_sel	0x0B	DPLL3 Holdover Storage Delay and Reference Edge Selection register	R/W
0x179	dpll3_damping_ctrl	0x05	DPLL3 Damping Control	R/W
0x17B:0x17E	dpll3_buff_ptr_diff	0x00	DPLL3 Buffer Fill Level	R/W
0x17F	page_sel_register	0x00	Page Selection register	R/W
0x180	dpll_hold_lock_status	0x00	DPLL Lock and holdover status	StickyR/W
0x181	ext_fb_ctrl	0x00	External Feedback Control	R/W
0x182	dpll_config	0x04	DPLL configuration register	R/W
0x183	dpll_lock_selection	0xAA	DPLL lock selection	R/W
DPLL Delta Frequency Registers				
0x18D:0x191	dpll0_df_offset	0x0000000000	DPLL0 Delta Frequency offset	W
0x192:0x196	dpll1_df_offset	0x0000000000	DPLL1 Delta Frequency offset	W
0x197:0x19B	dpll2_df_offset	0x0000000000	DPLL2 Delta Frequency offset	W
0x19C:0x1A0	dpll3_df_offset	0x0000000000	DPLL3 Delta Frequency offset	W
Output Synthesizer Configuration Registers				
0x1B0	synth_drive_pll	0xE4	DPLL to Synthesizer assignment selection	R/W
0x1B1	synth_enable	0x0F	Synthesizer Enable register	R/W
0x1B6	sync_fail_flag_status	0x00	Synthesizer APLL syncFailFlag status	R

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x1B7	clear_sync_fail_flag	0x00	Synthesizer APLL Clear sync-FailFlag	R/W
Output Reference Selection and Output Driver Control				
0x1B8:0x1B9	synth0_base_freq	0x9C40	Synthesizer0 base frequency Bs0	R/W
0x1BA:0x1BB	synth0_freq_multiple	0x0798	Synthesizer0 base frequency multiple Ks0	R/W
0x1BC:0x1BF	synth0_ratio_M_N	0x00010001	Synthesizer0 Forward Error Correction (FEC) multiplication ratio Ms0 / Ns0 (numerator Ms0 and denominator Ns0 values)	R/W
0x1C0:0x1C1	synth1_base_freq	0x61A8	Synthesizer1 base frequency Bs1	R/W
0x1C2:0x1C3	synth1_freq_multiple	0x0C35	Synthesizer1 base frequency multiple Ks1	R/W
0x1C4:0x1C7	synth1_ratio_M_N	0x00010001	Synthesizer1 Forward Error Correction (FEC) multiplication ratio Ms1 / Ns1 (numerator Ms1 and denominator Ns1 values)	R/W
0x1C8:0x1C9	synth2_base_freq	0x61A8	Synthesizer2 base frequency Bs2	R/W
0x1CA:0x1CB	synth2_freq_multiple	0x0C35	Synthesizer2 base frequency multiple Ks2	R/W
0x1CC:0x1CF	synth2_ratio_M_N	0x00010001	Synthesizer2 Forward Error Correction (FEC) multiplication ratio Ms2 / Ns2 (numerator Ms2 and denominator Ns2 values)	R/W
0x1D0:0x1D1	synth3_base_freq	0x9C40	Synthesizer3 base frequency Bs3	R/W
0x1D2:0x1D3	synth3_freq_multiple	0x0798	Synthesizer3 base frequency multiple Ks3	R/W
0x1D4:0x1D7	synth3_ratio_M_N	0x00010001	Synthesizer3 Forward Error Correction (FEC) multiplication ratio Ms3 / Ns3 (numerator Ms3 and denominator Ns3 values)	R/W
0x1FF	page_sel_register	0x00	SPI Page Selection register	R/W
0x200:0x202	synth0_post_div_A	0x000002	Synthesizer0 Post Divider A	R/W
0x203:0x205	synth0_post_div_B	0x000008	Synthesizer0 Post Divider B	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x206:0x208	synth0_post_div_C	0x000010	Synthesizer0 Post Divider C	R/W
0x209:0x20B	synth0_post_div_D	0x000040	Synthesizer0 Post Divider D	R/W
0x20C:0x20E	synth1_post_div_A	0x000002	Synthesizer1 Post Divider A	R/W
0x20F:0x211	synth1_post_div_B	0x000008	Synthesizer1 Post Divider B	R/W
0x212:0x214	synth1_post_div_C	0x00000A	Synthesizer1 Post Divider C	R/W
0x215:0x217	synth1_post_div_D	0x000032	Synthesizer1 Post Divider D	R/W
0x218:0x21A	synth2_post_div_A	0x000002	Synthesizer2 Post Divider A	R/W
0x21B:0x21D	synth2_post_div_B	0x000008	Synthesizer2 Post Divider B	R/W
0x21E:0x220	synth2_post_div_C	0x00000A	Synthesizer2 Post Divider C	R/W
0x221:0x223	synth2_post_div_D	0x000032	Synthesizer2 Post Divider D	R/W
0x224:0x226	synth3_post_div_A	0x000002	Synthesizer3 Post Divider A	R/W
0x227:0x229	synth3_post_div_B	0x000008	Synthesizer3 Post Divider B	R/W
0x22A:0x22C	synth3_post_div_C	0x000010	Synthesizer3 Post Divider C	R/W
0x22D:0x22F	synth3_post_div_D	0x000040	Synthesizer3 Post Divider D	R/W
0x234:0x235	phase_shift_s0_postdiv_c	0x0000	Synthesizer0 Post Divider C phase shift	R/W
0x236:0x237	phase_shift_s0_postdiv_d	0x0000	Synthesizer0 Post Divider D phase shift	R/W
0x23C:0x23D	phase_shift_s1_postdiv_c	0x0000	Synthesizer1 Post Divider C phase shift	R/W
0x23E:0x23F	phase_shift_s1_postdiv_d	0x0000	Synthesizer1 Post Divider D phase shift	R/W
0x244:0x245	phase_shift_s2_postdiv_c	0x0000	Synthesizer2 Post Divider C phase shift	R/W
0x246:0x247	phase_shift_s2_postdiv_d	0x0000	Synthesizer2 Post Divider D phase shift	R/W
0x24C:0x24D	phase_shift_s3_postdiv_c	0x0000	Synthesizer3 Post Divider C phase shift	R/W
0x24E:0x24F	phase_shift_s3_postdiv_d	0x0000	Synthesizer3 Post Divider D phase shift	R/W
0x250	synth0_fine_phase_shift	0x00	Synth0 fine phase shift (skew) in steps of VCO period over 256	R/W
0x251	synth1_fine_phase_shift	0x00	Synth1 fine phase shift (skew) in steps of VCO period over 256	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x252	synth2_fine_phase_shift	0x00	Synth2 fine phase shift (skew) in steps of VCO period over 256	R/W
0x253	synth3_fine_phase_shift	0x00	Synth3 fine phase shift (skew) in steps of VCO period over 256	R/W
0x254	synth1_0_stop_clk	0x00	Synthesizer0 and Synthesizer1 Post Dividers D and C stop clock	R/W
0x255	synth3_2_stop_clk	0x00	Synthesizer3 and Synthesizer2 Post Dividers D and C stop clock	R/W
0x261	hp_diff_en	0x00	High Performance Differential Output enable	R/W
0x262	hp_cmos_en	0x00	High Performance CMOS Output enable	R/W
GPIO Related Registers				
0x266	gpio_function_pin0	0x00	GPIO0 select or status	R/W
0x267	gpio_function_pin1	0x00	GPIO1 select or status	R/W
0x268	gpio_function_pin2	0x60	GPIO2 select or status	R/W
0x269	gpio_function_pin3	0x00	GPIO3 select or status	R/W
0x26A	gpio_function_pin4	0x00	GPIO4 select or status	R/W
0x26B	gpio_function_pin5	0x00	GPIO5 select or status	R/W
0x26C	gpio_function_pin6	0x00	GPIO6 select or status	R/W
0x276	gpio_in_6_0	0x00	GPIO6:0 Input Register	R
0x278	gpio_out_6_0	0x00	GPIO6:0 Output Register	R/W
0x27A	gpio_out_en_6_0	0x00	GPIO6:0 Output Enable Register	R/W
0x27C	gpio_latch_6_0	0x00	GPIO6:0 Latch Register	R
0x27E	buffer_fill_irq_status	0x00	Buffer-fill Frequency status	StickyR/W
0x27F	page_sel_register	0x00	SPI Page Selection Register	R/W
Buffer-fill Level Algorithm Control Registers				
0x280	dpll0_buff_fill_ctrl	0x96	DPLL0 Buffer Fill Control Register	R/W
0x281:0x284	dpll0_buff_fill_offs	0x00000100	DPLL0 Buffer Fill Offset Control	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x285	dpll0_ext_divider	0x02	DPLL0 Buffer Fill External Divider	R/W
0x286	dpll0_inp_freq_mon_limit	0x05	DPLL0 Buffer Fill Input Frequency Monitor Limit	R/W
0x287	dpll0_inp_freq_mon_time	0x07	DPLL0 Buffer Fill Input Frequency Monitor Time	R/W
0x288	dpll0_out_freq_mon_limit	0x0D	DPLL0 Buffer Fill Output Frequency Monitor Limit	R/W
0x289	dpll0_attenuation	0x00	DPLL0 Attenuation	R/W
0x28A	dpll0_err_polarity	0x00	DPLL0 Buffer Fill Phase error polarity	R/W
0x28B	dpll0_buf_fill_misc_ctrl	0x00	DPLL0 Buffer Fill Misc Control	R/W
0x28C	dpll0_buf_fill_misc_ctrl2	0x00	DPLL0 Buffer Fill Misc Control	R/W
0x290	dpll1_buff_fill_ctrl	0x96	DPLL1 Buffer Fill Control Register	R/W
0x291:0x294	dpll1_buff_fill_offs	0x00000100	DPLL1 Buffer Fill Offset Control	R/W
0x295	dpll1_ext_divider	0x02	DPLL1 Buffer Fill External Divider	R/W
0x296	dpll1_inp_freq_mon_limit	0x05	DPLL1 Buffer Fill Input Frequency Monitor Limit	R/W
0x297	dpll1_inp_freq_mon_time	0x07	DPLL1 Buffer Fill Input Frequency Monitor Time	R/W
0x298	dpll1_out_freq_mon_limit	0x0D	DPLL1 Buffer Fill Output Frequency Monitor Limit	R/W
0x299	dpll1_attenuation	0x00	DPLL1 Attenuation	R/W
0x29A	dpll1_err_polarity	0x00	DPLL1 Buffer Fill Phase error polarity	R/W
0x29B	dpll1_buf_fill_misc_ctrl	0x00	DPLL1 Buffer Fill Misc Control	R/W
0x29C	dpll1_buf_fill_misc_ctrl2	0x00	DPLL1 Buffer Fill Misc Control	R/W
0x2A0	dpll2_buff_fill_ctrl	0x96	DPLL2 Buffer Fill Control Register	R/W
0x2A1:0x2A4	dpll2_buff_fill_offs	0x00000100	DPLL2 Buffer Fill Offset Control	R/W
0x2A5	dpll2_ext_divider	0x02	DPLL2 Buffer Fill External Divider	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x2A6	dpll2_inp_freq_mon_limit	0x05	DPLL2 Buffer Fill Input Frequency Monitor Limit	R/W
0x2A7	dpll2_inp_freq_mon_time	0x07	DPLL2 Buffer Fill Input Frequency Monitor Time	R/W
0x2A8	dpll2_out_freq_mon_limit	0x0D	DPLL2 Buffer Fill Output Frequency Monitor Limit	R/W
0x2A9	dpll2_attenuation	0x00	DPLL2 Attenuation	R/W
0x2AA	dpll2_err_polarity	0x00	DPLL2 Buffer Fill Phase error polarity	R/W
0x2AB	dpll2_buf_fill_misc_ctrl	0x00	DPLL2 Buffer Fill Misc Control	R/W
0x2AC	dpll2_buf_fill_misc_ctrl2	0x00	DPLL2 Buffer Fill Misc Control	R/W
0x2B0	dpll3_buff_fill_ctrl	0x96	DPLL3 Buffer Fill Control Register	R/W
0x2B1:0x2B4	dpll3_buff_fill_offs	0x00000100	DPLL3 Buffer Fill Offset Control	R/W
0x2B5	dpll3_ext_divider	0x02	DPLL3 Buffer Fill External Divider	R/W
0x2B6	dpll3_inp_freq_mon_limit	0x05	DPLL3 Buffer Fill Input Frequency Monitor Limit	R/W
0x2B7	dpll3_inp_freq_mon_time	0x07	DPLL3 Buffer Fill Input Frequency Monitor Time	R/W
0x2B8	dpll3_out_freq_mon_limit	0x0D	DPLL3 Buffer Fill Output Frequency Monitor Limit	R/W
0x2B9	dpll3_attenuation	0x00	DPLL3 Attenuation	R/W
0x2BA	dpll3_err_polarity	0x00	DPLL3 Buffer Fill Phase error polarity	R/W
0x2BB	dpll3_buf_fill_misc_ctrl	0x00	DPLL3 Buffer Fill Misc Control	R/W
0x2BC	dpll3_buf_fill_misc_ctrl2	0x00	DPLL3 Buffer Fill Misc Control	R/W
Buffer-fill Level Algorithm Status Registers				
0x2C0	buff_fill_irq_mask	0x00	Buffer Fill Input and Output Mask	R/W
0x2C1	buff_fill_status	0x00	Buffer Fill Input and Output Status	StickyR/W
Additional DPLL Configuration Registers				
0x2C2	dpll0_fast_lock_ctrl	0x10	Controls fast lock in DPLL0	R/W

Table 7 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x2C5	dpll1_fast_lock_ctrl	0x10	Controls fast lock in DPLL1	R/W
0x2C8	dpll2_fast_lock_ctrl	0x10	Controls fast lock in DPLL2	R/W
0x2CB	dpll3_fast_lock_ctrl	0x10	Controls fast lock in DPLL3	R/W
0x2D4	dpll0_holdover_filt_ctrl	0x00	Holdover Filter Value	R/W
0x2D5	dpll1_holdover_filt_ctrl	0x00	Holdover Filter Value	R/W
0x2D6	dpll2_holdover_filt_ctrl	0x00	Holdover Filter Value	R/W
0x2D7	dpll3_holdover_filt_ctrl	0x00	Holdover Filter Value	R/W
0x2FF	page_sel_register	0x00	SPI Page Selection Register	R/W

Table 7 - Register Map (continued)

8.0 Detailed Register Map

Register_Address: **0x000** Register Name: **ready** Default Value: **0x1F** Type: **R**		
Bit Field	**Function Name**	**Description**
7	Ready indication	After reset this bit goes high when device is ready. This signals that user can start to program/configure the device.
6:5	Reserved	Leave as default
4:0	Chip family identification	Family Identification = 0b11111

Register_Address: **0x001** Register Name: **chip_id** Default Value: **0x14** Type: **R**		
Bit Field	**Function Name**	**Description**
7:0	Chip ID register	Chip id number: Unsigned binary value of these bits represent chip id number. Customer should not write to this register.

Register_Address: **0x002** Register Name: **hw_rev_reg** Default Value: **0x04** Type: **R**		
Bit Field	**Function Name**	**Description**
7:0	Chip Hardware Revision register	Chip hardware revision number: Unsigned binary value of these bits represent chip hardware revision number. Customer should not write to this register.

Register_Address: **0x00B:0x00E**
Register Name: **central_freq_offset**
Default Value: **0x046AAAAB**
Type: **R/W**

Bit Field	Function Name	Description
31:0	Central frequency offset	2's complement binary value of these bits represent central frequency offset for the device. This value should be used to compensate for oscillator inaccuracy. This register the controls central frequency of all 4 Synthesizers. Expressed in steps of +/- 2^-32 of nominal setting. When the oscillator inaccuracy is known: inacc_osc = (f_osc - f_nom)/f_nom (usually specified in ppm), value to be programmed in this register is calculated using the following formula: X = (1/(1 + inacc_osc) - 1)*2^32, when f_osc < f_nom X = (1/(1 + inacc_osc))*2^32, when f_osc > f_nom, where inacc_osc - represents oscillator frequency inaccuracy, f_osc - represents oscillator frequency, and f_nom - represents oscillator nominal frequency (i.e. 25MHz, 20MHz, 40MHz or 50MHz) Generally, when the oscillator frequency is lower than the nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1): if oscillator inaccuracy is -2% (f_osc = 24.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = -0.02), X= (1/(1+(-0.02)) - 1)*2^32 = (1/0.98 - 1)*2^32 = 87652394 = 0x0539782A Example 2): if oscillator inaccuracy is +2% (f_osc = 25.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = 0.02), X= (1/(1+ 0.02))*2^32 = (1/1.02)*2^32 = 4210752251 = 0xFAFAFAFB **Note 1:** The nominal frequency for central frequency offset calculation is 25 MHz. With the master clock frequency of 24.576 MHz this register should be set to 0x046AAAAB (default value). The value of 0x046AAAAB also applies to 49.152 MHz (from a nominal of 50 MHz). **Note 2:** Central Frequency Offset should not exceed +/-5% off nominal. **Note 3:** The **spurs_supression** register must be programmed after changing the **central_freq_offsetspurs_supression** even if the value has not changed..

Register_Address: **0x010**
Register Name: **spurs_supression**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	Spurs_supression	This register is used for spurs suppression. Depending on the synthesizer configuration GUI will generate recommended value. When this register is changed, the ZL30168 requires 85 msec to reconfigure itself. No reads or writes to the device are permitted during this configuration period. The **spurs_suppression** register should only be written with values recommended by the GUI. **Note:** This register must be programmed after changing the **central_freq_offset** even if the value of **spurs_suppression** has not changed.

Register_Address: **0x011**
Register Name: **sticky_lock**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	Sticky Lock Register	This register needs to be set to a non-zero value prior to clearing sticky (status) registers, to avoid race condition that can happen when the internal state machine updates the status register while the host clears it. Setting this register to a non-zero value stops the updating of any of the sticky registers, and clearing this register restarts the updating of the sticky registers. For proper sticky register monitoring, see the procedure in section 7.0, “Register Map“.

Register_Address: **0x020**
Register Name: **ref_fail_isr_status_7_0**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7	Ref7 Fail	This bit will be set high when 'Ref7 fail mask' bit of the **ref_fail_isr_mask_7_0** register is high and conditions for Ref7 failure have occurred. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so once set it will stay high until the user clears it. Conditions for Ref7 failure are satisfied when either of LOS (external Loss of Signal), SCM (Single Cycle Monitor), CFM (Coarse Frequency Monitor), GST (Guard Soak Timer) or PFM (Precise Frequency Monitor) indicators are active and the appropriate mask bit (specified in the **ref_mon_fail_mask_X** register) is high. The failure indicators can be checked in the **ref_mon_fail_X** register.
6	Ref6 Fail	See Ref7 above
5	Ref5 Fail	See Ref7 above
4	Ref4 Fail	See Ref7 above
3	Ref3 Fail	See Ref7 above
2	Ref2 Fail	See Ref7 above
1	Ref1 Fail	See Ref7 above
0	Ref0 Fail	See Ref7 above

Register_Address: **0x022**
Register Name: **dpll_isr_status**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7	DPLL3 Lost Lock	The device will set this bit to high when 'DPLL3 Lost Lock Mask' bit of the dpll_isr_mask register is high and DPLL3 has lost lock. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. The lost lock indicator can be checked in the 'DPLL lock and holdover status' register.

Register_Address: **0x022**
Register Name: **dpll_isr_status**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
6	DPLL3 Holdover	The device will set this bit to high when 'DPLL3 Holdover Mask' bit of the dpll_isr_mask register is high and DPLL3 went into holdover mode. When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until the user clears it. The holdover indicator can be checked in the 'DPLL lock and holdover status' register.
5	DPLL2 Lost Lock	See description for DPLL3 Lost Lock above
4	DPLL2 Holdover	See description for DPLL3 Holdover above
3	DPLL1 Lost Lock	See description for DPLL3 Lost Lock above
2	DPLL1 Holdover	See description for DPLL3 Holdover above
1	DPLL0 Lost Lock	See description for DPLL3 Lost Lock above
0	DPLL0 Holdover	See description for DPLL3 Holdover above

Register_Address: **0x023**
Register Name: **ref_fail_isr_mask_7_0**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7	Ref7 Fail Mask	When set to high, this bit allows Ref7 fail indicator to appear in the ref_fail_isr_status_7_0 register and on the IRQ line. When low, the Ref7 failure indicator is masked.
6	Ref6 Fail Mask	See description for Ref7 above
5	Ref5 Fail Mask	See description for Ref7 above
4	Ref4 Fail Mask	See description for Ref7 above
3	Ref3 Fail Mask	See description for Ref7 above
2	Ref2 Fail Mask	See description for Ref7 above
1	Ref1 Fail Mask	See description for Ref7 above
0	Ref0 Fail Mask	See description for Ref7 above

Register_Address: **0x025**
Register Name: **dpll_isr_mask**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7	DPLL3 Lost Lock Mask	When set to high, this bit allows DPLL3 lost lock indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL3 lost lock indicator is masked.
6	DPLL3 Holdover Mask	When set to high, this bit allows DPLL3 holdover indicator to appear in the dpll_isr_status register and on the IRQ line. When low, the DPLL3 holdover indicator is masked.
5	DPLL2 Lost Lock	See description for DPLL3 Lost Lock Mask above
4	DPLL2 Holdover	See description for DPLL3 Holdover Mask above
3	DPLL1 Lost Lock	See description for DPLL3 Lost Lock Mask above
2	DPLL1 Holdover	See description for DPLL3 Holdover Mask above
1	DPLL0 Lost Lock	See description for DPLL3 Lost Lock Mask above
0	DPLL0 Holdover	See description for DPLL3 Holdover Mask above

Register_Address: **0x026**
Register Name: **ref_mon_fail_0**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref0 Fail PFM	Ref0 Precise Frequency Monitor (PFM) failure: This bit is set high when Ref0 fails to meet the Precise Frequency Monitor (PFM) failure criteria specified by the 'PFM limit' bits of the pfm_limit_ref1_0 register. The PFM failure criteria is typically referred to as reference frequency drift. This bit is 'sticky', so it will remain high until the user clears it. **Note:** This bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits

Register_Address: **0x026**
Register Name: **ref_mon_fail_0**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
3	Ref0 Fail GST	Guard Soak Timer failure (GST): This bit is set when Ref0 fails to meet Guard Soak Timer (GST) failure criteria specified by the 'GST disqualify Ref0' bits of the gst_disqualif_time_3_0 register. The GST timer is triggered by either CFM or SCM failure and this bit will be set if either of the two failures still exists upon expiration of the GST time. This bit is 'sticky', so it will stay high until customer clears it. **Note:** This bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits
2	Ref0 Fail CFM	Ref0 Coarse Frequency Monitor (CFM) failure: This bit is set this when Ref0 fails to meet Coarse Frequency Monitor (CFM) failure criteria specified by the 'Ref0 CFM Limit' bits of the scm_cfm_limit_ref0 register. The CFM failure criteria is usually referred to as reference phase hit. This bit is 'sticky', so it will stay high until customer clears it. **Note:** this bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits
1	Ref0 Fail SCM	Ref0 Single Cycle Monitor (SCM) failure: This bit is set when Ref0 fails to meet Single Cycle Monitor (SCM) failure criteria specified by the 'Ref0 SCM limit' bits of the scm_cfm_limit_ref0 register. The SCM failure criteria is usually referred to as reference phase irregularity. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits
0	Ref0 Fail LOS	External Ref0 Loss Of Signal (LOS) indicator: This bit is set when the external Ref0 LOS signal, applied to a selected GPIO, goes high. This bit is 'sticky', so it will stay high until the user clears it. The Ref0 LOS signal can be selected to appear on any of available GPIOs through the gpio_function_pin[0:6] registers. **Note:** this bit is not maskable, i.e. whenever conditions for it to be set are met, it will be set, regardless of any mask bits

Register_Address: **0x027**
Register Name: **ref_mon_fail_1**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:0	Ref1 Fail	Leave as default
4	Ref1 Fail PFM	Ref1 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref1 Fail GST	Ref1 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3

Register_Address: **0x027**
Register Name: **ref_mon_fail_1**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
2	Ref1 Fail CFM	Ref1 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref1 Fail SCM	Ref1 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref1 Fail LOS	Ref1 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x028**
Register Name: **ref_mon_fail_2**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref2 Fail PFM	Ref2 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref2 Fail GST	Ref2 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref2 Fail CFM	Ref2 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref2 Fail SCM	Ref2 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref2 Fail LOS	Ref2 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x029**
Register Name: **ref_mon_fail_3**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref3 Fail PFM	Ref3 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref3 Fail GST	Ref3 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3

Register_Address: **0x029**
Register Name: **ref_mon_fail_3**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
2	Ref3 Fail CFM	Ref3 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref3 Fail SCM	Ref3 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref3 Fail LOS	Ref3 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02A**
Register Name: **ref_mon_fail_4**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref4 Fail PFM	Ref4 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref4 Fail GST	Ref4 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref4 Fail CFM	Ref4 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref4 Fail SCM	Ref4 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref4 Fail LOS	Ref4 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02B**
Register Name: **ref_mon_fail_5**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref5 Fail PFM	Ref5 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4

Register_Address: **0x02B**
Register Name: **ref_mon_fail_5**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
3	Ref5 Fail GST	Ref5 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref5 Fail CFM	Ref5 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref5 Fail SCM	Ref5 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref5 Fail LOS	Ref5 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02C**
Register Name: **ref_mon_fail_6**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref6 Fail PFM	Ref6 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4
3	Ref6 Fail GST	Ref6 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref6 Fail CFM	Ref6 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref6 Fail SCM	Ref6 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref6 Fail LOS	Ref6 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x02D**
Register Name: **ref_mon_fail_7**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref7 Fail PFM	Ref7 Precise Frequency Monitoring (PFM) failure. See description for register at address 0x026 bit 4

Register_Address: **0x02D**
Register Name: **ref_mon_fail_7**
Default Value: **0x00**
Type: **StickyR/W**

Bit Field	Function Name	Description
3	Ref7 Fail GST	Ref7 Guard Soak Timer (GST) failure. See description for register at address 0x026 bit 3
2	Ref7 Fail CFM	Ref7 Coarse Frequency Monitor (CFM) failure. See description for register at address 0x026 bit 2
1	Ref7 Fail SCM	Ref7 Single Cycle Monitor (SCM) failure. See description for register at address 0x026 bit 1
0	Ref7 Fail LOS	Ref7 Loss of Signal (LOS). See description for register at address 0x026 bit 0

Register_Address: **0x036**
Register Name: **ref_mon_fail_mask_0**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref0 Fail PFM Mask	When set to high, this bit will allow Ref0 Fail PFM to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 Fail PFM will be masked from appearing in the ref_fail_isr_status_7_0 register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail PFM' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.
3	Ref0 Fail GST Mask	When set to high, this bit will allow Ref0 Fail GST to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 Fail GST will be masked from appearing in the ef_fail_isr_status_7_0 register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail GST' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.

Register_Address: **0x036**
Register Name: **ref_mon_fail_mask_0**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
2	Ref0 Fail CFM Mask	When set to high, this bit will allow Ref0 Fail CFM to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 CFM failure will be masked from appearing, as part of Ref0 failure indicator, in the ref_fail_isr_mask_7_0 register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail CFM' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.
1	Ref0 Fail SCM Mask	When set to high, this bit will allow Ref0 Fail SCM to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 SCM failure will be masked from appearing, as part of Ref0 failure indicator, in the 'Reference status interrupt failure' register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail SCM' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.
0	Ref0 Fail LOS Mask	When set to high, this bit will allow Ref0 Fail LOS to appear in ref_fail_isr_status_7_0 register and on IRQ line if not masked by 'Ref0 Fail Mask' bit in the ref_fail_isr_mask_7_0 register. When low, Ref0 external LOS failure will be masked from appearing, as part of Ref0 failure indicator, in the 'Reference status interrupt failure' register and on IRQ line. **Note:** This bit will not affect 'Ref0 Fail LOS' bit in the ref_mon_fail_0 register since the ref_mon_fail_0 register values are not maskable.

Register_Address: **0x037**
Register Name: **ref_mon_fail_mask_1**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref1 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref1 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref1 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref1 Fail SCM Mask	See description for register at address 0x036 bit 1

Register_Address: **0x037**
Register Name: **ref_mon_fail_mask_1**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
0	Ref1 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x038**
Register Name: **ref_mon_fail_mask_2**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref2 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref2 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref2 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref2 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref2 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x039**
Register Name: **ref_mon_fail_mask_3**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref3 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref3 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref3 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref3 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref3 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03A**
Register Name: **ref_mon_fail_mask_4**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref4 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref4 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref4 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref4 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref4 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03B**
Register Name: **ref_mon_fail_mask_5**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref5 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref5 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref5 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref5 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref5 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03C**
Register Name: **ref_mon_fail_mask_6**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref6 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref6 Fail GST Mask	See description for register at address 0x036 bit 3

Register_Address: **0x03C**
Register Name: **ref_mon_fail_mask_6**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
2	Ref6 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref6 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref6 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x03D**
Register Name: **ref_mon_fail_mask_7**
Default Value: **0x16**
Type: **R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	Ref7 Fail PFM Mask	See description for register at address 0x036 bit 4
3	Ref7 Fail GST Mask	See description for register at address 0x036 bit 3
2	Ref7 Fail CFM Mask	See description for register at address 0x036 bit 2
1	Ref7 Fail SCM Mask	See description for register at address 0x036 bit 1
0	Ref7 Fail LOS Mask	See description for register at address 0x036 bit 0

Register_Address: **0x046**
Register Name: **gst_disqualif_time_3_0**
Default Value: **0xAA**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Ref3 GST disqualification time	Guard soak timer disqualify time: Time to disqualify Ref3 input clock after detection of either a Ref3 CFM or Ref3 SCM failure indications. The expiration of the GST disqualify time after starting of the Ref3 GST disqualify timer will cause the Ref3 GST indicator to go high if the source of the timer triggering is still present. Selection: 00 = minimum delay possible 01 = 10 ms 10 = 50 ms (default) 11 = 2.5 s
5:4	Ref2 GST disqualification time	See bits 7:6 (Ref3) for details
3:2	Ref1 GST disqualification time	See bits 7:6 (Ref3) for details
1:0	Ref0 GST disqualification time	See bits 7:6 (Ref3) for details

Register_Address: **0x047**
Register Name: **gst_disqualif_time_7_4**
Default Value: **0xAA**
Type: R/W

Bit Field	Function Name	Description
7:6	Ref7 GST disqualification time	See description for register at address 0x046 bits 7:6
5:4	Ref6 GST disqualification time	See description for register at address 0x046 bits 7:6
3:2	Ref5 GST disqualification time	See description for register at address 0x046 bits 7:6
1:0	Ref4 GST disqualification time	See description for register at address 0x046 bits 7:6

Register_Address: **0x04A**
Register Name: **gst_qualif_time_3_0**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Ref3 GST qualification time	Guard soak timer qualify time selection: Time to qualify Ref3 input clock after disappearance of both the Ref3 CFM and the Ref3 SCM failure indications. The expiration of the GST qualify time after starting of the Ref3 GST qualify timer will cause Ref3 GST failure indicator to go low if neither the Ref3 CFM nor the Ref3 SCM indicator is present. Selection: 00 = 2 x selected Ref3 GST disqualify time 01 = 4 x selected Ref3 GST disqualify time (default) 10 = 8 x selected Ref3 GST disqualify time 11 = 16 x selected Ref3 GST disqualify time
5:4	Ref2 GST qualification time	See bits 7:6 (Ref3) for details
3:2	Ref1 GST qualification time	See bits 7:6 (Ref3) for details
1:0	Ref0 GST qualification time	See bits 7:6 (Ref3) for details

Register_Address: **0x04B**
Register Name: **gst_qualif_time_7_4**
Default Value: **0x55**
Type: R/W

Bit Field	Function Name	Description
7:6	Ref7 GST qualification time	See description for register at address 0x04A bits 7:6
5:4	Ref6 GST qualification time	See description for register at address 0x04A bits 7:6
3:2	Ref5 GST qualification time	See description for register at address 0x04A bits 7:6
1:0	Ref4 GST qualification time	See description for register at address 0x04A bits 7:6

Register_Address: **0x050**
Register Name: **scm_cfm_limit_ref0**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref0 SCM limit	These bits represent Ref0 Single Cycle Monitor (SCM) limit selection. When Ref0 fails the criteria specified by these bits, the SCM failure indicator will go high (can be read in the ref_mon_fail_0 register) Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that Ref0 clock is sampled by a 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes a limitation to SCM limits that can be programmed depending on Ref0 clock frequencies: +/- 0.1% can be programmed for frequencies below 800 kHz +/- 0.5%: below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note** 1:The SCM indicator should not be used (it should be masked) for reference frequencies above 400MHz. **Note** 2: For frequencies below 16 kHz, the CFM and SCM limits should be set to the same values for proper operation.
3	Reserved	Leave as default

Register_Address: **0x050**
Register Name: **scm_cfm_limit_ref0**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
2:0	Ref0 CFM Limit	These bits represent the Ref0 Coarse Frequency Monitor (CFM) limit selection. When Ref0 fails the criteria specified by these bits, the CFM failure indicator will go high (can be read in the ref_mon_fail_0 register). Selection: 000 = +/- 0.1% (in Ref0 frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% **Note**: For frequencies below 16 kHz, the CFM and SCM limits should be set to the same values for proper operation.

Register_Address: **0x051**
Register Name: **scm_cfm_limit_ref1**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref1 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref1 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x052**
Register Name: **scm_cfm_limit_ref2**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref2 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref2 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x053**
Register Name: **scm_cfm_limit_ref3**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref3 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref3 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x054**
Register Name: **scm_cfm_limit_ref4**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref4 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref4 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x055**
Register Name: **scm_cfm_limit_ref5**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref5 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref5 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x056**
Register Name: **scm_cfm_limit_ref6**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref6 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref6 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x057**
Register Name: **scm_cfm_limit_ref7**
Default Value: **0x55**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref7 SCM limit	See description for register at address 0x050 bits 6:4
3	Reserved	Leave as default
2:0	Ref7 CFM Limit	See description for register at address 0x050 bits 2:0

Register_Address: **0x060**
Register Name: **pfm_limit_ref1_0**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default

Register_Address: **0x060**
Register Name: **pfm_limit_ref1_0**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
6:4	Ref1 PFM Limit	These bits represent the Ref1 Precise Frequency Monitor (PFM) limit selection. When Ref1 fails this criteria, the PFM failure indicator will go high that can be read in the ref_mon_fail_1 register. Selection: 000 = 9.2 --- 12 ppm (in Ref1 frequency units) 001 = 40 --- 52 ppm 010 = 64 --- 83 ppm 011 = 100 --- 130 ppm 100 = 13.8 --- 18 ppm 101 = 24.6 --- 32 ppm 110 = 36.6 --- 47.5 ppm 111 = 52 --- 67.5 ppm **Example:** For Ref1 PFM Limit = 000, the input reference will be accepted if its frequency accuracy is lower than +/- 9.2 ppm. If the input reference frequency accuracy exceeds +/- 12 ppm, than the reference will be rejected. If the input reference frequency accuracy is in between +/-9.2 ppm and +/-12 ppm the state remains unchanged (hysteresis). **Note :** PFM supports any reference (input) frequency from 1 Hz to 750 MHz except for non integer (in Hz) frequencies below 5,000,000 Hz. For example 1 Hz, 8 kHz, 2.048 MHz, 156.25*66/64 MHz are supported frequencies but 0.5 Hz and 1.5 Hz are not supported.
3	Reserved	Leave as default
2:0	Ref0 PFM Limit	See bits 6:4 (Ref1)

Register_Address: **0x061**
Register Name: **pfm_limit_ref3_2**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref3 PFM Limit	See description for register at address 0x060 bits 6:4
3	Reserved	Leave as default
2:0	Ref2 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x062**
Register Name: **pfm_limit_ref5_4**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref5 PFM Limit	See description for register at address 0x060 bits 6:4
3	Reserved	Leave as default
2:0	Ref4 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x063**
Register Name: **pfm_limit_ref7_6**
Default Value: **0x33**
Type: **R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6:4	Ref7 PFM Limit	See description for register at address 0x060 bits 6:4
3	Reserved	Leave as default
2:0	Ref6 PFM Limit	See description for register at address 0x060 bits 2:0

Register_Address: **0x068**
Register Name: **phase_acq_en_7_0**
Default Value: **0xFF**
Type: **R/W**

Bit Field	Function Name	Description
7	Phase Acquisition 7 enable	When this bit is set to high, it will enable Phase Acquisition module for Ref7 input. When low, Phase Acquisition 7 is disabled (i.e. powered down).
6	Phase Acquisition 6 enable	See bit 7 for details
5	Phase Acquisition 5 enable	See bit 7 for details

Register_Address: **0x068**
Register Name: **phase_acq_en_7_0**
Default Value: **0xFF**
Type: **R/W**

Bit Field	Function Name	Description
4	Phase Acquisition 4 enable	See bit 7 for details
3	Phase Acquisition 3 enable	See bit 7 for details
2	Phase Acquisition 2 enable	See bit 7 for details
1	Phase Acquisition 1 enable	See bit 7 for details
0	Phase Acquisition 0 enable	See bit 7 for details

Register_Address: **0x06A**
Register Name: **phasemem_limit_ref0**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref0	These bits specify the Ref0 phase memory limit as per the following formula, using E32 series style: Value = round(32 * log(PhaseMemLimit/10)), where PhaseMemLimit is given in us units Example, if the desired delay is 10us, the value to be written to this register is 0x00, for 1 ms the value is 0x40, while for 930 seconds the value is 0xFF. **Note:** This register should be programmed to have a value that represents at least one reference period.

Register_Address: **0x06B**
Register Name: **phasemem_limit_ref1**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref1	See description for register at address 0x06A

Register_Address: **0x06C**
Register Name: **phasemem_limit_ref2**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref2	See description for register at address 0x06A

Register_Address: **0x06D**
Register Name: **phasemem_limit_ref3**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref3	See description for register at address 0x06A

Register_Address: **0x06E**
Register Name: **phasemem_limit_ref4**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref4	See description for register at address 0x06A

Register_Address: **0x06F**
Register Name: **phasemem_limit_ref5**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref5	See description for register at address 0x06A

Register_Address: **0x070**
Register Name: **phasemem_limit_ref6**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref6	See description for register at address 0x06A

Register_Address: **0x071**
Register Name: **phasemem_limit_ref7**
Default Value: **0x1B**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Phase memory limit for Ref7	See description for register at address 0x06A

Register_Address: **0x07A**
Register Name: **ref_config_7_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	Ref7 differential input enable	When this bit is set high, the device expects differential signal on its Ref7 pins (REF7_P and REF7_N). When low, the device expects single-ended signal on the REF7_P input, and the REF7_N input should be tied to GND.
6	Ref6 differential input enable	See bit 7 for details
5	Ref5 differential input enable	See bit 7 for details
4	Ref4 differential input enable	See bit 7 for details
3	Ref3 differential input enable	See bit 7 for details
2	Ref2 differential input enable	See bit 7 for details
1	Ref1 differential input enable	See bit 7 for details

Register_Address: **0x07A**
Register Name: **ref_config_7_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
0	Ref0 differential input enable	See bit 7 for details

Register_Address: **0x07C**
Register Name: **ref_pre_divide_7_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	Ref7 pre-divider enable	When this bit is set to high, the Ref7 input clock will be divided by 2 prior being processed by the DPLLs. All registers requiring Ref7 frequency information are programmed as if the divider output frequency is actual Ref7 frequency. When low, the Ref7 input clock is not divided prior being processed by the DPLLs.
6	Ref6 pre-divider enable	See bit 7 for details
5	Ref5 pre-divider enable	See bit 7 for details
4	Ref4 pre-divider enable	See bit 7 for details
3	Ref3 pre-divider enable	See bit 7 for details
2	Ref2 pre-divider enable	See bit 7 for details
1	Ref1 pre-divider enable	See bit 7 for details
0	Ref0 pre-divider enable	See bit 7 for details

Register_Address: **0x07F**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page selection register	The unsigned binary value written to this register selects the 128 byte page of registers that the host can write to. 0x00: page 0 (register addresses 0x000 to 0x07F) 0x01: page 1 (register addresses 0x080 to 0x0FF) 0x02: page 2 (register addresses 0x100 to 0x17F) 0x03: page 3 (register addresses 0x180 to 0x1FF) 0x04: page 4 (register addresses 0x200 to 0x27F) 0x05: page 5 (register addresses 0x280 to 0x2FF) 0x06-0xFF: reserved

Register_Address: **0x080:0x081**
Register Name: **ref0_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref0 base frequency Br0	Unsigned binary value of these bits represents Ref0 base frequency Br in Hz. Examples of values fro Br that can be programmed: 0x0001 for 1Hz, 0x000A for 10Hz, 0x0064 for 100Hz 0x03E8 for 1kHz, 0x07D0 for 2kHz, 0x1F40 for 8kHz, 0x61A8 for 25kHz, 0x9C40 for 40kHz. **Note 1:** Br has to be directly divisible from 1600000000, i.e. mod (1600000000, Br) has to be 0. The evaluation board GUI can generate recommended Br, Kr, Mr and Nr values for required input frequency. **Note 2:** in order to write e.g. 0x9C40 to this register (and any other register whose value is larger than 8 bits), 0x9C has to be written to the lower address and 0x40 to the upper address (big endian) with the 0x40 (LSBs) written last.

Register_Address: **0x082:0x083**
Register Name: **ref0_freq_multiple**
Default Value: **0x0F30**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref0 base frequency multiple Kr0	Unsigned binary value represents the Ref0 base frequency multiplication number. For a regular (non-FEC) reference frequency, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Ref0 frequency — Base frequency Br — Base frequency multiple Kr 2.048 MHz — 8 kHz (0x1F40) — 256 (0x0100) 1.544 MHz — 8 kHz (0x1F40) — 193 (0x00C1) 19.44 MHz — 40 kHz (0x9C40) — 486 (0x01E6) 177.5.MHz — 25 kHz (0x61A8) — 7100 (0x1BBC) 125 MHz — 40 kHz (0x9C40) — 18752 (0x4940) 156.25.MHz — 25 kHz (0x61A8) — 6250 (0x186A) 155.52 MHz — 40 kHz (0x9C40) — 3888 (0x0F30) 1234 Hz — 1 Hz (0x0001) — 1234 (0x04D2) 8 kHz — 1 kHz (0x03E8) — 8 (0x0008)

Register_Address: **0x084:0x087**
Register Name: **ref0_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref0 FEC ratio numerator Mr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref0 FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr For regular (non-FEC) reference frequencies, Mr and Nr should be programmed to 0x0001 (default values).
15:0	Ref0 FEC ratio denominator Nr	

Register_Address: **0x088:0x089**
Register Name: **ref1_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref1 base frequency Br1	See description for registers at address 0x080:0x081

Register_Address: **0x08A:0x08B**
Register Name: **ref1_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref1 base frequency multiple Kr1	See description for registers at address 0x082:0x083

Register_Address: **0x08C:0x08F**
Register Name: **ref1_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref1 FEC ratio numerator Mr1	See description for registers at address 0x084:0x087
15:0	Ref1 FEC ratio denominator Nr1	

Register_Address: **0x090:0x091**
Register Name: **ref2_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref2 base frequency Br2	See description for registers at address 0x080:0x081

Register_Address: **0x092:0x093**
Register Name: **ref2_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref2 base frequency multiple Kr2	See description for registers at address 0x082:0x083

Register_Address: **0x094:0x097**
Register Name: **ref2_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref2 FEC ratio numerator Mr2	See description for registers at address 0x084:0x087
15:0	Ref2 FEC ratio denominator Nr2	

Register_Address: **0x098:0x099**
Register Name: **ref3_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref3 base frequency Br3	See description for registers at address 0x080:0x081

Register_Address: **0x09A:0x09B**
Register Name: **ref3_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref3 base frequency multiple Kr3	See description for registers at address 0x082:0x083

Register_Address: **0x09C:0x09F**
Register Name: **ref3_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref3 FEC ratio numerator Mr3	See description for registers at address 0x084:0x087
15:0	Ref3 FEC ratio denominator Nr3	

Register_Address: **0x0A0:0x0A1**
Register Name: **ref4_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref4 base frequency Br4	See description for registers at address 0x080:0x081

Register_Address: **0x0A2:0x0A3**
Register Name: **ref4_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref4 base frequency multiple Kr4	See description for registers at address 0x082:0x083

Register_Address: **0x0A4:0x0A7**
Register Name: **ref4_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref4 FEC ratio numerator Mr4	See description for registers at address 0x084:0x087
15:0	Ref4 FEC ratio denominator Nr4	

Register_Address: **0x0A8:0x0A9**
Register Name: **ref5_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref5 base frequency Br5	See description for registers at address 0x080:0x081

Register_Address: **0x0AA:0x0AB**
Register Name: **ref5_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref5 base frequency multiple Kr5	See description for registers at address 0x082:0x083

Register_Address: **0x0AC:0x0AF**
Register Name: **ref5_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref5 FEC ratio numerator Mr5	See description for registers at address 0x084:0x087
15:0	Ref5 FEC ratio denominator Nr5	

Register_Address: **0x0B0:0x0B1**
Register Name: **ref6_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref6 base frequency Br6	See description for registers at address 0x080:0x081

Register_Address: **0x0B2:0x0B3**
Register Name: **ref6_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref6 base frequency multiple Kr6	See description for registers at address 0x082:0x083

Register_Address: **0x0B4:0x0B7**
Register Name: **ref6_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref6 FEC ratio numerator Mr6	See description for registers at address 0x084:0x087
15:0	Ref6 FEC ratio denominator Nr6	

Register_Address: **0x0B8:0x0B9**
Register Name: **ref7_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref7 base frequency Br7	See description for registers at address 0x080:0x081.

Register_Address: **0x0BA:0x0BB**
Register Name: **ref7_freq_multiple**
Default Value: **0x01E6**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Ref7 base frequency multiple Kr7	See description for registers at address 0x082:0x083

Register_Address: **0x0BC:0x0BF**
Register Name: **ref7_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Ref7 FEC ratio numerator Mr7	See description for registers at address 0x084:0x087
15:0	Ref7 FEC ratio denominator Nr7	

Register_Address: **0x0FF**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page Selection register	Unsigned binary value of these bits represents selected page for SPI access. See register at address 0x07F for details

Register_Address: **0x100**
Register Name: **dpll0_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL loop filter corner frequency selection	These bits control DPLL0 loop filter corner frequency. Bit selection: 000 = 14 Hz 001 = 28 Hz 010 = 56 Hz 011 = 112 Hz 100 = 224 Hz 101 = 448 Hz 110 = 896 Hz 111 = Variable bandwidth (see register 0x101)

Register_Address: **0x100**
Register Name: **dpll0_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
4	Time Interval Error (TIE) clear enable	This bit controls the DPLL0 output to input alignment. When this bit is set to high, the DPLL0 will align its outputs to the reset position (specified by appropriate phase shift selection). This bit should be set when initial output to input alignment is desired after numerous reference rearrangement. To achieve 'hitless' reference switch, this bit has to be kept low.
3:2	phase_slope_limit	These bits control DPLL0 phase slope limiter. Bit selection: 00 = 61 usec/sec 01 = 7.5 usec/sec 10 = 0.885 usec/sec 11 = unlimited (1/256) Note: Under certain configurations, the output of the DPLL may exceed these phase slope limit values. This depends on the input transient (phase or frequency) and the bandwidth of the DPLL.
1:0	Reserved	Leave as default

Register_Address: **0x101**
Register Name: **dpll0_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Variable Bandwidth Selection	When DPLL loop filter corner frequency selection is programmed to '111', these bits specify DPLL corner frequency as per the following formula, using E32 series style: Value = round(32 * log(BandWidth*10^4)), where BandWidth is given in Hz For this device, the bandwidth must in the range of 5.23Hz (0x97) to 13.33Hz (0xA4). If the bandwidth is programmed to less than 5.23, then the device will operate with a 5.23Hz bandwidth. Likewise, if bandwidth is programmed to greater than 13.33Hz, then the device will operate with a 13.33Hz bandwidth. Therefore, the default value of 0x00 results in a bandwidth of 5.23Hz.

Register_Address: **0x102**
Register Name: **dpll0_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	DPLL0 Pull-in Hold-in selection register	These bits control DPLL0 pull-in / hold-in range selection. Bit selection: 000 = +/- 12 ppm 001 = +/- 52 ppm 010 = +/- 83 ppm 011 = +/- 130 ppm 100 = +/- 400 ppm 101 = reserved 110 = reserved 111 = unlimited (1/256)

Register_Address: **0x103**
Register Name: **dpll0_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	When the 'DPLL0 mode' bits of this register (bits 2:0) are set to '10' (forced reference mode), these bits specify which reference the DPLL0 is forced to select. When the forced reference fails, the DPLL0 will go into holdover mode When the 'DPLL0 mode' bits of this register are set to are set to anything other than forced reference mode, these bits are ignored.
3	External feedback enable	When this bit is set, the DPLL0 will use the external feedback phase to compensate for the delay on all related output clocks (all output clocks coming from all synthesizers that are associated with the DPLL0). When this bit is 0, DPLL0 will ignore external feedback. **Note 1:** There is only one external feedback available, so the external feedback phase will be used if this bit is set, regardless whether DPLL0 is used to create the external feedback phase or one of other DPLLs. **Note 2:** This bit should be set only if external feedback is enabled (bit 7 in the External Feedback Control Register (register 0x181). If this bit is set while the external feedback is not enabled, input to output misalignment can be expected.

Register_Address: **0x103**
Register Name: **dpll0_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
2:0	DPLL0 Mode	These bits determine DPLL0 mode of operation. Selection: 000 = freerun mode 001 = forced holdover mode 010 = forced reference lock mode 011 = automatic mode 100 = NCO mode 101 = Buffer Fill Mode 110, 111 = reserved In 'automatic mode', reference selection is based on reference availability and reference priority selection. In this mode, the DPLL0 will go into holdover only if none of references is available. In 'forced reference lock mode', the DPLL0 has to lock to specified reference (selected by the 'Reference selection ' bits of this register. If the selected reference is not available, the DPLL0 will go to holdover mode and will not switch to another reference, regardless of the status of the other reference inputs. When the 'forced holdover mode' is programmed, all references are ignored and DPLL0 goes into holdover (based on last selected reference). When the 'freerun mode' is selected, the DPLL generates all its output clocks based only on the device oscillator OSCI input. When the 'NCO mode' is selected the DPLL is run in adjustable free-run mode where the output frequency of each Synthesizer connected to the DPLL can be simultaneously shifted by writing to the **dpll0_df_offset register.** When the ’Buffer fill mode’ is selected, the DPLL is locked to the phase error coming though the **dpll0_buff_ptr_diff** register. This value represent the buffer fill FIFO point difference.

Register_Address: **0x104**
Register Name: **dpll0_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default

Register_Address: **0x104**
Register Name: **dpll0_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
3:0	Selected reference status	When the 'DPLL0 mode' bits of the dpll0_mode_refsel register are set to '11' (automatic mode), these bits represent the selected reference status, i.e. '0000' = Ref0, '0001' = Ref1 and so on.

Register_Address: **0x105**
Register Name: **dpll0_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	When the DPLL0 is in automatic mode of operation programmed in the DPLL0 Mode field in dpll_mode_refsel , these bits are used to select priority of Ref1 for DPLL. 0000 is highest priority and 1110 is lowest priority. Setting these bits to 1111 will disable Ref1 reference (that will prevent DPLL0 from locking to Ref1). When references are programmed to have different priority number, the DPLL0 will perform 'REVERTIVE' switching between them. This means that the DPLL0 will always switch to the highest priority reference available with lowest priority number) when that reference becomes available (input is valid). When two or more input references are programmed to have same priority number, the DPLL0 will perform 'NON-REVERTIVE' switching between them. This means that the DPLL0 will not perform a switch to another reference with the same priority when that reference becomes available. Combinations of the same and different priority numbers can be used, such that the DPLL0 performs revertive switching between different priority references, but non-revertive switching among references with the same priority. Example: if Ref0 has priority 0 (highest), Ref1, Ref2 and Ref3 have priority 1. Whenever Ref0 becomes available, DPLL0 will switch to it. But, if Ref0 is not available, DPLL0 will remain locking to currently selected reference (e.g. Ref3) even when Ref1 or Ref2 become available.
3:0	priority selection Ref0	See description for bits 7:4 above

Register_Address: **0x106**
Register Name: **dpll0_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x107**
Register Name: **dpll0_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x108**
Register Name: **dpll0_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x10D**
Register Name: **dpll0_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	When set high, this bit allows the selected reference GST failure to cause the DPLL0 to perform a reference switch. When set low, the selected reference GST failure will be masked and DPLL0 will not perform a reference switch due to a GST failure. 0 = mask 1 = enable (activate)
6	refswitch mask CFM	When set high, this bit allows the selected reference CFM failure to cause DPLL0 to perform a reference switch. When low, the selected reference CFM failure will be masked and DPLL0 will not perform a reference switch due to a CFM failure. 0 = mask 1 = enable (activate)
5	refswitch mask SCM	When set high, this bit allows the selected reference SCM failure to cause DPLL0 to perform a reference switch. When low, the selected reference SCM failure will be masked and DPLL0 will not perform a reference switch due to a SCM failure. 0 = mask 1 = enable (activate)
4	refswitch mask LOS	When set high, this bit allows the selected reference LOS failure to cause DPLL0 to perform reference switch. When low, the selected reference LOS failure will be masked and DPLL0 will not perform a reference switch due to a LOS failure. 0 = mask 1 = enable (activate)
3	holdover mask GST	When set high, this bit allows the selected reference GST failure to cause DPLL0 to go into holdover. When low, the selected reference GST failure will be masked and DPLL0 will not go into holdover due to a GST failure. 0 = mask 1 = enable (activate) **Note:** This bit should never be programmed to 1 if neither 'holdover mask CFM' nor 'holdover mask SCM' bit is programmed to 1 (e.g. bits 3:1 should never be programmed to '100').
2	holdover mask CFM	When set high, this bit allows the selected reference CFM failure to cause DPLL0 to go into holdover. When low, the selected reference CFM failure will be masked and DPLL0 will not go into holdover due to a CFM failure. 0 = mask 1 = enable (activate)

Register_Address: **0x10D**
Register Name: **dpll0_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
1	holdover mask SCM	When set high, this bit allows the selected reference SCM failure to cause DPLL0 to go into holdover. When low, the selected reference SCM failure will be masked and DPLL0 will not go into holdover due to a SCM failure. 0 = mask 1 = enable (activate)
0	holdover mask LOS	When set high, this bit allows the selected reference external LOS signal to cause DPLL0 to go into holdover. When low, selected reference external LOS signal will be masked and DPLL0 will not go to holdover when the LOS signal is active high. 0 = mask 1 = enable (activate)

Register_Address: **0x10E**
Register Name: **dpll0_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	refswitch mask PFM	When set high, this bit allows selected reference PFM failure to cause DPLL to perform a reference switch. When low, selected reference PFM failure will be masked and DPLL will not perform reference switch due to a PFM failure.
3:1	Reserved	Leave as default
0	holdover mask PFM	When set high, this bit allows selected reference PFM failure to cause DPLL to go into holdover. When low, selected reference PFM failure will be masked and DPLL will not go into holdover due to the PFM failure.

Register_Address: **0x10F**
Register Name: **dpll0_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL0 reference edge selection	These bits define the selected reference edge sensitivity 00 = positive (rising) edge 01 = negative (falling) edge 10 = low pulse 11 = high pulse The low pulse and the high pulse options select a middle sample point halfway between the clock edges.
5	Reserved	Leave as default
4:0	DPLL0 holdover storage delay	These bits specify the DPLL0 holdover storage delay as per the following formula, using E8 series style: Value = round(8 * log(StorageDelay/10)), where StorageDelay is given in ms Example, if desired delay is 10ms, value to be written to this register is 0x00, for 1 second the value is 0x10, while for 75 seconds the value is 0x1F

Register_Address: **0x119**
Register Name: **dpll0_damping_ctrl**
Default Value: **0x05**
Type:**R/W**

Bit Field	Function Name	Description
7:6	Reserved	Leave as default
5:0	DPLL0 Damping Factor	Unsigned value of these bits represent the DPLL0 damping factor The upper limit of the damping factor is 50. Note: A damping factor of 5 corresponds to a gain peaking of less than 0.1 dB.

Register_Address: **0x11B:0x11E**
Register Name: **dpll0_buff_ptr_diff**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
31:0	DPLL0 Buffer Level Value	This register contains a two's (2's) complement binary value of the buffer pointer for generating a demultiplexer output clock from DPLL0. Note: This value is used in buffer fill mode only as selected by **dpll0_mode_refsel**.

Register_Address: **0x120**
Register Name: **dpll1_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL1 loop filter corner frequency selection	See description for register at address 0x100
4	Time Interval Error (TIE) clear enable	See description for register at address 0x100
3:2	phase_slope_limit	See description for register at address 0x100
1:0	Reserved	Leave as default

Register_Address: **0x121**
Register Name: **dpll1_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Variable Bandwidth Selection	See description for register at address 0x101

Register_Address: **0x122**
Register Name: **dpll1_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	DPLL1 Pull-in Hold-in selection register	See description for register at address 0x102

Register_Address: **0x123**
Register Name: **dpll1_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	See description for register at address 0x103
3	External feedback enable	See description for register at address 0x103
2:0	DPLL1 Mode	See description for register at address 0x103

Register_Address: **0x124**
Register Name: **dpll1_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Selected reference status	See description for register at address 0x104

Register_Address: **0x125**
Register Name: **dpll1_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	See description for register at address 0x105
3:0	priority selection Ref0	See description for register at address 0x105

Register_Address: **0x126**
Register Name: **dpll1_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x127**
Register Name: **dpll1_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x128**
Register Name: **dpll1_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x12D**
Register Name: **dpll1_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	See description for register at address 0x10D
6	refswitch mask CFM	See description for register at address 0x10D
5	refswitch mask SCM	See description for register at address 0x10D
4	refswitch mask LOS	See description for register at address 0x10D
3	holdover mask GST	See description for register at address 0x10D
2	holdover mask CFM	See description for register at address 0x10D
1	holdover mask SCM	See description for register at address 0x10D
0	holdover mask LOS	See description for register at address 0x10D

Register_Address: **0x12E**
Register Name: **dpll1_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default

Register_Address: **0x12E**
Register Name: **dpll1_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
4	refswitch mask PFM	See description for register at address 0x10E
3:1	Reserved	Leave as default
0	holdover mask PFM	See description for register at address 0x10E

Register_Address: **0x12F**
Register Name: **dpll1_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL1 reference edge selection	See description for register at address 0x10F
5	Reserved	Leave as default
4:0	DPLL1 holdover storage delay	See description for register at address 0x10F

Register_Address: **0x139**
Register Name: **dpll1_damping_ctrl**
Default Value: **0x05**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	DPLL1 Damping Factor	See description for register at address 0x119

Register_Address: **0x13B:0x13E**
Register Name: **dpll1_buff_ptr_diff**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
31:0	DPLL1 Buffer Level Value	See description for register at address 0x11B:0x11E

Register_Address: **0x140**
Register Name: **dpll2_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL2 loop filter corner frequency selection	See description for register at address 0x100
4	Time Interval Error (TIE) clear enable	See description for register at address 0x100
3:2	phase_slope_limit	See description for register at address 0x100
1:0	Reserved	Leave as default

Register_Address: **0x141**
Register Name: **dpll2_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Variable Bandwidth Selection	See description for register at address 0x101

Register_Address: **0x142**
Register Name: **dpll2_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
7:0	DPLL2 Pull-in Hold-in selection register	See description for register at address 0x102

Register_Address: **0x143**
Register Name: **dpll2_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	See description for register at address 0x103
3	External feedback enable	See description for register at address 0x103
2:0	DPLL2 Mode	See description for register at address 0x103

Register_Address: **0x144**
Register Name: **dpll2_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Selected reference status	See description for register at address 0x104

Register_Address: **0x145**
Register Name: **dpll2_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	See description for register at address 0x105
3:0	priority selection Ref0	See description for register at address 0x105

Register_Address: **0x146**
Register Name: **dpll2_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x147**
Register Name: **dpll2_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x148**
Register Name: **dpll2_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x14D**
Register Name: **dpll2_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	See description for register at address 0x10D
6	refswitch mask CFM	See description for register at address 0x10D
5	refswitch mask SCM	See description for register at address 0x10D
4	refswitch mask LOS	See description for register at address 0x10D
3	holdover mask GST	See description for register at address 0x10D
2	holdover mask CFM	See description for register at address 0x10D
1	holdover mask SCM	See description for register at address 0x10D
0	holdover mask LOS	See description for register at address 0x10D

Register_Address: **0x14E**
Register Name: **dpll2_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	refswitch mask PFM	See description for register at address 0x10E
3:1	Reserved	Leave as default

Register_Address: **0x14E**
Register Name: **dpll2_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
0	holdover mask PFM	See description for register at address 0x10E

Register_Address: **0x14F**
Register Name: **dpll2_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL2 reference edge selection	See description for register at address 0x10F
5	Reserved	Leave as default
4:0	DPLL2 holdover storage delay	See description for register at address 0x10F

Register_Address: **0x159**
Register Name: **dpll2_damping_ctrl**
Default Value: **0x05**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	DPLL2 Damping Factor	See description for register at address 0x119

Register_Address: **0x15B:0x15E**
Register Name: **dpll2_buff_ptr_diff**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
31:0	DPLL2 Buffer Level Value	See description for register at address 0x11B:0x11E

Register_Address: **0x160**
Register Name: **dpll3_ctrl**
Default Value: **0x0C**
Type:**R/W**

Bit Field	Function Name	Description
7:5	DPLL3 loop filter corner frequency selection	See description for register at address 0x100
4	Time Interval Error (TIE) clear enable	See description for register at address 0x100
3:2	phase_slope_limit	See description for register at address 0x100
1:0	Reserved	Leave as default

Register_Address: **0x161**
Register Name: **dpll3_var_bw_sel**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Variable Bandwidth Selection	See description for register at address 0x101

Register_Address: **0x162**
Register Name: **dpll3_pull_in_hold_in**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	DPLL3 Pull-in Hold-in selection register	See description for register at address 0x102

Register_Address: **0x163**
Register Name: **dpll3_mode_refsel**
Default Value: **0x03**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reference selection	See description for register at address 0x103
3	External feedback enable	See description for register at address 0x103
2:0	DPLL3 Mode	See description for register at address 0x103

Register_Address: **0x164**
Register Name: **dpll3_refsel_stat**
Default Value: **0x00**
Type:**R**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Selected reference status	See description for register at address 0x104

Register_Address: **0x165**
Register Name: **dpll3_ref_priority1_0**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref1	See description for register at address 0x105
3:0	priority selection Ref0	See description for register at address 0x105

Register_Address: **0x166**
Register Name: **dpll3_ref_priority3_2**
Default Value: **0x32**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref3	See description for register at address 0x105
3:0	priority selection Ref2	See description for register at address 0x105

Register_Address: **0x167**
Register Name: **dpll3_ref_priority5_4**
Default Value: **0x54**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref5	See description for register at address 0x105
3:0	priority selection Ref4	See description for register at address 0x105

Register_Address: **0x168**
Register Name: **dpll3_ref_priority7_6**
Default Value: **0x76**
Type:**R/W**

Bit Field	Function Name	Description
7:4	priority selection Ref7	See description for register at address 0x105
3:0	priority selection Ref6	See description for register at address 0x105

Register_Address: **0x16D**
Register Name: **dpll3_ref_fail_mask**
Default Value: **0x87**
Type:**R/W**

Bit Field	Function Name	Description
7	refswitch mask GST	See description for register at address 0x10D
6	refswitch mask CFM	See description for register at address 0x10D
5	refswitch mask SCM	See description for register at address 0x10D
4	refswitch mask LOS	See description for register at address 0x10D
3	holdover mask GST	See description for register at address 0x10D
2	holdover mask CFM	See description for register at address 0x10D
1	holdover mask SCM	See description for register at address 0x10D
0	holdover mask LOS	See description for register at address 0x10D

Register_Address: **0x16E**
Register Name: **dpll3_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4	refswitch mask PFM	See description for register at address 0x10E

Register_Address: **0x16E**
Register Name: **dpll3_pfm_fail_mask**
Default Value: **0x01**
Type:**R/W**

Bit Field	Function Name	Description
3:1	Reserved	Leave as default
0	holdover mask PFM	See description for register at address 0x10E

Register_Address: **0x16F**
Register Name: **dpll3_ho_edge_sel**
Default Value: **0x0B**
Type:**R/W**

Bit Field	Function Name	Description
7:6	DPLL3 reference edge selection	See description for register at address 0x10F
5	Reserved	Leave as default
4:0	DPLL3 holdover storage delay	See description for register at address 0x10F

Register_Address: **0x179**
Register Name: **dpll3_damping_ctrl**
Default Value: **0x05**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	DPLL3 Damping Factor	See description for register at address 0x119

Register_Address: **0x17B:0x17E**
Register Name: **dpll3_buff_ptr_diff**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
31:0	DPLL3 Buffer Level Value	See description for register at address 0x11B:0x11E

Register_Address: **0x17F**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page Selection register	See description for register at address 0x07F

Register_Address: **0x180**
Register Name: **dpll_hold_lock_status**
Default Value: **0x00**
Type::**Sticky R/W**

Bit Field	Function Name	Description
7	DPLL3 lock status	When DPLL3 is locked to a reference, the device will set this bit high. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL3, it will be set regardless of any mask bits. **Note**: This status bit is undefined in buffer-fill mode. Use the status bits in 0x2C1 to determine the status of the DPLL.
6	DPLL3 holdover status	This bit is set high when DPLL3 is in holdover mode. This bit is 'sticky', so it will stay high until the user clears it. **Note:** this bit is not maskable, i.e. whenever DPLL3 is in holdover, it will be set regardless of any mask bits.
5	DPLL2 lock status	See description for bit 7
4	DPLL2 holdover status	See description for bit 7
3	DPLL1 lock status	See description for bit 7
2	DPLL1 holdover status	See description for bit 7
1	DPLL0 lock status	See description for bit 7

Register_Address: **0x180**
Register Name: **dpll_hold_lock_status**
Default Value: **0x00**
Type::**Sticky R/W**

Bit Field	Function Name	Description
0	DPLL0 holdover status	See description for bit 7

Register_Address: **0x181**
Register Name: **ext_fb_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	External feedback enable	When this bit is set to 1, External feedback is enabled
6:5	Reserved	Leave as default
5:2	External feedback source	Specifies the reference to be used as the external feedback source input. 000 = ref0 001 = ref1 ... 111 = ref7 **Note:** In order to have proper behaviour when external feedback is enabled, it is required that the main reference and the external feedback source are frequency locked (they do not have to have the same carrier frequency).
1:0	External feedback DPLL selection	Specifies the DPLL to be used for the external feedback feature. The DPLL selected is used for determining the phase difference between its input reference and the selected feedback source. ‘00‘ - DPLL0 ‘01‘ - DPLL1 ‘10‘ - DPLL2 ‘11‘ - DPLL3 **Note:** If external feedback is enabled for particular DPLL ('external feedback enable' bit of the 'dpll_mode_refsel' register is set), the resulting DPLL output phase will be compensated for the external feedback phase, regardless of which DPLL is used for the external feedback phase calculation.

Register_Address: **0x182**
Register Name: **dpll_config**
Default Value: **0x04**
Type: **R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as default
2:0	DPLL Configuration	Selects which DPLLs are enabled Selection: 000 = none 001 = DPLL0 010 = DPLL0 and DPLL1 011 = DPLL0, DPLL1 and DPLL2 100 = all four DPLLs are enabled 101-111 = reserved

Register_Address: **0x183**
Register Name: **dpll_lock_selection**
Default Value: **0xAA**
Type:R/W

Bit Field	Function Name	Description
7:6	DPLL3 lock selection	These bits select DPLL3 lock indicator condition (appearing in the dpll_hold_lock_status register). Selection: 00 = reserved 01 = phase error is smaller than 1 us during 1 s 10 = phase error is smaller than 10 us during 1 s 11 = phase error is smaller than 10 us during 10 s
5:4	DPLL2 lock selection	See description for bits 7:6
3:2	DPLL1 lock selection	See description for bits 7:6
1:0	DPLL0 lock selection	See description for bits 7:6

Register_Address: **0x18D:0x191** Register Name: **dpll0_df_offset** Default Value: **0x0000000000** Type: **W**		
Bit Field	**Function Name**	**Description**
39:0	NCO0 Delta Frequency offset	When DPLL0 is programmed into NCO0 mode (dpll0_mode_refsel register), this register contains a 2's complement binary value of delta frequency offset. This register controls delta frequency of Synthesizers that are associated with the DPLL0/NCO0. Delta frequency is expressed in steps of +/- 2^-40 of nominal setting. The output frequency should be calculated as per formula: f_out = (1 - X/2^40)*f_nom where, X is 2's complement number specified in this register, f_nom is the nominal frequency set by Bs, Ks, Ms, Ns and postdivider number for particular Synthesizer and f_out is the desired output frequency **Note 1:** Delta frequency offset combined with the Synthesizer Frequency should be between 1.0 GHz and 1.5 GHz. **Note 2:** The delta frequency offset should not exceed +/-5000 ppm of the nominal value. **Note 3:** The delta frequency offset should not be changed by more than 7 ppm in a single update.

Register_Address: **0x192:0x196** Register Name: **dpll1_df_offset** Default Value: **0x0000000000** Type: **W**		
Bit Field	**Function Name**	**Description**
39:0	NCO1 Delta Frequency offset	See description of the register at address 0x18D:0x191

Register_Address: **0x197:0x19B** Register Name: **dpll2_df_offset** Default Value: **0x0000000000** Type: **W**		
Bit Field	**Function Name**	**Description**
39:0	NCO2 Delta Frequency offset	See description of the register at address 0x18D:0x191

Register_Address: **0x19C:0x1A0**
Register Name: **dpll3_df_offset**
Default Value: **0x0000000000**
Type: **W**

Bit Field	Function Name	Description
39:0	NCO3 Delta Frequency offset	See description of the register at address 0x18D:0x191

Register_Address: **0x1B0**
Register Name: **synth_drive_pll**
Default Value: **0xE4**
Type:R/W

Bit Field	Function Name	Description
7:6	DPLL for Synth 3	Selects DPLL that drives Synthesizer 3 Selection: 00 = DPLL0 01 = DPLL1 10 = DPLL2 11 = DPLL3 **Note:** If this register needs to be changed when external feedback is enabled; please disable external feedback, change the register value then enable external feedback.
5:4	DPLL for Synth 2	See description for bits 7:6
3:2	DPLL for Synth 1	See description for bits 7:6
1:0	DPLL for Synth 0	See description for bits 7:6

Register_Address: **0x1B1**
Register Name: **synth_enable**
Default Value: **0x0F**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3	Synth3 Enable	When this bit is set high, Synthesizer 3 is enabled. When low, Synthesizer 3 is disabled.
2	Synth2 Enable	See description for bit 3

Register_Address: **0x1B1**
Register Name: **synth_enable**
Default Value: **0x0F**
Type:**R/W**

Bit Field	Function Name	Description
1	Synth1 Enable	See description for bit 3
0	Synth0 Enable	See description for bit 3

Register_Address: **0x1B6**
Register Name: **sync_fail_flag_status**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3	Synth3 APLL syncfailFlag status	When high, this bit indicates that Synth3 APLL has lost lock, therefore generating wrong output frequency. This sticky bit is cleared by the **clear_sync_fail_flag** register bit. To check the status, first clear the bit using **clear_sync_fail_flag** register bit 3 for Synth3, then check the bit from this register. Note: This bit will be set upon power up or device reset
2	Synth2 APLL syncfailFlag status	See description for bit 3
1	Synth1 APLLsyncfailFlag status	See description for bit 3
0	Synth0 APLLsyncfailFlag status	See description for bit 3

Register_Address: **0x1B7**
Register Name: **clear_sync_fail_flag**
Default Value: **0x00**
Type:R/W

Bit Field	Function Name	Description
7:4	Reserved	
3	Synthesizer 3 APLL clear syncfailFlag	When high, this bit clears sticky hardware syncFailFlag in Synthesizer 3 APLL. Note: after using it for clearing syncFailFlag, this bit MUST be set to low for normal device functions

Register_Address: **0x1B7**
Register Name: **clear_sync_fail_flag**
Default Value: **0x00**
Type:R/W

Bit Field	Function Name	Description
2	Synthesizer 2 APLL clear syncfailFlag	When high, this bit clears sticky hardware syncFailFlag in Synthesizer 2 APLL. Note: after using it for clearing syncFailFlag, this bit MUST be set to low for normal device functions
1	Synthesizer 1 APLL clear syncfailFlag	When high, this bit clears sticky hardware syncFailFlag in Synthesizer 1 APLL. Note: after using it for clearing syncFailFlag, this bit MUST be set to low for normal device functions
0	Synthesizer 0 APLL clear syncfailFlag	When high, this bit clears sticky hardware syncFailFlag in Synthesizer 0 APLL. Note: after using it for clearing syncFailFlag, this bit MUST be set to low for normal device functions

Register_Address: **0x1B8:0x1B9**
Register Name: **synth0_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth0 base frequency Bs0	nsigned binary value of these bits represents Synthesizer 0 base frequency Bs in Hz. Examples of values for Bs that can be programmed: 0x1F40 for 8kHz, 0x61A8 for 25kHz, 0x9C40 for 40kHz. **Note 1:** Br has to be directly divisible from 1600000000, i.e. mod (1600000000, Br) has to be 0. The evaluation board GUI can generate recommended Br, Kr, Mr and Nr values for required input frequency. **Note 2:** in order to write e.g. 0x9C40 to this register (and any other register whose value is larger than 8 bits), 0x9C has to be written to the lower address and 0x40 to the upper address (big endian) with the 0x40 (LSBs) written last.

Register_Address: **0x1BA:0x1BB**
Register Name: **synth0_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth0 base frequency multiple Ks0	Unsigned binary value that represents Synthesizer 0 base frequency multiplication number. For a regular (non-FEC) synthesizer frequency, the 'Base frequency' number Bs is multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 is equal the synthesizer frequency in Hz. The synthesizer frequency must be programmed to be between 1 GHz and 1.5 GHz, so: Bs x Ks x 16 x Ms / Ns has to be between 1 000 000 000 and 1 500 000 000 Hz. Examples of appropriate values that can be programmed for Bs and Ks to get desired synthesizer frequency: Synthesizer frequency Base frequency Bs Base frequency multiple Ks 1.048576 GHz 8 kHz (0x1F40) 8192 (0x2000) 1.24416 GHz 40 kHz (0x9C40) 1944 (0x0798) 1.25 GHz 25 kHz (0x61A8) 3125 (0x0C35) **Note 1:** Br has to be directly divisible from 1600000000, i.e. mod (1600000000, Br) has to be 0. The evaluation board GUI can generate recommended Br, Kr, Mr and Nr values for required input frequency. **Note 2**: For proper operation of the synthesizer, Bs x Ks x Ms / Ns must not be a multiple any of the following frequencies: 65,536,000; 69,632,000; 73,728,000; 77,824,000; 81,920,000; 86,016,000 or 90,112,000.

Register_Address: **0x1BC:0x1BF**
Register Name: synth0_ratio_M_N
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth0 FEC ratio numerator Ms0	The unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer 0 FEC multiplication ratio. Synthesizer 0 FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns For regular (non-FEC) synthesizer frequencies, Ms and Ns should be programmed to be 0x0001 Examples of some synthesizer FEC frequencies and appropriate values for Bs, Ks, Ms and Ns registers to get those FEC frequencies are: a) OC-192 mode, standard EFEC for long reach: Desired frequency - 155.52MHz x 255/237 Synth frequency - 1.24416 GHz x 255/237 Base freq. Bs - 40 kHz (0x9C40) Base freq. mul. Ks - 1944 (0x0798) FEC ratio num. Ms - 255 (0x00FF) FEC ratio den. - 237 (0x00ED) Post div PA - 8 b) Long reach 10GE mode, double rate conversion (synth freq : 1250MHz x 66/64 x 255/238): Desired frequency - 156.25MHz x 66/64 x 255/238 Base frequency Bsr - 25 kHz (0x061A8 Base freq mul. Ks - 3125 (0x0C35) FEC ratio num. Ms - 66x255 (0x41BE) FEC ratio den. Ns - 64x238 (0x3B80) Post div PA - 8
15:0	Synth0 FEC ratio denominator Ns0	

Register_Address: **0x1C0:0x1C1**
Register Name: **synth1_base_freq**
Default Value: **0x61A8**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth1 base frequency Bs1	See description for register at address 0x1B8:0x1B9

Register_Address: **0x1C2:0x1C3**
Register Name: **synth1_freq_multiple**
Default Value: **0x0C35**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth1 base frequency multiple Ks1	See description for register at address 0x1BA:0x1BB

Register_Address: **0x1C4:0x1C7**
Register Name: **synth1_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth1 FEC ratio numerator Ms1	See description for register at address 0x1BC:0x1BF
15:0	Synth1 FEC ratio denominator Nr1	

Register_Address: **0x1C8:0x1C9**
Register Name: **synth2_base_freq**
Default Value: **0x61A8**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth2 base frequency Bs2	See description for register at address 0x1B8:0x1B9

Register_Address: **0x1CA:0x1CB**
Register Name: **synth2_freq_multiple**
Default Value: **0x0C35**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth2 base frequency multiple Ks2	See description for register at address 0x1BA:0x1BB

Register_Address: **0x1CC:0x1CF**
Register Name: **synth2_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth2 FEC ratio numerator Ms2	See description for register at address 0x1BC:0x1BF
15:0	Synth2 FEC ratio denominator Nr2	

Register_Address: **0x1D0:0x1D1**
Register Name: **synth3_base_freq**
Default Value: **0x9C40**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth3 base frequency Bs3	See description for register at address 0x1B8:0x1B9

Register_Address: **0x1D2:0x1D3**
Register Name: **synth3_freq_multiple**
Default Value: **0x0798**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Synth3 base frequency multiple Ks3	See description for register at address 0x1BA:0x1BB

Register_Address: **0x1D4:0x1D7**
Register Name: **synth3_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
31:16	Synth3 FEC ratio numerator Ms3	See description for register at address 0x1BC:0x1BF
15:0	Synth3 FEC ratio denominator Nr3	

Register_Address: **0x1FF**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page Selection register	See description for register at address 0x07F

Register_Address: **0x200:0x202** Register Name: **synth0_post_div_A** Default Value: **0x000002** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. ’1111’ and bits[17:16] == ’00’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. ’1111’ and bits[17:16] != ’00’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’00’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’00’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: low frequency clock 01: clock 1 (Synth 0 postdivider B) 10: clock 2 (Synth 0 postdivider C) 11: clock 3 (Synth 0 postdivider D)

Register_Address: **0x200:0x202**
Register Name: **synth0_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’00’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’00’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x203:0x205**
Register Name: **synth0_post_div_B**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. ’1111’ and bits[17:16] == ’01’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. ’1111’ and bits[17:16] != ’01’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’01’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0x203:0x205**
Register Name: **synth0_post_div_B**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’01’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: clock 0 (Synth 0 postdivider A) 01: low frequency clock 10: clock 2 (Synth 0 postdivider C) 11: clock 3 (Synth 0 postdivider D)
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’01’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’01’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x206:0x208** Register Name: **synth0_post_div_C** Default Value: **0x000010** Type:**R/W**		
Bit Field	**Function Name**	**Description**
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. ’1111’ and bits[17:16] == ’10’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. ’1111’ and bits[17:16] != ’10’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’10’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’10’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: clock 0 (Synth 0 postdivider A) 01: clock 1 (Synth 0 postdivider B) 10: low frequency clock 11: clock 3 (Synth 0 postdivider D)

Register_Address: **0x206:0x208**
Register Name: **synth0_post_div_C**
Default Value: **0x000010**
Type:**R/W**

Bit Field	Function Name	Description
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’10’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’10’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x209:0x20B**
Register Name: **synth0_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse or clock selection	When these bits are programmed ’1111’ the output clock will be a frame pulse or a low frequency clock (below 1 KHz). Selection between frame pulse and low frequency clock depends on the value of bits 17:16. ’1111’ and bits[17:16] == ’11’ : The output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer 0 base frequency Bs0 (synth0_base_freq register) divided by the value in bits[15:0] of this register. ’1111’ and bits[17:16] != ’11’ : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] If these bits are different from ’1111’ than the output is a clock with 50% duty cycle and frequency equal to the Synthesizer0 frequency (1 GHz to 1.5 GHz) divided by the value in bits [23:0] of this register.
19	Frame pulse type	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’11’ ,this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse

Register_Address: **0x209:0x20B**
Register Name: **synth0_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
18	Frame pulse polarity	Whenever bits[23:20] == ’1111’ and bits[17:16] != ’11’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
17:16	Frame pulse reference clock	Whenever bits[23:20] == ’1111’ these bits select between the low frequency clock and a the frame pulse related output clock (The Frame pulse width will be equal to the period of the related output clock). Otherwise it is used as part of divider ratio (bits[23:0]) Selection: 00: clock 0 (Synth 0 postdivider A) 01: clock 1 (Synth 0 postdivider B) 10: clock 2 (Synth 0 postdivider C) 11: low frequency clock
15:0	Division or frame pulse rate	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] ==’1111’ and bits[17:16] != ’11’ these bits represent the number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] ==’1111’ and bits[17:16] == ’11’ these bits represent the division factor for the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer 0 base frequency (synth0_base_freq register) divided by the value stored in these bits. Whenever bits[23:20] !=’1111’ the value is these bits is part of the output divider (bits[23:0]). The output frequency is then equal to Synthesizer 0 output frequency divided by the value stored in bits[23:0].

Register_Address: **0x20C:0x20E**
Register Name: **synth1_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x200:0x202
19	Frame pulse type	See description for the register at address 0x200:0x202
18	Frame pulse polarity	See description for the register at address 0x200:0x202

Register_Address: **0x20C:0x20E**
Register Name: **synth1_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
17:16	Frame pulse related clock selection	See description for the register at address 0x200:0x202
15:0	Frame pulse or divider	See description for the register at address 0x200:0x202

Register_Address: **0x20F:0x211**
Register Name: **synth1_post_div_B**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x203:0x205
19	Frame pulse type	See description for the register at address 0x203:0x205
18	Frame pulse polarity	See description for the register at address 0x203:0x205
17:16	Frame pulse related clock selection	See description for the register at address 0x203:0x205
15:0	Frame pulse or divider	See description for the register at address 0x203:0x205

Register_Address: **0x212:0x214**
Register Name: **synth1_post_div_C**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x206:0x208
19	Frame pulse type	See description for the register at address 0x206:0x208
18	Frame pulse polarity	See description for the register at address 0x206:0x208
17:16	Frame pulse related clock selection	See description for the register at address 0x206:0x208
15:0	Frame pulse or divider	See description for the register at address 0x206:0x208

Register_Address: **0x215:0x217**
Register Name: **synth1_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x209:0x20B
19	Frame pulse type	See description for the register at address 0x209:0x20B
18	Frame pulse polarity	See description for the register at address 0x209:0x20B
17:16	Frame pulse related clock selection	See description for the register at address 0x209:0x20B
15:0	Frame pulse or divider	See description for the register at address 0x209:0x20B

Register_Address: **0x218:0x21A**
Register Name: **synth2_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x200:0x202
19	Frame pulse type	See description for the register at address 0x200:0x202
18	Frame pulse polarity	See description for the register at address 0x200:0x202
17:16	Frame pulse related clock selection	See description for the register at address 0x200:0x202
15:0	Frame pulse or divider	See description for the register at address 0x200:0x202

Register_Address: **0x21B:0x21D**
Register Name: **synth2_post_div_B**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x203:0x205
19	Frame pulse type	See description for the register at address 0x203:0x205
18	Frame pulse polarity	See description for the register at address 0x203:0x205
17:16	Frame pulse related clock selection	See description for the register at address 0x203:0x205
15:0	Frame pulse or divider	See description for the register at address 0x203:0x205

Register_Address: **0x21E:0x220**
Register Name: **synth2_post_div_C**
Default Value: **0x00000A**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x206:0x208
19	Frame pulse type	See description for the register at address 0x206:0x208
18	Frame pulse polarity	See description for the register at address 0x206:0x208
17:16	Frame pulse related clock selection	See description for the register at address 0x206:0x208
15:0	Frame pulse or divider	See description for the register at address 0x206:0x208

Register_Address: **0x221:0x223**
Register Name: **synth2_post_div_D**
Default Value: **0x000032**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x209:0x20B
19	Frame pulse type	See description for the register at address 0x209:0x20B
18	Frame pulse polarity	See description for the register at address 0x209:0x20B
17:16	Frame pulse related clock selection	See description for the register at address 0x209:0x20B
15:0	Frame pulse or divider	See description for the register at address 0x209:0x20B

Register_Address: **0x224:0x226**
Register Name: **synth3_post_div_A**
Default Value: **0x000002**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x200:0x202
19	Frame pulse type	See description for the register at address 0x200:0x202
18	Frame pulse polarity	See description for the register at address 0x200:0x202
17:16	Frame pulse related clock selection	See description for the register at address 0x200:0x202
15:0	Frame pulse or divider	See description for the register at address 0x200:0x202

Register_Address: **0x227:0x229**
Register Name: **synth3_post_div_B**
Default Value: **0x000008**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x203:0x205
19	Frame pulse type	See description for the register at address 0x203:0x205
18	Frame pulse polarity	See description for the register at address 0x203:0x205
17:16	Frame pulse related clock selection	See description for the register at address 0x203:0x205
15:0	Frame pulse or divider	See description for the register at address 0x203:0x205

Register_Address: **0x22A:0x22C**
Register Name: **synth3_post_div_C**
Default Value: **0x000010**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x206:0x208
19	Frame pulse type	See description for the register at address 0x206:0x208
18	Frame pulse polarity	See description for the register at address 0x206:0x208
17:16	Frame pulse related clock selection	See description for the register at address 0x206:0x208
15:0	Frame pulse or divider	See description for the register at address 0x206:0x208

Register_Address: **0x22D:0x22F**
Register Name: **synth3_post_div_D**
Default Value: **0x000040**
Type:**R/W**

Bit Field	Function Name	Description
23:20	Frame pulse selection	See description for the register at address 0x209:0x20B
19	Frame pulse type	See description for the register at address 0x209:0x20B
18	Frame pulse polarity	See description for the register at address 0x209:0x20B
17:16	Frame pulse related clock selection	See description for the register at address 0x209:0x20B
15:0	Frame pulse or divider	See description for the register at address 0x209:0x20B

Register_Address: **0x234:0x235**
Register Name: **phase_shift_s0_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth0 Divider C quadrature phase shift	These bits select the quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer0 Post Divider C. Selection: 000 = 0 degrees (no shift) 001 = -45 degrees 010 = -90 degrees 011 = -135 degrees 100 = -180 (or 180) degrees 101 = 135 degrees 110 = 90 degrees 111 = 45 degrees **Note:** Only use the 0b000 selection with 1 Hz output signals
12:0	Synth0 Divider C coarse phase shift	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer0 frequency for all clocks coming from Synthesizer0 Post Divider C (0=no shift, -1= delay output clock for 1 period, 1 = advance output for 1 period, and so on).

Register_Address: **0x236:0x237**
Register Name: **phase_shift_s0_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth 0 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth0 Divider D course phase shift	See description for the register at address 0x234:235

Register_Address: **0x23C:0x23D**
Register Name: **phase_shift_s1_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth 1 Divider C quadrature phase shift	See description for the register at address 0x234:235

Register_Address: **0x23C:0x23D**
Register Name: **phase_shift_s1_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
12:0	Synth1 Divider C coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x23E:0x23F**
Register Name: **phase_shift_s1_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth1 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth1 Divider D coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x244:0x245**
Register Name: **phase_shift_s2_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth2 Divider C quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth2 Divider C coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x246:0x247**
Register Name: **phase_shift_s2_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth2 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth2 Divider D coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x24C:0x24D**
Register Name: **phase_shift_s3_postdiv_c**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth3 Divider C quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth3 Divider C coarse phase shift	See description for the register at address 0x234:235

Register_Address: **0x24E:0x24F**
Register Name: **phase_shift_s3_postdiv_d**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
15:13	Synth3 Divider D quadrature phase shift	See description for the register at address 0x234:235
12:0	Synth3 Divider D course phase shift	See description for the register at address 0x234:235

Register_Address: **0x250**
Register Name: **synth0_fine_phase_shift**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth0 fine phase shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of VCO period over 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 0 (including all four postdividers)

Register_Address: **0x251**
Register Name: **synth1_fine_phase_shift**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth1 fine phase shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of VCO period over 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 0 (including all four postdividers)

Register_Address: **0x252**
Register Name: **synth2_fine_phase_shift**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth2 fine phase shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of VCO period over 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 0 (including all four postdividers)

Register_Address: **0x253**
Register Name: **synth3_fine_phase_shift**
Default Value: **0x0000**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Synth3 fine phase shift	Unsigned binary value of these bits represent Synth0 fine phase shift (advancement) in steps of VCO period over 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer 0 (including all four postdividers)

Register_Address: **0x254**
Register Name: **Synth1_0_stop_clk**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:6	Synth1 Post Divider D stop clock	Setting of these bits will cause Synthesizer 1 Post Divider D to stop clock on either the rising or falling edge. Selection: 00 - 01 = continuous run (stop clock function is disabled) 10 = stop HPOUTCLK3 on the falling edge (stays low) 11 = stop HPOUTCLK3 on the rising edge (stays high)
5:4	Synth1 Post Divider C stop clock	See description for bits 7:6
3:2	Synth0 Post Divider D stop clock	See description for bits 7:6
1:0	Synth0 Post Divider C stop clock	See description for bits 7:6

Register_Address: **0x255**
Register Name: **synth3_2_stop_clk**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:6	Synth3 Post Divider D stop clock	See description for register at address 0x254
5:4	Synth3 Post Divider C stop clock	See description for register at address 0x254
3:2	Synth2 Post Divider D stop clock	See description for register at address 0x254
1:0	Synth2 Post Divider C stop clock	See description for register at address 0x254

Register_Address: **0x261**
Register Name: **hp_diff_en**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	enable HPDIFF7	When this bit is set to high, it will enable HPDIFF7_P and HPDIFF7_N outputs. When low, the outputs are tristated.

Register_Address: **0x261** Register Name: **hp_diff_en** Default Value: **0x00** Type:**R/W**		
Bit Field	Function Name	Description
6	enable HPDIFF6	See description for bit 7
5	enable HPDIFF5	See description for bit 7
4	enable HPDIFF4	See description for bit 7
3	enable HPDIFF3	See description for bit 7
2	enable HPDIFF2	See description for bit 7
1	enable HPDIFF1	See description for bit 7
0	enable HPDIFF0	See description for bit 7

Register_Address: **0x262** Register Name: **hp_cmos_en** Default Value: **0x00** Type:**R/W**		
Bit Field	Function Name	Description
7	enable HPOUTCLOCK7	When this bit is set to high, it will enable HPOUTCLK7 output. When low, the output is tristated.
6	enable HPOUTCLOCK6	See description for bit 7
5	enableHPOUTCLOCK5	See description for bit 7
4	enable HPOUTCLOCK4	See description for bit 7
3	enable HPOUTCLOCK3	See description for bit 7
2	enable HPOUTCLOCK2	See description for bit 7
1	enable HPOUTCLOCK1	See description for bit 7
0	enable HPOUTCLOCK0	See description for bit 7

Register_Address: **0x266** Register Name: **gpio_function_pin0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	GPIO0 control or status select	This bit determines whether GPIO0 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0x266**
Register Name: **gpio_function_pin0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
6:0	GPIO0 table bit address	Unsigned binary value of these bits represent the address in the control or status table, depending on 'GPIO0 control or status select' bit. The GPIO control and status tables are specified in 5.3, “GPIO Configuration“ Default: No function assigned

Register_Address: **0x267**
Register Name: **gpio_function_pin1**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO1 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO1 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x268**
Register Name: **gpio_function_pin2**
Default Value: **0x60**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO2 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO2 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x269**
Register Name: **gpio_function_pin3**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	GPIO3 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO3 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x26A** Register Name: **gpio_function_pin4** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	GPIO4 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO4 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x26B** Register Name: **gpio_function_pin5** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	GPIO5 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO5 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x26C** Register Name: **gpio_function_pin6** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	GPIO6 control or status select	See description for register at address 0x266 bit 7
6:0	GPIO6 table bit address	See description for register at address 0x266 bits 6:0

Register_Address: **0x276** Register Name: **gpio_in_6_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default
6	Input value for GPIO6	Logic values on pin GPIO6
5	Input value for GPIO5	See description for bit 6
4	Input value for GPIO4	See description for bit 6

Register_Address: **0x276**
Register Name: **gpio_in_6_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
3	Input value for GPIO3	See description for bit 6
2	Input value for GPIO2	See description for bit 6
1	Input value for GPIO1	See description for bit 6
0	Input value for GPIO0	See description for bit 6

Register_Address: **0x278**
Register Name: **gpio_out_6_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6	Set GPIO6 output	Sets the output value for the pin GPIO6. **Note:** GPIO6 output needs to be enabled in gpio_out_en_6_0
5	Set GPIO5 output	See description for bit 6
4	Set GPIO4 output	See description for bit 6
3	Set GPIO3 output	See description for bit 6
2	Set GPIO2 output	See description for bit 6
1	Set GPIO1 output	See description for bit 6
0	Set GPIO0 output	See description for bit 6

Register_Address: **0x27A**
Register Name: **gpio_out_en_6_0**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7	**Reserved**	**Leave as default**
6	Enable GPIO6 output	Configures the GPIO6 to be either input or output. If this bit is set, GPIO6 output driver is enabled and the GPIO output pin drives out the value stored in the corresponding bit position of the gpio_ouput_6_0 register
5	Enable GPIO5 output	See description for bit 6
4	Enable GPIO4 output	See description for bit 6
3	Enable GPIO3 output	See description for bit 6

Register_Address: **0x27A** Register Name: **gpio_out_en_6_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
2	Enable GPIO2 output	See description for bit 6
1	Enable GPIO1 output	See description for bit 6
0	Enable GPIO0 output	See description for bit 6

Register_Address: **0x27C** Register Name: **gpio_latch_6_0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default
6	Latch GPIO6 input	Set to latch the current value on GPIO6 pin. If this bit is zero, the value in bit 6 of gpio_in_6_0 will change as the logic level on GPIO6 changes.
5	Latch GPIO5 input	See description for bit 6
4	Latch GPIO4 input	See description for bit 6
3	Latch GPIO3 input	See description for bit 6
2	Latch GPIO2 input	See description for bit 6
1	Latch GPIO1 input	See description for bit 6
0	Latch GPIO0 input	See description for bit 6

Register_Address: **0x27E** Register Name: **buffer_fill_irq_status** Default Value: **0x00** Type:**StickyR/W**		
Bit Field	**Function Name**	**Description**
7	DPLL3 Bufferfill Output Frequency Failure Status	The device will set this bit to high when 'DPLL3 output frequency failure' bit of the **buffer_fill_irq_mask** register is high and DPLL3 has an output frequency failure (as described by **dplln_out_freq_mon_limit** register). When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until customer clears it (after finishing serving interrupt routine). The unmasked failure status can be also be checked in the **buff_fill_status** register.
6	DPLL2 Bufferfill Output Frequency Failure Status	See description for bit 7

Register_Address: **0x27E** Register Name: **buffer_fill_irq_status** Default Value: **0x00** Type:**StickyR/W**		
Bit Field	**Function Name**	**Description**
5	DPLL1 Bufferfill Output Frequency Failure Status	See description for bit 7
4	DPLL0 Bufferfill Output Frequency Failure Status	See description for bit 7
3	DPLL3 Bufferfill Input Frequency Failure Status	The device will set this bit to high when 'DPLL3 input frequency failure' bit of the **buffer_fill_irq_mask** register is high and DPLL3 has an input frequency failure (as described by **dplln_inp_freq_mon_lim** and **dplln_inp_freq_mon_time** registers). When this bit is set to high, it also sets IRQ line to high. This bit is 'sticky', so it will stay high until customer clears it (after finishing serving interrupt routine). The unmasked failure status can be also be checked in the **buff_fill_status** register.
2	DPLL2 Bufferfill Input Frequency Failure Status	See description for bit 3
1	DPLL1 Bufferfill Input Frequency Failure Status	See description for bit 3
0	DPLL0 Bufferfill Input Frequency Failure Status	See description for bit 3

Register_Address: **0x27F** Register Name: **page_sel_register** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	Page Selection register	See description for register at address 0x07F

Register_Address: **0x280** Register Name: **dpll0_buff_fill_ctrl** Default Value: **0x96** Type:**R/W**		
Bit Field	Function Name	Description
7:6	Related synthesizer output	Output assigned to buffer-fill clock Selection: 00 = Postdivider A 01 = Postdivider B 10 = Postdivider C (default) 11 = Postdivider D Note: The frequency of the output is used within the buffer-fill clock generation calculation for converting from the value to the equivalent phase.
5:2	Buffer level input gain	Buffer level input gain = 2^ (n-5) when n=**dpll0_buff_fill_ctrl**[5:2] Default setting is 0b0101 for a gain of 1.
1:0	Level format	Buffer level (pointer difference) format Selection: 00 = Reserved 01 = 8 bits two's complement 10 = 16 bits two's complement (default) 11 = 32 bits two's complement

Register_Address: **0x281:0x284** Register Name: **dpll0_buff_fill_offset** Default Value: **0x00000100** Type:**R/W**		
Bit Field	**Function Name**	**Description**
31:0	Buffer Level Offset Value	Two's complement value to be subtracted from the buff_ptr_diff values for DPLL0

Register_Address: **0x285** Register Name: **dpll0_ext_divider** Default Value: **0x02** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	External division rate in powers of two	Value in powers of 2 of the divider in the external signal path. Value = 2^(**dpll0_ext_divider)**

Register_Address: **0x286** Register Name: **dpll0_inp_freq_mon_limit** Default Value: **0x05** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:3	Reserved	Leave as Default
2:0	Input frequency monitor limit	Appropriate Buffer fill status bit will be asserted when this limit is violated.(These values are used to determine input failure as indicated by the GPIOs and by the **buff_fill_status** register.) Selection: 0 = +/- 5 ppm (based on buffer driving clock frequency) 1 = +/- 10 2 = +/- 20 3 = +/- 40 4 = +/- 80 5 = +/- 160 (default) 6 = +/- 320 7 = +/- 640 Note 1: Input frequency monitoring is valid when the DPLL is in locked or holdover modes. Note 2: The value of the **dpll0_inp_freq_mon_limit** register must be smaller than the **dpll0_out_freq_mon_limit** for proper operation.

Register_Address: **0x287** Register Name: **dpll0_inp_freq_mon_time** Default Value: **0x07** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:5	Reserved	Leave as default
4:0	Input reference monitor time	The unsigned value of this register sets the time that the input frequency monitor waits before determining wheather the reference frequency violates the input frequency monitor limit (**dpll0_inp_freq_mon_limit**)**.** Selection: Monitor time = 2^(n-7) seconds where n = **dpll0_inp_freq_mon_time[4:0]** Default is 0b111 or 1 second. **Note 1:** Input frequency monitoring can be used when the DPLL is in holdover mode.

Register_Address: **0x288** Register Name: **dpll0_out_freq_mon_limit** Default Value: **0x0D** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:5	Reserved	Leave as default
4:0	Output frequency monitor limit	The unsigned value of this register sets the output frequency monitor limit value. Selection: Monitor limit = +/-2^(n-10) ppm where n = **dpll0_out_freq_mon_limit[4:0]** The maximum value is when n=22 which results a limit from +/-0.976 ppb and +/-2^12 ppm. Default is 13 which corresponds to +/- 8 ppm. The appropriate buffer fill status bit will be asserted when the limit is violated. Note 1: Output frequency monitoring MUST NOT exceed selected pull-in/hold-in range of the DPLL. Note 2: In holdover mode, output monitoring is not valid.

Register_Address: **0x289** Register Name: **dpll0_attenuation** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	Attenuation applied to the buffer fill error	Value of the attenuation applied to the buffer fill error Value = 2^(-**dpll0_attenuation)**

Register_Address: **0x28A** Register Name: **dpll0_err_polarity** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:1	Reserved	Leave as default

Register_Address: **0x28A** Register Name: **dpll0_err_polarity** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	DPLL0 Error Polarity	The value of this bit determines the polarity of the error. Selection: 0 = Regular polarity – the phase error sign is not inverted before being passed to the rest of Dpll filter module. This mode assumes that reference clock is used for the Buffer fill FIFO write clock, while ZL30168 output clock is used as the FIFO read clock. (default) 1 = Inverted polarity - the phase error sign is inverted before being passed to the rest of Dpll filter module. This mode would assume that reference clock is used for the Buffer fill FIFO read clock, while ZL30168 output clock is used as the FIFO write clock. Other scenarios are possible for usage of this inverted polarity mode.

Register_Address: **0x28B** Register Name: **dpll0_buf_fill_misc_ctrl** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default
6	Buffer Fill Holdover Exit Condition	These bits specify the conditions under which a DPLL in buffer fill mode will exit holdover: Selection: 0 = Device will automatically leave holdover after a short hysteresis period 1 = If the device is in holdover and the buffer-fill input monitor changes to passing, then the device will automatically leave holdover **Note 1:** If a GPIO pin is configured to control buffer-fill holdover, then the GPIO pin must be de-asserted before the device will leave holdover. **Note 2:** Also note that a buffer-fill data input timeout will also cause an unmaskable transition to holdover, independent of the above.

Register_Address: **0x28B** Register Name: **dpll0_buf_fill_misc_ctrl** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
5:4	Buffer Fill Holdover Entry Condition	These bits specify the conditions under which a DPLL in buffer fill mode will enter holdover: Selection: 00 = No automatic transitions into holdover are enabled 01 = If the buffer-fill input monitor is failing, then the device will automatically enter holdover 10 = If the buffer-fill output monitor is failing, then the device will automatically enter holdover 11 = Both the input and output monitor must be failing before the device will automatically enter holdover **Note 1:** If a GPIO pin is configured to control buffer-fill holdover, then the GPIO pin can independently cause a transition to holdover. **Note 2:** A buffer-fill data input timeout will also cause an unmaskable transition to holdover, independent of the above.
3:2	Reserved	Leave as default
1	Zero-error compensation	The value of this bit determines the compensation used Selection: 0 = No compensation added(default) 1 = If selected, a half UI offset is introduced to the input error to avoid a zero value input to the filter.
0	Damping Correction Control	The value of this bit determines the damping correction used Selection: 0 = Damping correction is disabled (default) 1 = Damping correction is based on selected gain/attenuation.

Register_Address: **0x28C** Register Name: **dpll0_buf_fill_misc_ctrl** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:3	Reserved	Leave as default

Register_Address: **0x28C**
Register Name: **dpll0_buf_fill_misc_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	**Function Name**	**Description**
2:0	Buffer Fill Quarter Size	This field specifies the size of the host buffer (divided by 4) that is controlling DPLL0 in buffer-fill mode. A value of zero provides the default size of 128 (or total buffer size of 128 * 4 = 512). Otherwise, the buffer size is encoded as = 16 * 2^value. Selection: 000 = 128 (default; total buffer size of 512)) 001 = 32 (total buffer size of 32 * 4 = 128) 010 = 64 011 = 128 100 = 256 101 = 512 110 = 1024 111 = 2048

Register_Address: **0x290**
Register Name: **dpll1_buff_fill_ctrl**
Default Value: **0x96**
Type:**R/W**

Bit Field	Function Name	Description
7:6	Related synthesizer output	See Description for DPLL0
5:2	Buffer level input gain	See Description for DPLL0
1:0	Level format	See Description for DPLL0

Register_Address: **0x291:0x294**
Register Name: **dpll1_buff_fill_offset**
Default Value: **0x00000100**
Type:**R/W**

Bit Field	**Function Name**	**Description**
31:0	Buffer Level Offset Value	See Description for DPLL0

Register_Address: **0x295**
Register Name: **dpll1_ext_divider**
Default Value: **0x02**
Type:**R/W**

Bit Field	Function Name	Description
7:0	External division rate in powers of two	See Description for DPLL0

Register_Address: **0x296**
Register Name: **dpll1_inp_freq_mon_limit**
Default Value: **0x05**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as Default
2:0	Input frequency monitor limit	See Description for DPLL0

Register_Address: **0x297**
Register Name: **dpll1_inp_freq_mon_time**
Default Value: **0x07**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	Input reference monitor time	See Description for DPLL0

Register_Address: **0x298**
Register Name: **dpll1_out_freq_mon_limit**
Default Value: **0x0D**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	Output frequency monitor limit	See Description for DPLL0

Register_Address: **0x299** Register Name: **dpll1_attenuation** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	Additional attenuation applied to the buffer fill error	See Description for DPLL0

Register_Address: **0x29A** Register Name: **dpll1_err_polarity** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:1	Reserved	Leave as default
0	DPLL1 Error Polarity	See Description for DPLL0

Register_Address: **0x29B** Register Name: **dpll1_buf_fill_misc_ctrl** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default
6	Buffer Fill Holdover Exit Condition	See Description for DPLL0
5:4	Buffer Fill Holdover Entry Condition	See Description for DPLL0
3:2	Reserved	Leave as default
1	Zero-error compensation	See Description for DPLL0
0	Damping Correction Control	See Description for DPLL0

Register_Address: **0x29C** Register Name: **dpll1_buf_fill_misc_ctrl2** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:3	Reserved	Leave as default
2:0	Buffer Fill Quarter Size	See Description for DPLL0

Register_Address: **0x2A0** Register Name: **dpll2_buff_fill_ctrl** Default Value: **0x96** Type:**R/W**		
Bit Field	Function Name	Description
7:6	Related synthesizer output	See Description for DPLL0
5:2	Buffer level input gain	See Description for DPLL0
1:0	Level format	See Description for DPLL0

Register_Address: **0x2A1:0x2A4** Register Name: **dpll2_buff_fill_offset** Default Value: **0x00000100** Type:**R/W**		
Bit Field	**Function Name**	**Description**
31:0	Buffer Level Offset Value	See Description for DPLL0

Register_Address: **0x2A5** Register Name: **dpll2_ext_divider** Default Value: **0x02** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	External division rate in powers of two	See Description for DPLL0

Register_Address: **0x2A6**
Register Name: **dpll2_inp_freq_mon_limit**
Default Value: **0x05**
Type:**R/W**

Bit Field	Function Name	Description
7:3	Reserved	Leave as Default
2:0	Input frequency monitor limit	See Description for DPLL0

Register_Address: **0x2A7**
Register Name: **dpll2_inp_freq_mon_time**
Default Value: **0x07**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	Input reference monitor time	See Description for DPLL0

Register_Address: **0x2A8**
Register Name: **dpll2_out_freq_mon_limit**
Default Value: **0x0D**
Type:**R/W**

Bit Field	Function Name	Description
7	Reserved	Leave as default
6	Buffer Fill Holdover Exit Condition	See Description for DPLL0
5:4	Buffer Fill Holdover Entry Condition	See Description for DPLL0
3:2	Reserved	Leave as default
1	Zero-error compensation	See Description for DPLL0
0	Damping Correction Control	See Description for DPLL0

Register_Address: **0x2A9** Register Name: **dpll2_attenuation** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	Additional attenuation applied to the buffer fill error	See Description for DPLL0

Register_Address: **0x2AA** Register Name: **dpll2_err_polarity** Default Value: **0x05** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:1	Reserved	Leave as default
0	DPLL2 Error Polarity	See Description for DPLL0

Register_Address: **0x2AB** Register Name: **dpll2_buf_fill_misc_ctrl** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:2	Reserved	Leave as default
1	Zero-error compensation	See Description for DPLL0
0	Damping Correction Control	See Description for DPLL0

Register_Address: **0x2AC** Register Name: **dpll2_buf_fill_misc_ctrl2** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:3	Reserved	Leave as default
2:0	Buffer Fill Quarter Size	See Description for DPLL0

Register_Address: **0x2B0** Register Name: **dpll3_buff_fill_ctrl** Default Value: **0x96** Type:**R/W**		
Bit Field	Function Name	Description
7:6	Related synthesizer output	See Description for DPLL0
5:2	Buffer level input gain	See Description for DPLL0
1:0	Level format	See Description for DPLL0

Register_Address: **0x2B1:0x2B4** Register Name: **dpll3_buff_fill_offset** Default Value: **0x00000100** Type:**R/W**		
Bit Field	**Function Name**	**Description**
31:0	Buffer Level Offset Value	See Description for DPLL0

Register_Address: **0x2B5** Register Name: **dpll3_ext_divider** Default Value: **0x02** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	External division rate in powers of two	See Description for DPLL0

Register_Address: **0x2B6** Register Name: **dpll3_inp_freq_mon_limit** Default Value: **0x05** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:3	Reserved	Leave as Default
2:0	Input frequency monitor limit	See Description for DPLL0

Register_Address: **0x2B7**
Register Name: **dpll3_inp_freq_mon_time**
Default Value: **0x07**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	Input reference monitor time	See Description for DPLL0

Register_Address: **0x2B8**
Register Name: **dpll3_out_freq_mon_limit**
Default Value: **0x0D**
Type:**R/W**

Bit Field	Function Name	Description
7:5	Reserved	Leave as default
4:0	Output frequency monitor limit	See Description for DPLL0

Register_Address: **0x2B9**
Register Name: **dpll3_attenuation**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Additional attenuation applied to the buffer fill error	See Description for DPLL0

Register_Address: **0x2BA**
Register Name: **dpll3_err_polarity**
Default Value: **0x05**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	DPLL3 Error Polarity	See Description for DPLL0

Register_Address: **0x2BB** Register Name: **dpll3_buf_fill_misc_ctrl** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default
6	Buffer Fill Holdover Exit Condition	See Description for DPLL0
5:4	Buffer Fill Holdover Entry Condition	See Description for DPLL0
3:2	Reserved	Leave as default
1	Zero-error compensation	See Description for DPLL0
0	Damping Correction Control	See Description for DPLL0

Register_Address: **0x2BC** Register Name: **dpll3_buf_fill_misc_ctrl2** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:3	Reserved	Leave as default
2:0	Buffer Fill Quarter Size	See Description for DPLL0

Register_Address: **0x2C0** Register Name: **buf_fill_irq_mask** Default Value: **0x05** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	Buffer Fill IRQ Mask	When set, these bits will allow appropriate status bit from buffer_fill_status register to appear on the selected IRQ line. Selection: Bit 0 – DPLL0 input frequency failure mask Bit 1 – DPLL1 input frequency failure mask Bit 2 – DPLL2 input frequency failure mask Bit 3 – DPLL3 input frequency failure mask Bit 4 – DPLL0 output frequency failure mask Bit 5 – DPLL1 output frequency failure mask Bit 6 – DPLL2 output frequency failure mask Bit 7 – DPLL3 output frequency failure mask

Register_Address: **0x2C1** Register Name: **buff_fill_status** Default Value: **0x00** Type:**R**		
Bit Field	**Function Name**	**Description**
7:0	Buffer Fill Status	When set by device, these bits represent reference failure status. Selection: Bit 0 – DPLL0 input frequency failure status Bit 1 – DPLL1 input frequency failure status Bit 2 – DPLL2 input frequency failure status Bit 3 – DPLL3 input frequency failure status Bit 4 – DPLL0 output frequency failure status Bit 5 – DPLL1 output frequency failure status Bit 6 – DPLL2 output frequency failure status Bit 7 – DPLL3 output frequency failure status

Register_Address: **0x2C2** Register Name: **dpll0_fast_lock_ctrl** Default Value: **0x10** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:1	Reserved	Leave as default
0	fast_lock_master_enable	This bit is the master-enable control for the fast-lock feature for DPLL0. 0 - Feature disabled (default) 1 - Feature enabled

Register_Address: **0x2C5** Register Name: **dpll1_fast_lock_ctrl** Default Value: **0x10** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:1	Reserved	Leave as default
0	fast_lock_master_enable	This bit is the master-enable control for the fast-lock feature for DPLL1.

Register_Address: **0x2C8**
Register Name: **dpll2_fast_lock_ctrl**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	fast_lock_master_enable	This bit is the master-enable control for the fast-lock feature for DPLL2.

Register_Address: **0x2CB**
Register Name: **dpll3_fast_lock_ctrl**
Default Value: **0x10**
Type:**R/W**

Bit Field	Function Name	Description
7:1	Reserved	Leave as default
0	fast_lock_master_enable	This bit is the master-enable control for the fast-lock feature for DPLL3.

Register_Address: **0x2D4**
Register Name: **dpll0_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default

Register_Address: **0x2D4**
Register Name: **dpll0_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
3:0	Holdover Filter Value	This register specifies the holdover filter bandwidth. The default value of 0x00 means that the filter is bypassed. These are the possible settings (BW = 343/(2^n*2*pi) Hz): Setting BW 0x00 Bypass (default) 0x01 27.3 Hz 0x02 13.6 Hz 0x03 6.8 Hz 0x04 3.4 Hz 0x05 1.7 Hz 0x06 883 mHz 0x07 426 mHz 0x08 213 mHz 0x09 107 mHz 0x0A 53.3 mHz 0x0B 26.6 mHz 0x0C 13.3 mHz 0x0D 6.7 mHz 0x0E 3.3 mHz 0x0F 1.7 mHz

Register_Address: **0x2D5**
Register Name: **dpll1_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Holdover Filter Value	See description for register at address 0x2D4

Register_Address: **0x2D6**
Register Name: **dpll2_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Holdover Filter Value	See description for register at address 0x2D4

Register_Address: **0x2D7**
Register Name: **dpll3_holdover_filt_ctrl**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:4	Reserved	Leave as default
3:0	Holdover Filter Value	See description for register at address 0x2D4

Register_Address: **0x2FF**
Register Name: **page_sel_register**
Default Value: **0x00**
Type:**R/W**

Bit Field	Function Name	Description
7:0	Page Selection register	See description for register at address 0x07F

9.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	3.135	3.30	3.465	V
2	Core supply voltage	V_{CORE}	1.71	1.80	1.89	V
3	Operating temperature	T_A	-40	25	85	°C
4	Input voltage	V_{DD-IN}	2.97	3.30	3.63	V

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Power - Core

	Characteristics	Sym	Typ.	Units	Notes
1	Core supply current (Vcore)	I_{CORE} (V_{DD} 3.3V)	75	mA	
		I_{CORE} (V_{CORE} 1.8V)	242	mA	
2	Current for each HP Synthesis Engine	I_{SYN} (V_{DD} 3.3V)	54	mA	
		I_{SYN}(V_{CORE} 1.8V)	8	mA	

DC Electrical Characteristics - Power - High Performance Outputs

	Characteristics	Sym.	Typ.	Units	Notes
1	Power for each hpdiff clock driver	$P_{hpdiff}(V_{DD}$ 3.3V)	89	mW	Including power to biasing and load resistors
2	Power for each hpdiff clock driver minus power dissipated in the biasing and load resistors.	$P_{hpdiff}(V_{DD}$ 3.3V)	49	mW	Without power to biasing and load resistors
3	Power for each hpoutclk clock driver	$P_{hpout}(V_{DD}$ 3.3V)	23	mW	C_L = 5 pF f_{out} = 20 MHz

DC Electrical Characteristics - Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	$0.7 \cdot V_{DD}$			V	Excluding pins below
2	CMOS low-level input voltage	V_{CIL}			$0.3 \cdot V_{DD}$	V	Excluding pins below
3	CMOS Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Schmitt high-level input voltage for tck, pwr_b, sck_scl, trst_b	V_{SIH}	2.0			V	
5	Schmitt low-level input voltage for tck, pwr_b, sck_scl, trst_b	V_{SIL}			0.7	V	
6	Differential input common mode voltage	V_{CM}	1.1		2.0	V	
7	Differential input voltage difference	V_{ID}	0.25		1.0	V	

AC/DC Electrical Characteristics - Master Clock Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage (OSCi_3V3)	V_{CIH}	$0.7 \cdot V_{DD}$			V	
2	CMOS low-level input voltage (OSCi_3V3)	V_{CIL}			$0.3 \cdot V_{DD}$	V	
3	Input leakage current (OSCi_3V3)	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	CMOS high-level input voltage (OSCi_1V8)	V_{CIH}	1.37			V	
5	CMOS low-level input voltage (OSCi_1V8))	V_{CIL}			0.59	V	
6	Input leakage current (OSCi_1V8))	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V

AC/DC Electrical Characteristics - Master Clock Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
7	CMOS high-level input voltage (XOin)	V_{CIH}	2.0			V	
8	CMOS low-level input voltage (XOin)	V_{CIL}			0.8	V	
9	Input leakage current (XOin)	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
10	Duty Cycle		40		60	%	

DC Electrical Characteristics - High Performance Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPCMOS High-level output voltage	V_{OH}	$0.8*V_{DD}$			V	22 Ohms series C_L = 10 pF
2	HPCMOS Low-level output voltage	V_{OL}			$0.2*V_{DD}$	V	22 Ohms series C_L = 10 pF
3	LVPECL: High-level output voltage	V_{OH_LVPECL}	V_{DD} - 1.16		V_{DD} - 0.88	V	R_L = 50Ω to V_{DD} - 2V, C_L = 1pF
4	LVPECL: Low-level output voltage	V_{OL_LVPECL}	V_{DD} - 1.81		V_{DD} - 1.55	V	R_L = 50Ω to V_{DD} - 2V, C_L = 1pF
5	LVPECL: Differential output voltage*	V_{OD_LVPECL}	0.38		0.94	V	R_L = 50Ω to V_{DD} - 2V, C_L = 1pF

* IBIS model should be used to estimate differential output voltage for different trace lengths and different output frequencies.

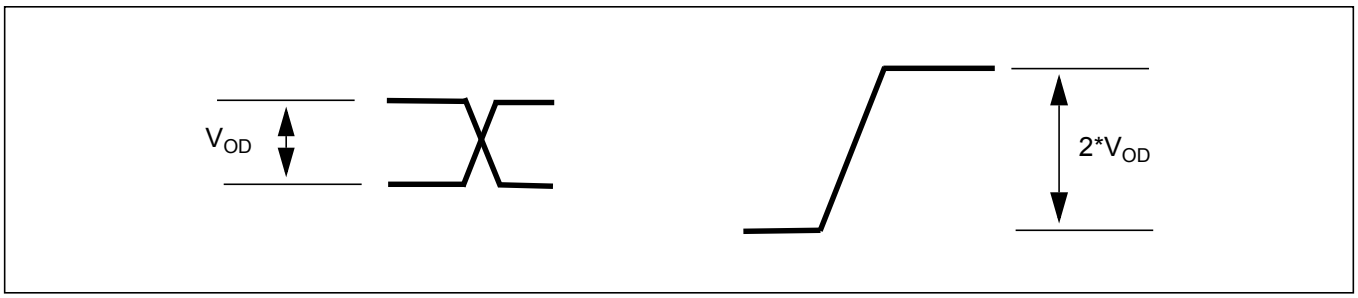


Figure 25 - Timing Parameter - Output Differential

AC Electrical Characteristics* -Output Timing Parameters Measurement Voltage Levels (see Figure 26)

	Characteristics	Sym.	CMOS	LVPECL	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$	$0.5*V_{DD}$	V_{DD}-1.35	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.8*V_{DD}$	$0.8*V_{OD\_LVPECL}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.2*V_{DD}$	$0.2*V_{OD\_LVPECL}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated

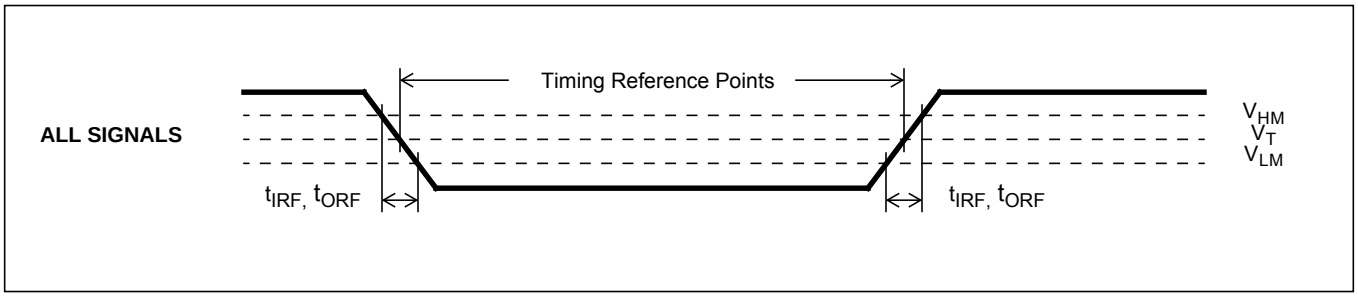


Figure 26 - Timing Parameter Measurement Voltage Levels

* Supply voltage and operating temperature are as per Recommended Operating Conditions

AC Electrical Characteristics* - Inputs (see Figure 27).

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference Frequency (CMOS Inputs)	$1/t_{REFP}$			177.5	MHz
2	Input reference Frequency (LVPECL Inputs)	$1/t_{REFP}$			750	MHz
3	Input reference pulse width high or low	t_{REFW}	0.55			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions

AC Electrical Characteristics* - Input To Output Timing (see Figure 27)

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference to hpoutclk0 (single-ended) output clock (with same frequency) delay	t_{HP_REFD}	-2	0	2	ns
2	Input reference to hpdiff0 (differential) output clock (with same frequency) delay	$t_{HP\_DIFF\_REFD}$	-1.2	0	1.6	ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

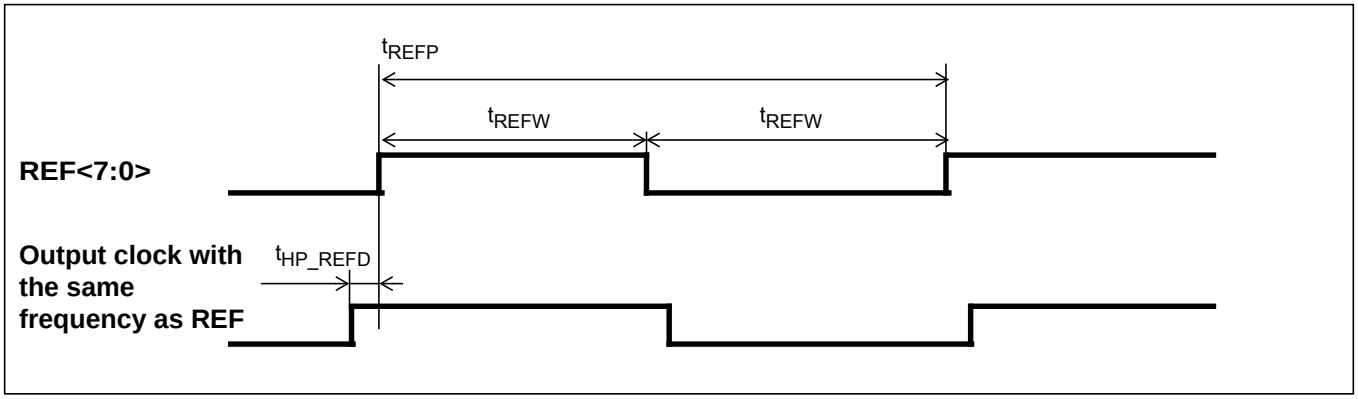


Figure 27 - Input To Output Timing for hpoutclk0

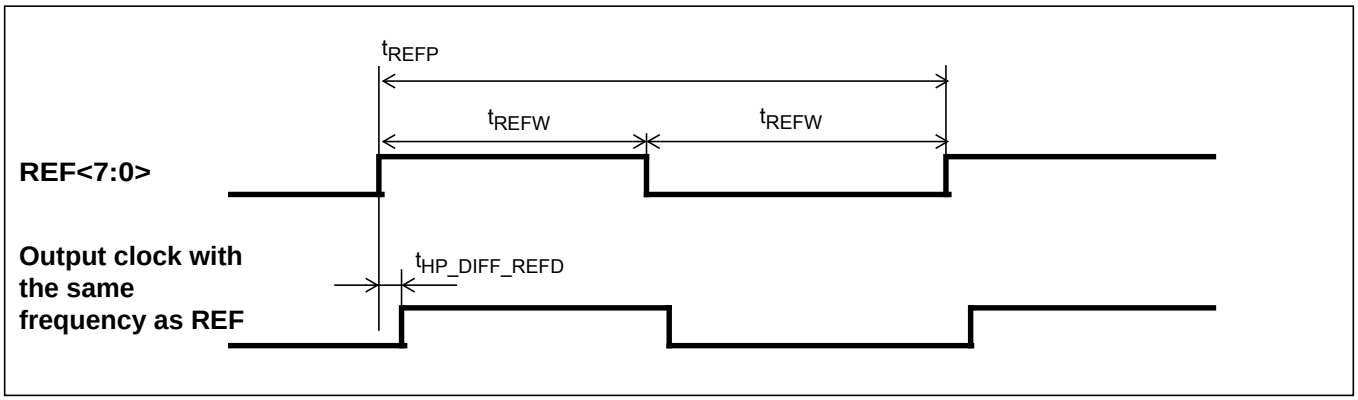


Figure 28 - Input To Output Timing To hpdiff0_P/N

AC Electrical Characteristics* - Outputs (see Figure 29).

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Clock skew between high performance outputs	$t_{OUT2OUTD}$	-2	0	2	ns	
2	Output clock Duty Cycle - hpdiff	t_{PWH}, t_{PWL}	45	50	55	Duty Cycle	RL = 50 ohm to V_{DD} - 2V C_L = 1pF
3	Output clock Duty Cycle - hpoutclk	t_{PWH}, t_{PWL}	40	50	60	Duty Cycle	22 ohm n series C_L = 10pF
4	hpdiff (LVPECL) Output clock rise or fall time	t_r / t_f	265		515	ps	
5	hpoutclk (LVCMOS) clock rise and fall time	t_r / t_f	620		1490	ps	10pF load
6	Output Clock Frequency (hpdiff)	F_{hpdiff}			750	MHz	
7	Output Clock Frequency (hpoutclk)	F_{hpout}			177.5	MHz	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

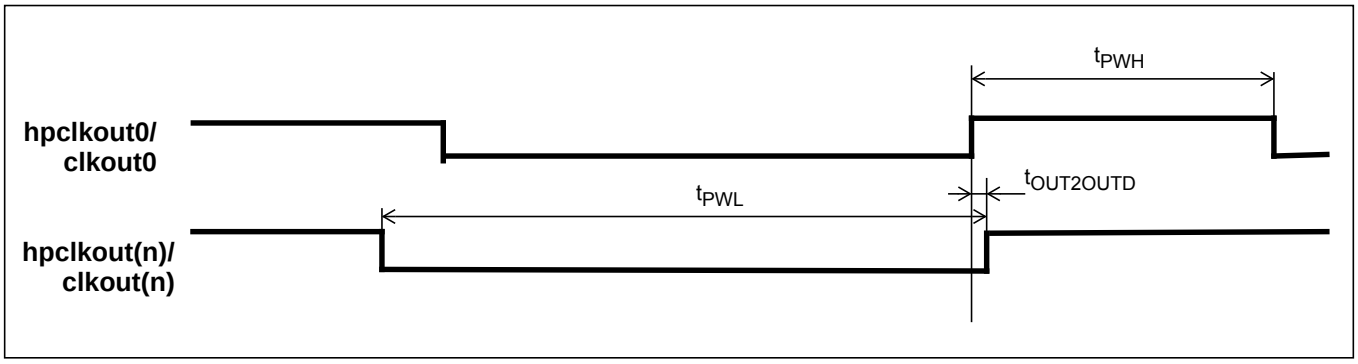


Figure 29 - Output Timing Referenced To hpclkout0/clkout0

Functional waveforms and timing characteristics for the LSB first mode are shown in Figure 30, and Figure 31 describe the MSB first mode. Table 8 shows the timing specifications.

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 8 - Serial Peripheral Interface Timing

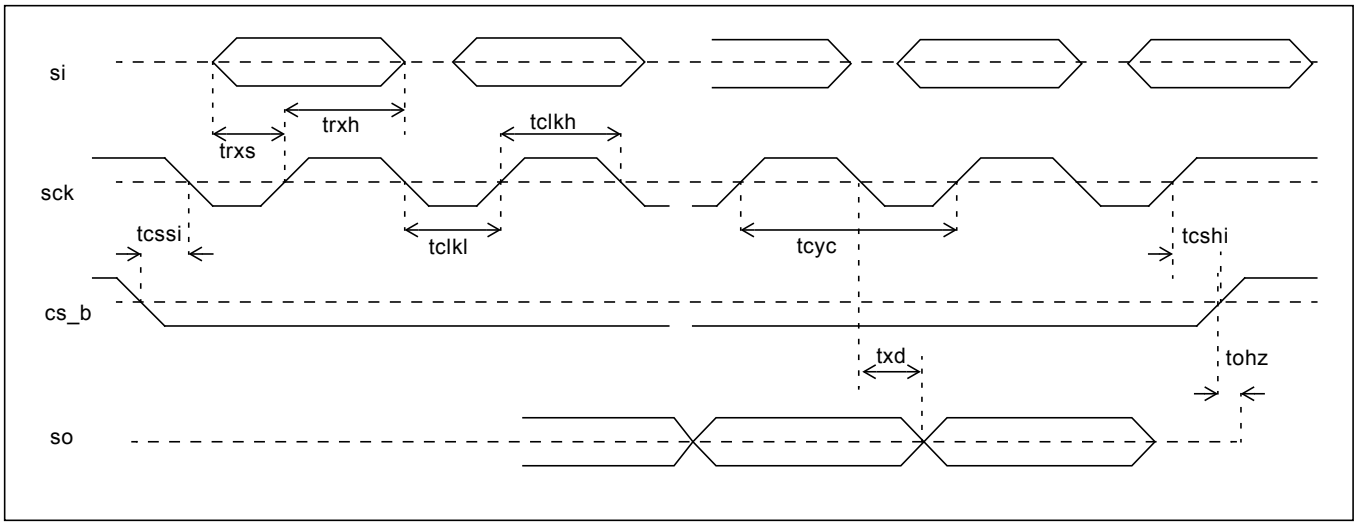


Figure 30 - Serial Peripheral Interface Timing - LSB First Mode

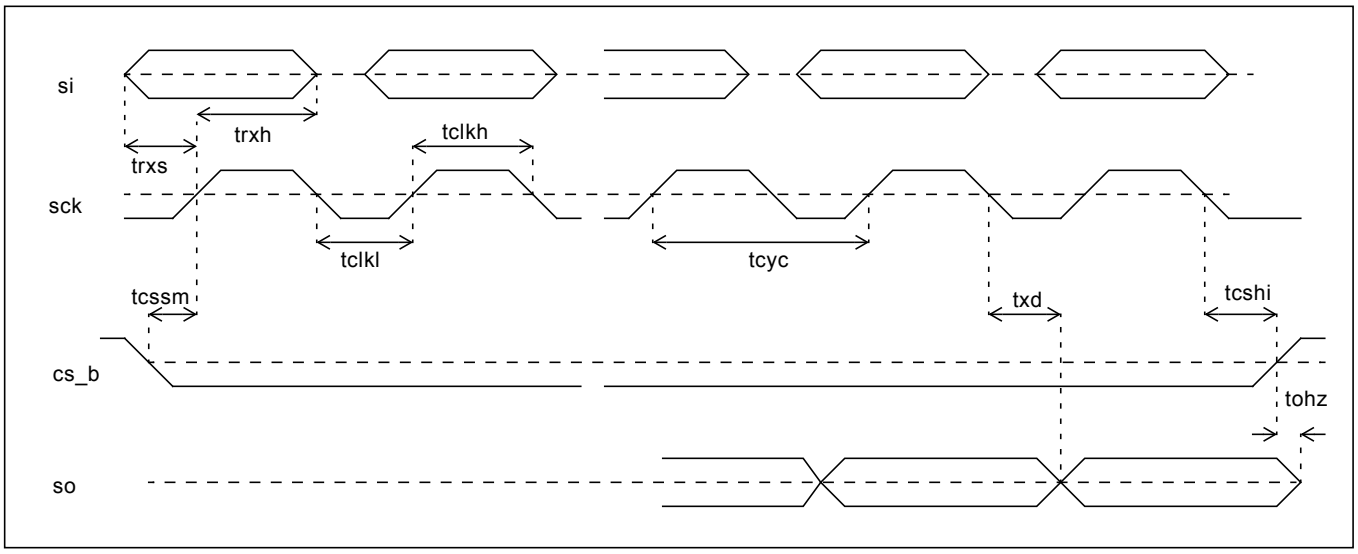


Figure 31 - Serial Peripheral Interface Timing - MSB First Mode

The timing specification for the I^2C interface is shown in Figure 32 and Table 9.

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by choice of pull-up resistor
Fall time	t_f	20 + $0.1C_b$		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 9 - I^2C Serial Microport Timing

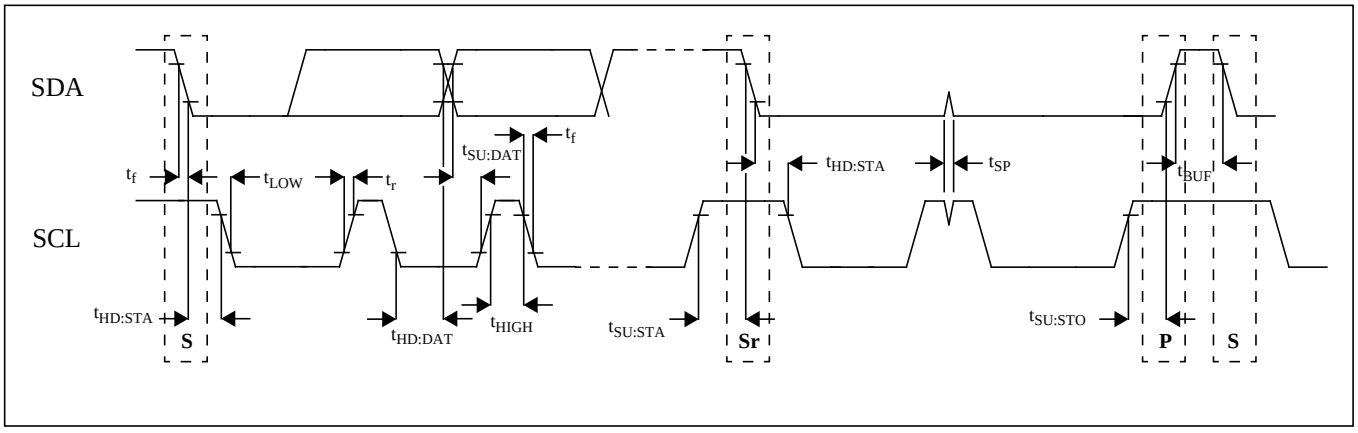


Figure 32 - I^2C Serial Microport Timing

10.0 Performance Characterization

10.1 Output Clocks Jitter Generation

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
622.08 MHz	12 kHz - 20 MHz	0.67	ps_{rms}	
	50 kHz - 80 MHz	0.63	ps_{rms}	

Table 10 - Jitter Generation Specifications - LVPECL Differential (HPDIFF) Outputs

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12 kHz - 5 MHz	0.74	ps_{rms}	
77.76 MHz	12 kHz - 20 MHz	0.97	ps_{rms}	
125 MHz	12 kHz - 20 MHz	1.10	ps_{rms}	
156.25 MHz	12 kHz - 20 MHz	0.97	ps_{rms}	

Table 11 - Jitter Generation Specifications - LVCMOS Single-ended (HPOUT) Outputs

10.2 DPLL Performance Characteristics

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in/Hold-in Range	+/-12		+/-2000	ppm	user selectable
2	Lock Time *			2	sec	For bandwidths of 5.2 Hz and above
3	Reference Switching MTIE			5	nsec	
4	Entry into Holdover MTIE			5	nsec	
5	Exit from Holdover MTIE			5	nsec	
6	Holdover Accuracy - jitter free input			10	ppb	
7	Holdover Accuracy - jittered input			50	ppb	

Table 12 - DPLL Characteristics

* Lock time of 1 sec is achieved when pulling a 9.2 ppm reference for any selected bandwidth and when phase slope limit is larger than 7.5 usec.

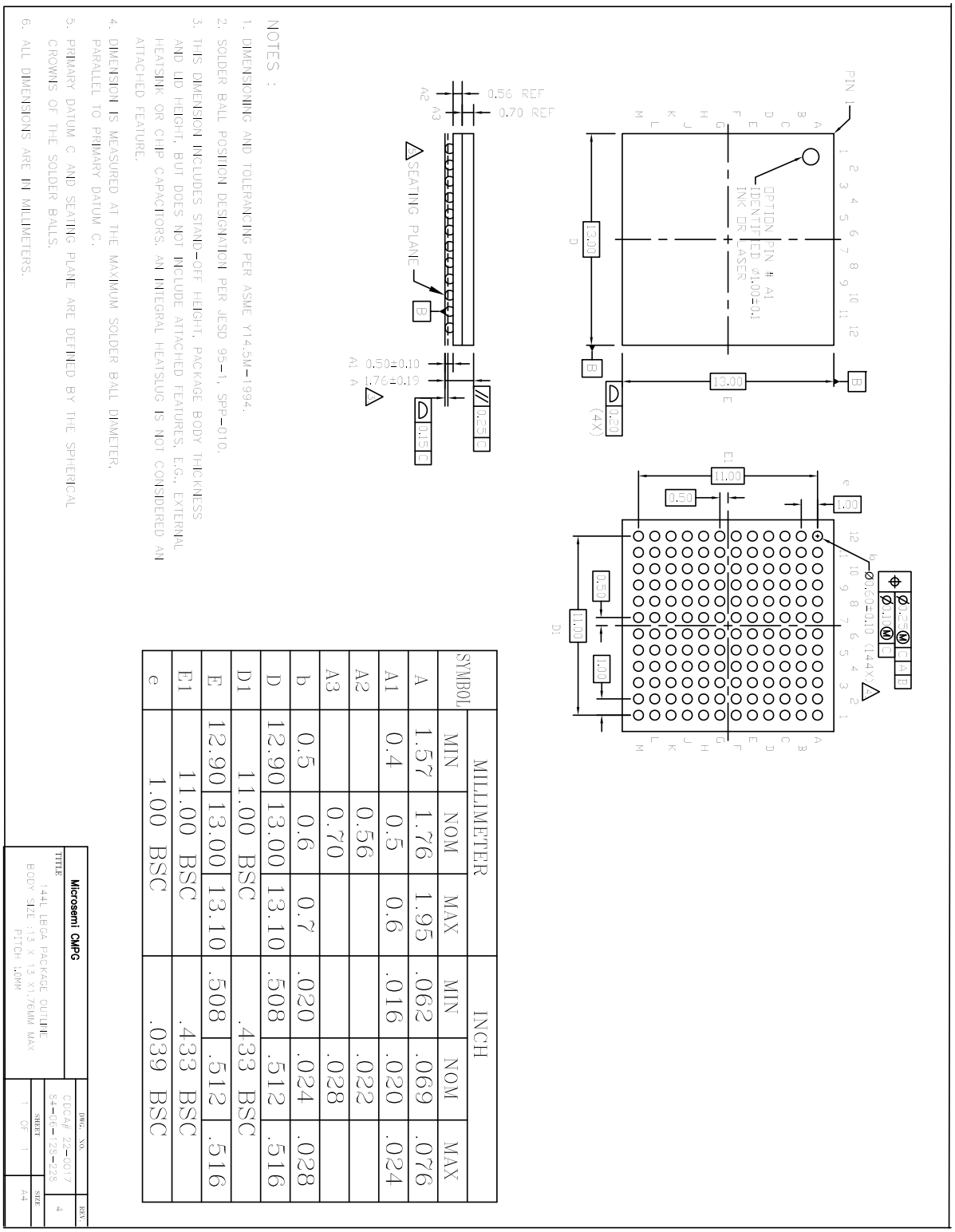
11.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	Still Air 1 m/s 2 m/s	21.3 19.0 17.8	^{o}C/W
Junction to Case Thermal Resistance	θ_{JC}		4.2	^{o}C/W
Junction to Board Thermal Resistance	θ_{JB}		10.1	^{o}C/W
Maximum Junction Temperature*	T_{jmax}		125	^{o}C
Maximum Ambient Temperature	T_{A}		85	^{o}C

Table 13 - Thermal Care

* Proper thermal management must be practiced to ensure that T_{jmax} is not exceeded.

12.0 Mechanical Drawing



NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.57	1.76	1.95	.062	.069	.076
A1	0.4	0.5	0.6	.016	.020	.024
A2		0.56			.022	
A3		0.70			.028	
b	0.5	0.6	0.7	.020	.024	.028
D	12.90	13.00	13.10	.508	.512	.516
D1		11.00 BSC			.433 BSC	
E	12.90	13.00	13.10	.508	.512	.516
E1		11.00 BSC			.433 BSC	
e		1.00 BSC			.039 BSC	

Microsemi CMPG

TITLE: 144L LBGA PACKAGE OUTLINE 13 X 13 X1.76MM MAX BODY SIZE PITCH 1.0MM

DWG. NO. CUCA# Z2-0017

REV. 4

SHEET 1 OF 1

SIZE A4

13.0 Package Markings

13.1 144-pin BGA. Package Top Mark Format

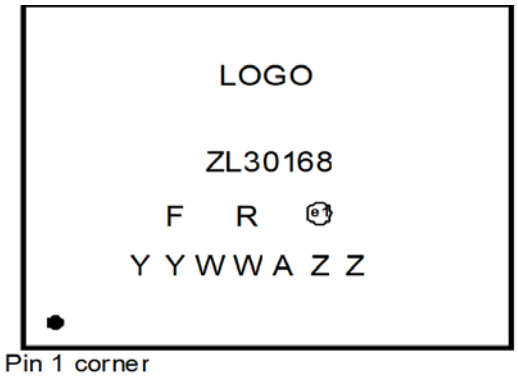


Figure 33 - Non-customized Device Top Mark

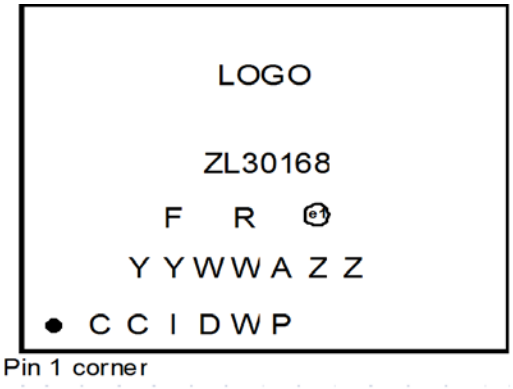


Figure 34 - Custom Factory Programmed Device Top Mark

Line	Characters	Description
1	ZL30168	Part Number
2	F	Fab Code
2	R	Product Revision Code
2	e1	Denotes Pb-Free Package
3	YY	Last Two Digits of the Year of Encapsulation
3	WW	Work Week of Assembly
3	A	Assembly Location Code
3	ZZ	Assembly Lot Sequence
4	CCID	Custom Programming Identification Code
4	WP	Work Week of Programming

Table 14 - Package Marking Legend

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