Quad Channel Clock Translator

Features

- Four independent OTN De-Synchronizers
- Excellent jitter performance of 180 fs rms in 12 kHz to 20 MHz band meets jitter requirements of 10G/40G and 100G PHYs
- Three programmable ultra-low jitter synthesizers generate frequencies from 1 Hz to 900 MHz.
- One programmable general purpose synthesizer generates any clock from 1 Hz to 180 MHz
- 6 differential (CML) or 12 single ended (CMOS) ultra-low jitter outputs plus two general purpose CMOS outputs
- Accepts up to 10 LVPECL/LVDS/HCSL/LVCMOS inputs

Ordering Information

ZL30174LDG6*	100 Pin aQFN Trays *Pb Free Tin/Silver/Copper

Package size: 10 x 10 mm

-40°C to +85°C

- Up to four programmable digital PLLs/NCOs with loop bandwidth from 14 Hz to 470 Hz synchronize to any clock rate from 1 kHz to 900 MHz
- Automatic hitless reference switching and digital holdover on reference fail with initial holdover accuracy better than 10 ppb

Applications

- OTN Transponders/Muxponeders
- OTN Switches
- Test Equipment

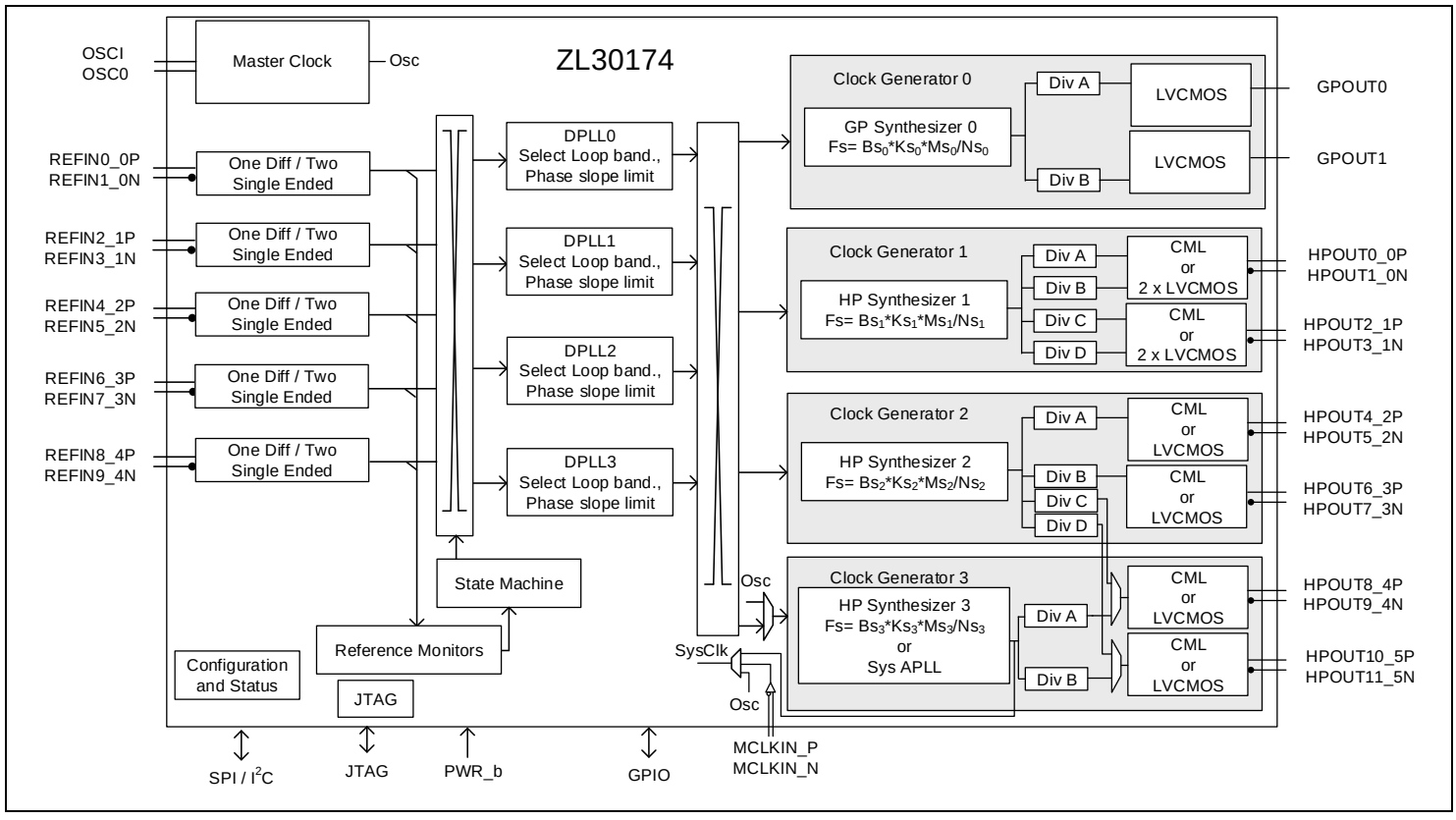

Figure 1. Functional Block Diagram

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5 Feature List

5.1 General features

- Four independent clock channels
- Operates from a single crystal resonator or clock oscillator
  - Supports split XO mode for low-frequency stability TCXO/OCXO with ultra-low jitter clock outputs
- Configurable from SPI/I2C bus or from pre-configured flash memory

5.2 Electrical Clock Inputs

- Accepts up to 10 LVCMOS or 5 LVDS/HCSL/LVPECL/CML differential inputs
- Frequencies from 1 kHz to 180 MHz for LVCMOS
- Frequencies from 1 kHz to 900 MHz for LVDS/HCSL/LVPECL/CML
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities.
  - Each input reference has its own set of monitors which can be independently programmed.
  - Loss of signal (LOS)
  - Single Cycle Monitor (Triggers on glitches or variation in duty-cycle)
  - Coarse Frequency Monitor
  - Precise Frequency Monitor
- Programmable phase slope limiting down to 1 ns/s
- Locks to gapped clocks

5.3 Electrical Clock Engine

- Digital PLLs filter jitter from 14Hz up to 470 Hz
- Multiple modes of operation
  - Freerun
  - Forced holdover
  - Forced reference
  - Automatic
  - NCO
- Internal state machine automatically controls state
  - Locked
  - Acquiring
  - Holdover
- Automatic hitless reference switching and digital holdover on reference fail
- Programmable bandwidth
- Programmable damping & phase gain (gain peaking)
- Programmable lock and fast lock options
- Support for fast lock with lock times in seconds
- Support for hitless reference switching with typical performance 0.6 ns
- Holdover better than 1ppb with post holdover filter. Without the post holdover filter the initial holdover accuracy is better than 10ppb.
- Full rate conversion between input and output clock frequencies

5.4 Electrical Clock Generation

- Four programmable synthesizers
- Precision Synthesizers
  - Each ultra-low jitter output can be independently set to be differential (CML) or two CMOS
  - Six CML outputs
    - Generate clock rates from 1 Hz to 900 MHz
    - Jitter performance of 180 fs rms (12 kHz – 20 MHz)
    - Meets OC-192, STM-64, 1 GbE & 10 GbE interface jitter requirements
  - Twelve LVCMOS outputs
    - Generate clock rates from 1 Hz to 180 MHz
    - Jitter performance of 290 fs rms (12 kHz – 20 MHz)
- General Synthesizer
  - Two LVCMOS outputs
  - Generate clock rates from 1 Hz to 180 MHz
  - Jitter performance of 17 ps rms (12 kHz – 20 MHz
- Programmable output advancement to accommodate trace delays or compensate for system routing paths
- Each output has its own power supply pin which can be hooked to 3.3V, 2.5V or 1.8V supplies. Outputs may be disabled to save power

6 Companion Documentation

Application Notes

- ZLAN-442 Crystals and Oscillators for Next Generation Timing Solutions
- ZLAN-620 Precision Input-Output Alignment Process
- ZLAN-599 Jitter Measurements
- ZLAN-600 Cyle-to-Cycle & Periodic Jitter (PCIe Applications)
- ZLAN-517 Power Supply Decoupling and Layout Guidelines
- ZLAN-527 Assembly and PCB Layout Guidelines for DR aQFN100 Package

Evaluation & Demonstration Board (SyncE and clock input-output focused)

- ZLE30174 EVB (with schematic)
- ZLE30174 GUI
  - Windows register configuration tool
  - Generates Flash image configuration file
  - Generates raw register list configuration file
  - Includes useful power calculator for desired PLL configuration

7 Application Examples

ZL30174 is multifunctional device which can be used in many OTN applications. It provides three independent PLL channels which can synchronize to any input frequency from 1KHz up to 900MHz. ZL30174 can generate frequencies from 1Hz up to 180MHz for LVCMOS and up to 900MHz for CML outputs. Each channel is comprised of a DPLL and a Synthesizer.

ZL30174 with its three ultra-low jitter channels can be used in OTN Transponder OTU-4 applications as shown in Figure 4. To simplify the block diagram ZL30174 is split into two blocks each containing one PLL. Each PLL here comprises of DPLL with sub 300Hz loop bandwidth as required by OTN specs and a Synthesizer used to generate required frequency with ultra-low jitter required by Serializers. The third ultra-low jitter synthesizer is used to generate system clock.

Figure 2 shows one channel (PLL0) used as De-Synchronizer to filter gapped OTN line clock. The gapped clock is generated in demapper justification block by removing pulses from the extracted OTN line clock. The gapped clock needs to be cleaned from jitter before it can be used to drive 100G Ethernet CAUI Serializers. The second PLL (PLL1) is used to drive OTN line. It can be set in a free run mode where the clock is synchronized to free run crystal oscillator used as ZL30174 master clock or the OTN line can be synchronized to 100G client by synchronizing PLL1 to the Ethernet clock as shown in Figure 2.

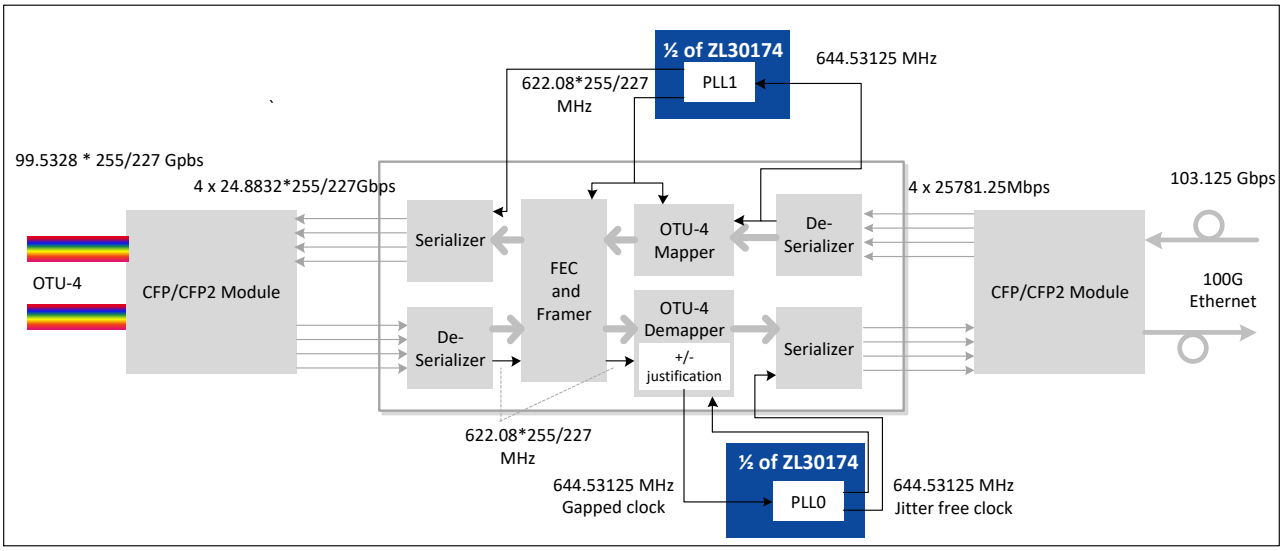


Figure 2. OTU-4 Transponder

An example of phase noise at the output of one of ultra-low jitter synthesizers is shown in following figure.

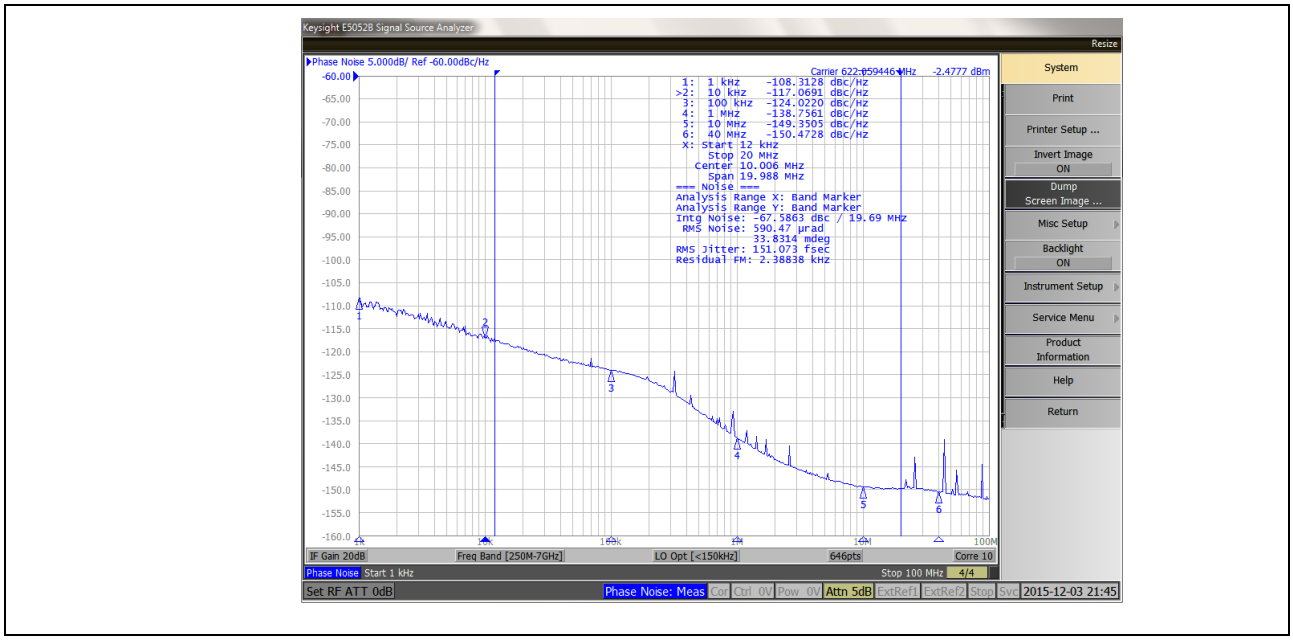


Figure 3. Phase noise plot for 622.08MHz output clock with 200MHz XO (151fs jitter in 12kHz to 20MHz band)

8 Pin Diagram

The device is packaged in a 10x10mm 100-pin aQFN.

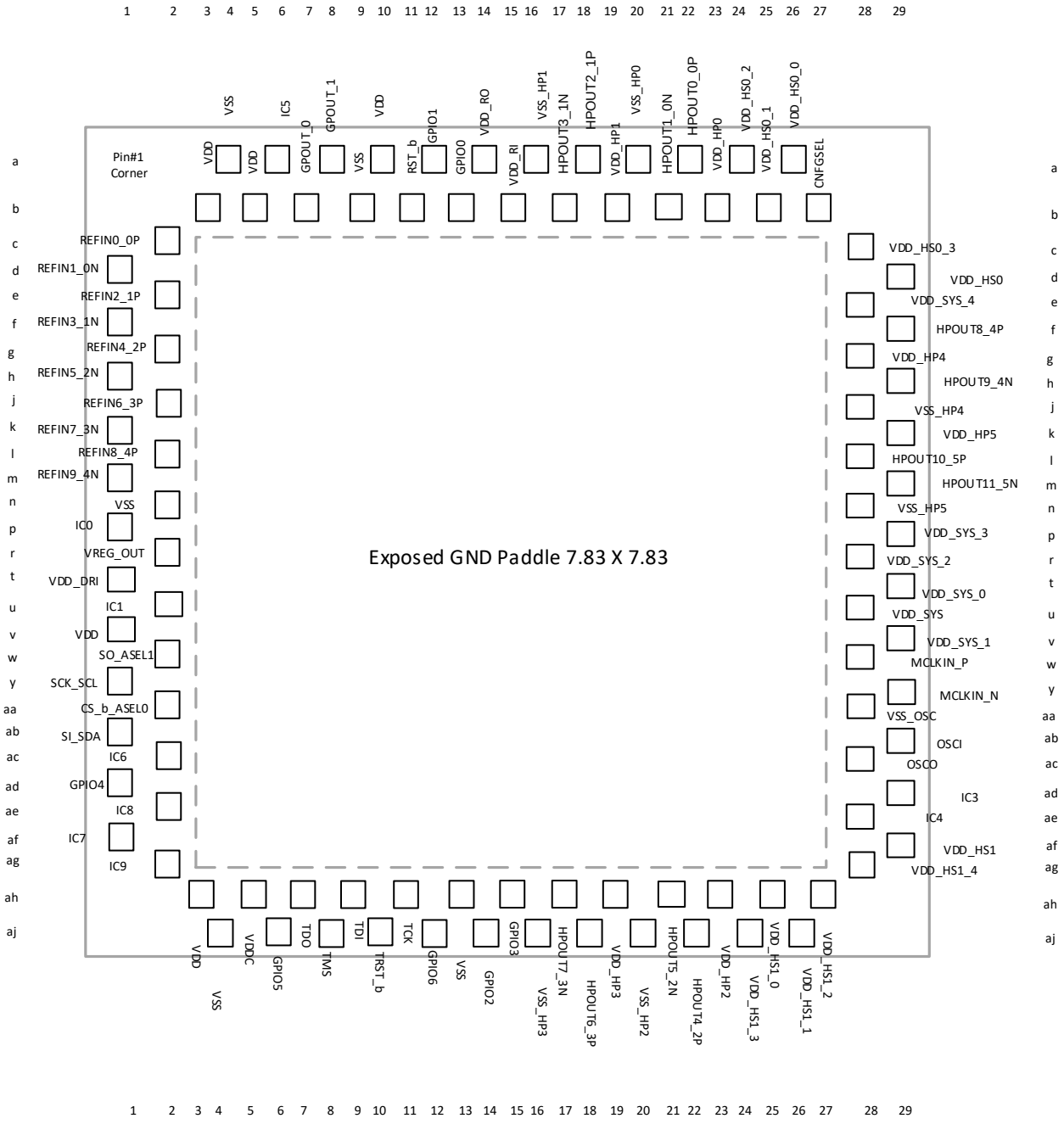


Figure 4. Pin Diagram

9 Pin Descriptions

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, I_{PU} – input with 50kΩ internal pull-up resistor, O – output, A – analog, P – power supply pin. All GPIO and SPI/I^2C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

Table 1 · Pin Descriptions

#	Name	I/O	Description
Input Reference			
C2 D1 E2 F1 G2 H1 J2 K1 L2 M1	REFIN0_0P REFIN1_0N REFIN2_1P REFIN3_1N REFIN4_2P REFIN5_2N REFIN6_3P REFIN7_3N REFIN8_4P REFIN9_4N	I	**Input References 0 to 9 (LVCMOS, LVDS, LVPECL, CML, HCSL).** These input references can accept up to ten single ended or up to five differential input signal sources used for synchronization. Each input pair can be programmed to be a differential input or two single ended inputs. Input frequency range for LVPECL, LVDS, HCSL, CML is from 1 kHz to 900 MHz Input frequency range for LVCMOS is from 1 kHz to 180 MHz.
Output Clocks			
A22 B21 A18 B17 AJ22 AH21 AJ18 AH17 F29 H29 L28 M29	HPOUT0_0P HPOUT1_0N HPOUT2_1P HPOUT3_1N HPOUT4_2P HPOUT5_2N HPOUT6_3P HPOUT7_3N HPOUT8_4P HPOUT9_4N HPOUT10_5P HPOUT11_5N	O	**High Performance (Ultra Low Jitter) Outputs 0 to 11 (CML or LVCMOS)** Each output pair can be configured to be CML differential output or two independent LVCMOS outputs. CML output frequency range is from 1 Hz to 900 MHz. LVCMOS output frequency range is from 1 Hz to 180 MHz
B7 A8	GPOUT0 GPOUT1	O	**General Purpose Outputs 0 to 1 (LVCMOS).** LVCMOS output frequency range is from 1 Hz to 180 MHz
Control and Status			
B11	RST_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The RST_b pin should be held low for 2 ms. This pin is internally pulled-up to V_{DD}. User can access device registers either 500 ms after RST_b goes high, or after bit 7 in register at address 0x00 goes high which can be determined by polling address 0x00.

B13 A12 AJ14 AH15 AD1 AJ6 AJ12	GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6	I/O	**General Purpose Input and Output pins.** These are general purpose pins managed by the internal processor based on device configuration. Recommended usage of GPIO include: DPLL lock indicators DPLL holdover indicators Reference fail indicators Reference select control or monitor Differential output clock enable (per output or as a bank of 2 or 4 outputs) High performance LVCMOS outputs enable Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR). Pins 6:0 are internally pulled down to GND. If not used GPIO can be kept unconnected. After power on reset, device GPIO[5:0] configure some of device basic functions, GPIO[4] sets SPI (low) or I2C (high) control mode, GPIO[3,0] and GPIO[5] set master clock rate selection. The GPIO[5:0] pins must be either pulled low or high with an external 1KΩ resistor as needed for their assigned functions at reset; or they must be driven low or high for 500ms after reset, and released and used for normal GPIO functions. Refer to section10.5.2 and Table 3 · for how GPIO[5,3,2,1,0] is used to set the master oscillator frequency.
B27	CNFGSEL	I	**Configuration Select.** This pin is three level input which selects one of three custom configurations on the power up. Custom configurations have to be pre-loaded by MSCC. If custom configurations are not loaded, this pin is ignored on the power up and the device registers are loaded with default values. Configuration / CNFGSEL 0 / GND 1 / V_{DD} (has to be pulled up with 4.7kΩ resistor) 2 / V_{DD} /2 or Open
Host Interface			
Y1	SCK_SCL	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. As an input this pin is internally pulled up to V_{DD}. In I2C mode this pin should be externally pulled high by 1KΩ to 5KΩ resistor.
AB1	SI_SDA	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}. In I2C mode this pin should be externally pulled high by 1KΩ to 5KΩ resistor.
W2	SO_ASEL1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I2C address select when host interface is configured for I2C mode.

AA2	CS_b_ASEL0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I2C address select when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}.
JTAG (IEEE 1149.1)			
AH7	TDO	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
AH9	TDI	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
AJ10	TRST_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be held low, or pulsed low on power-up, to ensure that the device is in the normal functional state. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
AH11	TCK	I	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
AJ8	TMS	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
AC28	OSCO	A-O	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to OSCI. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected. If OSCI is not used (MCLKIN is used) this pin is left unconnected.
AB29	OSCI	I	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to OSCO. For clock oscillator operation, this pin is connected to a clock source. Supported Crystal/Oscillator frequencies: 10 MHz, 20 MHz, 24.576 MHz, 25 MHz, 49.152 MHz, 50 MHz, 98.304 MHz, 100 MHz, 114.285 MHz,125 MHz. If 98.304 MHz, 100 MHz, 114.285 MHz or 125 MHz is available then the system PLL can be used as a third synthesizer. If OSCI is not used (MCLKIN is used), it should be pulled-up or pulled-down.
W28 Y29	MCLKIN_P MCLKIN_N	I	**Differential Oscillator Master Clock** This input is connected to a differential clock oscillator. Supported oscillator frequencies: 98.304 MHz, 100 MHz, 114.285 MHz, 125 MHz, 200 MHz. If the differential master clock input is not used, MCLKIN_P and MCLK_N should be pulled low.
Miscellaneous			
P1 A6 AC2 AF1 AG2	IC0 IC5 IC6 IC7 IC9	A-I/O	**Internal Connection** Leave unconnected.

AD29 AE28	IC3 IC4	I	**Internal Connection** Connect to GND.
U2 AE2	IC1 IC8	I	**Internal Connection** Pull-down with 1KΩ resistor or connect directly to ground.
Power and Ground			
T1	VDD_DRI	P	**Positive Supply Voltage.** Connect to +1.8V_{DC}. Associated with core operation (internal regulator block). Refer to section 10.6.5 for more details.
R2	VREG_OUT	P	**Positive Supply Voltage** Connect to an external capacitor to ground. Connect to an external 340Ω resistor to ground. Connect to an external 150Ω resistor to VDD_DRI (pin T1). 340Ω and 150Ω resistors are required only for devices with chip_revision_id equal to 0 or 1. For devices with chip_revision_id equal to 2 these resistors are optional. Refer to section 10.6.5 for more details. Associated with core operation (internal regulator block).
AH5	VDDC	P	**Positive Supply Voltage** Connect to VREG_OUT (pin R2). Associated with core operation.
V1 AH3 A10 B5 B3	VDD	P	**Positive Supply Voltage.** Connect to +2.5 V_{DC} or +3.3V_{DC}. Associated with Control & Status signals (GPIO[4:6]), Host Interface signals, JTAG signals, Input Reference signals, Output Clocks (GPOUT[0:1]) signals, and core operation.
A26 A24	VDD_HS0_0 VDD_HS0_2	P	**Positive Supply Voltage.** Connect to +1.8V_{DC}. Associated with core operation of synthesizer 1.
B25 C28	VDD_HS0_1 VDD_HS0_3	P	**Positive Supply Voltage.** Connect to +2.5 V_{DC} or +3.3V_{DC}. Associated with core operation of synthesizer 1. The choice of +2.5 V_{DC} or +3.3V_{DC} must be the same across all synthesizers.
D29	VDD_HS0	P	**Positive Supply Voltage** Connect to +2.5 V_{DC} if the device is powered by 1.8V_{DC} /+2.5 V_{DC}. Connect only to an external capacitor to ground if the device is powered by 1.8V_{DC} /+3.3 V_{DC}. Associated with core operation of synthesizer 1.
AH25 AJ26 AH27 AJ24	VDD_HS1_0 VDD_HS1_1 VDD_HS1_2 VDD_HS1_3	P	**Positive Supply Voltage.** Connect to +1.8V_{DC}. Associated with core operation of synthesizer 2.
AG28	VDD_HS1_4	P	**Positive Supply Voltage.** Connect to +2.5 V_{DC} or +3.3V_{DC}. Associated with core operation of synthesizer 2. The choice of +2.5 V_{DC} or +3.3V_{DC} must be the same across all synthesizers.
AF29	VDD_HS1	P	**Positive Supply Voltage** Connect to +2.5 V_{DC} if the device is powered by 1.8V_{DC} /+2.5 V_{DC}. Connect only to an external capacitor to ground if the device is powered by 1.8V_{DC} /+3.3 V_{DC}. Associated with core operation of synthesizer 2.
T29 V29	VDD_SYS_0 VDD_SYS _1	P	**Positive Supply Voltage.** Connect to +2.5 V_{DC} or +3.3V_{DC}. Associated with core operation of synthesizer 3 (system PLL). The choice of +2.5 V_{DC} or +3.3V_{DC} must be the same across all synthesizers.
R28 P29 E28	VDD_SYS _2 VDD_SYS _3 VDD_SYS_4	P	**Positive Supply Voltage.** Connect to +1.8V_{DC}. Associated with core operation of synthesizer 3 (system PLL)

U28	VDD_SYS	P	**Positive Supply Voltage** Connect to +2.5 V_{DC} if the device is powered by 1.8V_{DC} /+2.5 V_{DC}.Connect only to an external capacitor to ground if the device is powered by 1.8V_{DC} /+3.3 V_{DC}. Associated with core operation of synthesizer 3 (system PLL).
B23 B19 AH23 AH19 G28 K29	VDD_HP0 VDD_HP1 VDD_HP2 VDD_HP3 VDD_HP4 VDD_HP5	P	**Positive Supply Voltage** Connect to +1.8V_{DC} or +2.5 V_{DC} or +3.3 V_{DC} These pins are used to power high performance outputs. Each pin can be connected to different supply voltage.
B15	VDD_RI	P	**Positive Supply Voltage** Connect to the highest supply voltage: +2.5 V_{DC} or +3.3 V_{DC}. Associated with Control & Status signals (RST_b, GPIO[0:3]) and core operation (internal regulator block).
A14	VDD_RO	P	**Positive Supply Voltage.** Connect to +1.8V_{DC}. Associated with core operation (internal regulator block).
N2 AJ4 B9 A4 AH13	VSS	P	**Ground.** 0 Volts.
A20 A16 AJ20 AJ16 J28 N28	VSS_HP0 VSS_HP1 VSS_HP2 VSS_HP3 VSS_HP4 VSS_HP5	P	**Ground.** 0 Volts.
AA28	VSS_OSC	P	**Ground.** 0 Volts.
E-Pad	VSS	P	**Analog Ground.** 0 Volts.

10 Hardware Functional Description

10.1 Input References

10.1.1 Input Sources

The device has twelve input sources: ten input references (ten single ended or five differentials), and two oscillator clock sources (one single ended or one differential).

The device master clock frequency is configured on reset via external voltage levels on GPIO[5,3,2,1,0] pins as described in the pin description section.

The device synchronizes (locks) to any input reference which is a 1 kHz multiple, or it synchronizes (locks) to any input reference which is an M/N x 1 kHz multiple (FEC rate) where M and N are 16 bits wide. . In some cases M/N x 1 Hz, M/N x 10 Hz and M/N x 100 Hz is supported.

The device input reference frequency is programmed during initialization. The input reference frequency can be changed when the input reference is not the active source for a DPLL.

The device accepts an input reference with a maximum frequency of 180 MHz through single ended LVCMOS input or 900 MHz frequency through differential inputs.

If the frequency of an input reference exceeds 400 MHz, the reference must be internally divided by 2 before being fed to DPLL (Refer to **ref_config** registers).

10.1.2 Input Reference Monitoring

The input references are monitored by reference monitor indicators which are independent for each reference. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

10.1.2.1 Input Loss of Signal Monitor (LOS)

LOS is an external signal, fed to one of ZL30174 GPIO pins. LOS is typically generated by a PHY device whose recovered clock is fed to one of the reference inputs. The PHY device will generate a LOS signal when it cannot reliably extract the clock from the line. The user can set one of GPIO pins as a LOS input by programming corresponding GPIO register.

The GPIO inputs are read approximately every 10 ms, except with using system PLL bypass mode with 100 MHz oscillator where they are read approximately every 25 ms.

10.1.2.2 Input Coarse Frequency Monitor (CFM)

The CFM monitors the input reference frequency for 1.25 ms so that it can quickly detect large changes in frequency. CFM limit for each input reference can be selected in **ref_cfm** mailbox register with range from 0.1% to 50%. If the CFM limit is exceeded, then CFM failure is declared for corresponding reference.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

10.1.2.3 Input Precise Frequency Monitor (PFM)

The PFM block measures the frequency accuracy of the reference and updates the indicator bit. To prevent PFM from being false triggered by jitter/wander at the reference input, PFM averages frequency for more than 10 second period and indicate failure when the measured frequency exceeds limit specified in **ref_pfm_disqualify** register. To ensure an accurate frequency measurement, the PFM measurement interval is re-started if phase or frequency irregularities are detected by SCM or CFM. The PFM provides a level of hysteresis to prevent a failure indication from toggling between valid and invalid for input references that are on the edge of the acceptance range. . PFM limit should be set as described in **ref_pfm_disqualify** and **ref_pfm_qualify** mailbox registers.

When determining the frequency accuracy of the reference input, the PFM uses the external master clock oscillator's frequency as its reference. As a result, the actual acceptance and rejection frequencies can be offset with respect to the external oscillator's output frequency. This is accounted for in the acceptance and rejection requirements as described in Telcordia GR-1244 section 3.4.1. An example of the acceptance and rejection ranges for Stratum 3 application (acceptance in the range of +/- 9.2 ppm, rejection at +/- 12 ppm) given a +/- 4.6 ppm freerun frequency accuracy of a Stratum 3 reference oscillator is shown in Figure 5.

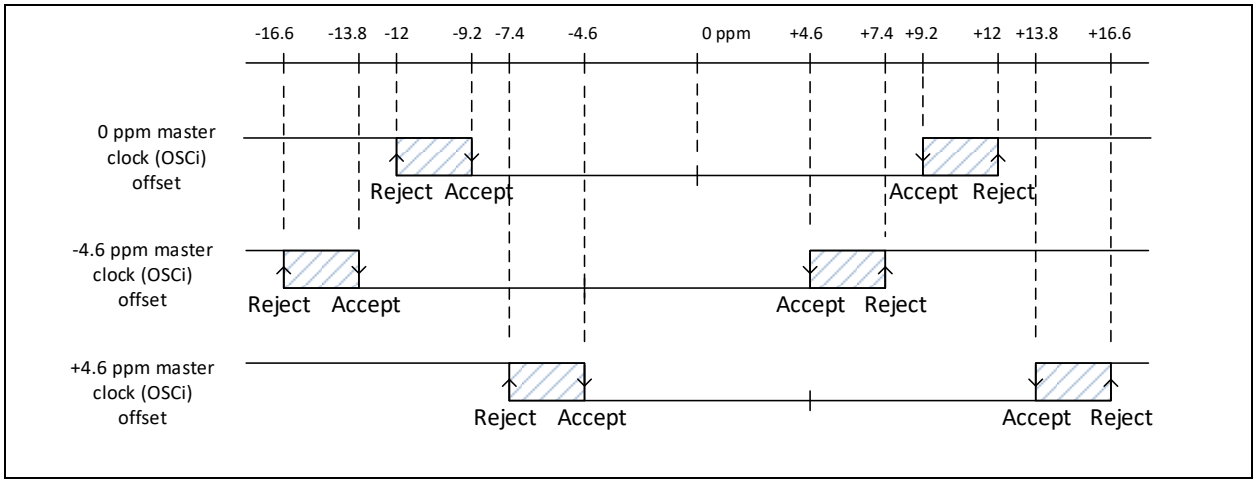


Figure 5. Stratum 3/G.8262 Option I Frequency Acceptance and Rejection Ranges

10.1.2.4 Input Single Cycle Monitor (SCM)

This detector measures the rising to rising edge and falling to falling edge periods of the input reference. If either exceeds the predefined SCM limit then a SCM failure is declared. The SCM limit for each input reference can be selected in the **ref_scm** mailbox registers with range from 0.1% to 50%. The limits are input frequency dependent. Please refer to the description in **ref_scm** mailbox register.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

For frequencies above 400 MHz, SCM (and the GST) should not be used.

10.1.2.5 Input Guard Soak Timer (GST)

When selected, the guard soak timer adds extra time to qualify and disqualify a reference. The default time to wait to qualify a reference is 50 ms after the CFM and SCM limits have been satisfied. When disqualifying a reference, the time starts after a CFM or SCM failure is detected and before the reference is disqualified. The default disqualification time is 4 times the qualification time. A PFM failure does not affect this timer.

When a reference is currently qualified and a failure occurs, the timer for disqualification is started. When the timer reaches the programmed threshold the reference is dis-qualified. If at any time between the starting of the timer and reaching the programmed threshold the input reference returns to a good state then the disqualification timer is reset.

When a reference is currently disqualified and the reference returns to good status, the timer for qualification is started. When the timer reaches the programmed threshold the reference is qualified. If at any time between the starting of the timer and reaching the programmed threshold the input reference returns to a failure state then the qualification timer is reset.

For frequencies above 400 MHz, the GST should not be used because the single cycle monitor (SCM) will never be valid.

It is possible to mask an individual reference monitor from triggering a reference failure by setting corresponding bits in **ref_mon_mask** register.

10.1.2.6 Input Reference Monitoring Interrupt Generation

Block diagram describing how reference monitoring block interact and how they generate an interrupt is shown in Figure 6. As can be seen from the block diagram the reference monitoring interrupt generation is separate from reference monitoring DPLL control which is described in the next section. The purpose of this is to allow user full flexibility during forced reference (manual) control.

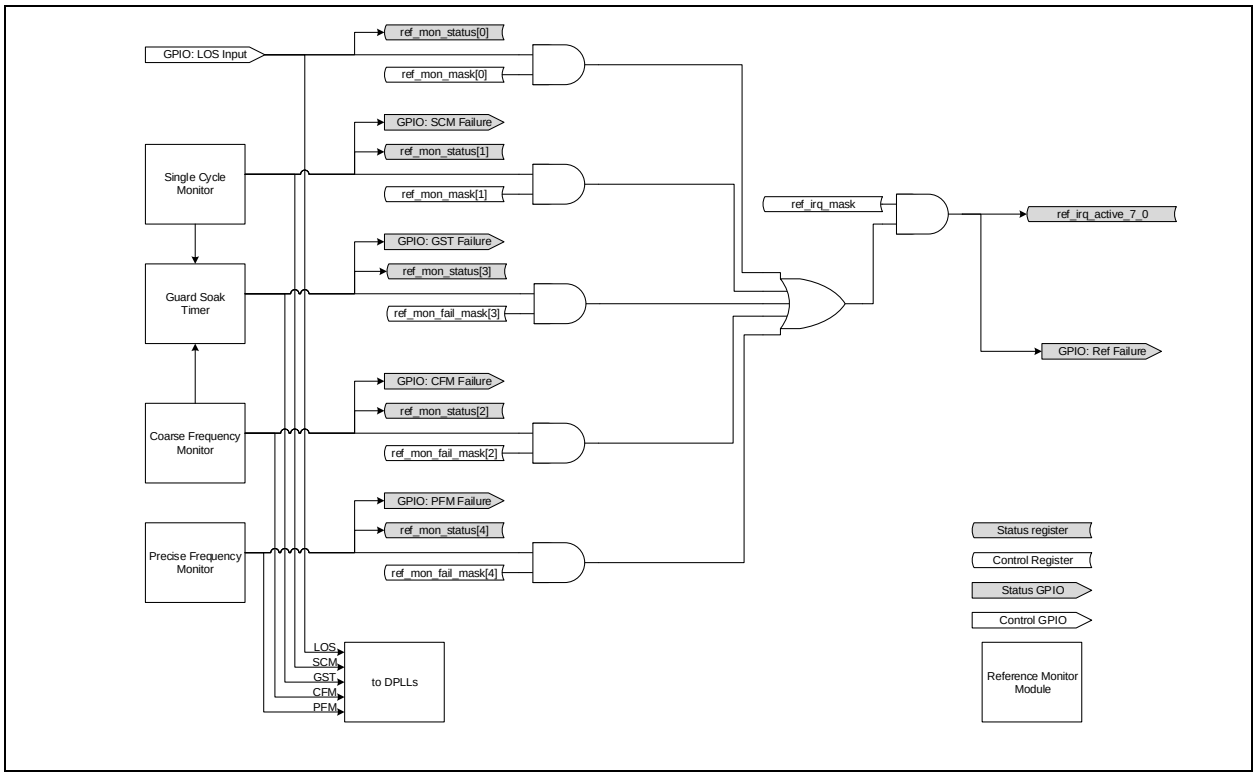


Figure 6. Reference monitoring interrupt generation

10.1.3 Input Gapped Clocks

The device supports locking to input gapped clocks.

10.1.4 Input Buffers

The device has ten single ended reference inputs REFIN[0:9] and each reference input pair REFIN[2n]/REFIN[2n+1]can be used as a differential input for the total of five differential inputs. By default all reference inputs are single ended. This can be changed by programming **ref_config** register.

Each input pair REFIN[2n]/REFIN[2n+1] can terminate two LVCMOS inputs, one differential input or two LVDS/LVPECL/HCSL inputs where only the positive signal of differential pair if fed to the input pins as shown in Figure 7.

Figure 7b shows how each input pair can terminate two LVCMOS inputs where the supply voltage of LVCMOS drivers is the same as the VDD of MSCC device (3.3V or 2.5V).

Figure 7c shows how to terminate two differential inputs by taking only the positive signal out of each differential pair. In this case the device's common mode voltage (VREF-PECL) is set at 55% of VDD so the common mode voltage will have to be created with external biasing resistors (10k in parallel with 12.7k) as in Figure 7c which shows an example how to terminate CML signals—CML drivers require 50 Ω pull-up resistors to VDD. For other differential formats 50 Ω resistors should be replaced with appropriate termination resistor(s): LVPECL with 127 Ω and 82 Ω resistors connected in Thevenin termination, source terminated HCSL does not need any termination and LVDS

with 100 Ω resistor between p and n. It should be noted that common mode voltage is different for differential input (Figure 7a) where it needs to be between 1.1V and 1.2V. If only one of the inputs in the P/N pair needs to be single ended LVPECL and the other needs to be set as a standard LVCMOS than single ended LVPECL should be connected to the N input and standard LVCMOS on the P input. If the second input is unused than it should be left unconnected.

Figure 7d shows how each input pair can terminate two LVCMOS inputs where the supply voltage of their drivers is lower than the VDD of MSCC device. This is very usefull in applications where input references are sources from a device with low output voltages (1.2V, 1.5V, 1.8V, or 2.5V). The input pair needs to be set into single ended LVPECL mode and the external Thevenin termination resistors (90 Ω and 110 Ω) need to provide biasing (55% of VDD) and 50 Ω transmission line termination. The series termination resistors Rs should be inserted at the source and the sum of their resistance and internal resistance of the driver should match the characteristic impedance of the transmission line (50 Ω). The table below Figure 7d provides commonly used values for series termination resistors but the user should always use the recommended serier termination for the particular driver.

The input frequency range for differential inputs (Figure 7a, Figure 7c and Figure 7d) is: 1 kHz to 900 MHz; for single LVCMOS ended inputs (Figure 7b) is: 1 kHz to 180 MHz.

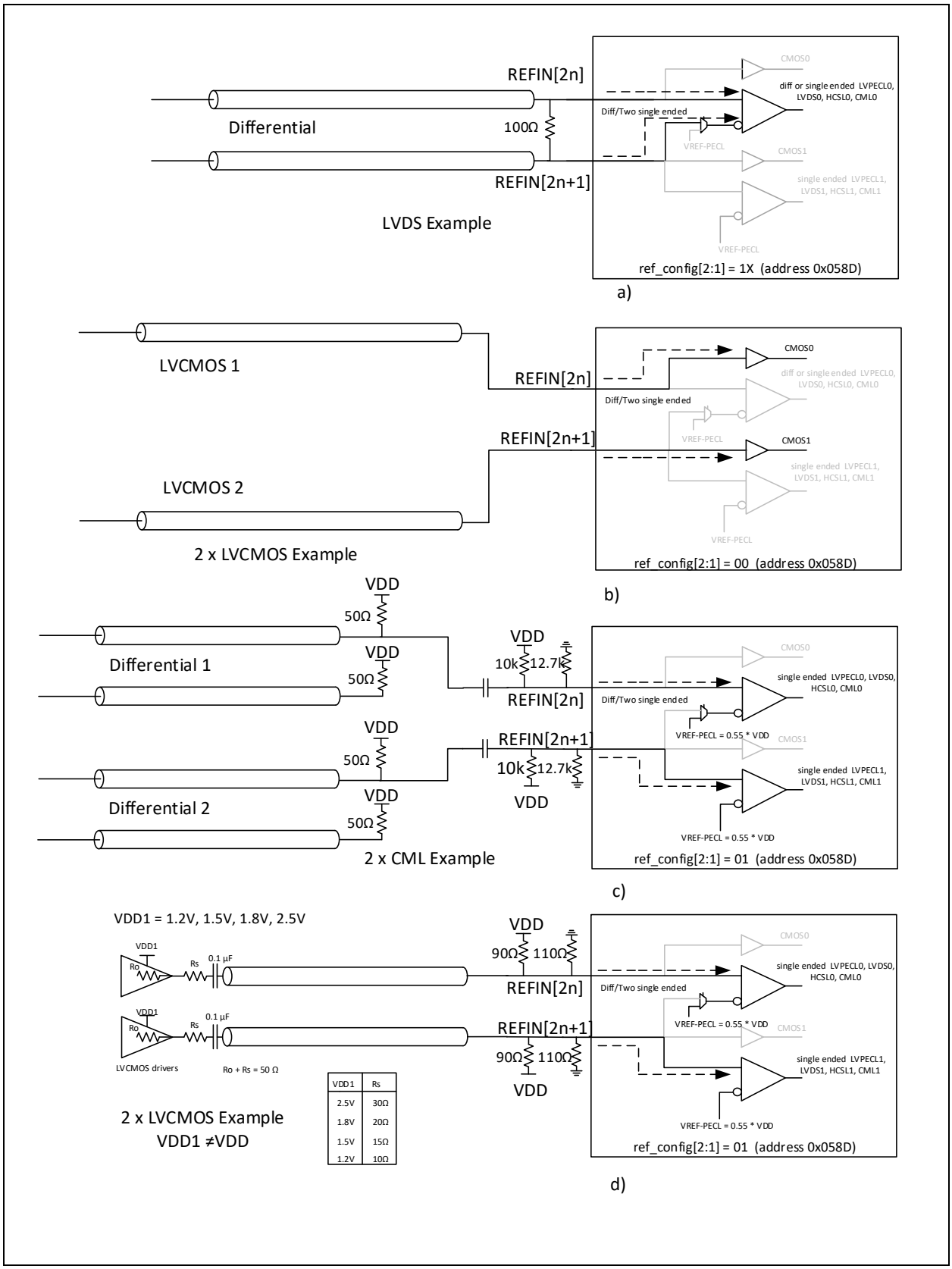


Figure 7. Input buffers & termination

When terminating LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC couple the LVPECL driver because differential inputs have different common mode (bias) voltage than LVPECL receivers as shown in Figure 8. Thevenin termination (182 Ω and 68 Ω resistors) provide 50 Ω equivalent termination as well as biasing of the input buffer for DC coupled line. For AC coupled line, Thevenin termination with 127 Ω and 82 Ω resistors should be used as shown in Figure 8. The value of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10 nF is good for input clock frequencies above 100 MHz. For lower clock frequencies capacitor values will have to be increased accordingly.

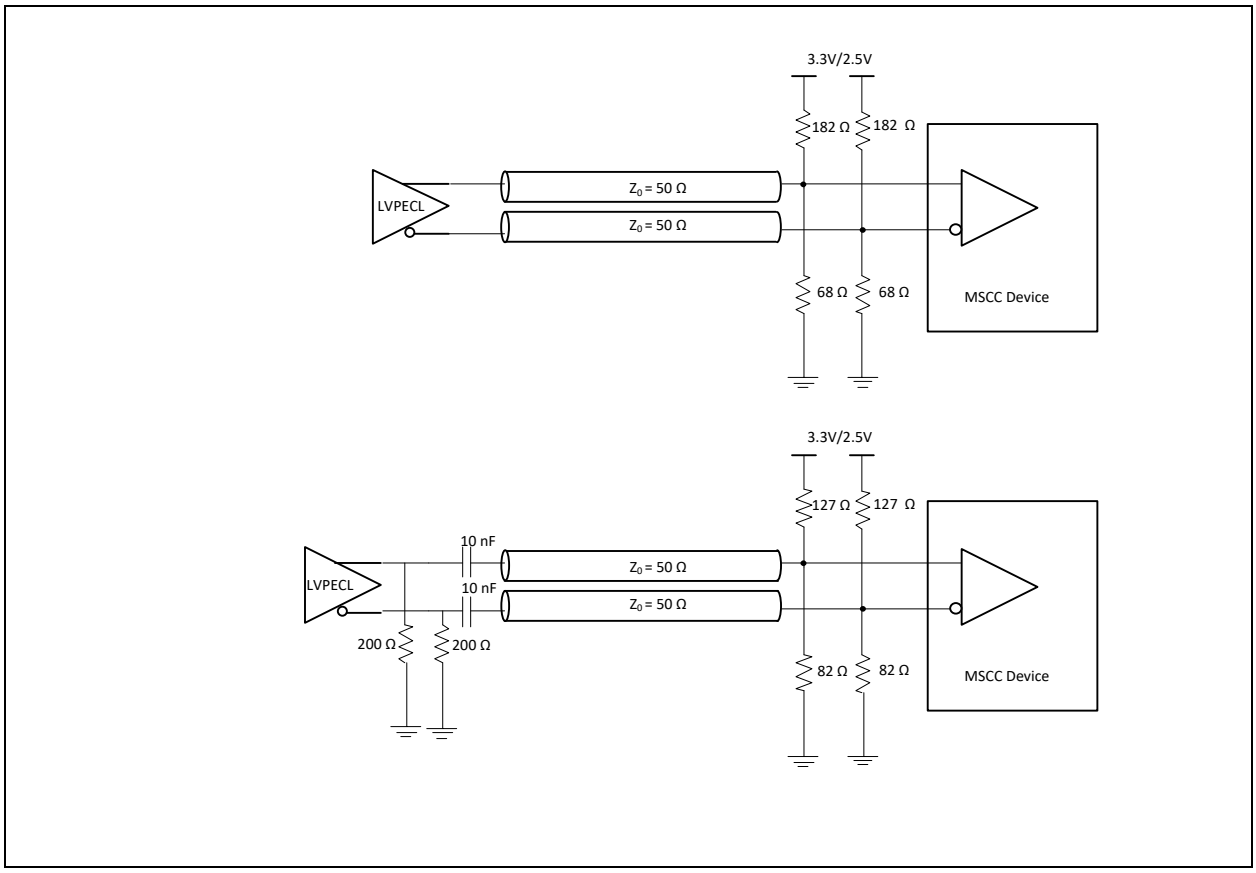


Figure 8. Differential DC and AC Coupled LVPECL Termination

Terminations for DC and AC coupled LVDS lines are shown in Figure 9. Differential input biasing is provided by LVDS driver in case of DC coupling whereas for AC coupling biasing is generated by 12 kΩ and 8.2 kΩ resistors. In both cases, the line is terminated with 100 Ω resistor.

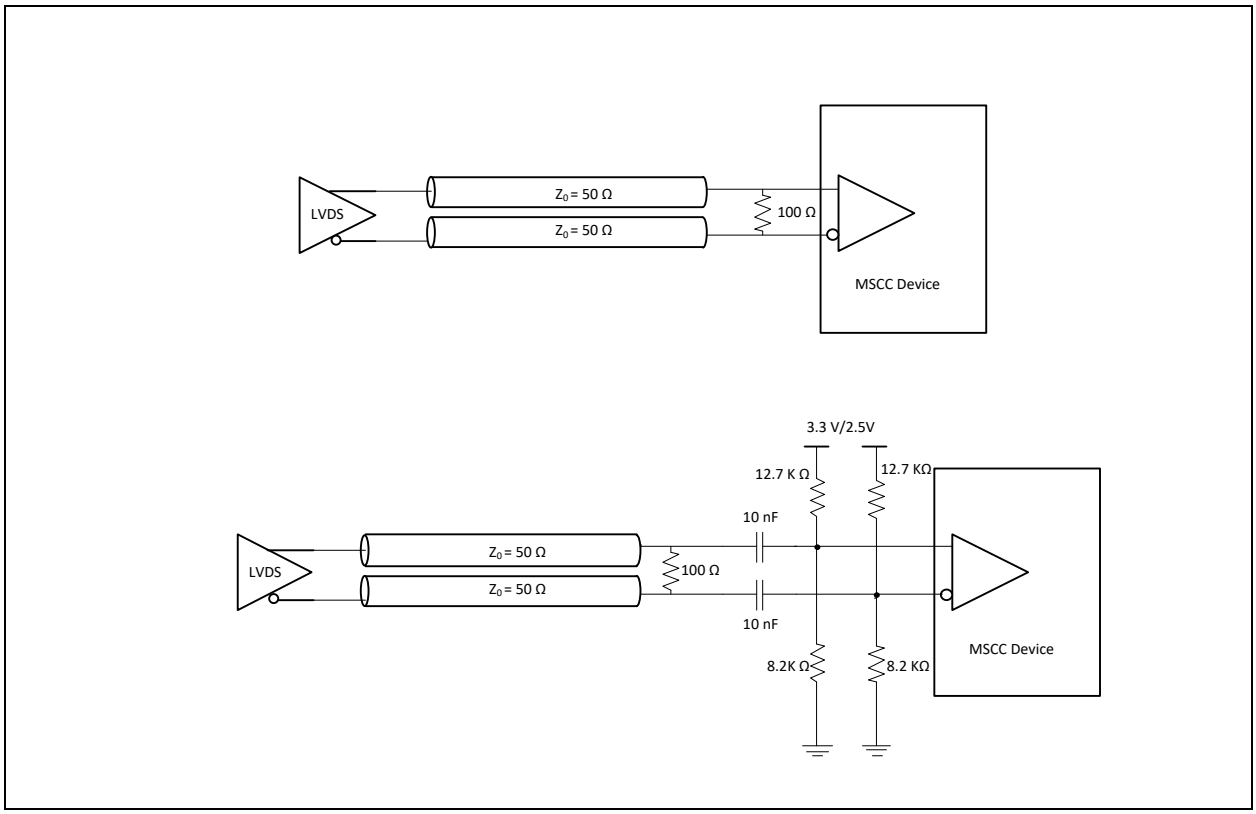


Figure 9. Differential DC and AC Coupled LVDS Termination

Transmission line should be terminated at the source with 22 Ω resistor as shown in Figure 10.

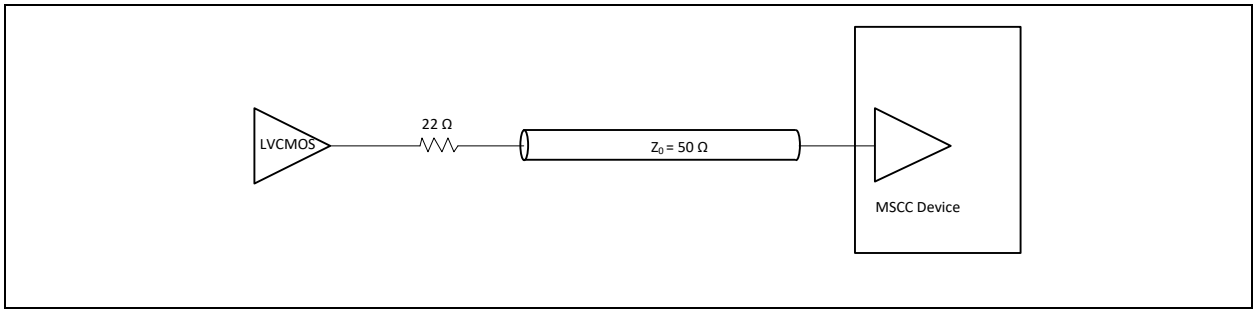


Figure 10. Single Ended LVCMOS Termination

10.2 Digital Phase Locked Loop (DPLL)

The device supports four independent digital PLL modules. All available DPLLs are enabled by default. Each DPLL can be enabled/disabled through the host registers.

10.2.1 DPLL Input Monitoring Masks

Each DPLL has its own reference switching (**dpll_ref_sw_mask**) and holdover (**dpll_ref_ho_mask**) mask mailbox registers which are used to prevent reference monitoring circuit form triggering DPLL to switch references or to go into the holdover state. Please note that the GST bit should not be unmasked (GST trigger enabled) without unmasking either the SCM or the CFM or both bits. The reference switching mask is used only in the automatic control mode. In forced reference mode this register is ignored. The holdover mask register is active in both: automatic and forced reference modes.
Refer to the **dpll_priority_1_0** through **dpll_priority_9_8** mailbox register,

10.2.2 DPLL Input Reference Priority

Every reference is assigned a local priority value (0 to 10) to allow system designers to specify the priority of each input references. The priorities are relative to each other, with lower value numbers being the higher priority. Value “1111" disables the ability to select the reference (i.e., don’t use for synchronization). If two or more inputs are given the same priority number, the input is selected based on the reference naming convention (i.e., ref0 is higher priority than ref1). The default reference selection priority is equal to its reference number (i.e., ref0 is highest priority and ref10 is the lowest priority).

When two references have the same priority they will not revert to each other (as reference availability change), but they will revert to a reference with a higher priority when it is available.

10.2.3 DPLL Input Pull-In, Hold-In Range

Pull-in/hold-in range is programmable in the **dpll_range** mailbox register. When the input reference input exceeds the pull-in hold-in limit a notification may be generated. Refer to **flhit** parameter in the register map.

10.2.4 DPLL Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, reference switching or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with input reference type.

10.2.5 DPLL Input Advance & Delay

The DPLL phase may be advanced or delayed in units of nanoseconds using **dpll_tie_data_x, dpll_tie_ctrl_x dpll_tie** and **dpll_tie_wr_thresh** mailbox registers. This phase adjustment feature acts as if the input signal was ahead or behind its true location by the programmed amount; therefore any changes to the phase adjustment are filtered through the DPLL bandwidth. There is no lifetime limit to the range. The value applied will be retained for all inputs and all modes of operation of the DLL, and is only cleared by the user.

10.2.6 DPLL Input Phase Slope Limiter

A sudden phase change at the input of the DPLL can occur due to reference rearrangement upstream the timing chain. While most modern devices (DPLL) can perform hitless switch between references, telecom standards (ITU-T G.8262 for example) provision for relatively large phase changes. For example ITU-T G.8262 Option 1, allows for up to 1000ns phase change within 15 second window (Requirement 11.1 Short-term phase transient response). The response of DPLL to such phase transient will be governed by the DPLL's loop bandwidth—narrower the loop bandwidth the slower the phase change at the output.

Some applications may be sensitive to fast phase transients and mitigating them with the DPLL loop bandwidth reduction may not be possible (the loop bandwidths are generally restricted to a specific range in compliance with a standard). In such cases MSCC device offers Phase Slope Limiter block which limits the slope of the phase change fed to the device.

The value of Phase Slope Limiter can be adjusted in **dpll_psl** mailbox register from 1ns/s to 65535ns/s. These low PSL values may be very useful to slow incoming clock transients, or to limit the frequency offset (compared with the master clock). Care must be taken when setting a low PSL value that the oscillator is sufficiently stable. Care must also be taken when wander transfer is important that the PSL does not impact any expected input-to-output wander transfer behavior.

When the input reference input exceeds the phase slope limit and the phase slope limit engages a notification may be generated. Refer to **pslhit** parameter in the register map.

10.2.7 DPLL Core Mode

The DPLL in the device support five modes: freerun, forced holdover, automatic, forced reference lock and numerically controlled oscillator (NCO). To lock the DPLL to a reference, automatic or forced reference mode should be used. In each of the locked modes, there are three states: acquiring, locked and holdover. The acquiring state is temporary state between the availability of a reference and the completion of the locking process. In the automatic mode, the DPLL may transition between the states depending on the availability of the references. In forced reference mode, the device will go into holdover if the reference selected is unavailable even if other references are available. The availability of a reference is determined by the reference qualification process. In the holdover mode or holdover state, the device provides output clocks which are not locked to an external reference signal, but are based on an estimate of the frequency during the previous time in the locked state. To force the DPLL into the holdover state even with good references present, the forced holdover mode is used.

In addition, the DPLL can be put into the freerun mode. This is used when the synchronization to a reference is not required or is not possible. Typically, this is used immediately following system power-up. In the freerun mode, the device provides timing and synchronization signals which are based on the master clock frequency only, and are not synchronized to the reference input signals. The freerun accuracy of the output clock is equal to the accuracy of the master clock. So if a ±20 ppm freerun output clock is required, the master clock must also be ±20 ppm.

The freerun mode:

- The DPLL has to generate all its output clocks based only on the device master clock input.
- The DPLL will not lock or switch to a reference or go into holdover.
- The reference switch mask and the reference holdover mask are ignored.

The forced holdover mode:

- All references are ignored and the DPLL has to go to holdover (based on last selected reference)
- The reference switch mask and the reference holdover mask are ignored.

The forced reference lock mode:

- The DPLL will try to lock to the host-specified reference.
- The reference switch mask is ignored. No reference switching will be performed.
- If the holdover mask is set, then the device will switch to holdover if the selected reference fails.
- If the holdover mask is not set, then the device will attempt to lock to the selected reference, even if it is failing one of the reference monitors. The input frequency tracking will be limited by the pull-in/hold-in settings of the DPLL.

The automatic mode:

- Reference selection and holdover is automatically handled by the device, based on the holdover and reference switch masks, and the reference priority.
- If the reference switch mask is set, then reference will be selected based on availability and priority. If all enabled references are bad, then the device will enter holdover.
- If holdover mask is set (and ref. switch mask cleared), then device switches to holdover on ref failure.
- If neither the reference switch nor the holdover masks are set, then device will keep trying to lock to a failed reference. The input frequency tracking will be limited by the pull-in/hold-in settings of the DPLL.

The NCO mode:

- The DPLL is run in freerun mode. The output clock is the requested synthesizer frequency with an offset specified by the **dpll_df_offset** register. This write-only register will change the output frequency of the DPLL.

10.2.8 DPLL Status Indicators

The DPLL provides lock and holdover indicators using the default lock indicator conditions. There are two major status indicators: LOL (Loss of Lock) and HO (Holdover) which may be used with the following truth table

nLOL	HO	State
0	1	Holdover
0	0	Acquiring
1	0	Locked

Table 2 · DPLL Status Indicators

10.2.9 DPLL Bandwidth (Jitter/Wander Transfer)

The DPLL loop bandwidth is programmable from 14 Hz to 470 Hz. The DPLL bandwidth is typically programmed during initialization. When changing the bandwidth dynamically, it is recommended to put the DPLL to Holdover mode first and then change the bandwidth. After the bandwidth has been changed, the DPLL should be set to the Normal mode.

Loop bandwidth is set by programming the **dpll_bw_fixed** mailbox register for one of five loop bandwidths: 14 Hz, 29 Hz, 61 Hz, 130 Hz, or 380 Hz. Additionally there is support for 470 Hz.

The DPLL locks to an input reference and provides a stable low jitter output clock when the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a DPLL fed with a 19.44 MHz reference can have loop bandwidth up to the maximum (470 Hz).For 1 kHz input reference, the DPLL loop bandwidth can be up to 14 Hz. For 8 kHz reference the recommended maximum loop bandwidth is 61 Hz.

10.2.10 DPLL Programmable Damping & Phase Gain

The device supports programmable damping & phase gain using the **dpll_damping** mailbox register. A common value would be the default value of 0x5 for gain peaking < 0.1 dB.

10.2.11 DPLL Lock Time

The lock time is dependent on employed loop bandwidth. The device has a lock time of less than 2sec for loop bandwidths larger or equal than 14 Hz and the phase slope limit set to unlimited. For the other loop bandwidths and phase slope limits please refer to DPLL Performance Characteristics* Table.

There is some configurability of the lock thresholds for phase stability and duration. Refer to **dpll_lock_phase** and **dpll_lock_period** mailbox registers for more details.

10.2.11.1 DPLL Fast Lock

It is recommended that the fast lock mode be enabled when phase slope limiting is used. It should be disabled with an unlimited PSL. This can be done in the **dpll_fast_lock_ctrl** mailbox register.

10.2.12 DPLL Hitless Reference Switching

Referring to Table 53 · the device is able to switch between input references with typical performance of 0.6 ns well below the ITU-T G.8262 specifications. Note that the device will transition through the holdover state when switching between input references. The switching between input references may be fully automated when an old input reference fails (is disqualified) and a new input reference is available (is qualified).

10.2.13 DPLL Holdover Capability

10.2.13.1 Holdover Stability

The DPLL initial holdover accuracy is documented in Table 53 · . The initial holdover accuracy depends on the core DPLL filter bandwidth as well as the additional holdover filter bandwidth and holdover storage delay.

- Initial accuracy of 2 ppb when the core DPLL filter bandwidth is higher (line card applications)

10.2.13.2 Hitless Entry & Exit from Holdover

Referring to Table 53 · the device has typical entry into holdover of 0.6 ns and typical exit from holdover of 0.6 ns, well below the ITU-T G.8262 specifications. The entry & exit into holdover may be fully automated when an old input reference fails (is disqualified) and a new input reference is available (is qualified).

10.2.13.3 Additional, Post-DPLL Holdover Options

In addition to the holdover benefits gained through the DPLL filter bandwidth there is a separate holdover filter bandwidth and holdover storage delay controlled using **dpll_ho_filter** and **dpll_ho_delay** registers.

The post-DPLL holdover filter bandwidth may be set very narrow even when the core DPLL bandwidth is higher or the local oscillator is less stable. The post-DPLL holdover filter bandwidth may be set as low as 1.7 mHz, which provides great benefits for holdover because the minimum loop bandwidth of the DPLL is 14 Hz.

The post-DPLL holdover storage delay is a history of the previous post-DPLL holdover filter bandwidth values. When the DPLL enters holdover it may use the most recently computed holdover value, or may go back in history to an earlier value. If a transient has just occurred on an input reference, causing the entry to holdover, it would be beneficial to use a holdover value that was computed before the start of the transient. Therefore the holdover storage delay is generally set based on the expected types of transients on the input references. Care should be taken not to go excessively back in time using the holdover storage delay register as the local oscillator may have drifted from that location due to temperature or ageing effects. The user may select a holdover storage value over one hour back in time

10.2.13.4 Additional, Post-DPLL Holdover Filter Details

If the input reference is noisy (have jitter and wander), the quality of holdover value will depend on jitter and wander and on loop bandwidth of the DPLL because the holdover value is taken from the DPLL low pass filter. Lower the loop bandwidth-better the attenuation of the noise and more accurate holdover value. As explained previously, narrower loop bandwidth require more stable (more expensive) master clock and require longer lock time. Holdover filter solves this problem because it is not part of the loop as shown in the simplified block diagram in Figure 11 so it can be freely adjusted without affecting any loop parameters.

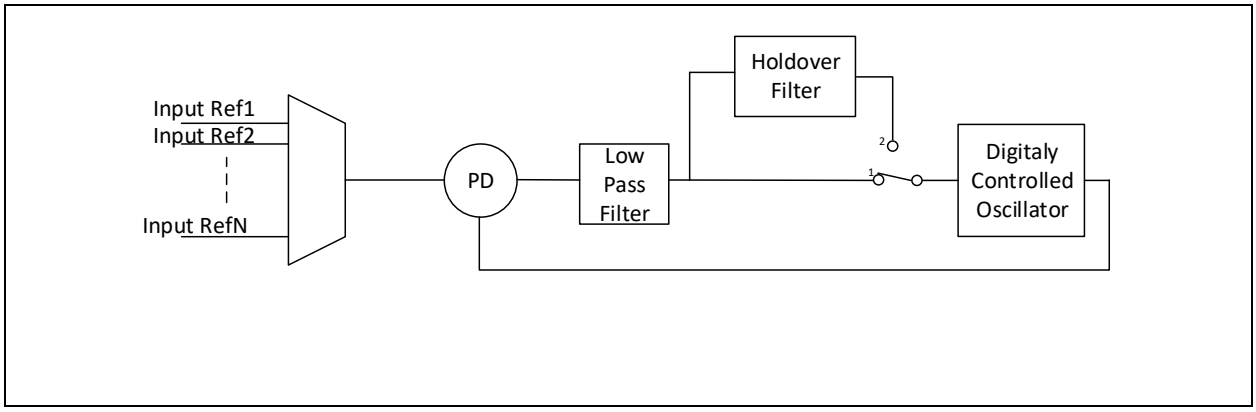


Figure 11. Simplified block diagram of the holdover filter

The functionality of the holdover filter can be illustrated with the following example.

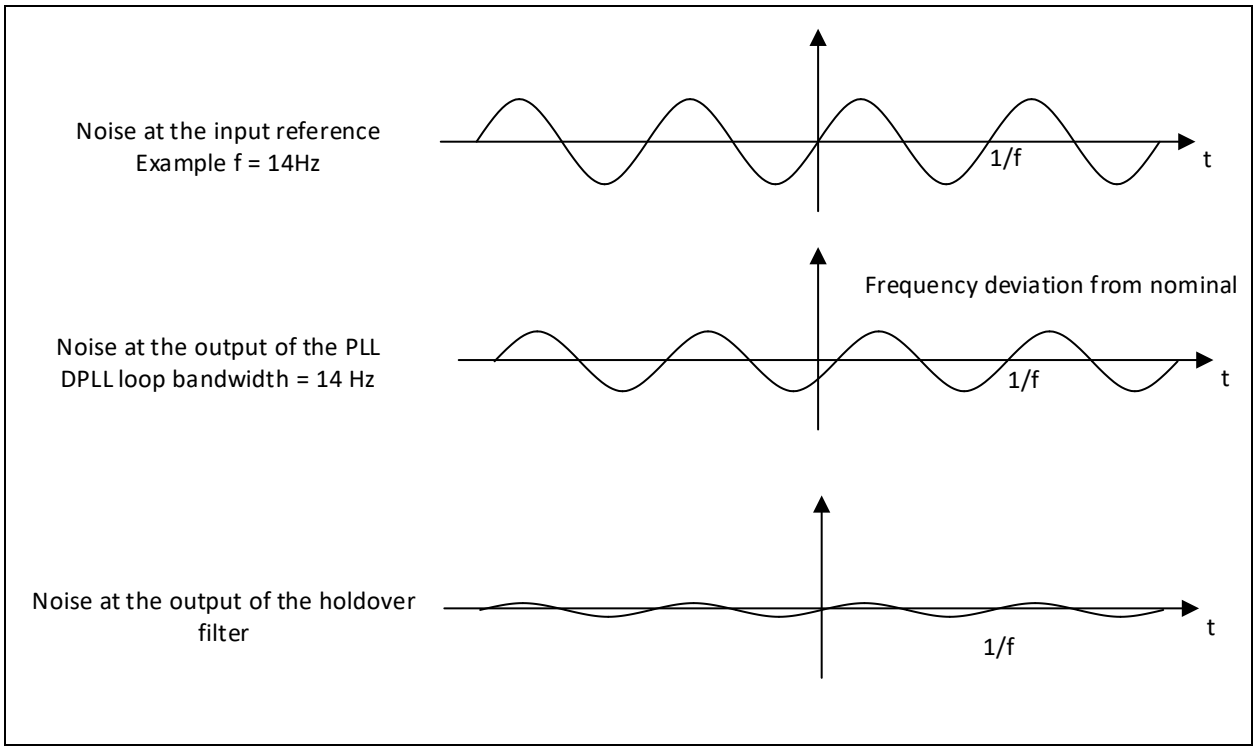


Figure 12. Benefits of holdover filter

If the input reference is modulated by a sine wave jitter, the instantaneous frequency of the input clock will also change in the sine wave fashion. This is shown in the top plot of the Figure 12. If the loop bandwidth of the DPLL is set to 14 Hz and if the jitter happens to have same frequency, the output of the DPLL will pass the jitter with 3dB attenuation and the output frequency will deviate 3dB less than the input frequency (middle plot). If the DPLL goes into holdover state its output frequency will be equal to the nominal frequency only at zero crossing of the sine wave which is highly unlikely. Hence assuming the jitter frequency is constant, the holdover value will depend on the amplitude of the input jitter—higher the amplitude lower the initial holdover accuracy. Deviation of the frequency can be calculated as

$$Dfm = \pi * fm * ja\ [\ in\ UIpp]$$

where the fm is frequency of the jitter (14 Hz in our example) and ja is jitter amplitude in unit intervals .

If we insert an additional filter (holdover filter) which is not part of the loop we will be to filter jitter without affecting the loop performance. Now when DPLL goes into holdover it will take value from holdover filter which is much more accurate (closer to nominal) than the value from the loop filter.

When holdover filter is enabled the Digitally Controlled Oscillator will use value from holdover filter (position 2 of the switch). Holdover filter bandwidth can be set in **dpll_ho_filter** mailbox register. If the value in this register is 0x00 the holdover filter is not used—holdover in this case is based on DPLL loop bandwidth.

10.2.13.5 User Holdover Compensation Support

The user may provide advanced holdover compensation schemes to reduce the effects of temperature variation or ageing of the local oscillator while in the holdover state or holdover mode. To support this operation the DPLL has several support tools.

During locked operation the user may read the core DPLL frequency offset. With this information the user may learn the ageing characteristics of the local oscillator. Additional, when combined with a temperature sensor, the user may learn the temperature characteristics of the local oscillator. Refer to **dpll_df_offset_x** and **dpll_df_ctrl_x** registers for more details.

The user may control the frequency offset by switching the DPLL mode to NCO (seeded with the initial holdover frequency offset value) and writing frequency offsets to the device. Refer to **dpll_df_offset_x** and **dpll_df_ctrl_x** registers for more details.

10.2.14 DPLL Supervision & Management

10.2.14.1 DPLL Management Mode Comparisons

In un-managed mode of operation, the DPLL state (locked, holdover, acquiring) and the selected reference is automatically set by the internal state machine of the device. It is based on availability of a valid reference and on the reference's selection priority.

In managed mode of operation, the DPLL state and the selected reference is manually set by the user.

The device allows for a smooth transition from in and out of the two modes of operation. Hence if the DPLL was in managed mode, for example locked to Ref2 reference and switched to un-managed mode of operation, then the state machine continues managing the DPLL, locked to the Ref2 and it will not force reference switching to any other reference unless a change in the Ref2 input conditions occurs that necessitate a change to an alternate input reference.

Each DPLL has its own independent state control and reference selection state machine.

10.2.14.2 DPLL Unmanaged Mode

The un-managed mode combines the functionality of the normal state with automatic holdover and automatic reference switching. In this mode, transitioning from one mode to the other is controlled by the device internal state machine.

The on-chip state machine monitors the DPLL status bits, and based on the status information the state machine makes a decision to force holdover or to perform reference switch.

The reference switching state machine is based on the internal clock monitoring of each of the available input references and their priorities.

The state machine selects a reference source based on its priority value defined in a control register and the current availability of the reference. If all the references are available, the reference with the highest priority is selected; if this reference fails, the next highest priority reference is selected, and so on.

In un-managed mode, the state machine only reacts to reference failure indicators and performs reference switching anytime one of the following conditions takes place assuming they are not masked with their corresponding mask bits:

- LOS detected a failure and refswitch mask LOS is at logic "1"
- SCM detected a failure and refswitch mask SCM is at logic "1"
- CFM detected a failure and refswitch mask CFM is at logic "1"
- PFM detected a failure and refswitch mask PFM is at logic "1"
- GST is triggered and refswitch mask GST is at logic "1"

In un-managed mode, the device automatically selects a valid reference input. If the current reference used for synchronization fails, the state machine switches to another available reference. If all the available references fail, then the device enters the holdover state under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic "1"
- SCM detected a failure and holdover mask SCM is at logic "1"
- CFM detected a failure and holdover mask CFM is at logic "1"
- PFM detected a failure and holdover mask PFM is at logic "1"
- GST is triggered and holdover mask GST is at logic "1"

In un-managed mode of operation, the state machine automatically recovers from holdover when the conditions to enter auto-holdover are not present.

The reference selection is based on reference priority. The current active reference for each DPLL can be read from DPLLx Reference Selection Status register.

If neither the reference switch nor the holdover masks are set, then device will keep trying to lock to a failed reference subject to the limits of the pull-in/hold-in range.

10.2.14.3 DPLL Managed (Manual) Mode

In managed mode, the device does not auto-select between different reference inputs. The user specifies which reference to use for synchronization and if it fails the DPLL enters the auto-holdover state without switching to another reference.

The user (external uP) monitors the device status bits. Based on the status information, the user makes a decision to force holdover or to perform reference switch. In managed mode the active reference input is selected based on reference selection control bits. If the user sets the device to lock to a failed reference, the device stays in auto-holdover and only locks to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"

The state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

Time critical transitions for entry into auto-holdover and exit from auto-holdover are managed by the internal state machine. A change of the reference select bits triggers an internal state transition into auto-holdover and then an exit into Normal state and locking to the new reference.

If neither the reference switch nor the holdover masks are set, then device will keep trying to lock to a failed reference subject to the limits of the pull-in/hold-in range.

10.2.15 DPLL Jitter/Wander Generation

The wander generation is dominated by the high-pass filter characteristics of the local oscillator above the programmed DPLL filter bandwidth.

The jitter generation performance is provided in Output Clocks Jitter Generation section.

10.3 Input-Output Conversions

10.3.1 Input to Output and Output to Output Phase Alignment

10.3.1.1 Phase Alignment Control

When the output clock is locked to a jitter free and wander free input clock, input to output latency is expected to have a typical error of 0 nsec. This is accomplished within the device using advanced, automatic precision input-output alignment routines at initialization.

Additionally, there are user accessible phase adjustments that allow for input to output and output to output latency corrections to compensate for PCB load delay, as detailed in section 10.2.5 DPLL Input Advance & Delay and section 10.4.3 Output Skew Management.

10.3.1.2 External Feedback

The PLL architecture allows for implementation of an external feedback (external output clock phase sense) of the PLL path that is fed through one of the available references. Such external feedback would allow for dynamic changes of PCB routing and external buffer delay caused by changes in temperature.

It is recommended that the DPLLs be fully configured before enabling external feedback. If a synthesizer or DPLL in the external feedback path need to be reconfigured, disable external feedback before changing the parameters and then enable external feedback.

Refer to **ext_fb_ctrl** and **ext_fb_sel** registers.

10.3.2 Rate Conversion Function and FEC Support

The DPLL provides up scaling and down scaling functions. It has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports:

Simple rate conversion (i.e., take in 19.44 MHz and create 255/238 FEC SONET/SDH clock of 666.51 MHz),

Double rate conversion (i.e., take in 19.44 MHz, create FEC 10GbE clock of 644.5313, which is 66/64 rate converted 625 MHz, or create 690.5692 which is 255/238 x 66/64 rate converted 625 MHz)

The following is just an example of the frequencies that can be supported at the input and output independently (many more frequencies can be supported):

GbE:

- 25 MHz
- 125 MHz

XAUI (chip to chip interface, which is a common chassis to chassis interface):

- 156.25 MHz or x2 or x4 version

OC-192/STM-64:

- 155.52 MHz or x2 or x4 version
- 155.52 MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
- 155.52 MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version

10 GbE:

- 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
- 155.52 MHz x 66/64 or x2 or x4 version

Long reach 10GE might require the following frequencies with simple rate conversion: (156.25 MHz x 255/237) and (156.25 MHz x 255/238).

The following frequencies with double rate conversion: (155.52 MHz x 66/64 x 255/237) or (155.52 MHz x 66/64 x 255/238) and (156.25 MHz x 66/64 x 255/238) or (156.25 MHz x 66/64 x 255/238). Also, user can use x2 or x4 version of the listed frequencies.

10.4 Output Clocks

10.4.1 Output Frequency Synthesis Engine

The device frequency synthesizers can generate output clocks which meet the jitter generation requirements for various timing requirements detailed in section 15.1.

The frequency synthesis engines can generate any clock frequency between

- Synthesizer 0: 750 MHz to 950 MHz
- Synthesizer 1: 3.8 GHz to 4.56 GHz
- Synthesizer 2: 3.0 GHz to 3.75 GHz
- Synthesizer 3: 2.304 GHz to 3.0 GHz

The frequency for each synthesizer is programmed as B * K * M/N Hz where B, M and N are 16 bits wide registers and K is a 24 bit wide register.

10.4.2 Output Dividers (High Performance Synthesizers)

Differential CML outputs can generate any frequency from 1 Hz to 900 MHz for Synthesizers 1 and 2. The outputs connected to the Synthesizer 3 can also generate any frequency between 1 Hz to 900 MHz except for frequencies in the range between 750 MHz and 768 MHz, however the boundary frequencies (750 MHz and 768 MHz) can themselves be generated. Single ended LVCMOS outputs can generate clocks between 0.5 Hz and 180 MHz. When differential CML outputs are generated, only one out of two independent dividers is used, while the other is powered down. Both dividers can be used to generate two independent LVCMOS output clocks. Refer to Figure 1 and section 10.5.3 for information on which synthesizers are assigned which dividers.

10.4.3 Output Skew Management

Each output may be advanced (not delayed) using **phase_step_ctrl**, **phase_step_data** and **phase_step_max** registers. The resolution is 1.25 ns and will internally be rounded to the nearest VCO cycle. The range is 1 UI per update, and unlimited lifetime updates.

10.4.4 Output Clock Polarity

The device supports programming per output clock polarity, refer to **synth_out_x_ctrl** register.

In the following scenario, the output clock polarity feature is not supported without additional configuration when

- The synthesizer output is configured with a post-divider value <= 24

To correctly enable the output clock polarity the user must first configure the output frequency & desired polarity with post divider value > 24, and then second set the post divider to the proper value <= 24.

In the following scenario, the output clock polarity feature is incorrectly enabled

- The device is not using custom configuration record option
- The device is in system PLL bypass mode (using high speed local master oscillator)
- The HPOUT[8:11] is configured with a post-divider value <= 24

To correctly enable the output clock polarity the user must first configure the output frequency & desired polarity with post divider value > 24 and then second set the post divider to the proper value <= 24.

10.4.5 Output Frame Sync Pulse Width

The default output clock duty cycle is 50/50. The user may program the output pulse width (duty cycle) using **synth_out_x_width** register. This may be useful for 1PPS outputs when a duty cycle other than 50/50 is required, such as setting the pulse high time to 1 UI of a companion clock.

10.4.6 Output Precision Alignment

The device supports precise input-output alignment per output clock (typically 0). Additionally, output-output alignment is a natural result of the input-output alignment. When the precision alignment is enabled (default), the outputs will meet the input-output alignment performance listed in Table 37 · AC Electrical Characteristics* - REF Input to HPOUT_DIFF, HPOUT and GPOUT Output Clock Timing, if the DPLL is appropriately configured with TIE clear enabled. A brief introduction is included in this section. For more complete details refer to ZLAN-620. Disabling the precision alignment is not recommended, even if the application does not require input-output alignment or the user operates with TIE clear disabled.

The alignment routine is triggered by a set of conditions and is then executed at the appropriate time. The alignment routine is triggered per output clock under the following conditions

- the output clock is changed from disabled to enabled
  - for example at power-up initialization
  - for example at power-up pre-configuration (pre-programming)
  - for example when the user manually toggles the output clock enable state
- the output clock configuration parameters are changed (e.g. frequency)
- the synthesizer is changed from disabled to enabled
- the synthesizer configuration parameters are changed (e.g. VCO frequency)
- the system clock configuration is changed (e.g. center frequency)

While the alignment routine is triggered, the output clock is not driven (not visible externally). It is expected that the alignment routine is only triggered at start-up once, as changing the above configuration capabilities is not typical during normal operation.

10.4.6.1 Precision Alignment Enabled with Freerun Mode

By default the device operates in Freerun mode. The user may poll to confirm the alignment routine is completed, as the process takes some time for each output (such as 80 ms for clock frequencies above 8 kHz). The alignment routine processes Synthesizer 0, 1, 2 and 3 in that order.

10.4.6.2 Precision Alignment Enabled with Pre-Configured Auto or Forced Reference Mode

In some instances the device may be pre-configured to startup in Automatic or Forced Reference mode of operation (rather than the default Freerun mode). This may be typical when the device is used in unmanaged mode. At power-up reset, the DPLL by default will qualify the input references according to the PFM (default 10 seconds). During this qualification time the alignment routine will execute, while the DPLL is in the holdover state.

10.4.7 Output Clocks Configuration

Figure 13 shows relationship between synthesizers and output dividers. Each output can be configured to be one differential CML output or two independent LVCMOS outputs. When an output is configured as differential CML output only upper divider is used while lower divider is powered down. As an example differential output HPOUT0_0p/HPOUT1_0n is driven from the divider A while divider B connected to the same synthesizer (Synthesizer 1) is powered down.

10.4.8 Output Drivers

The device has six high performance differential (CML) outputs. Each differential output can be programmed to be two independent single ended LVCMOS outputs for the total of twelve LVCMOS outputs.

Functional block diagram of the output driver is shown in Figure 13.

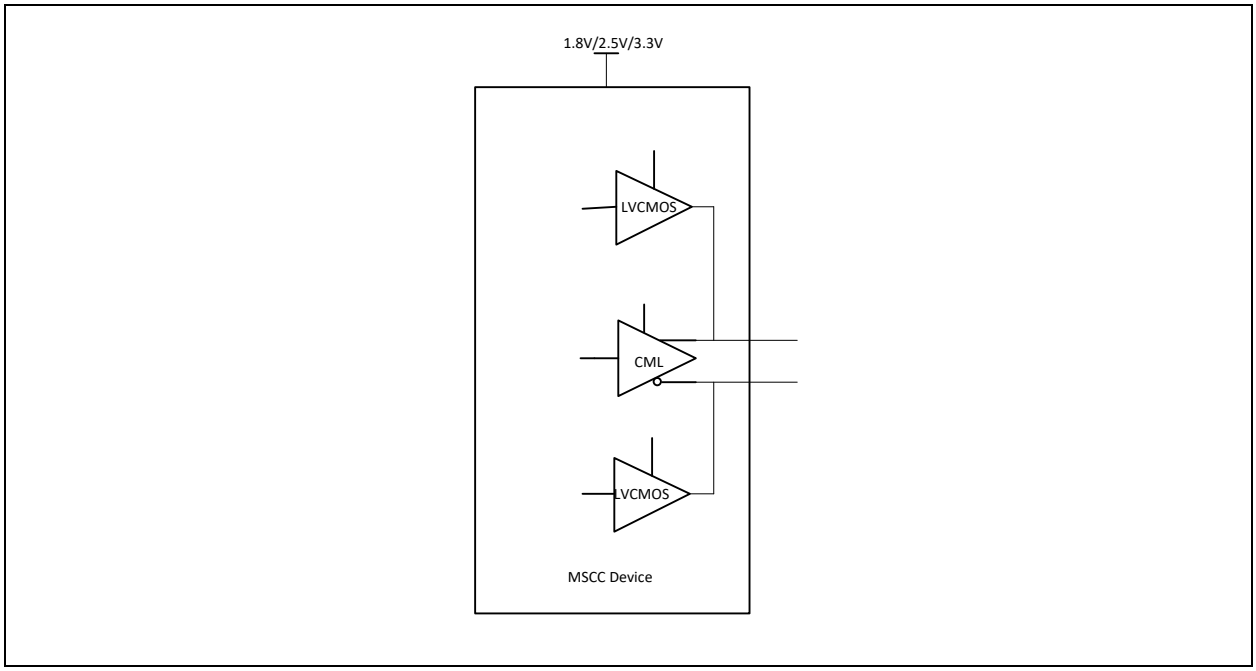


Figure 13. Functional block diagram of the output buffer

When operating with 3.3V&1.8V power supply mode, each output pair can be independently powered from 1.8V, 2.5V or 3.3V supply. When operating with 2.5V&1.8V power supply mode, each output pair can be independently powered from 1.8V or 2.5V supply.

The high performance single ended driver (LVCMOS) supports a maximum clock frequency of 180 MHz and the high performance differential driver (CML) supports a maximum clock frequency of 900 MHz, the jitter performance is detailed in section 15.1.

Following sections describe how to drive different differential receivers via DC and AC coupled transmission line. All resistors should have ±1% and capacitors ±5% tolerance. The coupling capacitance of AC coupled transmission lines should be adjusted (increased) for frequencies lower than 100 MHz to minimize voltage drop.

The CML outputs require external 50 Ω pull up resistors for biasing which should be placed as close as possible to the output pins. Figure 14 shows how to drive an external CML receiver via DC and AC coupled transmission line respectively. The line is terminated with 50 Ω resistors which should be placed as close as possible to the receiver pins.

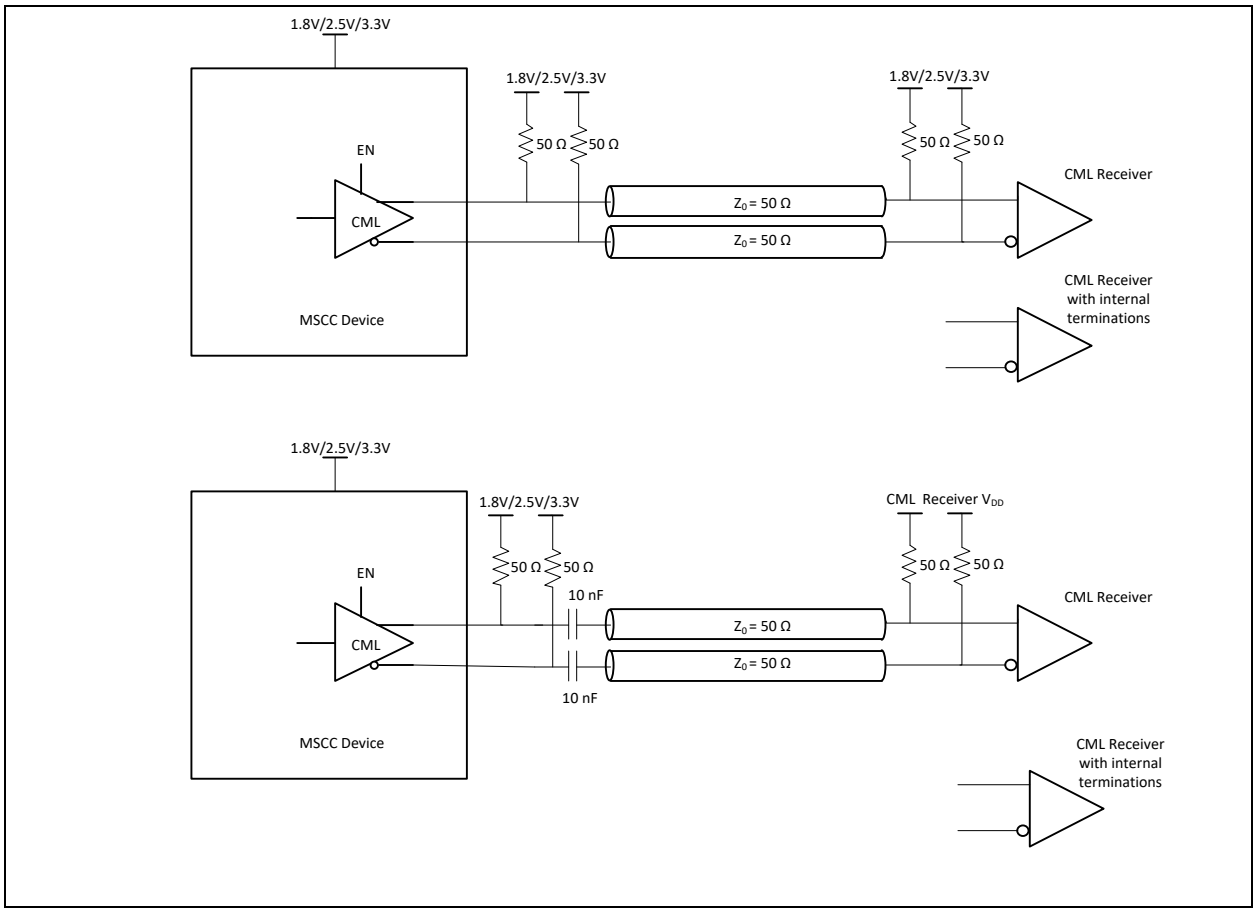


Figure 14. Driving CML Recevier

Figure 15 shows how to terminate an LVPECL receiver. Terminating resistors 82 Ω and 127 Ω provide 50 Ω equivalent Thevenin termination as well as biasing for the LVPECL receiver. Terminating resistors should be placed as close as possible to input pins of the LVPECL receiver. If the LVPECL receiver has internal biasing then AC coupling capacitors should be added.

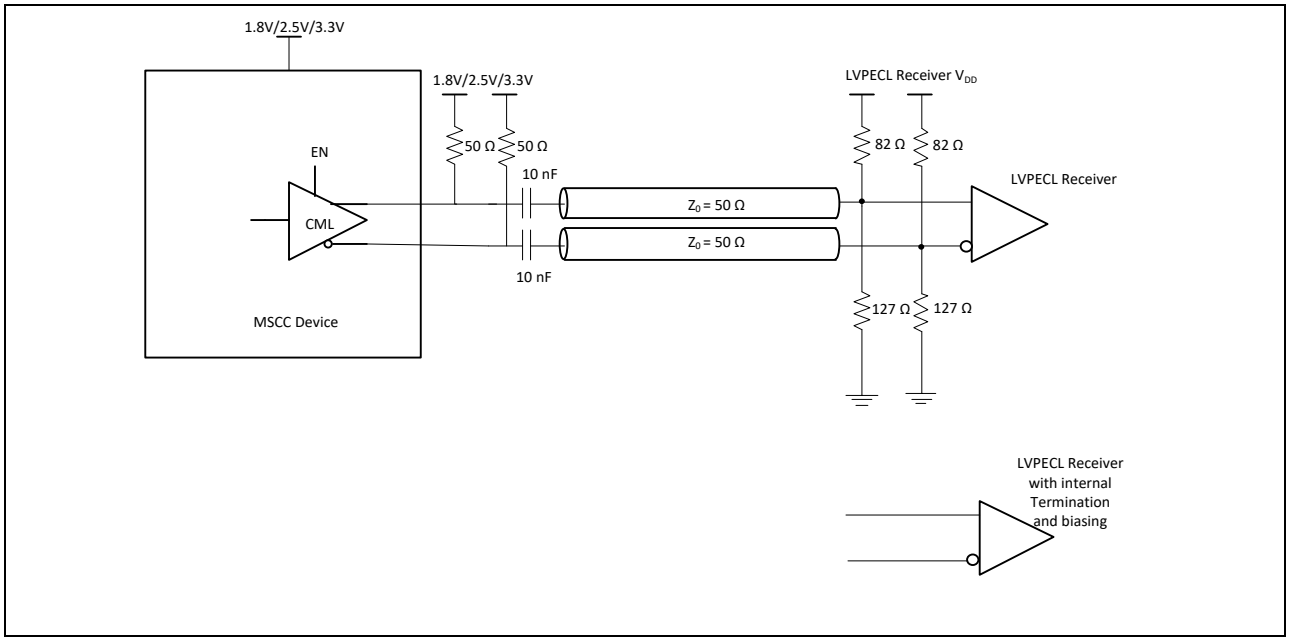


Figure 15. Driving LVPECL Receiver

Figure 16 shows how to terminate an LVDS recieiver.Transmission line needs to be terminated only with 100 Ω resistors if LVDS receiver contains interal biasing circuit. If the internal biasing is not provided than appropriate thevenine termination should be used insteead.

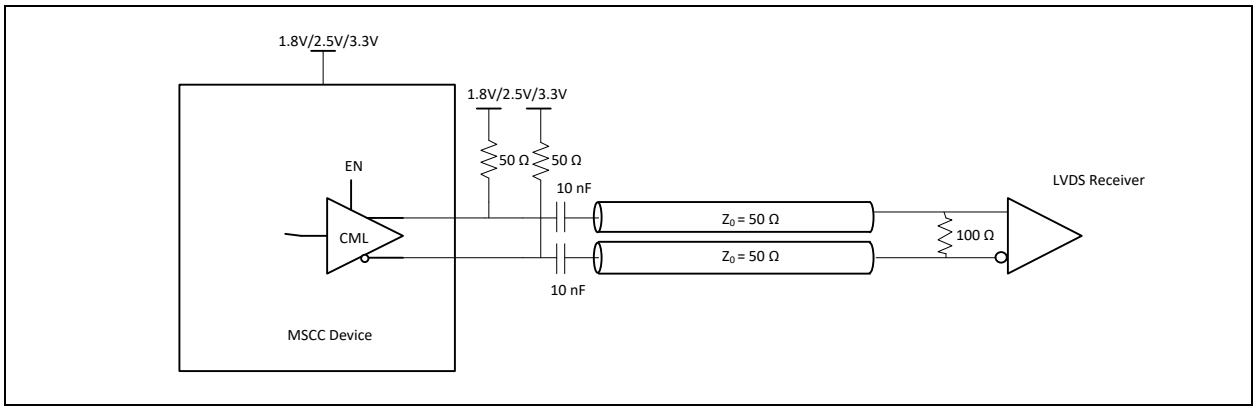


Figure 16. Driving LVDS Receiver

High performance LVCMOS outputs should be terminated at the source with 22 Ω resistors as shown in Figure 17.

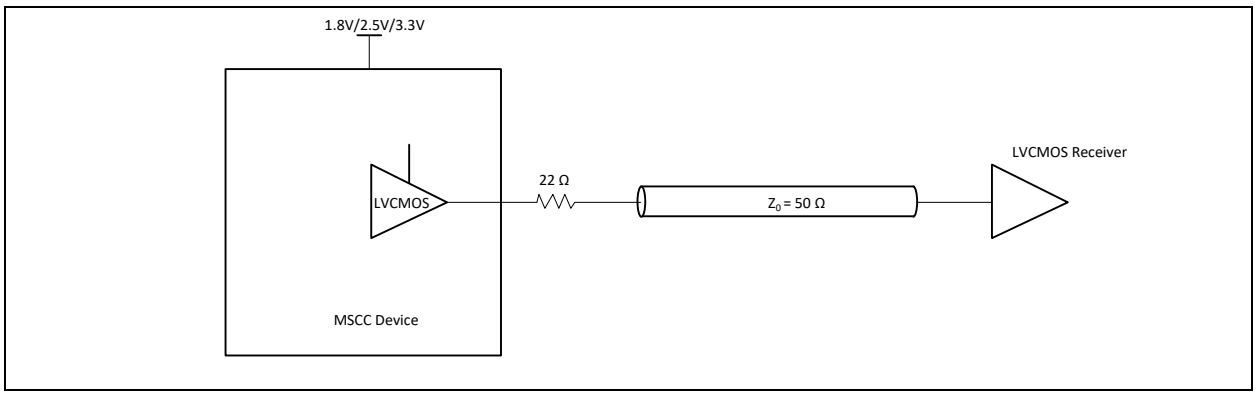


Figure 17. Driving LVCMOS Receiver

10.5 System Clock

The device internal system clocks are generated off the device master clock input (oscillator or a crystal employing an on-chip buffer/driver). The device can accept master clock from an XO, Crystal Resonator or from an XO with differential output. Only one master source shall be used at the time. Unused inputs shall be pulled high or low. For a list of reference crystals & oscillators, refer to ZLAN-442.

10.5.1 Master Clock Interface

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **OSCI** pin as shown in Figure 18. The connection to **OSCI** should be direct and not AC coupled.

When using a crystal resonator as the master timing source, connect the crystal between **OSCI** and **OSCO** pins as shown in Figure 18. The crystal should have bias resistor of 1MΩ and load capacitances C1 and C2. Value of the load capacitances is dependent on the crystal and should be per the crystal's datasheet. The crystal should be a fundamental mode type -- not an overtone.

When using high frequency XO with LVEPCL differential outputs, connect the oscillator's output to **MCLKIN_P** and **MCLKIN_N**. Thevenin termination resistors 182 Ω and 68 Ω should be used for termination and biasing.

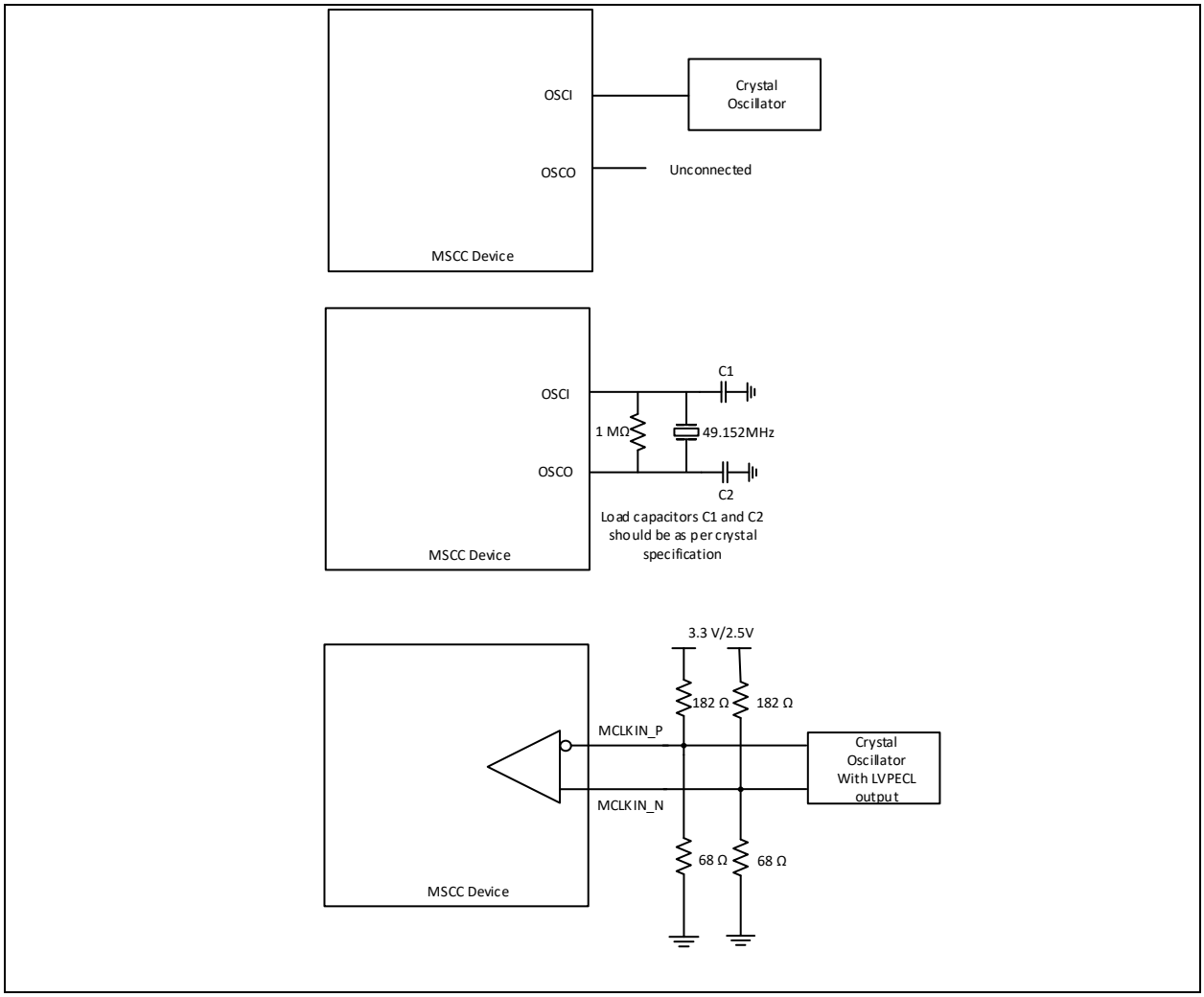


Figure 18. Master Clock Oscillator

10.5.2 Master Clock Frequency Selection

The master clock selection is done at start-up using the GPIO [5,3,2,1,0] pins, right after **RST_b** gets de-asserted. The GPIO [5,3,2,1,0] pins are required to be in desired configuration (high or low) for 500 ms after the de-assertion of **RST_b**, and then they can be released and used as regular GPIOs. Alternatively, these pins can be pulled high or low with 1 kΩ resistors.

GPIO[5,3,2,1,0]	Master Clock Frequency	Oscillator
10100	10 MHz	Single-ended (OSCI/O)
00010	20 MHz	Single-ended (OSCI/O)
00000	24.576 MHz, 25 MHz	Single-ended (OSCI/O)
00001	49.152 MHz, 50 MHz	Single-ended (OSCI/O)
11111	98.304 MHz, 100 MHz (System PLL Bypass)	Single-ended (OSCI/O)
01011	98.304 MHz, 100 MHz (System PLL Bypass)	Differential (MCLKIN_P/N)
11001	114.285 MHz, 125 MHz (System PLL Bypass)	Single-ended (OSCI/O)
01101	114.285 MHz, 125 MHz (System PLL Bypass)	Differential (MCLKIN_P/N)
01100	200 MHz (System PLL Bypass)	Differential (MCLKIN_P/N)

Table 3 · GPIO Master Clock Selection

10.5.2.1 Nominal Master Clock Frequencies

The device supports XO nominal frequencies: 10 MHz, 20 MHz, 25 MHz and 50 MHz. These nominal frequencies may have offsets down to -4%. This offset would then enable support for 24.576 MHz and 49.152 MHz, for example.

The device supports XO nominal frequencies: 100 MHz, 125 MHz and 200 MHz. These nominal frequencies may have offsets down to -10%. This offset would then enable support for 98.3048 MHz, and 114.285 MHz, for example.

10.5.2.2 Offset from Nominal Frequencies

Offset from nominal is programmed by writing **central_freq_offset** register. For example, when using 24.576 MHz or 49.152 MHz oscillators, the user should maintain the default value of the **central_freq_offset** register (0x046AAAAB).

For 114.285 MHz the value should be 0x180072B0.

For other oscillator values:10 MHz, 20 MHz, 25 MHz, 50 MHz, 100 MHz, 125 MHz and 200 MHz **central_freq_offset** register should be programmed to 0x00000000.

10.5.3 System PLL Bypass and Synthesizer 3

The signals HPOUT8_4P, HPOUT9_4N, HPOUT10_5P and HPOUT11_5N are driven by either the Synthesizer 2 (System PLL Bypass FALSE) or Synthesizer 3 (System PLL Bypass TRUE), depending on the utilization of “system PLL bypass” option as shown in Figure 19,

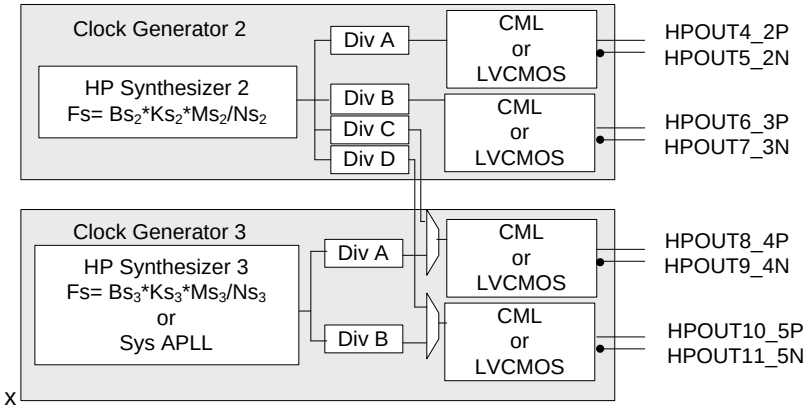


Figure 19. HPOUT[8:9] MUX

When a low frequency master clock is used, nominal frequencies 10 MHz, 20 MHz, 25 MHz and 50 MHz, the HPOUT[8:9] clocks are driven by synthesizer 2 as shown in Figure 20

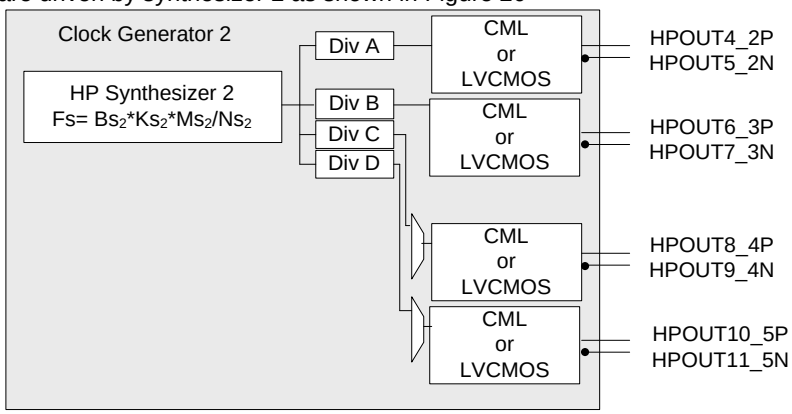


Figure 20. HPOUT[8:9] Driven by Synthesizer 2 (System PLL Bypass FALSE)

When a high frequency master clock is used (either nominal or offset from nominal), such as frequencies 98.304 MHz, 100 MHz, 114.285 MHz ,125 MHz and 200 MHz, the HPOUT[8:9] clocks are driven by synthesizer 3 as shown in Figure 21. This allows synthesizer 3 to create an independent frequency family from synthesizer 2 to drive HPOUT[8:9]. This may enable various LAN, WAN and FEC clock possibilities across Synthesizer 1, 2 and 3.

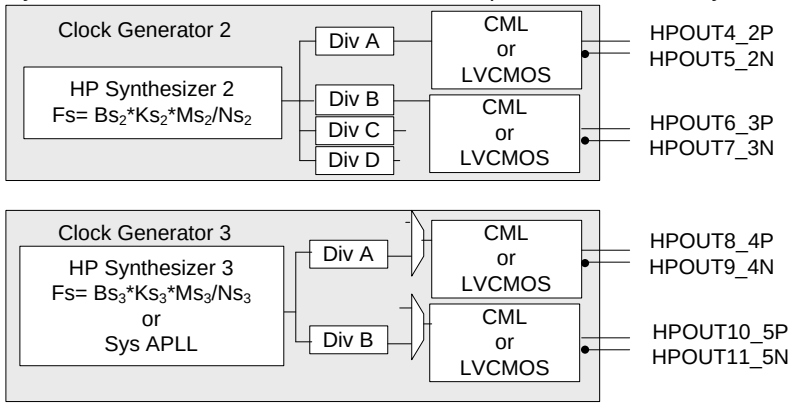


Figure 21. HPOUT[8:9] Driven by Synthesizer 3 (System PLL Bypass TRUE)

10.5.4 Split XO Mode

10.5.4.1 Split XO Mode Introduction

The device offers a “Split-XO mode” where the Synthesizer 3 is available to the user. Split XO mode is intended for timing card application or for line card applications requiring good holdover. In timing card applications the DPLL loop bandwidth needs to be narrow (for example 0.1 Hz for G.8262 Option 2) to be able to filter jitter and wander. A DPLL behaves as a low pass filter for phase noise coming from its input reference, but at the same time it behaves as a high pass filter for noise coming from its master clock source (XO). Hence the timing card DPLL requires very stable XO such as TCXO or OCXO. The TCXO or OCXO needs to have very good jitter because DPLL’s output clock jitter is a function of jitter from the master clock.

The Split XO mode uses a high frequency low cost XO and a TCXO/OCXO of any frequency as shown in **Error! Reference source not found.**. In this mode the device combines best of each component. It is called Split-XO because the device output jitter will be function of XO’ s jitter and output stability will be based on TCXO/OCXO stability. So in this mode the device merges good features from XO (jitter) and TCXO/OCXO (stability).

Because only stability of TCXO/OCXO is important, the TCXO/OCXO does not have to be placed close to the device and it can be shared among multiple ZL30601/602/603/604 devices—TCXO/OCXO can also be located on a different card.

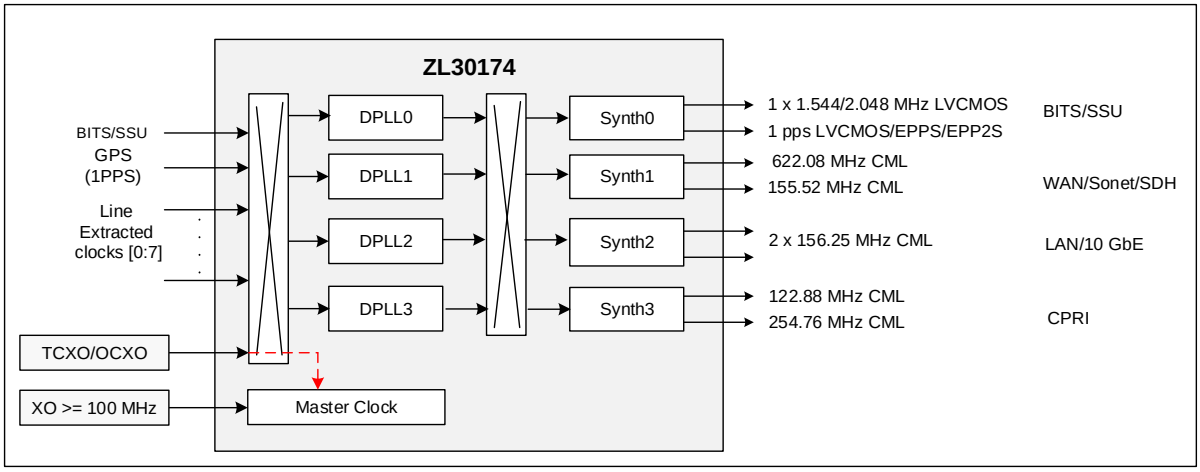


Figure 22. Split-XO mode (System PLL Bypass TRUE)

The benefits of Split-XO mode are summarized below:

- Output jitter generation is not affected by TCXO/OCXO jitter.
- Any TCXO/OCXO frequency can be used (for example 10 MHz)
- Because frequency and jitter of TCXO/OCXO are not important user can source TCXO/OCXO from many crystal vendors as long as the stability of TCXO/OCXO meets relevant standard.
- The TCXO/OCXO does not have to be located on the same card. One TCXO/OCXO can drive multiple devices
- The Synthesizer 3 is available for user application (with use of 100 MHz or higher nominal XO frequency)

10.6 Power Supply

The device power supply can be split into three distinct groups. All high performance outputs (differential or single ended pairs) can be independently powered with 1.8V, 2.5V or 3.3V supply. All the other device inputs & outputs are powered from either 2.5 V or 3.3V supply (only one at the time). The device core is powered from 1.8V supply.

10.6.1 Power Up/Down Sequence

The I/O supply (3.3V or 2.5V) should be powered before or simultaneously with the 1.8V supply. The 1.8 V supply must never be greater than the 3.3V/2.5V supply by more than 0.3V.

The power-down sequence is less critical; however it should be performed in the reverse order to reduce transient currents that consume power.

10.6.2 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3V and 1.8 V supply pins. The device has additional internal voltage regulators for 3.3V power rail.

For recommended power supply decoupling refer to ZLAN-517.

For recommended assembly and PCB layout guidelines refer to ZLAN-527.

10.6.3 Power Calculator

The ZLE30174 EVB GUI includes a useful power calculator that estimates power utilization for a specific configuration or application of the ZL30611/612/614.

10.6.4 Reset and Configuration Circuit

To ensure proper operation, the device must be reset by holding the **RST_b** pin low for at least 2 ms after power-up when 3.3V/2.5V and 1.8V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit. The **RST_b** input has a Schmidt trigger properties to prevent level bouncing.

Microsemi recommends that the power-on reset (**RST_b**) signal be controlled by an on-board reset circuit or by a commercially available voltage supervisory device.

It may also be possible to use a standalone power-up RC reset circuit. It is important to note that this circuit works reasonably well for power-up as long as the power supply rise time is fast with respect to the RC time constant, which may not always be the case. It is the board designer's responsibility to ensure that the circuit is properly tuned to each power supply's specific situation. As an example, for the capacitor C of 1 µF, the resistor should be 10 kΩ or higher.

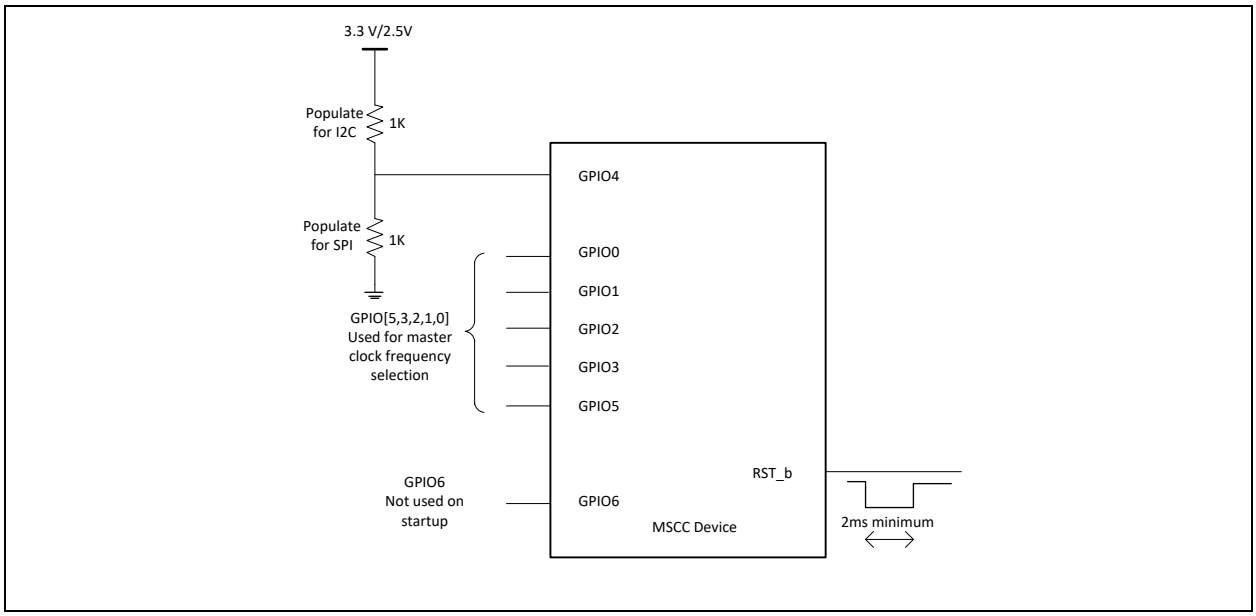


Figure 23. Typical Configuration and Power-Up Reset Circuit

General purpose pins gpio[5:0] are used to configure device on power up. They have to be pulled up/down with 1 kΩ resistors as shown in Figure 23 or they can be held at the desired level for at least 500 ms after **RST_b** goes high and then they can be released and used as general purpose I/O as described in Section Host Interface.

By default all outputs are disabled to allow programing of required frequencies for different outputs and enabling corresponding outputs.

10.6.5 VDD_DRI and VREG_OUT

Refer to ZLAN-517 for full power supply de-coupling scheme. Figure 24 highlights the recommended circuitry for VDD_DRI and VREG_OUT. 150 Ω and 340 Ω resistors are required only for devices whose chip_revision_id in **revision** register at address 0x0003 is 0 or 1. For chip_revision_id => 2 these resistors are optional.

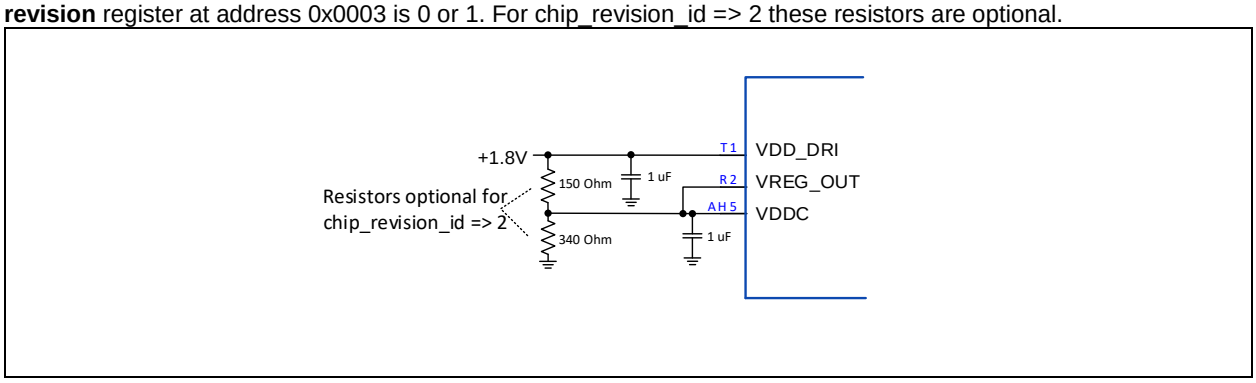


Figure 24. External Connection of VDD_DRI and VREG_OUT

11 Configuration and Control

The SPI/I²C host interface allows field programmability of the device's configuration registers. As an example, the user might start the device at nominal SONET/SDH rate, and then switch to an OTN FEC rate once the link's FEC rate is negotiated.

11.1 Pre-Configured Default Values on Power-Up

On the power up device registers will have values as described in Register Map section. If the device needs to come up with settings different from default it can be pre-configured (pre-programmed) by Microsemi. The device can be pre-configured with up to three different custom configurations. The device will select one of three pre-configured values based on the voltage level of CNFGSEL pin (pin B27). CNFGSEL is three level input pin and its input should be set as shown in Figure 25.

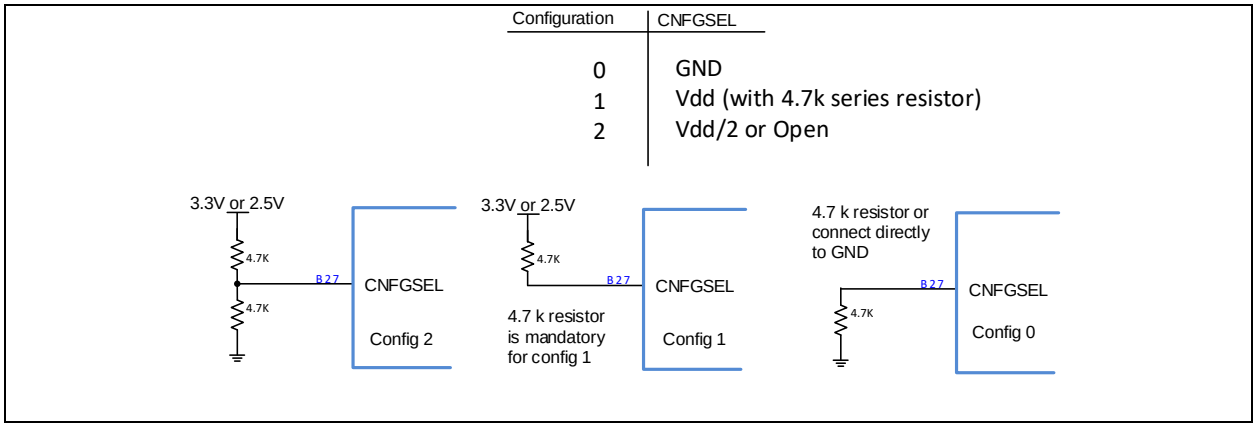


Figure 25. Selection of pre-configured values

It should be noted that 4.7 kΩ is required whenever this pin is connected to VDD (3.3V or 2.5V rails). This pin can be driven from a tristateable LVCMOS output to allow user to select one of three configurations. It should be noted that in this case a series resistor of 4.7kΩ is required as shown in Figure 26.

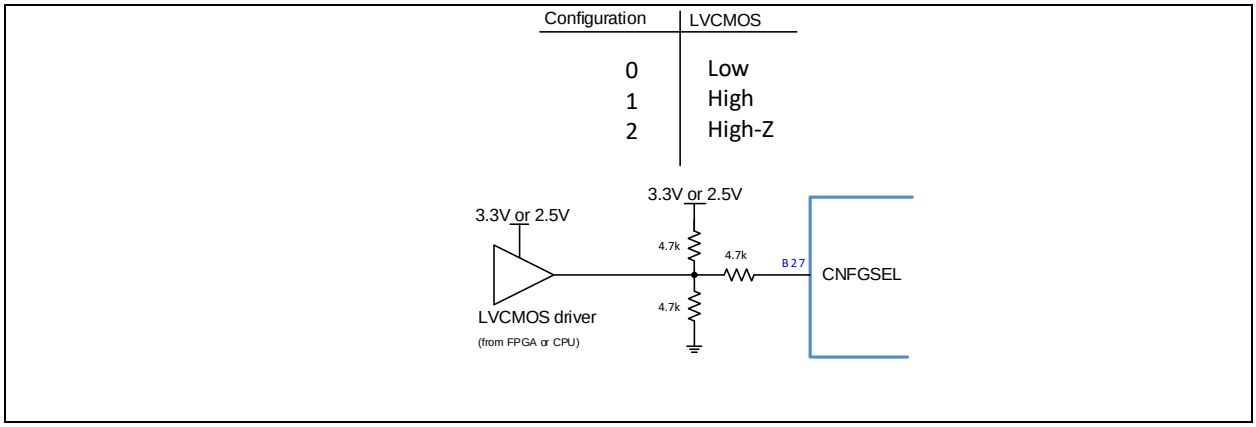


Figure 26. Selection of pre-configured values with FPGA/CPU

The level CNFGSEL pin is ignored if the device is not pre-configured.

11.2 Registers Configuration

This section refers to configuration registers that are set by the user to control operation of the device.

11.2.1 Input Reference Configuration

The following parameters can be configured for the reference input:

- Input reference frequency
- Default input reference selection
- Reference selection priority

- Automatic or manual reference switching
- Glitch-less or hit-less reference switching
- Reference switch based on single cycle monitor, coarse frequency monitor, guard soak timer and precise frequency monitor

11.2.2 DPLL Configuration

The following parameters can be configured for each DPLL:

- Input reference
- Loop bandwidth
- Phase slope limiter
- Pull-in range

11.2.3 Output Multiplexer Configuration

The following parameter can be configured:

- Select which DPLL drives which Synthesizer

11.2.4 Synthesizer Configuration

The following parameters can be configured for each Synthesizer:

- Synthesizers can be configured to be locked to any DPLL or disabled
- Synthesizer frequency:
  - Synthesizer 0: 750 MHz to 950 MHz
  - Synthesizer 1: 3.8 GHz to 4.56 GHz
  - Synthesizer 2: 3.0 GHz to 3.75 GHz
  - Synthesizer 3: 2.304 GHz to 3.0 GHz

11.2.5 Output Dividers and Output Phase Offset (skew) Configuration

The following parameters can be configured:

- Output divider enable/disable
- Divider ratio
- Output phase offset (fine and coarse)

11.2.6 Output Drivers Configuration

The following parameters can be configured:

- Output enable/disable
- Output driver type (CML, LVCMOS)

11.3 GPIO Configuration

The device GPIO is configured using the SPI/I^{2}C. Each GPIO pin can be programmed independently to be:

General Input: In this mode the user can read the logic level of the corresponding pin (either high or low). For example the logic level of GPIO0 is reflected in the register **gpio_in_status_6_0** , bit 0 at address 0x100.

General Output: In this mode the user can program GPIO pin to drive either high or low. For example GPIO0 would drive the value specified in register **gpio_out_6_0**, bit 0, at address 0x0AE.

Control Inputs: In this mode the user can control the device function via GPIOs. For example, the function controlled by GPIO0 is selected by configuring **gpio_select_0** at address 0x0B6:0x0B7. Nearly any device function that is controllable through the host register may be controlled via GPIO. Small subset of control functions is shown below:

- Select DPLL reference
- External Loss Of Signal (LOS) indications
- Enable/disable differential and single ended outputs
- Enable/disable TIE Clear
- Stop/start output clocks

Status Outputs: In this mode the user can feed a status message from any of status registers to the corresponding GPIO pin. For example GPIO0 will mirror a bit from the status register specified in register **gpio_select_0** at address 0x0B6:0x0B7. A subset of status messages is listed below:

- DPLL loss of lock indicators
- DPLL holdover indicators
- Reference 0 to 9 fail indicators

Loss of Signal (LOS) input: This function can be used to indicate to the device that one of input references have failed. When the active input is forced to indicate failure the DPLL may be programmed to automatically enter the holdover state or some alternate action. For example GPIO0 can be used to indicate a reference failure by programming **gpio_select_0** at address 0x0B6:0x0B7.

The GPIO outputs are updated, and the GPIO inputs are read, approximately every 10 ms, except with using system bypass mode with 100 MHz oscillator where they are read approximately every 25 ms.

NOTE: If a GPIO is programmed as a Control Input, the corresponding **gpio_select** register must always point to a valid control register bit. Therefore, when switching GPIO from a Control Input to another mode, the user should first switch the mode via the **gpio_config** register and then switch the **gpio_select** register if necessary. Conversely, when switching a GPIO to a Control Input from another mode, the user should specifiy the desired control register bit in the **gpio_select** register first, then switch to the control input mode via the **gpio_config** register.

11.4 Ready Status

The user may start to configure the device registers when the ready bit in register **info** is asserted. This is typically 500 ms after power-up/reset.

12 Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or an I²C interface.

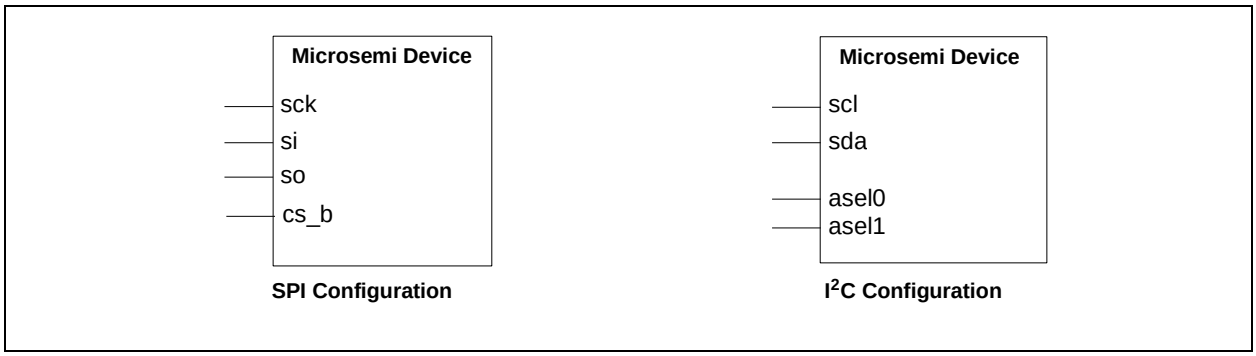


Figure 27. Serial Interface Configuration

The selection between I²C and SPI interfaces is performed at start-up using GPIO[4] pin, as **RST_b** gets de-asserted. The GPIO[4] pin needs to be held at required level for 500 ms after the de-assertion of **RST_b**, after which time they can be released and used as regular GPIO.

GPIO[4]	Serial Interface
0	SPI
1	I2C

Table 4 · Serial Interface Selection

Both interfaces use seven bit address field and the device has eight bit address space. Hence, the device register space is divided in fourteen pages of 127 register each. Page 0 has addresses 0x000 to 0x07E and Page 1 with addresses 0x080 to 0x0FF and so on until page 13 which has addresses 0x680 to 0x6FF. The host selects between the pages by writing to the Page Select register (address 0x7F on each page). e.g. writing a 0x03 to the page select register makes registers 0x180 to 0x1FF available through the host interface.

The device registers are divided into direct access and indirect (mailbox) access registers. The direct access registers (Pages 0 to 10) are accessed simply by reading or writing specific memory location. For example to set DPLL0 to freerun mode user needs to write to **dpll_ctrl_0** register at address 0x021F. The mailbox access registers (Pages 11 to 13) have shared address space. For example Page 11 is shared among all input references. To initialize one of the input references the user needs to specify which input reference needs to be updated (**ref_ctrl** register at address 0x0582:0x0583), to program all the other registers that need to be modified and finally to issue the write command by writing to **ref_semaphore** register at the address 0x0584. The device will read the mailbox and clear the write bit in the **ref_semaphore** register.

12.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the device internal registers that are used to configure, read status, and allow manual control of the device.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **so**_asel1 pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs_b**_asel0 pin is active. If the **sck**_scl pin is low during **cs_b**_asel0 activation, then MSb first timing is selected. If the **sck**_scl pin is high during **cs_b**_asel0 activation, then LSb first timing is assumed.

The SPI port expects 1-bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **cs_b**_asel0 pin must be held low until the operation is complete. Burst

read/write mode is also supported by leaving the chip select signal **cs_b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 28, Figure 29 and Figure 30. Timing characteristics are shown in Table 8, Figure 32, and Figure 33.

12.1.1 Least Significant Bit (LSb) First Transmission Mode

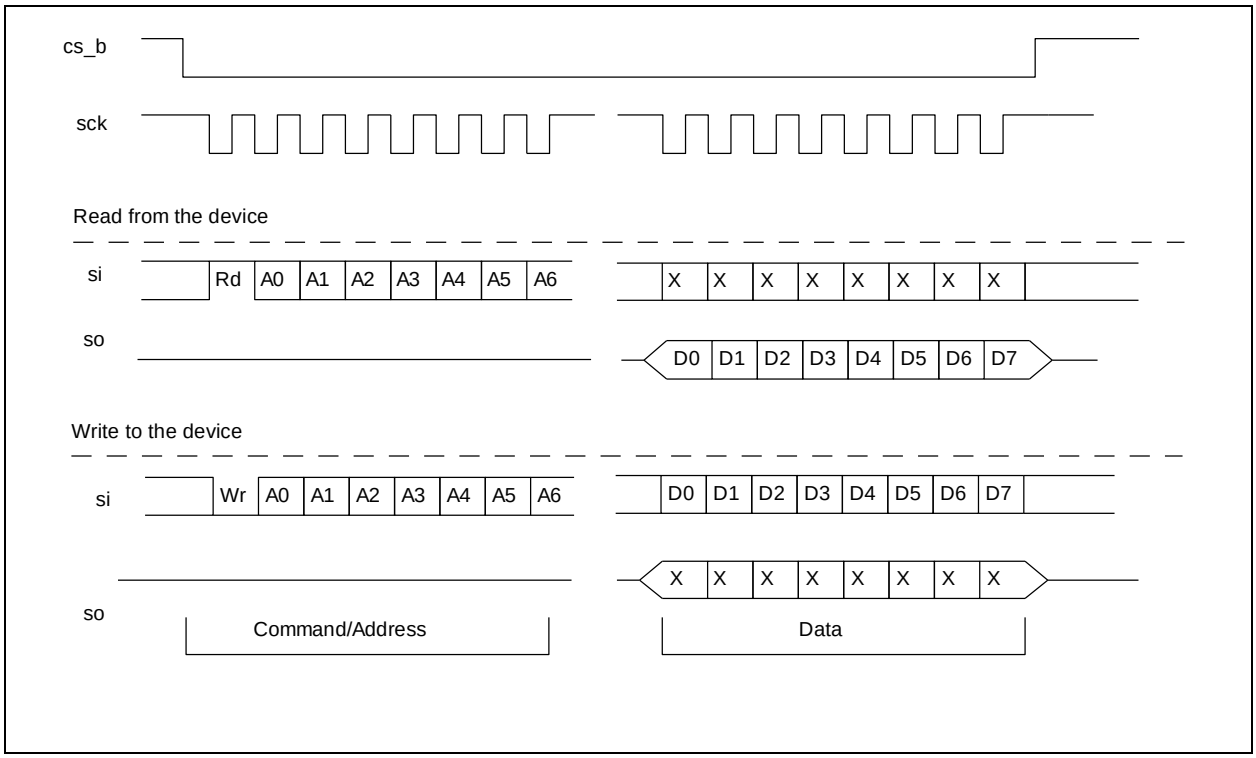


Figure 28. Serial Peripheral Interface Functional Waveform – LSB First Mode

12.1.2 Most Significant Bit (MSb) First Transmission Mode

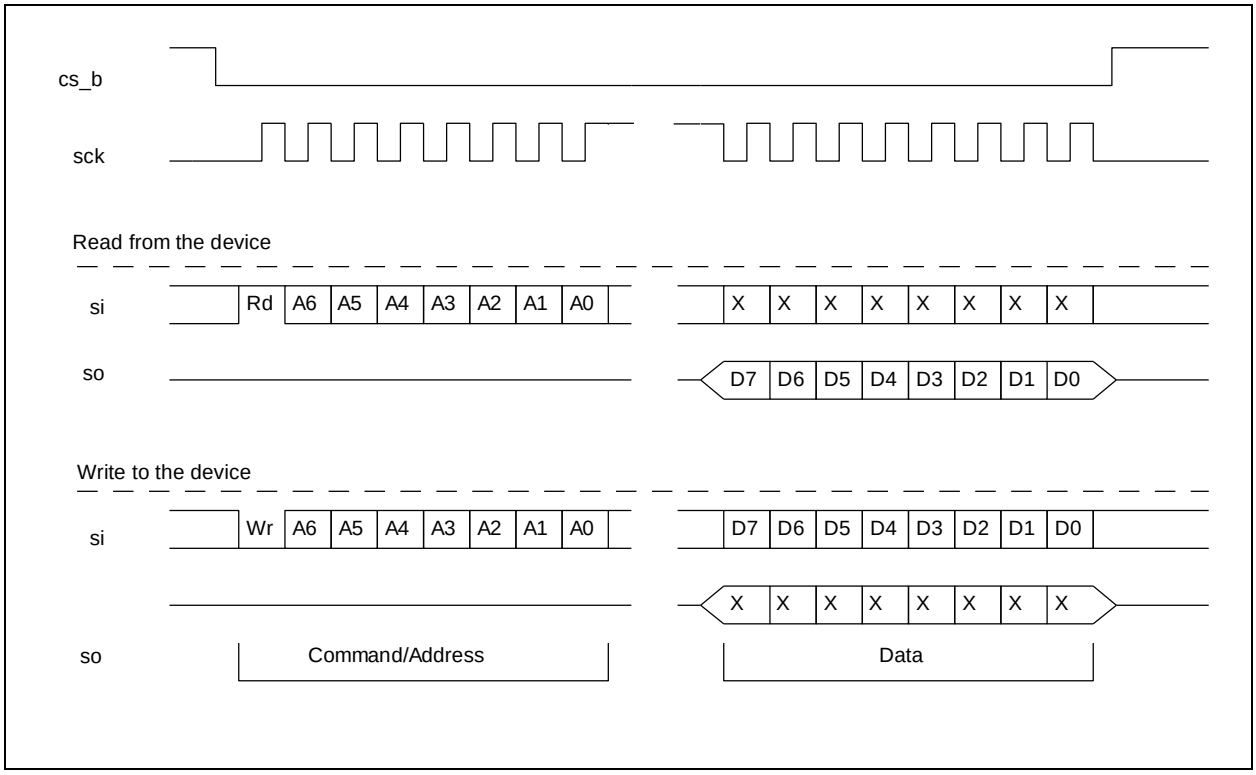


Figure 29. Serial Peripheral Interface Functional Waveform – MSB First Mode

12.1.3 SPI Burst Mode Operation

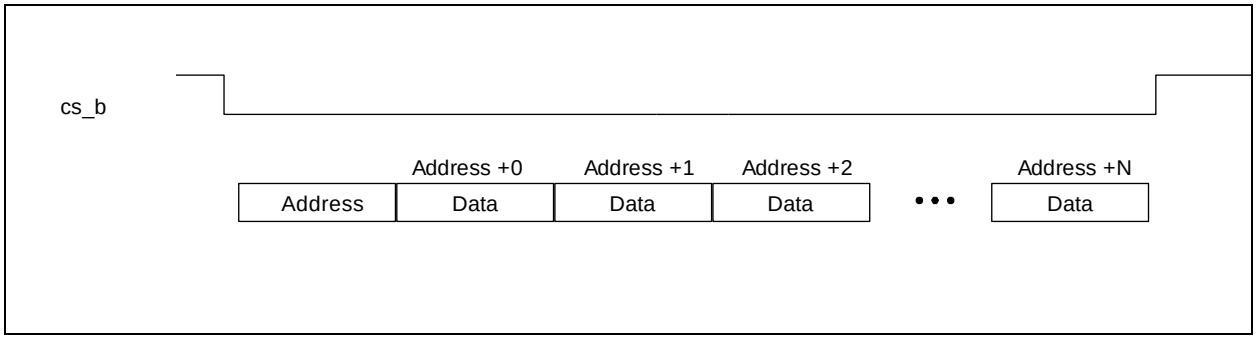


Figure 30. Example of the Burst Mode Operation

12.2 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSb first and occurs in 1 byte blocks. As shown in Figure 31, a write command consists of a 7-bit device (slave) address, a R/W indicator bit, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

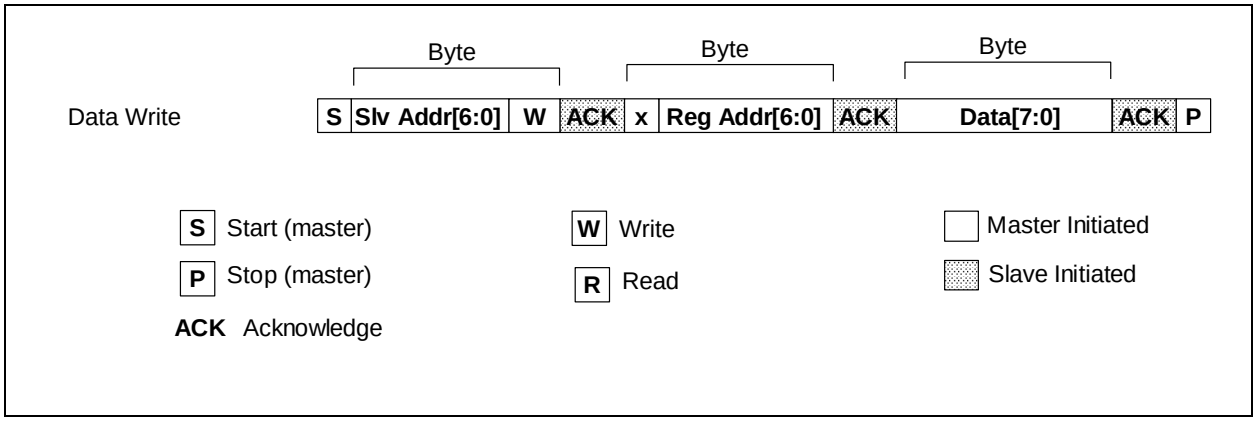


Figure 31. I²C Data Write Protocol

A read is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in following figure.

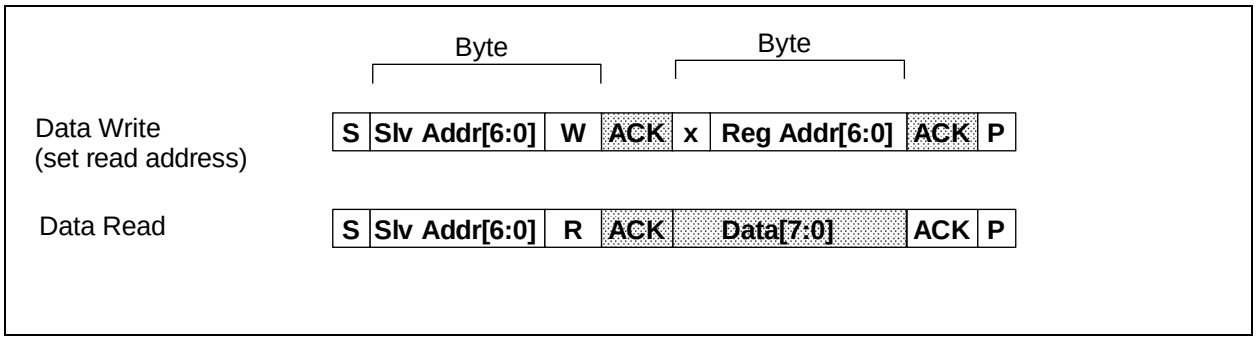


Figure 32. I²C Data Read Protocol

The 7-bit device (slave) address contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple devices to share the same I²C bus. The address configuration is shown in following figure.

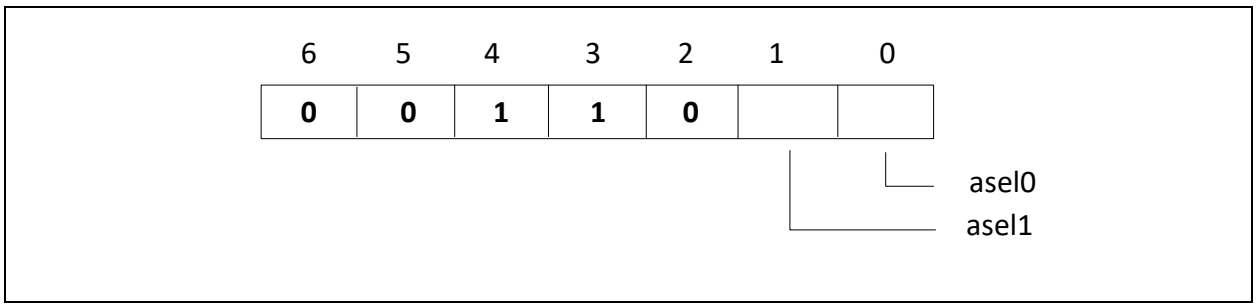


Figure 33. I²C 7 bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 31 (write) and Figure 32(read). The first data byte is written/read to/from the specified address, and subsequent data bytes are written/read using an automatically increment address. The maximum auto increment address of a burst operation is 0x7F and operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

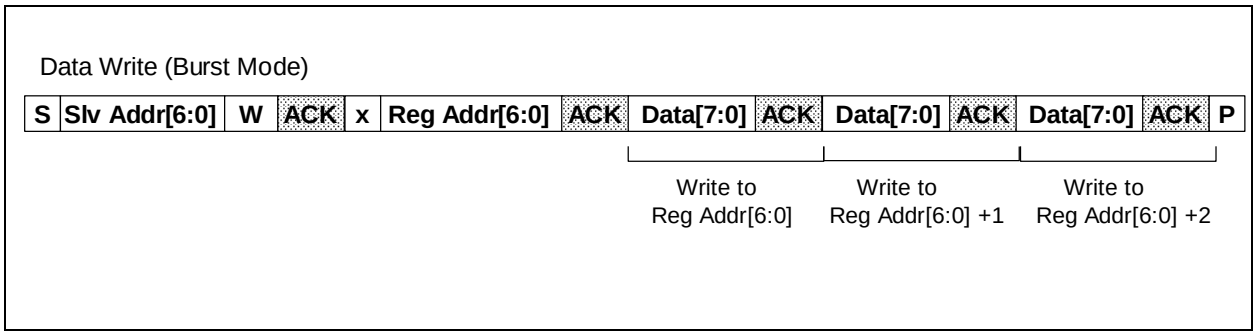


Figure 34. I²C Data Write Burst Mode

13 Register Map

The device is controlled by accessing registers through the serial interface (SPI or I^2C). The device can be configured to operate in un-managed (automatic) mode which minimizes its interaction with the system's processor, or it can operate in a managed (manual) mode where the system processor controls operation of the device.

The register map is big endian format.

A simple way to generate configuration for the device is to use the ZLE30174 evaluation board GUI which can operate standalone (without the evaluation board). Through the GUI the user can quickly set all required parameters and save the configuration to a text file which can then be used by the system processor to load and configure the device.

13.1 Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits are spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 35. When writing a multi-byte value, the value is latched when the LSB is written.

In this example the central_freq_offset register is written with the default value of 0x046AAAAB, a 32-bit value spread over four 8-bit registers. The MSB is contained in address 0x000B and the LSB in 0x000E. When reading or writing this multi-byte value, the MSB must be accessed first, then the middle bytes, and the LSB last.

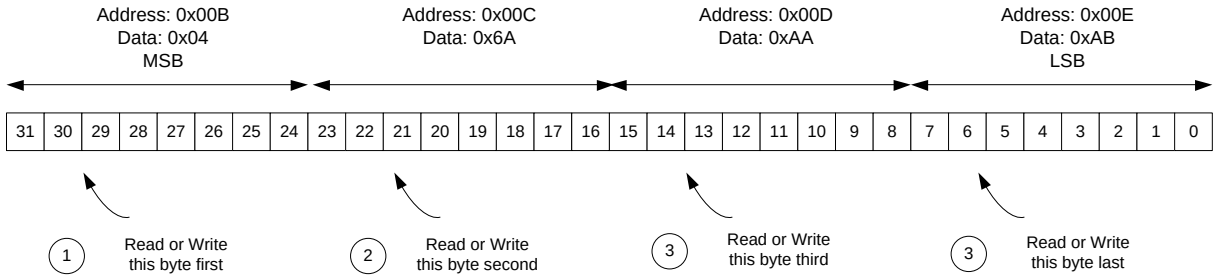


Figure 35. Accessing Multi-byte Register Values

13.1.1 Time between two write accesses to the same register

The user should not write to the same register faster than 25 ms. Some registers that control state machine or system clock operation will require larger delays after writing in order for the state and configurations to be updated. One example is the register **central_freq_offset** requires much larger time, but this register should not be changed dynamically. Other examples include those related to precise input-output alignment (refer to section 10.4.6).

The **dpll_df_offset_n** registers can be written with a minimum wait time of 600 microseconds between write accesses to the same register.

For the page selection register (at addresses 0x07F, 0x0FF, 0x17F, …,0x6FF), there is no waiting time required between write accesses.

13.1.2 Time after change to state machine or system-clock related configuration

The user should wait for appropriate time after configuration of state machine or system clock related configuration prior to updating other registers. One example is the register **central_freq_offset**. Other examples include those related to precise input-output alignment (refer to section 10.4.6).

13.2 Sticky Read

Basic Procedure for Refreshing Latest Device Status from Sticky Read (StickyR) Registers without Interrupt Handler

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-write 0x01 to Sticky Lock Register at address 0x180

-clear status register(s) by writing 0x00 to it

-write 0x00 to StickyR Lock Register at address 0x180

-wait for 25 ms

-read the status register(s)

13.3 Register Map List Summary

The following table provides a summary of the registers available for status and configuration of the device

Table 5 · Register Map (Page 0)

Address	Name	Default	Type
0x0000	info	0x1E	R
0x0001:0x0002	id	0x1C66	R
0x003	revison	0x04	R
0x0007:0x000A	custom_config_ver	0xFFFFFFFF	R/W
0x000B:0x000E	central_freq_offset	0x046AAAAB	R/W
0x007E	uport	0x00	R/W
0x007F	page_sel	0x00	R/W

Table 6 · Register Map (Page 1)

Address	Name	Default	Type
0x0080	ref_irq_mask_7_0	0x00	R/W
0x0081	ref_irq_mask_9_8	0x00	R/W
0x0082	dpll_irq_mask	0x00	R/W
0x0084	ref_mon_mask_0	0x00	R/W
0x0085	ref_mon_mask_1	0x00	R/W
0x0086	ref_mon_mask_2	0x00	R/W
0x0087	ref_mon_mask_3	0x00	R/W
0x0088	ref_mon_mask_4	0x00	R/W
0x0089	ref_mon_mask_5	0x00	R/W
0x008A	ref_mon_mask_6	0x00	R/W
0x008B	ref_mon_mask_7	0x00	R/W
0x008C	ref_mon_mask_8	0x00	R/W
0x008D	ref_mon_mask_9	0x00	R/W
0x0094	dpll_mon_mask_0	0x00	R/W
0x0095	dpll_mon_mask_1	0x00	R/W
0x0096	dpll_mon_mask_2	0x00	R/W
0x0097	dpll_mon_mask_3	0x00	R/W
0x00A4	gpio_irq_config	0x00	R/W
0x00A5	synth_irq_mask	0x00	R/W
0x00A6	synth_mon_mask_0	0x00	R/W
0x00A7	synth_mon_mask_1	0x00	R/W
0x00A8	synth_mon_mask_2	0x00	R/W
0x00A9	synth_mon_mask_3	0x00	R/W
0x00AE	gpio_out_6_0	0x00	R/W
0x00B2	gpio_freeze_6_0	0x00	R/W
0x00B6:0x00B7	gpio_select_0	0x0000	R/W
0x00B8	gpio_config_0	0x00	R/W
0x00B9:0x00BA	gpio_select_1	0x0000	R/W
0x00BB	gpio_config_1	0x00	R/W
0x00BC:0x00BD	gpio_select_2	0x0000	R/W
0x00BE	gpio_config_2	0x00	R/W
0x00BF:0x00C0	gpio_select_3	0x0000	R/W
0x00C1	gpio_config_3	0x00	R/W
0x00C2:0x00C3	gpio_select_4	0x0000	R/W
0x00C4	gpio_config_4	0x00	R/W
0x00C5:0x00C6	gpio_select_5	0x0000	R/W
0x00C7	gpio_config_5	0x00	R/W
0x00C8:0x00C9	gpio_select_6	0x044E	R/W
0x00CA	gpio_config_6	0x02	R/W
0x00FE	uport	0x00	R/W
0x00FF	page_sel	0x00	R/W

Table 7 · Register Map (Page 2)

Address	Name	Default	Type
0x0100	gpio_in_status_6_0	0x00	R
0x0106	ref_mon_status_0	0x00	R
0x0107	ref_mon_status_1	0x00	R
0x0108	ref_mon_status_2	0x00	R
0x0109	ref_mon_status_3	0x00	R
0x010A	ref_mon_status_4	0x00	R
0x010B	ref_mon_status_5	0x00	R
0x010C	ref_mon_status_6	0x00	R
0x010D	ref_mon_status_7	0x00	R
0x010E	ref_mon_status_8	0x00	R
0x010F	ref_mon_status_9	0x00	R
0x0116	dpll_mon_status_0	0x00	R
0x0117	dpll_mon_status_1	0x00	R
0x0118	dpll_mon_status_2	0x00	R
0x0119	dpll_mon_status_3	0x00	R
0x0126	dpll_refsel_status_1_0	0x00	R
0x0127	dpll_refsel_status_3_2	0x00	R
0x016E	synth_mon_status_0	0x00	R
0x016F	synth_mon_status_1	0x00	R
0x0170	synth_mon_status_2	0x00	R
0x0171	synth_mon_status_3	0x00	R
0x017E	uport	0x00	R/W
0x017F	page_sel	0x00	R/W

Table 8 · Register Map (Page 3)

Address	Name	Default	Type
0x0180	sticky_lock	0x00	R/W
0x0182	ref_irq_active_7_0	0x00	S
0x0183	ref_irq_active_9_8	0x00	S
0x0184	dpll_irq_active	0x00	S
0x0186	ref_mon_sticky_0	0x00	S
0x0187	ref_mon_sticky_1	0x00	S
0x0188	ref_mon_sticky_2	0x00	S
0x0189	ref_mon_sticky_3	0x00	S
0x018A	ref_mon_sticky_4	0x00	S
0x018B	ref_mon_sticky_5	0x00	S
0x018C	ref_mon_sticky_6	0x00	S
0x018D	ref_mon_sticky_7	0x00	S
0x018E	ref_mon_sticky_8	0x00	S
0x018F	ref_mon_sticky_9	0x00	S
0x0196	dpll_mon_sticky_0	0x00	S
0x0197	dpll_mon_sticky_1	0x00	S
0x0198	dpll_mon_sticky_2	0x00	S
0x0199	dpll_mon_sticky_3	0x00	S
0x01A6	dpll_fastlock_phase_sticky	0x00	S
0x01A8	dpll_fastlock_freq_sticky	0x00	S
0x01AA	dpll_tie_wr_sticky	0x00	S
0x01AC	synth_step_sticky_1_0	0x00	S
0x01AD	synth_step_sticky_3_2	0x00	S
0x01B0	synth_mon_sticky_0	0x00	S
0x01B1	synth_mon_sticky_1	0x00	S
0x01B2	synth_mon_sticky_2	0x00	S
0x01B3	synth_mon_sticky_3	0x00	S
0x01B7	synth_irq_active	0x00	S
0x01FE	uport	0x00	R/W
0x01FF	page_sel	0x00	R/W

Table 9 · Register Map (Page 4)

Address	Name	Default	Type
0x0200	ref_los_7_0	0x00	R/W
0x0201	ref_los_9_8	0x00	R/W
0x021C	dpll_enable	0x04	R/W
0x021E	dpll_mode_refsel_0	0x00	R/W
0x021F	dpll_ctrl_0	0x08	R/W
0x0221	dpll_mode_refsel_1	0x00	R/W
0x0222	dpll_ctrl_1	0x08	R/W
0x0224	dpll_mode_refsel_2	0x00	R/W
0x0225	dpll_ctrl_2	0x08	R/W
0x0227	dpll_mode_refsel_3	0x00	R/W
0x0228	dpll_ctrl_3	0x08	R/W
0x024E	gp_out_ctrl	0x00	R/W
0x0250	hp_out_ctrl_1	0xF0	R/W
0x0251	hp_out_routing_1	0x00	R/W
0x0252	hp_out_ctrl_2	0xA0	R/W
0x0253	hp_out_routing_2	0x00	R/W
0x0254	hp_out_ctrl_3	0xA0	R/W
0x0255	hp_out_routing_3	0x00	R/W
0x025C	calibr_alignment_ctrl	0x01	R/W
0x027E	uport	0x00	R/W
0x027F	page_sel	0x00	R/W

Table 10 · Register Map (Page 5)

Address	Name	Default	Type
0x02D0	ext_fb_ctrl	0x00	R/W
0x02D1	ext_fb_sel	0x00	R/W
0x02FE	uport	0x00	R/W
0x02FF	page_sel	0x00	R/W

Table 11 · Register Map (Page 6)

Address	Name	Default	Type
0x0300:0x0304	dpll_df_offset_0	0x0000000000	R/W
0x0305	dpll_df_ctrl_0	0x00	R/W
0x0306:0x0309	dpll_tie_data_0	0x00000000	R/W
0x030A	dpll_tie_ctrl_0	0x00	R/W
0x0310:0x0314	dpll_df_offset_1	0x0000000000	R/W
0x0315	dpll_df_ctrl_1	0x00	R/W
0x0316:0x0319	dpll_tie_data_1	0x00000000	R/W
0x031A	dpll_tie_ctrl_1	0x00	R/W
0x0320:0x0324	dpll_df_offset_2	0x0000000000	R/W
0x0325	dpll_df_ctrl_2	0x00	R/W
0x0326:0x0329	dpll_tie_data_2	0x00000000	R/W
0x032A	dpll_tie_ctrl_2	0x00	R/W
0x0330:0x0334	dpll_df_offset_3	0x0000000000	R/W
0x0335	dpll_df_ctrl_3	0x00	R/W
0x0336:0x0339	dpll_tie_data_3	0x00000000	R/W
0x033A	dpll_tie_ctrl_3	0x00	R/W
0x037E	uport	0x00	R/W
0x037F	page_sel	0x00	R/W

Table 12 · Register Map (Page 10)

Address	Name	Default	Type
0x0501	phase_step_ctrl	0x00	R/W
0x0502:0x0505	phase_step_data	0x00000000	R/W
0x0506	phase_step_max	0x00	R/W
0x0510	synth_step_div_mask_1_0	0x00	R/W
0x0511	synth_step_div_mask_3_2	0x00	R/W
0x057E	uport	0x00	R/W
0x057F	page_sel	0x00	R/W

Table 13 · Register Map (Page 11)

Address	Name	Default	Type
0x0582:0x0583	ref_ctrl	0x0001	R/W
0x0584	ref_mb_sem	0x00	R/W
0x0585:0x0586	ref_freq_base	0x9C40	R/W
0x0587:0x0588	ref_freq_mult	0x0001	R/W
0x0589:0x058A	ref_ratio_m	0x0001	R/W
0x058B:0x058C	ref_ratio_n	0x0001	R/W
0x058D	ref_config	0x01	R/W
0x058F	ref_scm	0x05	R/W
0x0590	ref_cfm	0x05	R/W
0x0591	ref_gst	0x21	R/W
0x0592	ref_pfm_ctrl	0x00	R/W
0x0593:0x0594	ref_pfm_disqualify	0x32B4	R/W
0x0595:0x0596	ref_pfm_qualify	0x2724	R/W
0x0597:0x0598	ref_pfm_period	0x0000	R/W
0x0599	ref_pfm_filter_limit	0x28	R/W
0x059A	ref_phase_mem	0x1B	R/W
0x05FE	uport	0x00	R/W
0x05FF	page_sel	0x00	R/W

Table 14 · Register Map (Page 12)

Address	Name	Default	Type
0x0602:0x0603	dpll_ctrl	0x0001	R/W
0x0604	dpll_semaphore	0x00	R/W
0x0605	dpll_bw_fixed	0x00	R/W
0x0606	reserved	0x00	R/W
0x0608	dpll_config	0x00	R/W
0x0609:0x060A	dpll_psl	0x0000	R/W
0x060B:0x060C	dpll_psl_max_phase	0x0064	R/W
0x060F:0x0610	dpll_range	0x0078	R/W
0x0611	dpll_ref_sw_mask	0x08	R/W
0x0612	dpll_ref_ho_mask	0x17	R/W
0x0613	dpll_ho_filter	0x00	R/W
0x0614	dpll_ho_delay	0x4C	R/W
0x0615	dpll_priority_1_0	0x10	R/W
0x0616	dpll_priority_3_2	0x32	R/W
0x0617	dpll_priority_5_4	0x54	R/W
0x0618	dpll_priority_7_6	0x76	R/W
0x0619	dpll_priority_9_8	0x98	R/W
0x061D	dpll_lock_phase	0x92	R/W

0x061E	dpll_lock_period	0x80	R/W
0x061F	dpll_fast_lock_ctrl	0x01	R/W
0x0620	dpll_fast_lock_phase_err	0xFF	R/W
0x0621	dpll_fast_lock_freq_err	0x04	R/W
0x0622	dpll_damping	0x00	R/W
0x0624	dpll_tie	0x00	R/W
0x0625	dpll_tie_wr_thresh	0x00	R/W
0x0638	dpll_lock_delay	0x00	R/W
0x067E	uport	0x00	R/W
0x067F	page_sel	0x00	R/W

Table 15 · Register Map (Page 13)

Address	Name	Default	Type
0x0682:0x0683	synth_ctrl	0x0001	R/W
0x0684	synth_semaphore	0x00	R/W
0x0685:0x0686	synth_vco_freq_base	0x1F40	R/W
0x0687:0x0689	synth_vco_freq_mult	0x017BB0	R/W
0x068A:0x068B	synth_vco_freq_m	0x0001	R/W
0x068C:0x068D	synth_vco_freq_n	0x0001	R/W
0x0693	synth_config	0x01	R/W
0x0694	synth_config2	0x00	R/W
0x0699:0x069D	synth_out_a_div	0x0000000005	R/W
0x069E	synth_out_a_driver	0x03	R/W
0x069F	synth_out_a_ctrl	0x00	R/W
0x06A1:0x06A4	synth_out_a_width	0x00000000	R/W
0x06A5:0x06A9	synth_out_a_shift	0x0000000000	R/W
0x06AD:0x06B1	synth_out_b_div	0x0000000028	R/W
0x06B2	synth_out_b_driver	0x03	R/W
0x06B3	synth_out_b_ctrl	0x00	R/W
0x06B5:0x06B8	synth_out_b_width	0x00000000	R/W
0x06B9:0x06BD	synth_out_b_shift	0x0000000000	R/W
0x06C1:0x06C5	synth_out_c_div	0x0000000000	R/W
0x06C6	synth_out_c_driver	0x00	R/W
0x06C7	synth_out_c_ctrl	0x00	R/W
0x06C9:0x06CC	synth_out_c_width	0x00000000	R/W
0x06CD:0x06D1	synth_out_c_shift	0x0000000000	R/W
0x06D5:0x06D9	synth_out_d_div	0x0000000000	R/W
0x06DA	synth_out_d_driver	0x00	R/W
0x06DB	synth_out_d_ctrl	0x00	R/W
0x06DD:0x06E1	synth_out_d_width	0x00000000	R/W
0x06E1:0x06E5	synth_out_d_shift	0x0000000000	R/W
0x06FE	uport	0x00	R/W
0x06FF	page_sel	0x00	R/W

13.4 Register List

13.4.1 Register List (Page 0)

Address: 0x0000 Name: info Default: 0x1E Type: R		
Bit Field	Function Name	Description
7	ready	Status bit indicating when the device has performed initialization and it is ready to be programmed. Typically 500 ms from power-up.
6:0	reserved	

Address: 0x0001:0x0002 Name: id Default: 0x1C66 Type: R		
Bit Field	Function Name	Description
15:0	chip_id	Chip identification number: Unsigned binary value of these bits represent chip identification number

Address: 0x0003 Name: revision Default: 0x04 Type: R		
Bit Field	Function Name	Description
7:0	chip_revision_id	Chip revision number: Unsigned binary value of these bits represent chip revision number. Refer to section 10.6.5 **NOTE**: Following the warm start initiated by enabling Split_XO mode (see register 0x021D), this register will be reset to 0x00. To determine the correct revision of the device, this register should be read before split_xo mode is enabled. If the device uses a custom configuration, the revision register will be correct after the device is automatically configured, even if split-xo mode is enabled by the custom configuration).

Address: 0x0007:0x000A Name: custom_config_ver Default: 0xFFFFFFFF Type: R/W		
Bit Field	Function Name	Description
31:0		This register is intended (but not limited) to be used as configuration version number. Up to 3 custom register configurations can be programmed into the device.

Address:	0x000B:0x000E	
Name:	central_freq_offset	
Default:	0x046AAAAB	
Type:	R/W	
Bit Field	Function Name	Description
31:0		2's complement binary value of these bits represent central frequency offset for the device. This value should be used to compensate for oscillator inaccuracy, or make the device look like Numerically Controlled Oscillator (NCO). This register controls central frequency of all 4 Synthesizers. Expressed in steps of +/- 2^-32 of nominal setting. When oscillator inaccuracy is known: inacc_osc = (f_osc - f_nom)/f_nom (usually specified in ppm), the value to be programmed in this register is calculated with the following formula: X = (1/(1 + inacc_osc) - 1)*2^32, when f_osc < f_nom X = (1/(1 + inacc_osc))*2^32, when f_osc > f_nom, where inacc_osc - represents oscillator frequency inaccuracy, f_osc - represents oscillator frequency, and f_nom - represents oscillator nominal frequency (i.e. 25MHz, 20MHz, or 50MHz) When the oscillator frequency is lower than the nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1: if oscillator inaccuracy is -2% (f_osc = 24.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = -0.02) X = (1/(1+(-0.02)) - 1)*2^32 = (1/0.98 - 1)*2^32 = 87652394 = 0x0539782A When NCO behavior is desired, the output frequency should be calculated as per formula: fout = (1 + X/2^32)*finit where X -represent 2's complement number specified in this register finit - initial frequency set by Bs, Ks, Ms, Ns and postdivider number for particular VCO fout - output frequency Note: CFN offset should not be programmed to exceed +0% to -4% or -10% (depending on master clock frequency) Note: This register cannot be accessed more than once per 25ms.

Address:	0x007E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x007F Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.2 Register List (Page 1)

Address: 0x0080 Name: ref_irq_mask_7_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	mask_7	See description for mask_0.
6	mask_6	See description for mask_0.
5	mask_5	See description for mask_0.
4	mask_4	See description for mask_0.
3	mask_3	See description for mask_0.
2	mask_2	See description for mask_0.
1	mask_1	See description for mask_0.
0	mask_0	This bit is only considered when GPIO interrupt (IRQ) is turned on. It determines if a GPIO interrupt is generated when ref0 status changes. 0: A ref0 status change will not generate a GPIO interrupt. Register 0x182 bit 0 (ref_irq_active_7_0::fail_0) will not be set. 1: Certain ref0 status changes will generate a GPIO interrupt. Register 0x182 bit 0 (ref_irq_active_7_0::fail_0) will be set to 1. See register 0x084 (ref_mon_mask_0) to configure which status changes will generate a GPIO interrupt.

Address: 0x0081 Name: ref_irq_mask_9_8 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:2	reserved	
1	mask_9	See description for register at address 0x080, bit 0 (ref_irq_mask_7_0::mask_0).
0	mask_8	See description for register at address 0x080, bit 0 (ref_irq_mask_7_0::mask_0).

Address: 0x0082 Name: dpll_irq_mask Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	reserved	
3	mask_3	See description for mask_0.
2	mask_2	See description for mask_0.
1	mask_1	See description for mask_0.
0	mask_0	This bit is only considered when GPIO interrupt (IRQ) is turned on. It determines if a GPIO interrupt is generated when DPLL0 status changes. 0: A DPLL0 status change will not generate a GPIO interrupt. Register 0x184 bit 0 (dpll_irq_active::fail_0) will not be set. 1: Certain DPLL0 status changes will generate a GPIO interrupt. Register 0x184 bit 0 (dpll_irq_active::fail_0) will be set to 1. See register 0x094 (dpll_mon_mask_0) to configure which status changes will generate a GPIO interrupt.

Address: 0x0084 Name: ref_mon_mask_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	0: ref0 PFM status changes are masked. 1: ref0 PFM status changes are unmasked. A GPIO interrupt will be generated and register 0x182 bit 0 (ref_irq_active_7_0::fail_0) will be set to 1.
3	gst	0: ref0 GST status changes are masked. 1: ref0 GST status changes are unmasked. A GPIO interrupt will be generated and register 0x182 bit 0 (ref_irq_active_7_0::fail_0) will be set to 1.
2	cfm	0: ref0 CFM status changes are masked. 1: ref0 CFM status changes are unmasked. A GPIO interrupt will be generated and register 0x182 bit 0 (ref_irq_active_7_0::fail_0) will be set to 1.
1	scm	0: ref0 SCM status changes are masked. 1: ref0 SCM status changes are unmasked. A GPIO interrupt will be generated and register 0x182 bit 0 (ref_irq_active_7_0::fail_0) will be set to 1.
0	los	0: ref0 LOS status changes are masked. 1: ref0 LOS status changes are unmasked. A GPIO interrupt will be generated and register 0x182 bit 0 (ref_irq_active_7_0::fail_0) will be set to 1.

Address: 0x0085 Name: ref_mon_mask_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x0086 Name: ref_mon_mask_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x0087 Name: ref_mon_mask_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x0088 Name: ref_mon_mask_4 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x0089 Name: ref_mon_mask_5 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x008A Name: ref_mon_mask_6 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x008B Name: ref_mon_mask_7 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x008C Name: ref_mon_mask_8 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x008D Name: ref_mon_mask_9 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x084, bit 4 (ref_mon_mask_0::pfm).
3	gst	See description for register at address 0x084, bit 3 (ref_mon_mask_0::gst).
2	cfm	See description for register at address 0x084, bit 2 (ref_mon_mask_0::cfm).
1	scm	See description for register at address 0x084, bit 1 (ref_mon_mask_0::scm).
0	los	See description for register at address 0x084, bit 0 (ref_mon_mask_0::los).

Address: 0x0094 Name: dpll_mon_mask_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 phase slope limit status changes are masked. 1: DPLL0 phase slope limit status changes are unmasked. A GPIO interrupt will be generated and register 0x184 bit 0 (dpll_irq_active::fail_0) will be set to 1.
6	pmlhit	0: DPLL0 phase memory limit status changes are masked. 1: DPLL0 phase memory limit status changes are unmasked. A GPIO interrupt will be generated and register 0x184 bit 0 (dpll_irq_active::fail_0) will be set to 1.
5	flhit	0: DPLL0 pull-in/hold-in range limit status changes are masked. 1: DPLL0 pull-in/hold-in range limit status changes are unmasked. A GPIO interrupt will be generated and register 0x184 bit 0 (dpll_irq_active::fail_0) will be set to 1.
4:2	reserved	
1	ho	0: DPLL0 holdover status changes are masked. 1: DPLL0 holdover status changes are unmasked. A GPIO interrupt will be generated and register 0x184 bit 0 (dpll_irq_active::fail_0) will be set to 1.
0	lol	0: DPLL0 loss-of-lock status changes are masked. 1: DPLL0 loss-of-lock status changes are unmasked. A GPIO interrupt will be generated and register 0x184 bit 0 (dpll_irq_active::fail_0) will be set to 1.

Address: 0x0095 Name: dpll_mon_mask_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x094, bit 7 (dpll_mon_mask_0::pslhit).
6	pmlhit	See description for register at address 0x094, bit 6 (dpll_mon_mask_0::pmlhit).
5	flhit	See description for register at address 0x094, bit 5 (dpll_mon_mask_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x094, bit 1 (dpll_mon_mask_0::ho).
0	lol	See description for register at address 0x094, bit 0 (dpll_mon_mask_0::lol).

Address: 0x0096 Name: dpll_mon_mask_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x094, bit 7 (dpll_mon_mask_0::pslhit).
6	pmlhit	See description for register at address 0x094, bit 6 (dpll_mon_mask_0::pmlhit).
5	flhit	See description for register at address 0x094, bit 5 (dpll_mon_mask_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x094, bit 1 (dpll_mon_mask_0::ho).
0	lol	See description for register at address 0x094, bit 0 (dpll_mon_mask_0::lol).

Address: 0x0097 Name: dpll_mon_mask_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x094, bit 7 (dpll_mon_mask_0::pslhit).
6	pmlhit	See description for register at address 0x094, bit 6 (dpll_mon_mask_0::pmlhit).
5	flhit	See description for register at address 0x094, bit 5 (dpll_mon_mask_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x094, bit 1 (dpll_mon_mask_0::ho).
0	lol	See description for register at address 0x094, bit 0 (dpll_mon_mask_0::lol).

Address: 0x00A4 Name: gpio_irq_config Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2	high_z	0: The device actively drives the GPIO IRQ pin low when the interrupt is inactive. 1: The device puts the GPIO IRQ pin in high-z mode when the interrupt is inactive.
1	active_high	0: The GPIO IRQ pin will be high when the interrupt is inactive (active-low mode). 1: The GPIO IRQ pin will be high when the interrupt is active (active-high mode).
0	level_trig	0: The GPIO IRQ pin is in edge-triggered mode. When an interrupt occurs, the device will generate a short pulse on the GPIO IRQ pin then return it to the inactive state immediately. Once the interrupt has been acknowledged, new interrupts can be generated. 1: The GPIO IRQ pin is in level-triggered mode. The GPIO IRQ pin will stay low or high (depending on the active_high bit) until the interrupt has been acknowledged. New interrupts cannot be generated until the host has acknowledged the current one by clearing the sticky bits in registers: 0x182 (ref_irq_active_7_0) 0x183 (ref_irq_active_9_8) 0x184 (dpll_irq_active) 0x1B7 (synth_irq_active) 0x1B9 (xomon_irq_active) For both modes, interrupts are generated whenever the status changes (0-to-1 or 1-to-0).

Address: 0x00A5 Name: synth_irq_mask Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	reserved	
6	reserved	
5	reserved	
4	reserved	
3	mask_3	See description for mask_0.
2	mask_2	See description for mask_0.
1	mask_1	See description for mask_0.
0	mask_0	This bit is only considered when GPIO interrupt (IRQ) is turned on. It determines if a GPIO interrupt is generated when synth0 status changes. 0: A synth0 status change will not generate a GPIO interrupt. Register 0x1B7 bit 0 (synth_irq_active::fail_0) will not be set. 1: Certain synth0 status changes will generate a GPIO interrupt. Register 0x1B7 bit 0 (synth_irq_active::fail_0) will be set to 1. See register 0x0A6 (synth_mon_mask_0) to configure which status changes will generate a GPIO interrupt.

Address: 0x00A6 Name: synth_mon_mask_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_b	See description for io_align_done_a.
4	io_align_done_a	0: synth0 I/O alignment status changes on divider A are masked. 1: synth0 I/O alignment status changes on divider A are unmasked. A GPIO interrupt will be generated and register 0x1B7 bit 0 (synth_irq_active::fail_0) will be set to 1.
3	reserved	
2	loss_of_lock	0: synth0 lock status changes are masked. 1: synth0 lock status changes are unmasked. A GPIO interrupt will be generated and register 0x1B7 bit 0 (synth_irq_active::fail_0) will be set to 1.
1:0	reserved	

Address: 0x00A7 Name: synth_mon_mask_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	io_align_done_d	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
6	io_align_done_c	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
5	io_align_done_b	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x0A6, bit 2 (synth_mon_mask_0::loss_of_lock).
1:0	reserved	

Address: 0x00A8 Name: synth_mon_mask_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	io_align_done_d	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
6	io_align_done_c	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
5	io_align_done_b	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x0A6, bit 2 (synth_mon_mask_0::loss_of_lock).
1:0	reserved	

Address: 0x00A9 Name: synth_mon_mask_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_b	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x0A6, bit 4 (synth_mon_mask_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x0A6, bit 2 (synth_mon_mask_0::loss_of_lock).
1:0	reserved	

Address: 0x00AE Name: gpio_out_6_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	reserved	
6	gpio6	Sets the output value on pin GPIO6.
5	gpio5	Sets the output value on pin GPIO5.
4	gpio4	Sets the output value on pin GPIO4.
3	gpio3	Sets the output value on pin GPIO3.
2	gpio2	Sets the output value on pin GPIO2.
1	gpio1	Sets the output value on pin GPIO1.
0	gpio0	Sets the output value on pin GPIO0.

Address: 0x00B2 Name: gpio_freeze_6_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	reserved	
6	gpio6	See description for gpio0.
5	gpio5	See description for gpio0.
4	gpio4	See description for gpio0.
3	gpio3	See description for gpio0.
2	gpio2	See description for gpio0.
1	gpio1	See description for gpio0.
0	gpio0	Freeze the value in register 0x100, bit 0 (gpio_in_status_6_0::gpio0) if GPIO0 is configured as input, control or LOS mode.

Address: 0x00B6:0x00B7 Name: gpio_select_0 Default: 0x0000 Type: R/W		
Bit Field	Function Name	Description
15	reserved	
14:12	bit	This field works with the page and offset field to select a single bit in the host register map. Specifically, this field selects the bit position of the selected register byte.
11:8	page	This field works with the bit and offset fields to select a single bit in the host register map. Specifically, this field selects the page.
7	reserved	
6:0	offset	When GPIO0 is configured as as a Status or Control, then this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page. When GPIO0 is configured as an LOS, then this field selects the target reference.

Address: 0x00B8 Name: gpio_config_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	This field determines the mode of operation for GPIO0. Register 0x0B6-0x0B7 (gpio_select_0) should be set before writing this register, if the mode being set requires additional configuration. 000: Input The logic value sensed on GPIO0 is reflected in register 0x100, bit 0 (gpio_in_status_6_0::gpio0). 001: Output GPIO0 actively drives the value specified in register 0x0AE, bit 0 (gpio_out_6_0::gpio0). 010: Control Certain device functions can be actively controlled via GPIO0. The device function to be controlled is selected by configuring register gpio_select_0. Whenever a change is detected on GPIO0 or the selected host register bit, then the device ORs together the GPIO and register bit values before applying the corresponding configuration. In this mode, the selected host register bit must be a R/W type. 011: Status The device status can be actively supervised via GPIO0. The device mirrors the host register bit, specified in register gpio_select_0, onto GPIO0. Typically, the selected host register bit is a status bit (either R or S type) in this mode. 100: Input (GPIO0 to 3), or IRQ (all other GPIOs) No matter how many GPIOs are configured to IRQ mode, only the GPIO that most recently configured will generate interrupts. If the latest GPIO is then configured to other modes, the next latest GPIO will become active and generate interrupts. GPIO interrupt is disabled only if all the GPIOs are set to non-IRQ modes. 101: LOS The input reference specified by register 0x0B7, bits 6:0 (gpio_select_0::offset) can be forced into failure via GPIO0 control.

Address: 0x00B9:0x00BA Name: gpio_select_1 Default: 0x0000 Type: R/W		
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at address 0x0B6, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0B6, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at address 0x0B7, bits 6:0 (gpio_select_0::offset).

Address: 0x00BB Name: gpio_config_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at address 0x0B8, bits 2:0 (gpio_config_0::ctrl).

Address: 0x00BC:0x00BD Name: gpio_select_2 Default: 0x0000 Type: R/W		
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at address 0x0B6, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0B6, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at address 0x0B7, bits 6:0 (gpio_select_0::offset).

Address: 0x00BE Name: gpio_config_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at address 0x0B8, bits 2:0 (gpio_config_0::ctrl).

Address: 0x00BF:0x00C0 Name: gpio_select_3 Default: 0x0000 Type: R/W		
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at address 0x0B6, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0B6, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at address 0x0B7, bits 6:0 (gpio_select_0::offset).

Address: 0x00C1 Name: gpio_config_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at address 0x0B8, bits 2:0 (gpio_config_0::ctrl).

Address: 0x00C2:0x00C3 Name: gpio_select_4 Default: 0x0000 Type: R/W		
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at address 0x0B6, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0B6, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at address 0x0B7, bits 6:0 (gpio_select_0::offset).

Address: 0x00C4 Name: gpio_config_4 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at address 0x0B8, bits 2:0 (gpio_config_0::ctrl).

Address: 0x00C5:0x00C6 Name: gpio_select_5 Default: 0x0000 Type: R/W		
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at address 0x0B6, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0B6, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at address 0x0B7, bits 6:0 (gpio_select_0::offset).

Address: 0x00C7 Name: gpio_config_5 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at address 0x0B8, bits 2:0 (gpio_config_0::ctrl).

Address: 0x00C8:0x00C9 Name: gpio_select_6 Default: 0x044E Type: R/W		
Bit Field	Function Name	Description
15	reserved	
14:12	bit	See description for register at address 0x0B6, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0B6, bits 11:8 (gpio_select_0::page).
7	reserved	
6:0	offset	See description for register at address 0x0B7, bits 6:0 (gpio_select_0::offset).

Address: 0x00CA Name: gpio_config_6 Default: 0x02 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	ctrl	See description for register at address 0x0B8, bits 2:0 (gpio_config_0::ctrl).

Address: 0x00FE Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x00FF Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.3 Register List (Page 2)

Address: 0x0100 Name: gpio_in_status_6_0 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	reserved	
6	gpio6	See description for gpio0.
5	gpio5	See description for gpio0.
4	gpio4	See description for gpio0.
3	gpio3	See description for gpio0.
2	gpio2	See description for gpio0.
1	gpio1	See description for gpio0.
0	gpio0	Logic value seen on pin GPIO0 if it is configured as input, control or LOS mode.

Address: 0x0106 Name: ref_mon_status_0 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	0: No PFM failure on ref0. 1: PFM failure on ref0 detected.
3	gst	0: No GST failure on ref0. 1: GST failure on ref0 detected.
2	cfm	0: No CFM failure on ref0. 1: CFM failure on ref0 detected.
1	scm	0: No SCM failure on ref0. 1: SCM failure on ref0 detected.
0	los	0: No LOS failure on ref0. 1: LOS failure on ref0 detected.

Address: 0x0107 Name: ref_mon_status_1 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x0108 Name: ref_mon_status_2 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x0109 Name: ref_mon_status_3 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x010A Name: ref_mon_status_4 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x010B Name: ref_mon_status_5 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x010C Name: ref_mon_status_6 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x010D Name: ref_mon_status_7 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x010E Name: ref_mon_status_8 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x010F Name: ref_mon_status_9 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x106, bit 4 (ref_mon_status_0::pfm).
3	gst	See description for register at address 0x106, bit 3 (ref_mon_status_0::gst).
2	cfm	See description for register at address 0x106, bit 2 (ref_mon_status_0::cfm).
1	scm	See description for register at address 0x106, bit 1 (ref_mon_status_0::scm).
0	los	See description for register at address 0x106, bit 0 (ref_mon_status_0::los).

Address: 0x0116 Name: dpll_mon_status_0 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 is below the configured phase slope limit. 1: DPLL0 has hit the configured phase slope limit.
6	pmlhit	0: DPLL0 has not exceeded the configured phase memory limit for the active reference. 1: DPLL0 has exceeded the configured phase memory limit for the active reference.
5	flhit	0: DPLL0 is within the configured pull-in/hold-in range limit. 1: DPLL0 has hit the specified pull-in/hold-in range limit.
4:2	reserved	
1	ho	0: DPLL0 is not in holdover (is either locking or already locked). 1: DPLL0 is in holdover.
0	lol	0: DPLL0 is locked. 1: DPLL0 is not locked.

Address: 0x0117 Name: dpll_mon_status_1 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x116, bit 7 (dpll_mon_status_0::pslhit).
6	pmlhit	See description for register at address 0x116, bit 6 (dpll_mon_status_0::pmlhit).
5	flhit	See description for register at address 0x116, bit 5 (dpll_mon_status_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x116, bit 1 (dpll_mon_status_0::ho).
0	lol	See description for register at address 0x116, bit 0 (dpll_mon_status_0::lol).

Address: 0x0118 Name: dpll_mon_status_2 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x116, bit 7 (dpll_mon_status_0::pslhit).
6	pmlhit	See description for register at address 0x116, bit 6 (dpll_mon_status_0::pmlhit).
5	flhit	See description for register at address 0x116, bit 5 (dpll_mon_status_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x116, bit 1 (dpll_mon_status_0::ho).
0	lol	See description for register at address 0x116, bit 0 (dpll_mon_status_0::lol).

Address: 0x0119 Name: dpll_mon_status_3 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x116, bit 7 (dpll_mon_status_0::pslhit).
6	pmlhit	See description for register at address 0x116, bit 6 (dpll_mon_status_0::pmlhit).
5	flhit	See description for register at address 0x116, bit 5 (dpll_mon_status_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x116, bit 1 (dpll_mon_status_0::ho).
0	lol	See description for register at address 0x116, bit 0 (dpll_mon_status_0::lol).

Address: 0x0126 Name: dpll_refsel_status_1_0 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:4	dpll_1	Indicates the reference selected by DPLL1 (only valid in automatic mode).
3:0	dpll_0	Indicates the reference selected by DPLL0 (only valid in automatic mode).

Address: 0x0127 Name: dpll_refsel_status_3_2 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:4	dpll_3	Indicates the reference selected by DPLL3 (only valid in automatic mode).
3:0	dpll_2	Indicates the reference selected by DPLL2 (only valid in automatic mode).

Address: 0x016E Name: synth_mon_status_0 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	reserved	
6	reserved	
5	io_align_done_b	See description for io_align_done_a.
4	io_align_done_a	0: I/O alignment has not completed on synth0 divider A. 1: I/O alignment has completed on synth0 divider A. This bit will be cleared when the corresponding output or synth0 is disabled.
3	reserved	
2	loss_of_lock	0: synth0 is locked (VCO frequency is in the correct range). 1: synth0 is not locked (VCO frequency is out of the correct range).
1:0	reserved	

Address: 0x016F Name: synth_mon_status_1 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	io_align_done_d	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
6	io_align_done_c	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
5	io_align_done_b	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x16E, bit 2 (synth_mon_status_0::loss_of_lock).
1:0	reserved	

Address: 0x0170 Name: synth_mon_status_2 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7	io_align_done_d	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
6	io_align_done_c	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
5	io_align_done_b	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x16E, bit 2 (synth_mon_status_0::loss_of_lock).
1:0	reserved	

Address: 0x0171 Name: synth_mon_status_3 Default: 0x00 Type: R		
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_b	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x16E, bit 4 (synth_mon_status_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x16E, bit 2 (synth_mon_status_0::loss_of_lock).
1:0	reserved	

Address: 0x017E Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be host read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x017F Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.4 Register List (Page 3)

Address: 0x0180 Name: sticky_lock Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		This register needs to be set to a non-zero value prior to clearing sticky bits, to avoid race condition that can happen when the internal processor updates the register while the host clears the bit. Having non-zero value in this register will prevent the internal processor from updating the sticky bit registers. For proper sticky bit monitoring, the following procedure is recommended: 1) Write non-zero value into this register 2) Clear sticky bits in other registers 3) Write 0 into this register 4) Read sticky bits status registers

Address: 0x0182 Name: ref_irq_active_7_0 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	fail_7	0: ref7 has no unacknowledged interrupts. 1: ref7 interrupt has occurred, not yet acknowledged.
6	fail_6	0: ref6 has no unacknowledged interrupts. 1: ref6 interrupt has occurred, not yet acknowledged.
5	fail_5	0: ref5 has no unacknowledged interrupts. 1: ref5 interrupt has occurred, not yet acknowledged.
4	fail_4	0: ref4 has no unacknowledged interrupts. 1: ref4 interrupt has occurred, not yet acknowledged.
3	fail_3	0: ref3 has no unacknowledged interrupts. 1: ref3 interrupt has occurred, not yet acknowledged.
2	fail_2	0: ref2 has no unacknowledged interrupts. 1: ref2 interrupt has occurred, not yet acknowledged.
1	fail_1	0: ref1 has no unacknowledged interrupts. 1: ref1 interrupt has occurred, not yet acknowledged.
0	fail_0	0: ref0 has no unacknowledged interrupts. 1: ref0 interrupt has occurred, not yet acknowledged.

Address: 0x0183 Name: ref_irq_active_9_8 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:2	reserved	
1	fail_9	0: ref9 has no unacknowledged interrupts. 1: ref9 interrupt has occurred, not yet acknowledged.
0	fail_8	0: ref8 has no unacknowledged interrupts. 1: ref8 interrupt has occurred, not yet acknowledged.

Address: 0x0184 Name: dpll_irq_active Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:4	reserved	
3	fail_3	0: DPLL3 has no unacknowledged interrupts. 1: DPLL3 interrupt has occurred, not yet acknowledged.
2	fail_2	0: DPLL2 has no unacknowledged interrupts. 1: DPLL2 interrupt has occurred, not yet acknowledged.
1	fail_1	0: DPLL1 has no unacknowledged interrupts. 1: DPLL1 interrupt has occurred, not yet acknowledged.
0	fail_0	0: DPLL0 has no unacknowledged interrupts. 1: DPLL0 interrupt has occurred, not yet acknowledged.

Address: 0x0186 Name: ref_mon_sticky_0 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	0: ref0 has no unacknowledged PFM failures. 1: ref0 PFM failure has occurred, not yet acknowledged.
3	gst	0: ref0 has no unacknowledged GST failures. 1: ref0 GST failure has occurred, not yet acknowledged.
2	cfm	0: ref0 has no unacknowledged CFM failures. 1: ref0 CFM failure has occurred, not yet acknowledged.
1	scm	0: ref0 has no unacknowledged SCM failures. 1: ref0 SCM failure has occurred, not yet acknowledged.
0	los	0: ref0 has no unacknowledged LOS failures. 1: ref0 LOS failure has occurred, not yet acknowledged.

Address: 0x0187 Name: ref_mon_sticky_1 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x0188 Name: ref_mon_sticky_2 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x0189 Name: ref_mon_sticky_3 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x018A Name: ref_mon_sticky_4 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x018B Name: ref_mon_sticky_5 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x018C Name: ref_mon_sticky_6 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x018D Name: ref_mon_sticky_7 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x018E Name: ref_mon_sticky_8 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x018F Name: ref_mon_sticky_9 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	See description for register at address 0x186, bit 4 (ref_mon_sticky_0::pfm).
3	gst	See description for register at address 0x186, bit 3 (ref_mon_sticky_0::gst).
2	cfm	See description for register at address 0x186, bit 2 (ref_mon_sticky_0::cfm).
1	scm	See description for register at address 0x186, bit 1 (ref_mon_sticky_0::scm).
0	los	See description for register at address 0x186, bit 0 (ref_mon_sticky_0::los).

Address: 0x0196 Name: dpll_mon_sticky_0 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	pslhit	0: DPLL0 has no unacknowledged phase slope limit failures. 1: DPLL0 phase slope limit failure has occurred, not yet acknowledged.
6	pmlhit	0: DPLL0 has no unacknowledged phase memory limit failures. 1: DPLL0 phase memory limit failure has occurred, not yet acknowledged.
5	flhit	0: DPLL0 has no unacknowledged pull-in/hold-in range limit failures. 1: DPLL0 pull-in/hold-in range limit failure has occurred, not yet acknowledged.
4:2	reserved	
1	ho	0: DPLL0 is not in holdover (is locking or already locked). 1: DPLL0 holdover entry detected, not yet acknowledged.
0	lol	0: DPLL0 is locked. 1: DPLL0 loss of lock detected, not yet acknowledged.

Address: 0x0197 Name: dpll_mon_sticky_1 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x196, bit 7 (dpll_mon_sticky_0::pslhit).
6	pmlhit	See description for register at address 0x196, bit 6 (dpll_mon_sticky_0::pmlhit).
5	flhit	See description for register at address 0x196, bit 5 (dpll_mon_sticky_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x196, bit 1 (dpll_mon_sticky_0::ho).
0	lol	See description for register at address 0x196, bit 0 (dpll_mon_sticky_0::lol).

Address: 0x0198 Name: dpll_mon_sticky_2 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x196, bit 7 (dpll_mon_sticky_0::pslhit).
6	pmlhit	See description for register at address 0x196, bit 6 (dpll_mon_sticky_0::pmlhit).
5	flhit	See description for register at address 0x196, bit 5 (dpll_mon_sticky_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x196, bit 1 (dpll_mon_sticky_0::ho).
0	lol	See description for register at address 0x196, bit 0 (dpll_mon_sticky_0::lol).

Address: 0x0199 Name: dpll_mon_sticky_3 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	pslhit	See description for register at address 0x196, bit 7 (dpll_mon_sticky_0::pslhit).
6	pmlhit	See description for register at address 0x196, bit 6 (dpll_mon_sticky_0::pmlhit).
5	flhit	See description for register at address 0x196, bit 5 (dpll_mon_sticky_0::flhit).
4:2	reserved	
1	ho	See description for register at address 0x196, bit 1 (dpll_mon_sticky_0::ho).
0	lol	See description for register at address 0x196, bit 0 (dpll_mon_sticky_0::lol).

Address: 0x01A6 Name: dpll_fastlock_phase_sticky Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:4	reserved	
3	dpll_3	0: DPLL3 has no unacknowledged fast lock phase error status. 1: DPLL3 fast lock phase error threshold exceeded, not yet acknowledged.
2	dpll_2	0: DPLL2 has no unacknowledged fast lock phase error status. 1: DPLL2 fast lock phase error threshold exceeded, not yet acknowledged.
1	dpll_1	0: DPLL1 has no unacknowledged fast lock phase error status. 1: DPLL1 fast lock phase error threshold exceeded, not yet acknowledged.
0	dpll_0	0: DPLL0 has no unacknowledged fast lock phase error status. 1: DPLL0 fast lock phase error threshold exceeded, not yet acknowledged.

Address: 0x01A8 Name: dpll_fastlock_freq_sticky Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:4	reserved	
3	dpll_3	0: DPLL3 has no unacknowledged fast lock frequency error status. 1: DPLL3 fast lock frequency error threshold exceeded, not yet acknowledged.
2	dpll_2	0: DPLL2 has no unacknowledged fast lock frequency error status. 1: DPLL2 fast lock frequency error threshold exceeded, not yet acknowledged.
1	dpll_1	0: DPLL1 has no unacknowledged fast lock frequency error status. 1: DPLL1 fast lock frequency error threshold exceeded, not yet acknowledged.
0	dpll_0	0: DPLL0 has no unacknowledged fast lock frequency error status. 1: DPLL0 fast lock frequency error threshold exceeded, not yet acknowledged.

Address: 0x01AA Name: dpll_tie_wr_sticky Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	reserved	
6:4	reserved	
3	dpll_3	0: DPLL3 has no unacknowledged TIE write status. 1: DPLL3 TIE write completed, not yet acknowledged.
2	dpll_2	0: DPLL2 has no unacknowledged TIE write status. 1: DPLL2 TIE write completed, not yet acknowledged.
1	dpll_1	0: DPLL1 has no unacknowledged TIE write status. 1: DPLL1 TIE write completed, not yet acknowledged.
0	dpll_0	0: DPLL0 has no unacknowledged TIE write status. 1: DPLL0 TIE write completed, not yet acknowledged.

Address: 0x01AC Name: synth_step_sticky_1_0 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	synth1_div_d	0: synth1 divider D has no unacknowledged phase step status. 1: synth1 divider D phase step has completed, not yet acknowledged.
6	synth1_div_c	0: synth1 divider C has no unacknowledged phase step status. 1: synth1 divider C phase step has completed, not yet acknowledged.
5	synth1_div_b	0: synth1 divider B has no unacknowledged phase step status. 1: synth1 divider B phase step has completed, not yet acknowledged.
4	synth1_div_a	0: synth1 divider A has no unacknowledged phase step status. 1: synth1 divider A phase step has completed, not yet acknowledged.
3:2	reserved	
1	synth0_div_b	0: synth0 divider B has no unacknowledged phase step status. 1: synth0 divider B phase step has completed, not yet acknowledged.
0	synth0_div_a	0: synth0 divider A has no unacknowledged phase step status. 1: synth0 divider A phase step has completed, not yet acknowledged.

Address: 0x01AD Name: synth_step_sticky_3_2 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:6	reserved	
5	synth3_div_b	0: synth3 divider B has no unacknowledged phase step status. 1: synth3 divider B phase step has completed, not yet acknowledged.
4	synth3_div_a	0: synth3 divider A has no unacknowledged phase step status. 1: synth3 divider A phase step has completed, not yet acknowledged.
3	synth2_div_d	0: synth2 divider D has no unacknowledged phase step status. 1: synth2 divider D phase step has completed, not yet acknowledged.
2	synth2_div_c	0: synth2 divider C has no unacknowledged phase step status. 1: synth2 divider C phase step has completed, not yet acknowledged.
1	synth2_div_b	0: synth2 divider B has no unacknowledged phase step status. 1: synth2 divider B phase step has completed, not yet acknowledged.
0	synth2_div_a	0: synth2 divider A has no unacknowledged phase step status. 1: synth2 divider A phase step has completed, not yet acknowledged.

Address: 0x01B0 Name: synth_mon_sticky_0 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_b	See description for io_align_done_a.
4	io_align_done_a	0: synth0 divider A has no unacknowledged I/O alignment completions. 1: synth0 divider A has compeletd I/O alignment, not yet acknowledged.
3	reserved	
2	loss_of_lock	0: synth0 has no unacknowledged loss-of-lock failures. 1: synth0 loss-of-lock failure has occurred, not yet acknowledged.
1:0	reserved	

Address: 0x01B1 Name: synth_mon_sticky_1 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	io_align_done_d	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
6	io_align_done_c	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
5	io_align_done_b	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x1B0 bit 2 (synth_mon_sticky_0::loss_of_lock).
1:0	reserved	

Address: 0x01B2 Name: synth_mon_sticky_2 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7	io_align_done_d	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
6	io_align_done_c	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
5	io_align_done_b	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x1B0 bit 2 (synth_mon_sticky_0::loss_of_lock).
1:0	reserved	

Address: 0x01B3 Name: synth_mon_sticky_3 Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:6	reserved	
5	io_align_done_b	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
4	io_align_done_a	See description for register at address 0x1B0 bit 4 (synth_mon_sticky_0::io_align_done_a).
3	reserved	
2	loss_of_lock	See description for register at address 0x1B0 bit 2 (synth_mon_sticky_0::loss_of_lock).
1:0	reserved	

Address: 0x01B7 Name: synth_irq_active Default: 0x00 Type: S		
Bit Field	Function Name	Description
7:4	reserved	
3	fail_3	See description for fail_0.
2	fail_2	See description for fail_0.
1	fail_1	See description for fail_0.
0	fail_0	0: synth0 has no unacknowledged interrupts. 1: synth0 interrupt has occurred, not yet acknowledged.

Address: 0x01FE Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x01FF Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.5 Register List (Page 4)

Address: 0x0200 Name: ref_los_7_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7	los_7	Ref7 external Loss Of Signal (LOS) - indicator to DPLLs that Ref7 has failed. Internally in the DPLLs this signal is used for reference monitor indicator, reference switching or holdover entering and for ISR generation.
6	los_6	External LOS for Ref6
5	los_5	External LOS for Ref5
4	los_4	External LOS for Ref4
3	los_3	External LOS for Ref3
2	los_2	External LOS for Ref2
1	los_1	External LOS for Ref1
0	los_0	External LOS for Ref0

Address: 0x0201 Name: ref_los_9_8 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	reserved	
3:2	reserved	
1	los_9	External LOS for Ref9
0	los_8	External LOS for Ref8

Address: 0x021C Name: dpll_enable Default: 0x04 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	num	0: All DPLLs disabled. n: DPLL0 to DPLL(n-1) enabled. If n is greater than the highest numbered DPLL, all DPLLs will be enabled.

Address: 0x021D Name: split_xo_mode_control Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	ref	Sets the reference to use as the TCXO/OCXO input source. An invalid reference number will set the source to ref0.
3:1	reserved	
0	en	0: Split-XO mode disabled. 1: Split-XO mode enabled. **Note**: Changing this bit will cause the device to perform a warm start. **Note 2**: Following the warm start the **revision** register (0x003) will be set to 0x00. To determine the correct revision of the device, the revision register (0x003) should be read before split_xo mode is enabled.

Address: 0x021E Name: dpll_mode_refsel_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	ref	Specifies which reference the DPLL0 is forced to select, when the mode bitfield is set to '010' (forced reference lock mode). When this forced reference fails, DPLL0 will go to holdover state. An invalid reference number will select ref0. When DPLL0 is not in forced reference lock mode, this bitfield is ignored.
3	reserved	
2:0	mode	000: Freerun mode 001: Forced holodover mode 010: Forced reference lock mode 011: Automatic mode 100: NCO mode 101-111: Invalid (automatic mode)

Address: 0x021F Name: dpll_ctrl_0 Default: 0x08 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	nco_auto_read	0: DPLL0 automatic NCO read is disabled. 1: DPLL0 automatic NCO read is enabled. When switching to forced holdover or NCO modes, an NCO read operation is automatically performed, the device will write DPLL0's frequency offset to register 0x300-0x304 (dpll_df_offset_0).
3:2	reserved	
1	tie_clear	0: DPLL0 will not align its output to the reset position. This represents "hitless" reference switching mode. 1: DPLL0 will align its outputs to the reset position (specified by appropriate phase shift selection). This bit should be set when initial output to input alignment is desired after numerous reference rearrangements.
0	reserved	

Address: 0x0221 Name: dpll_mode_refsel_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	ref	See description for register at address 0x21E, bits 7:4 (dpll_mode_refsel_0::ref).
3	reserved	
2:0	mode	See description for register at address 0x21E, bits 2:0 (dpll_mode_refsel_0::mode).

Address: 0x0222 Name: dpll_ctrl_1 Default: 0x08 Type: R/W		
Bit Field	Function Name	Description
7	reserved	
6:5	reserved	
4	nco_auto_read	See description for register at address 0x21F, bit 4 (dpll_ctrl_0::nco_auto_read).
3:2	reserved	
1	tie_clear	See description for register at address 0x21F, bit 1 (dpll_ctrl_0::tie_clear).
0	reserved	

Address: 0x0224 Name: dpll_mode_refsel_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	ref	See description for register at address 0x21E, bits 7:4 (dpll_mode_refsel_0::ref).
3	reserved	
2:0	mode	See description for register at address 0x21E, bits 2:0 (dpll_mode_refsel_0::mode).

Address: 0x0225 Name: dpll_ctrl_2 Default: 0x08 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	nco_auto_read	See description for register at address 0x21F, bit 4 (dpll_ctrl_0::nco_auto_read).
3:2	reserved	
1	tie_clear	See description for register at address 0x21F, bit 1 (dpll_ctrl_0::tie_clear).
0	reserved	

Address: 0x0227 Name: dpll_mode_refsel_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	ref	See description for register at address 0x21E, bits 7:4 (dpll_mode_refsel_0::ref).
3	reserved	
2:0	mode	See description for register at address 0x21E, bits 2:0 (dpll_mode_refsel_0::mode).

Address: 0x0228 Name: dpll_ctrl_3 Default: 0x08 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	nco_auto_read	See description for register at address 0x21F, bit 4 (dpll_ctrl_0::nco_auto_read).
3:2	reserved	
1	tie_clear	See description for register at address 0x21F, bit 1 (dpll_ctrl_0::tie_clear).
0	reserved	

Address: 0x024E Name: gp_out_ctrl Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:2	reserved	
1	gp_en_1	gpoutclk1 is a CMOS output driven by synth0 divider B. 0: Output disabled 1: Output enabled
0	gp_en_0	gpoutclk0 is a CMOS output driven by synth0 divider A. 0: Output disabled 1: Output enabled

Address: 0x0250 Name: hp_out_ctrl_1 Default: 0xF0 Type: R/W		
Bit Field	Function Name	Description
7	hp_type_2	Controls the type of output on hpoutclk2 and 3. 0: Outputs are CMOS. 1: Outputs are a differential pair and depend on hp_route_2. hp_clone_2 and hp_route_3 are ignored.
6	hp_clone_2	0: hpoutclk2 depends on hp_route_2. hpoutclk3 depends on hp_route_3. 1: hpoutclk2 and 3 depend on hp_route_2. hp_route_3 is ignored.
5	hp_type_0	Controls the type of output on hpoutclk0 and 1. 0: Outputs are CMOS. 1: Outputs are a differential pair driven by synth1 divider A. hp_clone_0 is ignored.
4	hp_clone_0	0: hpoutclk0 is driven by synth1 divider A. hpoutclk1 is driven by synth1 divider B. 1: hpoutclk0 and 1 are driven by synth1 divider A.
3	hp_en_3	Controls the state of hpoutclk3 in CMOS mode. Ignored in differential mode. See hp_type_2 bit to set output mode. When this bit is set to 0, hp_clone_2 must also be set to 0. 0: Output disabled 1: Output enabled
2	hp_en_2	Controls the state of hpoutclk2 in CMOS mode. Controls the state of hpoutclk2 and 3 in differential mode. See hp_type_1 bit to set output mode. 0: Output(s) disabled 1: Output(s) enabled
1	hp_en_1	Controls the state of hpoutclk1 in CMOS mode. Ignored in differential mode. See hp_type_0 bit to set output mode. 0: Output disabled 1: Output enabled
0	hp_en_0	Controls the state of hpoutclk0 in CMOS mode. Controls the state of hpoutclk0 and 1 in differential mode. See hp_type_0 bit to set output mode. 0: Output(s) disabled 1: Output(s) enabled

Address: 0x0251 Name: hp_out_routing_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	reserved	
3	hp_route_3	0: synth1 divider D drives hpoutclk3 1: synth1 divider B drives hpoutclk3
2	hp_route_2	0: synth1 divider C drives hpoutclk2 1: synth1 divider A drives hpoutclk2
1:0	reserved	

Address: 0x0252 Name: hp_out_ctrl_2 Default: 0xA0 Type: R/W		
Bit Field	Function Name	Description
7	hp_type_6	Controls the type of output on hpoutclk6 and 7. Outputs dividers depend on register 0x253, bit 2 (hp_out_routing_2::hp_route_6). 0: Outputs are CMOS. 1: Outputs are a differential pair.
6	reserved	
5	hp_type_4	Controls the type of output on hpoutclk4 and 5. Outputs are driven by synth2 divider A. 0: Outputs are CMOS. 1: Outputs are a differential pair.
4	reserved	
3	hp_en_7	Controls the state of hpoutclk7 in CMOS mode. Ignored in differential mode. See hp_type_6 bit to set output mode. 0: Output disabled 1: Output enabled
2	hp_en_6	Controls the state of hpoutclk6 in CMOS mode. Controls the state of hpoutclk6 and 7 in differential mode. See hp_type_6 bit to set output mode. 0: Output(s) disabled 1: Output(s) enabled
1	hp_en_5	Controls the state of hpoutclk5 in CMOS mode. Ignored in differential mode. See hp_type_4 bit to set output mode. 0: Output disabled 1: Output enabled
0	hp_en_4	Controls the state of hpoutclk4 in CMOS mode. Controls the state of hpoutclk4 and 5 in differential mode. See hp_type_4 bit to set output mode. 0: Output(s) disabled 1: Output(s) enabled

Address: 0x0253 Name: hp_out_routing_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2	hp_route_6	0: synth2 divider B drives hpoutclk6 and 7 1: synth2 divider A drives hpoutclk6 and 7
1:0	reserved	

Address: 0x0254 Name: hp_out_ctrl_3 Default: 0xA0 Type: R/W		
Bit Field	Function Name	Description
7	hp_type_10	Controls the type of output on hpoutclk10 and 11. 0: Outputs are CMOS. 1: Outputs are a differential pair. Output dividers depend on register 0x255, bit 2 (hp_out_routing_3::hp_route_10).
6	reserved	
5	hp_type_8	Controls the type of output on hpoutclk8 and 9. 0: Outputs are CMOS. 1: Outputs are a differential pair. Output dividers depend on synth2 mailbox register 0x694, bit 0 (synth_config2::remap). remap = 0: Outputs are driven by synth3 divider A. remap = 1: Outputs are driven by synth2 divider C.
4	reserved	
3	hp_en_11	Controls the state of hpoutclk11 in CMOS mode. Ignored in differential mode. See hp_type_10 bit to set output mode. 0: Output disabled 1: Output enabled
2	hp_en_10	Controls the state of hpoutclk10 in CMOS mode. Controls the state of hpoutclk10 and 11 in differential mode. See hp_type_10 bit to set output mode. 0: Output(s) disabled 1: Output(s) enabled
1	hp_en_9	Controls the state of hpoutclk9 in CMOS mode. Ignored in differential mode. See hp_type_8 bit to set output mode. 0: Output disabled 1: Output enabled
0	hp_en_8	Controls the state of hpoutclk8 in CMOS mode. Controls the state of hpoutclk8 and 9 in differential mode. See hp_type_8 bit to set output mode. 0: Output(s) disabled 1: Output(s) enabled

Address: 0x0255 Name: hp_out_routing_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2	hp_route_10	The behavior of this bit depends on the value of synth2 mailbox register 0x694, bit 0 (synth_config2::remap). remap = 0: 0: synth3 divider B drives hpoutclk10 and 11 1: synth3 divider A drives hpoutclk10 and 11 remap = 1: 0: synth2 divider D drives hpoutclk10 and 11 1: synth2 divider C drives hpoutclk10 and 11
1:0	reserved	

Address: 0x025C Name: calibr_alignment_ctrl Default: 0x01 Type: R/W		
Bit Field	Function Name	Description
7:1	reserved	
0	master_en	0: Fine I/O alignment disabled. 1: Fine I/O alignment enabled.

Address: 0x027E Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x027F Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.6 Register List (Page 5)

Address:	0x02D0	
Name:	ext_fb_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	en	0: External feedback is disabled 1: External feedback is enabled Before modifying this bit, all synths driven by the DPLL specified in register 0x2D1, bits 2:0 (ext_fb_sel::dpll) should be disabled. After modifying this bit, the synths can then be re-enabled.

Address:	0x02D1	
Name:	ext_fb_sel	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref	Sets the reference to use as the external feedback source. An invalid reference number will disable external feedback.
3	reserved	
2:0	dpll	Sets the DPLL to use for external feedback. External feedback phase represents the difference in phase between this DPLL's selected active reference and selected feedback source. An invalid DPLL number will disable external feedback. Note 1: If external feedback is enabled for a specific DPLL (see mailbox register 0x608 bit 0, dpll_config::ext_fb_en), that DPLL's output phase will be compensated for by the external feedback phase, regardless which DPLL is used for the external feedback phase calculation. Note 2: In order to have proper behavior with external feedback, it is required that main reference and the external feedback source are frequency locked (they do not have to have the same carrier frequency).

Address:	0x02FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x02FF Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.7 Register List (Page 6)

Address: 0x0300:0x0304 Name: dpll_df_offset_0 Default: 0x0000000000 Type: R/W		
Bit Field	Function Name	Description
39:0		When DPLL0 is programmed into NCO mode (dpll_mode_refsel_0 register), this register contains a 2's complement binary value of delta frequency offset. This register controls delta frequency of synthesizers that are associated with DPLL0. Delta frequency is expressed in steps of +/- 2^-40 of nominal setting. The output frequency should be calculated as per formula: f_out = (1 - X/2^40)*f_nom where, X is 2's complement number specified in this register, f_nom is the nominal frequency set by Bs, Ks, Ms, Ns and postdivider number for particular Synthesizer and f_out is the desired output frequency Note 1: The delta frequency offset should not exceed +/-1% of the nominal value. Note 2: This register can be written as fast as once per 600us, but no faster. Note 3: This register should not be written while a read operation is pending.

Address:	0x0305	
Name:	dpll_df_ctrl_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	Set to 1 to perform a manual df offset read. When the operation has completed, the result is written to registers 0x300-0x304 (dpll_df_offset_0), then the device sets this bit to 0. The host always writes a 1 value, while the device writes 0. To avoid race conditions, the host should check this bit for a 0 value, before writing to it.
3	reserved	
2:0	cmd	Sets the type of delta frequency read operation for manual reads (by setting read_sem to 1) and automatic NCO reads (when dpll_ctrl_0::nco_auto_read is 1). Normal operation: x00: Read the accumulated I-part (iMemory) x01: Read the output of the holdover filter (filtered iMemory) x10: Read the sum of the P and I-parts (delta frequency) x11: Read P-part only Holdover: 0xx: Read the output of the holdover filter 100: Read the accumulated I-part, latched before entering holdover 101: Read the output of the holdover filter 110: Read the sum of the P and I-parts, latched before entering holdover 111: Read P-part only, latched before entering holdover NCO (all reads represent values latched before entering NCO): x00: Read the accumulated I-part x01: Read the output of the holdover filter 010: Depends on previous state... Normal: Read the sum of the P and I-parts Holdover: Read the output of the holdover filter 110: Read the sum of the P and I-parts x11: Read P-part only

Address:	0x0306:0x0309	
Name:	dpll_tie_data_0	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		This register contains the argument or results of a DPLL0 time interval error (TIE) control operation. LSB = 1ns. See register 0x30A (dpll_tie_ctrl_0) for details on TIE control operations. This register should only be read or written when register 0x30A bits 1:0 (dpll_tie_ctrl_0::op) == 00.

Address: 0x030A Name: dpll_tie_ctrl_0 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:2	reserved	
1:0	op	This field selects a time interval error (TIE) related operation to perform. When the operation request has been latched by the device, this bitfield reads 00. To prevent race conditions, the host only writes non-zero values to this register, while the device only writes zero. The host controller should read this register prior to writing, and should only write to this bitfield when it contains value 00. All operations provided by this register are only valid when DPLL0 is in forced reference or automatic or mode (see register 0x21E) with a valid, qualified reference. If an operation is requested on DPLL0 in another mode of operation (e.g., NCO mode), then the operation will be delayed until DPLL0 is configured to forced reference or automatic mode with a qualified reference. Available operations are: 00: Previous operation complete / new operation can be requested 01: Request a Snap MTIE operation 10: Request to read TIE 11: Request to write TIE Snap MTIE: When the input reference is 1Hz, the DPLL0 bandwidth must be <= 30 mHz. With such a low bandwidth and a low edge rate it would take very long time to do zero phase alignment between the input and output. This operation allows the user to perform an instantaneous I/O alignment. This alignment zeros out hitless reference switch TIE and Write TIE offsets, but excludes post-divider phase steps. The instantaneous alignment is completed when this bitfield reads 00. Read TIE: Reads the TIE between the input reference and output, not including post-divider phase steps. The results are returned in registers 0x306-0x309 (dpll_tie_data_0). The results are valid when this bitfield reads 00. The return value "wraps around" such that the range is -1s to 1s. When mailbox register 0x608, bit 3 (dpll_ctrl::low_freq_mode) is set to 1, the return range is -2s to 2s. Write TIE: Write the TIE between the input reference and output. The desired TIE value is written to registers 0x306-0x309 (dpll_tie_data_0) prior to writing this bitfield. The allowed range is -1s to 1s. When mailbox register 0x608, bit 3 (dpll_ctrl::low_freq_mode) is set to 1, the allowed range is -2s to 2s. Another write TIE request can be made only after this bitfield reads 00. Register 0x1AA (dpll_tie_wr_sticky) can be used to determine when the requested TIE has been fully applied to the output. Write TIE operations are cumulative; subsequent write TIEs are added to the previous TIE.

Address: 0x0310:0x0314 Name: dpll_df_offset_1 Default: 0x0000000000 Type: R/W		
Bit Field	Function Name	Description
39:0		See description for register at address 0x300-0x304 (dpll_df_offset_0).

Address: 0x0315 Name: dpll_df_ctrl_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at address 0x305, bit 4 (dpll_df_ctrl_0::read_sem).
3	reserved	
2:0	cmd	See description for register at address 0x305, bits 2:0 (dpll_df_ctrl_0::cmd).

Address: 0x0316:0x0319 Name: dpll_tie_data_1 Default: 0x00000000 Type: R/W		
Bit Field	Function Name	Description
31:0		See description for register at address 0x306-0x309 (dpll_tie_data_0).

Address: 0x031A Name: dpll_tie_ctrl_1 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:2	reserved	
1:0	op	See description for register at address 0x30A, bits 1:0 (dpll_tie_ctrl_0::op).

Address: 0x0320:0x0324 Name: dpll_df_offset_2 Default: 0x0000000000 Type: R/W		
Bit Field	Function Name	Description
39:0		See description for register at address 0x300-0x304 (dpll_df_offset_0).

Address: 0x0325 Name: dpll_df_ctrl_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at address 0x305, bit 4 (dpll_df_ctrl_0::read_sem).
3	reserved	
2:0	cmd	See description for register at address 0x305, bits 2:0 (dpll_df_ctrl_0::cmd).

Address: 0x0326:0x0329 Name: dpll_tie_data_2 Default: 0x00000000 Type: R/W		
Bit Field	Function Name	Description
31:0		See description for register at address 0x306-0x309 (dpll_tie_data_0).

Address: 0x032A Name: dpll_tie_ctrl_2 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:2	reserved	
1:0	op	See description for register at address 0x30A, bits 1:0 (dpll_tie_ctrl_0::op).

Address: 0x0330:0x0334 Name: dpll_df_offset_3 Default: 0x0000000000 Type: R/W		
Bit Field	Function Name	Description
39:0		See description for register at address 0x300-0x304 (dpll_df_offset_0).

Address: 0x0335 Name: dpll_df_ctrl_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	read_sem	See description for register at address 0x305, bit 4 (dpll_df_ctrl_0::read_sem).
3	reserved	
2:0	cmd	See description for register at address 0x305, bits 2:0 (dpll_df_ctrl_0::cmd).

Address: 0x0336:0x0339 Name: dpll_tie_data_3 Default: 0x00000000 Type: R/W		
Bit Field	Function Name	Description
31:0		See description for register at address 0x306-0x309 (dpll_tie_data_0).

Address: 0x033A Name: dpll_tie_ctrl_3 Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:2	reserved	
1:0	op	See description for register at address 0x30A, bits 1:0 (dpll_tie_ctrl_0::op).

Address: 0x037E Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x037F Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.8 Register List (Page 10)

Address:	0x0501	
Name:	phase_step_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:4	dpll	Selects the DPLL that is the target of the requested phase step operation. This bitfield should be set during the same write that changes the op bitfield to a non-zero value. If this value is invalid, no phase step operation will execute.
3:2	reserved	
1:0	op	This field selects a Phase-Step-related operation to perform. When the device has grabbed the information in phase_step_data and phase_step_max registers (see registers 0x0502-0x0506), this field is cleared to 0x00. To prevent race conditions, the host only writes non-zero values to this field, while the device only writes zero. The host controller should read this field prior to writing, and should only write to this field when it contains a 0x00 value. Available operations are: 00 = Previous operation complete / New operation can be requested 01 = Request a Phase Step Reset 10 = Request a Phase Step Read 11 = Request a Phase Step Write Below is a summary of each of the operations. Phase Step Write: Write and apply a new Phase Step Offset to the specified synthesizer (see Synthesizer Selection). The desired phase step value should be written to the phase_step_data register prior to writing this field. Phase step operations are cumulative -- subsequent phase steps are added to the previous accumulated phase step offset. Phase Step Read Read the current Phase Step Offset for the specified synthesizer (see Synthesizer Selection). The result of this operation is found in the phase_step_data register once the control field has returned to 0x00. Note that bits 7:4 are used to select which output is read, and that only one output should be selected for read operations. Phase Step Reset: Clears all previously applied phase steps.

Address:	0x0502:0x0505	
Name:	phase_step_data	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		This register contains the argument or results of a Phase Step control operation. For details, see the phase_step_ctrl register. This register should not be read or written while a Phase Step control operation is ongoing. The register should only be read or written when the phase_step_ctrl::op bitfield is zero. The phase step contained in this register is a 32-bit signed word with the MSB at the lowest address. The signed representation is in 2's complement form. A positive phase step implies phase advancement and a negative step implies phase delay. The step size of the phase step data is 1.25ns.

Address:	0x0506	
Name:	phase_step_max	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This register contains a numerical value which specifies the maximum phase step to be applied to an output clock/frame pulse. This value is specified as a percentage of the output clock/frame pulse period. This value must be between 1 and 49.

Address:	0x0510	
Name:	synth_step_div_mask_1_0	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7	synth1_div_d	Request phase step on synthesizer 1 divider D
6	synth1_div_c	Request phase step on synthesizer 1 divider C
5	synth1_div_b	Request phase step on synthesizer 1 divider B
4	synth1_div_a	Request phase step on synthesizer 1 divider A
3:2	reserved	
1	synth0_div_b	Request phase step on synthesizer 0 divider B
0	synth0_div_a	Request phase step on synthesizer 0 divider A

Address:	0x0511	
Name:	synth_step_div_mask_3_2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	synth3_div_b	Request phase step on synthesizer 3 divider B
4	synth3_div_a	Request phase step on synthesizer 3 divider A
3	synth2_div_d	Request phase step on synthesizer 2 divider D
2	synth2_div_c	Request phase step on synthesizer 2 divider C
1	synth2_div_b	Request phase step on synthesizer 2 divider B
0	synth2_div_a	Request phase step on synthesizer 2 divider A

Address:	0x057E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x057F Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.9 Register List (Page 11)

Address: 0x0582:0x0583 Name: ref_ctrl Default: 0x0001 Type: R/W		
Bit Field	Function Name	Description
15:12	reserved	
11:0	mask	For a write operation (see ref_semaphore_wr bit), this field determines which input reference's configuration is modified. Multiple bits can be set to affect multiple references in a single operation. For a read operation (see ref_semaphore_rd bit), this field determines which input reference configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 – REFIN0_0P Bit 1 – REFIN1_0N Bit 2 – REFIN2_1P Bit 3 – REFIN3_1N Bit 4 – REFIN4_2P Bit 5 – REFIN5_2N Bit 6 – REFIN6_3P Bit 7 – REFIN7_3N Bit 8 – REFIN8_4P Bit 9 – REFIN9_4N Bit 10 – unused Bit 11 – unused

Address:	0x0584	
Name:	ref_mb_sem	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	rd	When this bit is written to a one by the host controller, the device will perform a read of the masked reference (see ref_ctrl register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding Input Referecence configuration.
0	wr	When this bit is written to a one by the host controller (and the read bit is zero), the device will perform a write of the masked references (see ref_ctrl register). All of the configuration options on this page will be applied to each of the references indicated by the reg_ctrl mask. The write is complete when this register reads back a zero.

Address:	0x0585:0x0586	
Name:	ref_freq_base	
Default:	0x9C40	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the input reference base frequency (Br), in Hz. The final expected input reference is given by: f_hz = Br * Kr * Mr / Nr Some example frequency configurations are show below: Reference Frequency ref_freq_base(Br) ref_freq_mult(Kr) 8 kHz 1kHz (0x07D0) 8 (0x0008) 19.44 MHz 20kHz(0x9C40) 972 (0x01E6) 155.52 MHz 20kHz(0x9C40) 7776 (0x1E60)

Address:	0x0587:0x0588	
Name:	ref_freq_mult	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the input reference frequency multiple (Kr).

Address:	0x0589:0x058A	
Name:	ref_ratio_m	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the FEC ratio numerator (Mr).

Address: 0x058B:0x058C Name: ref_ratio_n Default: 0x0001 Type: R/W		
Bit Field	Function Name	Description
15:0		Sets the FEC ratio denominator (Nr).

Address: 0x058D Name: ref_config Default: 0x01 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pre_divide	When this bit is set, the associated reference input clock will be divided by 2 prior being processed by the DPLLs. All register programming that requires information about this reference's frequency should be done with half of the actual input frequency. When cleared, the associated reference input will not be divided prior to being processed by the DPLLs.
3	reserved	
2	diff_en	When this bit is set, the device expects a differential signal the associated reference pins (REFn REFn+1). When cleared, the device expects a single-ended signal on the associated REFn pin. This bit is ignored for odd-numbered references.
1	lvpecl_en	When this bit is set, the device expects a single-ended LVPECL signal on the associated REFn pin. This bit is ignored if the reference is part of a differential pair (e.g., if the diff_en bit is set for ref0, this bit is ignored on ref0 and ref1).
0	enable	When this bit is set, the phase acquisition module of the associated reference will be enabled. When cleared, the associated phase acquisition module is disabled (powered down).

Address: 0x058F Name: ref_scm Default: 0x05 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	limit	Sets the Single Cycle Monitor (SCM) limit selection. When the reference fails the specified criteria, the scm bit in the associated ref_mon_status_n register will be high. Selection: 000: +/- 0.1% (input frequency units) 001: +/- 0.5% 010: +/- 1% 011: +/- 2% 100: +/- 5% 101: +/- 10% 110: +/- 20% 111: +/- 50% Note that reference clock is sampled at 800MHz (for nominal oscillator frequencies),,, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on the input clock frequency: +/- 0.1% : can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz SCM indicator should not be used (should be masked) for reference frequencies above 400MHz.

Address: 0x0590 Name: ref_cfm Default: 0x05 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	limit	Sets the Coarse Frequency Monitor (CFM) limit selection. When the reference fails the specified criteria, the cfm bit in the associated ref_mon_status_n register will be high. Selection: 000: +/- 0.1% (input frequency units) 001: +/- 0.5% 010: +/- 1% 011: +/- 2% 100: +/- 5% 101: +/- 10% 110: +/- 20% 111: +/- 50%

Address:	0x0591	
Name:	ref_gst	
Default:	0x21	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5:4	disqualify	Sets the time to disqualify the reference after detecting either a CFM or SCM failure. If the Guard Soak Timer (GST) disqualify time expires and the source of the failure is still present, the gst bit in the associated ref_mon_status_n register will go high. Selection: 00: minimum delay possible 01: 10ms 10: 50ms (default) 11: 2.5s
3:2	reserved	
1:0	qualify	Sets the time to qualify the reference after both the CFM and SCM indicators are low. If the GST qualify timer expires without detecting a CFM or SCM failure, the gst bit in the associated ref_mon_status_n register will go low. Selection: 00: 2x configured GST disqualify time 01: 4x configured GST disqualify time (default) 10: 8x configured GST disqualify time 11: 16x configured GST disqualify time

Address:	0x0592	
Name:	ref_pfm_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	resolution	Sets the resolution and range of ref_pfm_disqualify (0x593-0x594) and ref_pfm_qualify (0x595-0x596). 0: Resolution is 0.01ppm, range is (+/-) 0.01ppm to 655.35ppm. 1: Resolution is 0.1ppm, range is (+/-) 0.1ppm to 6553.5ppm.

Address:	0x0593:0x0594	
Name:	ref_pfm_disqualify	
Default:	0x32B4	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the Precise Frequency Monitor (PFM) disqualify frequency offset. If a reference exceeds this offset, the pfm bit in the associated ref_mon_status_n register will go high. The default value is 130ppm.

Address:	0x0595:0x0596	
Name:	ref_pfm_qualify	
Default:	0x2724	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the PFM qualify frequency offset. If a reference is below this offset, the pfm bit in the associated ref_mon_status_n register will go low. The default value is 100ppm. Note that when the reference offset is between the qualify and disqualify limits (hysteresis), the state of the pfm bit in the ref_mon_status_n register will not be changed.

Address:	0x0597:0x0598	
Name:	ref_pfm_period	
Default:	0x0000	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Range 1 to 2048s with 1s resolution. Default value is 0. Setting value of 0 is recommended. Setting value of 0 disables this use register override, and uses the recommended defaults which are suitable for standard compliant behavior (e.g. 10 second observation interval).

Address:	0x0599	
Name:	ref_pfm_filter_limit	
Default:	0x28	
Type:	R/W	
Bit Field	Function Name	Description
7:0		The PFM filter limit represents a threshold. When the threshold is a non-zero value, and the difference between the PFM average filter output and 10 second PFM average is larger than this threshold, the PFM average filter will be replaced by 10 second PFM average output. The purpose of this is to speed up the filter reaction. The default value corresponds to a 4ppm filter limit. A value of 0 disables the filter limit check. Any other value is in units (or resolution) of 100ppb. Thus the allowed range is 100ppb to 25.5ppm. It is recommended to be used for PFM filter average time being larger than 10 sec. This threshold should be set to 0 (means disabled) when the average time is smaller than 10 sec.

Address: 0x059A Name: ref_phase_mem Default: 0x1B Type: R/W		
Bit Field	Function Name	Description
7:0		These bits specify reference phase memory limit using the following E32 series formula: Value = round(32 * log(phase_mem_limit / 10)), where phase_mem_limit is given in us. e.g., 10us (min) = 0x00, 1ms = 0x40, 1s (max) = 0xA0. This register should be programmed to have value that represents at least one reference period. Values 0xA1-0xFF will set the phase memory limit to 1s.

Address: 0x05FE Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x05FF Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.10 Register List (Page 12

Address:	0x0602:0x0603	
Name:	dpll_ctrl	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:7	reserved	
6:0	mask	For a write operation (see dpll_semaphore_wr bit), this field determines which DPLL's configuration is modified. Multiple bits can be set to affect multiple DPLLs in a single operation. For a read operation (see dpll_semaphore_rd bit), this field determines which DPLL configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 – DPLL0 Bit 1 – DPLL1 Bit 2 – DPLL2 Bit 3 – DPLL3 Bit 4 – unused Bit 5 – unused Bit 6 – unused

Address:	0x0604	
Name:	dpll_semaphore	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	rd	When this bit is written to a one by the host controller, the device will perform a read of the masked DPLL (see dpll_ctrl register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding DPLL configuration.
0	wr	When this bit is written to a one by the host controller (and the read bit is zero), the device will perform a write of the masked DPLL (see dpll_ctrl register). All of the configuration options on this page will be applied to each of the DPLLs indicated by the dpll_ctrl mask. The write is complete when this register reads back a zero.

Address: 0x0605 Name: dpll_bw_fixed Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	bw	Sets the DPLL loop filter corner frequency. 000: 14 Hz 001: 29 Hz 010: 61 Hz 011: 130 Hz 100: 380 Hz 101-110: reserved 111: variable value set from register 0x0606 To program 470 Hz bandwidth, set this bitfield to ‘111’ and set register at address 0x0606 value 0xC8

Address: 0x0606 Name: reserved Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		This register can be used to set up 470 Hz loop bandwidth as described in register dpll_bw_fixed

Address: 0x0608 Name: dpll_config Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:6	ref_edge	Sets the DPLL selected reference edge sensitivity. 00: positive (rising) edge 01: negative (falling) edge 10: low pulse 11: high pulse The low and high pulse options select the middle between edges.
5:1	reserved	
0	ext_fb_en	0: External feedback disabled 1: External feedback enabled

Address: 0x0609:0x060A Name: dpll_psl Default: 0x0000 Type: R/W		
Bit Field	Function Name	Description
15:0		Sets the phase slope limit, in units of ns/s. The range is 1ns/s to 65535ns/s. A value of 0 sets the PSL to "unlimited".

Address:	0x060B:0x060C	
Name:	dpll_psl_max_phase	
Default:	0x0064	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the maximum phase for which the phase slope will stay below specified PSL, in units of 100ns. Selection: 0: Maximum phase step while meeting the PSL will be 10us (default) 1-1000: Maximum phase step(us) = 0.1 * dpll_psl_max_phase >1000: Same as 1000 (100us) Note: For phase steps above the maximum phase, the DPLL will operate correctly but not guarantee that it will meet the given phase slope limit in mailbox registers 0x609-0x60A (dpll_psl).

Address:	0x060F:0x0610	
Name:	dpll_range	
Default:	0x0078	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the pull-in/hold-in range, in steps of 0.1ppm. (from 0.1ppm to 2100ppm, in 0.1ppm steps). Default value corresponds to 12ppm.

Address:	0x0611	
Name:	dpll_ref_sw_mask	
Default:	0x08	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	This bit acts as an enable mask for the PFM failure reference switch. When this bit is set, a PFM failure of the selected reference will cause the associated DPLL to perform a reference switch. When the bit is cleared, a PFM failure will be ignored by the reference switch algorithm (a switch to holdover may still be possible, see the dpll_ref_ho_mask::pfm bitfield for details). Note that the DPLL also will not switch to a reference which has a PFM failure while either the PFM reference switch or holdover mask bits are set.
3	gst	This bit acts as an enable mask for the GST failure reference switch. See pfm bit description.
2	cfm	This bit acts as an enable mask for the CFM failure reference switch. See pfm bit description.
1	scm	This bit acts as an enable mask for the SCM failure reference switch. See pfm bit description.
0	los	This bit acts as an enable mask for the LOS failure reference switch. See pfm bit description.

Address: 0x0612 Name: dpll_ref_ho_mask Default: 0x17 Type: R/W		
Bit Field	Function Name	Description
7:5	reserved	
4	pfm	When set to high, this bit will allow selected reference PFM failure to cause associated DPLL to go to holdover. When low, selected reference PFM failure will be masked and the associated DPLL will not go to holdover due to the PFM failure. A switch to holdover will only be attempted after all reference switching options have been exhausted, regardless of the state of the dpll_ref_ho_mask bits.
3	gst	This bit acts as an enable mask for the GST holdover switch. See pfm bit description.
2	cfm	This bit acts as an enable mask for the CFM holdover switch. See pfm bit description.
1	scm	This bit acts as an enable mask for the SCM holdover switch. See pfm bit description.
0	los	This bit acts as an enable mask for the LOS holdover switch. See pfm bit description.

Address: 0x0613 Name: dpll_ho_filter Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:4	reserved	
3:0	bw	This register specifies the holdover filter bandwidth. The default value of 0x00 means that the filter is bypassed. These are the possible settings: BW = 343/(2^n*2*pi) Hz Selection: 0x0: Bypass 0x1: 27.3 Hz 0x2: 13.6 Hz 0x3: 6.8 Hz 0x4: 3.4 Hz 0x5: 1.7 Hz 0x6: 883 mHz 0x7: 426 mHz 0x8: 213 mHz 0x9: 107 mHz 0xA: 53.3 mHz 0xB: 26.6 mHz 0xC: 13.3 mHz 0xD: 6.7 mHz 0xE: 3.3 mHz 0xF: 1.7 mHz

Address: 0x0614 Name: dpll_ho_delay Default: 0x4C Type: R/W		
Bit Field	Function Name	Description
		This register specifies the DPLL holdover storage delay using the following E32 series formula: Value = round(32 * log(delay)), where delay is in ms Example, if desired delay is 1ms, value to be written to this register is 0x00, for 1 second the value is 0x60, and for 2 hours the value is 0xDC. The default value of 0x4C corresponds to 237ms.

Address: 0x0615 Name: dpll_priority_1_0 Default: 0x10 Type: R/W		
Bit Field	Function Name	Description
7:4	ref_1	Priority of ref1 When the DPLL is in automatic mode of operation (see dpll_mode_refsel_x::mode bitfield), these bits set the priority of each reference for the DPLL. 0000 is highest priority and 1110 is lowest priority. Setting these bits to 1111 will disable the reference (the DPLL will never lock to it). When two references are programmed to have different priority numbers, the DPLL will perform revertive switching between them: the DPLL will always switch to the highest priority reference (lowest priority number) whenever that reference is qualified. When two references are programmed to have the same priority number, the DPLL will perform non-revertive switching between them: the DPLL will not switch to the reference with the same priority when that reference qualifies. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority. Example: if ref0 has priority 0 (highest), ref1, ref2 and ref3 have priority 1. Whenever ref0 is qualified, the DPLL will switch to it. If ref0 is not qualified, the DPLL will not change the currently selected reference (e.g., ref3) even if ref2 or ref2 become available.
3:0	ref_0	Priority of ref0

Address: 0x0616 Name: dpll_priority_3_2 Default: 0x32 Type: R/W		
Bit Field	Function Name	Description
7:4	ref_3	Priority of ref3
3:0	ref_2	Priority of ref2

Address:	0x0617	
Name:	dpll_priority_5_4	
Default:	0x54	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_5	Priority of ref5
3:0	ref_4	Priority of ref4

Address:	0x0618	
Name:	dpll_priority_7_6	
Default:	0x76	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_7	Priority of ref7
3:0	ref_6	Priority of ref6

Address:	0x0619	
Name:	dpll_priority_9_8	
Default:	0x98	
Type:	R/W	
Bit Field	Function Name	Description
7:4	ref_9	Priority of ref9
3:0	ref_8	Priority of ref8

Address:	0x061D	
Name:	dpll_lock_phase	
Default:	0x92	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Sets the phase for lock declaration using the following E32 series formula: dpll_lock_phase = round(32 * log(phase)), where phase is in ns. The minimum is 0x00 = 1ns. The maximum is 0xA0 = 100us. The default is 36.5us.

Address:	0x061E	
Name:	dpll_lock_period	
Default:	0x80	
Type:	R/W	
Bit Field	Function Name	Description
7:0		Sets the period for lock declaration using the following E32 series formula: dpll_lock_period = round(32 * log(period)), where period is in ms. The minimum is 0x56 = 487ms. The maximum is 0xC0 = 1000s. The default is 10s.

Address:	0x061F	
Name:	dpll_fast_lock_ctrl	
Default:	0x01	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2	nco_en	Controls whether fast-lock is forcibly disabled during transitions out of NCO mode. 0: Fast-lock is disabled during transitions out of NCO mode 1: Fast-lock is allowed during transitions out of NCO mode
1	force_en	This is the control to force-enable the fast-lock feature. Note that the the master-control (bit 0 of this register) still has to be enabled for this control to work. This control, when enabled, will ignore the outputs of the frequency and phase error monitors.
0	master_en	This is the master-enable control for the fast-lock feature.

Address:	0x0620	
Name:	dpll_fast_lock_phase_err	
Default:	0xFF	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This is the phase error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 250ns, with a value of zero being reserved for disabling the phase error threshold check.

Address:	0x0621	
Name:	dpll_fast_lock_freq_err	
Default:	0x04	
Type:	R/W	
Bit Field	Function Name	Description
7:0		This is the frequency error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 1ppm, programmable from 1 to 255ppm. If the threshold is programmed to zero, the fast-lock frequency error check is disabled.

Address:	0x0622	
Name:	dpll_damping	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:5	reserved	
4:0	factor	Sets the DPLL damping factor. 0: 5 1: 1 2: 2 3: 2.998801 4: 4.003204 5: 5 (default, peaking <0.1dB) 6: 6.019293 7: 7.0014 8: 8.006408 9: 8.980265 10: 10 11: 10.91089 12: 12.12678 13: 12.90994 14: 13.8675 15: 15.07557 16: 15.81139 17: 16.66667 18: 17.67767 19: 18.89822 20: 20.41241 21: 22.36068 22: 25 23: 28.86751 24: 35.35534 25-31: 50

Address:	0x0623	
Name:	split_xo_config	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	en	0: Split-XO mode disabled for DPLL (DPLL's will use master oscillator fed to OSCI) 1: Split-XO mode enabled for DPLL (DPLL will use TCXO/OCXO for stability and master oscillator (XO) for jitter)

Address:	0x0624	
Name:	dpll_tie	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	switch_clear_en	This bit enables the TIE-write clear on reference switch mode of operation. The DPLL's tie_clear bit (e.g., register 0x21F bit 1 for DPLL0) must also be set to 1 for this feature to be enabled. When this bit is set, the corresponding DPLL will clear the accumlated TIE from all

		previous TIE-write operations whenever the DPLL performs a reference switch, or whenever the DPLL mode is changed from NCO to either Automatic or Forced Reference.

Address: 0x0625 Name: dpll_tie_wr_thresh Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		This register specifies the threshold for declaring that the TIE Write operation has completed. When the output has moved within the threshold of the expected alignment position, then the dpll_tie_wr_status register will indicate that the TIE Write operation has completed. When this register is programmed to the default of 0x00, the sticky bits in dpll_tie_wr_status will never be set. Otherwise, a non-zero value specifies the threshold in 10 ns steps (10ns to 2.55us range).

Address: 0x0638 Name: dpll_lock_delay Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Sets the lock declaration delay time. The actual delay time will be the square of the value written to this register, giving a range of 0 to 255^2, in seconds. A value of 0 disables the lock delay timer.

Address: 0x067E Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x067F Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

13.4.11 Register List (Page 13)

Address: 0x0682:0x0683 Name: synth_ctrl Default: 0x0001 Type: R/W		
Bit Field	Function Name	Description
15:10	reserved	
9:0	mask	For a write operation (see synth_semaphore_wr bit), this field determines which synthesizer's configuration is modified. Multiple bits can be set to affect multiple synthesizers in a single operation. For a read operation (see synth_semaphore_rd bit), this field determines which synthesizer configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 – Synth0 (GP-Synth) Bit 1 – Synth1 Bit 2 – Synth2 Bit 3 – Synth3 Bit 4 – unused Bit 5 – unused Bit 6 – unused Bit 7 – unused Bit 8 – unused Bit 9 – unused

Address:	0x0684	
Name:	synth_semaphore	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:2	reserved	
1	rd	When this bit is written to a one by the host controller, the device will perform a read of the masked synthesizer (see synth_ctrl register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding Synthesizer configuration.
0	wr	When this bit is written to a one by the host controller (and the read bit is zero), the device will perform a write of the masked Synthesizer (see synth_ctrl register). All of the configuration options on this page will be applied to each of the Synthesizer indicated by the synth_ctrl mask. The write is complete when this register reads back a zero.

Address:	0x0685:0x0686	
Name:	synth_vco_freq_base	
Default:	0x1F40	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the synthesizer VCO base frequency (Bs), in Hz. The final VCO frequency is given by: fvco = Bs x Ks x Ms / Ns Some example frequency configurations are show below: VCO Frequency — synth_vco_freq_base (Bs) — synth_vco_freq_mult (Ks) 2.50000 GHz — 25kHz (0x61A8) — 100,000 (0x0186A0) 4.35456 GHz — 8kHz (0x1F40) — 544,320 (0x084E40)

Address:	0x0687:0x0689	
Name:	synth_vco_freq_mult	
Default:	0x017BB0	
Type:	R/W	
Bit Field	Function Name	Description
23:0		Sets the synthesizer frequency multiplier (Ks). See synth_vco_freq_base description for more information.

Address:	0x068A:0x068B	
Name:	synth_vco_freq_m	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the Ms component of the VCO frequency. See synth_vco_freq_base description for more information.

Address:	0x068C:0x068D	
Name:	synth_vco_freq_n	
Default:	0x0001	
Type:	R/W	
Bit Field	Function Name	Description
15:0		Sets the Ns component of the VCO frequency. See synth_vco_freq_base description for more information.

Address:	0x0693	
Name:	synth_config	
Default:	0x01	
Type:	R/W	
Bit Field	Function Name	Description
7	reserved	
6:4	dpll_sel	Selects the DPLL that drives the associated synthesizer. An invalid DPLL number will select DPLL0. To change this bitfield for an enabled synth, this sequence must be followed: 1) Set bit 0 to 0 (disable synthesizer) 2) Request mailbox write 3) Modify this bitfield and set bit 0 to 1 (re-enable synthesizer) 4) Request mailbox write
3:1	reserved	
0	en	0: Disable synthesizer 1: Enable synthesizer

Address:	0x0694	
Name:	synth_config2	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:1	reserved	
0	remap	For synth2: 0: synth2 dividers C and D are not exposed on any outputs. synth3 dividers A and B are exposed on hpoutclk8 to 11. 1: synth2 dividers C and D are exposed on outputs hpoutclk8 to 11. synth3 dividers A and B are not exposed on any outputs. See registers 0x254 (hp_out_ctrl_3) and 0x255 (hp_out_routing_3) for complete details. For synth2 in system PLL bypass FALSE (see Figure 20) the bit must be 1. For synth2 in system PLL bypass TRUE (see Figure 21) the bit must be 0. This bit is reserved for all other synths.

Address:	0x0699:0x069D	
Name:	synth_out_a_div	
Default:	0x0000000005	
Type:	R/W	
Bit Field	Function Name	Description
39:34	reserved	
33:0	div	Sets the associated synthesizer's A divider value, in units of VCO cycles.

Address: 0x069E Name: synth_out_a_driver Default: 0x03 Type: R/W		
Bit Field	Function Name	Description
7:3	reserved	
2:0	strength	For synth0, sets the drive strength for gpoutclk0: x00: 1x x01: 2x x10: 3x x11: 4x (default) For all other synths, the drive strength only applies to differential outputs. For synth1, sets the drive strength for hpoutclk0 and 1. For synth2, sets the drive strength for hpoutclk4 and 5, etc. 000: 8mA (0.4V @ 50ohm) 001: 12mA (0.6V @ 50ohm) 010: 14mA (0.7V @ 50ohm) 011: 16mA (0.4V @ 25ohm) 100: 24mA (0.6V @ 25ohm) 101: 28mA (0.7V @ 25ohm) 110-111: Invalid (8mA)

Address: 0x069F Name: synth_out_a_ctrl Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:6	reserved	
5	width_en	0: Output clock is 50% duty cycle 1: Output clock high pulse is programmed by synth_out_a_width register
4	polarity	0: Regular (non-inverse) polarity 1: Inverse polarity
3	reserved	
2:0	mode	This field selects the output clock mode: 000: Regular clock 001: Clock + PWM PPS 25/75 010: Clock + PWM PPS 75/25 011: Clock + PWM PP2S 25/75 100: Clock + PWM PP2S 75/25 101-111: Invalid (regular clock)

Address: 0x06A1:0x06A4 Name: synth_out_a_width Default: 0x00000000 Type: R/W		
Bit Field	Function Name	Description
31:0		Sets the width of the synthesizer's divider A high pulse, in units of VCO cycles. A value of 0 is invalid, and will default to 50% duty cycle. This register only takes effect when synth_out_a_ctrl::width_en is set to 1.

Address:	0x06A5:0x06A9	
Name:	synth_out_a_shift	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:34	reserved	
33:0	reserved	

Address:	0x06AD:0x06B1	
Name:	synth_out_b_div	
Default:	0x0000000028	
Type:	R/W	
Bit Field	Function Name	Description
39:34	reserved	
33:0	div	Sets the associated synthesizer's B divider value, in units of VCO cycles.

Address:	0x06B2	
Name:	synth_out_b_driver	
Default:	0x03	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	strength	For synth0, sets the drive strength for gpoutclk1: x00: 1x x01: 2x x10: 3x x11: 4x (default) For synth2 and 3, the drive strength only applies to differential outputs. For synth2, sets the drive strength for hpoutclk6 and 7. For synth3, sets the drive strength for hpoutclk10 and 11, etc. 000: 8mA (0.4V @ 50ohm) 001: 12mA (0.6V @ 50ohm) 010: 14mA (0.7V @ 50ohm) 011: 16mA (0.4V @ 25ohm) 100: 24mA (0.6V @ 25ohm) 101: 28mA (0.7V @ 25ohm) 110-111: Invalid (8mA) For all other synths, this register is reserved.

Address:	0x06B3	
Name:	synth_out_b_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	width_en	See description for register at address 0x69F bit 5 (synth_out_a_ctrl::width_en).
4	polarity	See description for register at address 0x69F bit 4 (synth_out_a_ctrl::polarity).
3	reserved	
2:0	mode	See description for register at address 0x69F bits 2:0 (synth_out_a_ctrl::mode).

Address:	0x06B5:0x06B8	
Name:	synth_out_b_width	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at address 0x6A1-0x6A4 (synth_out_a_width).

Address:	0x06B9:0x06BD	
Name:	synth_out_b_shift	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:34	reserved	
33:0	reserved	

Address:	0x06C1:0x06C5	
Name:	synth_out_c_div	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:34	reserved	
33:0	div	Sets the associated synthesizer's C divider value, in units of VCO cycles.

Address:	0x06C6	
Name:	synth_out_c_driver	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	strength	For synth1, the drive strength only applies to differential outputs. For synth1, sets the drive strength for hpoutclk2 and 3. 000: 8mA (0.4V @ 50ohm) 001: 12mA (0.6V @ 50ohm) 010: 14mA (0.7V @ 50ohm) 011: 16mA (0.4V @ 25ohm) 100: 24mA (0.6V @ 25ohm) 101: 28mA (0.7V @ 25ohm) 110-111: Invalid (8mA) For all other synths, this register is reserved.

Address: 0x06C7 Name: synth_out_c_ctrl Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:6	reserved	
5	width_en	See description for register at address 0x69F bit 5 (synth_out_a_ctrl::width_en).
4	polarity	See description for register at address 0x69F bit 4 (synth_out_a_ctrl::polarity).
3	reserved	
2:0	mode	See description for register at address 0x69F bits 2:0 (synth_out_a_ctrl::mode).

Address: 0x06C9:0x06CC Name: synth_out_c_width Default: 0x00000000 Type: R/W		
Bit Field	Function Name	Description
31:0		See description for register at address 0x6A1-0x6A4 (synth_out_a_width).

Address: 0x06CD:0x06D1 Name: synth_out_c_shift Default: 0x0000000000 Type: R/W		
Bit Field	Function Name	Description
39:34	reserved	
33:0	reserved	

Address: 0x06D5:0x06D9 Name: synth_out_d_div Default: 0x0000000000 Type: R/W		
Bit Field	Function Name	Description
39:34	reserved	
33:0	div	Sets the associated synthesizer's D divider value, in units of VCO cycles.

Address:	0x06DA	
Name:	synth_out_d_driver	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:3	reserved	
2:0	strength	For synth2 the drive strength only applies to differential outputs. For synth2, sets the drive strength for hpoutclk10 and 11. 000: 8mA (0.4V @ 50ohm) 001: 12mA (0.6V @ 50ohm) 010: 14mA (0.7V @ 50ohm) 011: 16mA (0.4V @ 25ohm) 100: 24mA (0.6V @ 25ohm) 101: 28mA (0.7V @ 25ohm) 110-111: Invalid (8mA) For all other synths, this register is reserved.

Address:	0x06DB	
Name:	synth_out_d_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	Function Name	Description
7:6	reserved	
5	width_en	See description for register at address 0x69F bit 5 (synth_out_a_ctrl::width_en).
4	polarity	See description for register at address 0x69F bit 4 (synth_out_a_ctrl::polarity).
3	reserved	
2:0	mode	See description for register at address 0x69F bits 2:0 (synth_out_a_ctrl::mode).

Address:	0x06DD:0x06E0	
Name:	synth_out_d_width	
Default:	0x00000000	
Type:	R/W	
Bit Field	Function Name	Description
31:0		See description for register at address 0x6A1-0x6A4 (synth_out_a_width).

Address:	0x06E1:0x06E5	
Name:	synth_out_d_shift	
Default:	0x0000000000	
Type:	R/W	
Bit Field	Function Name	Description
39:34	reserved	
33:0	reserved	

Address: 0x06FE Name: uport Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7.0	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	
0	status	This field indicates if microport attempted access had not been successful. The register content will be 0x00 if the access had been successful.

Address: 0x06FF Name: page_sel Default: 0x00 Type: R/W		
Bit Field	Function Name	Description
7:0		Unsigned binary value of these bits represents selected page for SPI access: 0x00: page 0 (first 128 bytes) 0x01: page 1 (second 128 bytes) 0x02: page 2 (third 128 bytes) 0x03: page 3 (fourth 128 bytes) 0x04: page 4 (fifth 128 bytes) 0x05: page 5 (sixth 128 bytes) 0x06: page 6 (seventh 128 bytes) 0x07: reserved 0x08: page 8 (ninth 128 bytes) 0x09: reserved 0x0A: page 10 (eleventh 128 bytes) 0x0B: page 11 (twelfth 128 bytes) 0x0C: page 12 (thirteenth 128 bytes) 0x0D: page 13 (fourteenth 128 bytes) 0x0E-0xFF: reserved

14 AC and DC Electrical Characteristics

14.1 Absolute Maximum Ratings

Table 16 · Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD_R}	-0.5		4.0	V	
2	Supply voltage 2.5V	V_{DD_R}	-0.5		4.0	V	
3	Supply voltage 1.8V	V_{DD18_R}	-0.5		2.5	V	
4	Output supply voltage	V_{DDO_R}	-0.5		4.0	V	
5	CML pull-up voltage	V_{DDPU_R}	-0.5		4.0	V	
6	Voltage on any digital pin	V_{PIN}	-0.5		4.0	V	
7	Voltage on any osci or osco pin	V_{OSC}	-0.3		V_{DD} + 0.3	V	
8	Storage temperature	T_{ST}	-55		125	°C	

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated
* The device supports two power supply modes (3.3V & 1.8V and 2.5V & 1.8V)

14.2 Recommended Operating Conditions

Table 17 · Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD}	2.375	2.50	2.625	V	
3	Supply voltage 1.8V	V_{DD18}	1.71	1.80	1.89	V	
4	Output supply voltage	V_{DDO}	1.71 2.375 3.135	1.8 2.5 3.3	1.89 2.625 3.465	V	
5	CML pull-up voltage (V_{DDPU} must equal V_{DDO})	V_{DDPU}	1.71 2.375 3.135	1.8 2.5 3.3	1.89 2.625 3.465	V	
6	Operating temperature	T_A	-40	25	85	°C	
7	Input voltage	V_{DD-IN}	V_{DD} - 0.3		V_{DD} + 0.3	V	

* Voltages are with respect to ground (GND) unless otherwise stated
* The device supports two power supply modes (3.3V & 1.8V, 2.5V & 1.8V)

14.3 DC Electrical Characteristics

Table 18 · DC Electrical Characteristics* - Current – Core

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core	I_{CORE} (V_{DD} 3.3V)		150	160	mA	3.3V/1.8V sysApll
2				90	100	mA	3.3V/1.8V bypApll
3		I_{CORE} (V_{DD18} 1.8V)		280	300	mA	3.3V/1.8V sysApll
4				190	210	mA	3.3V/1.8V bypApll
5		I_{CORE} (V_{DD} 2.5V)		130	150	mA	2.5V/1.8V sysApll
6				70	80	mA	2.5V/1.8V bypApll
7		I_{CORE} (V_{DD18} 1.8V)		280	300	mA	2.5V/1.8V sysApll
8				200	210	mA	2.5V/1.8V bypApll

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* Current is measured with synthesizers, dividers and outputs disabled

Table 19 · DC Electrical Characteristics* - Current – Core + Synthesizers 3:1

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn1	I_{C_SYN1} (V_{DD} 3.3V)		310	340	mA	3.3V/1.8V sysApll
2				250	270	mA	3.3V/1.8V bypApll
3		I_{C_SYN1} (V_{DD18} 1.8V)		350	370	mA	3.3V/1.8V sysApll
4				260	280	mA	3.3V/1.8V bypApll
5		I_{C_SYN1} (V_{DD} 2.5V)		280	310	mA	2.5V/1.8V sysApll
6				220	250	mA	2.5V/1.8V bypApll
7		I_{C_SYN1} (V_{DD18} 1.8V)		350	370	mA	2.5V/1.8V sysApll
8				260	280	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn2	I_{C_SYN2} (V_{DD} 3.3V)		240	270	mA	3.3V/1.8V sysApll
10				180	200	mA	3.3V/1.8V bypApll
11		I_{C_SYN2} (V_{DD18} 1.8V)		400	430	mA	3.3V/1.8V sysApll
12				320	340	mA	3.3V/1.8V bypApll
13		I_{C_SYN2} (V_{DD} 2.5V)		210	240	mA	2.5V/1.8V sysApll
14				150	180	mA	2.5V/1.8V bypApll
15		I_{C_SYN2} (V_{DD18} 1.8V)		400	430	mA	2.5V/1.8V sysApll
16				320	340	mA	2.5V/1.8V bypApll
17	Current for Core plus: Syn3	I_{C_SYN3} (V_{DD} 3.3V)		160	180	mA	3.3V/1.8V bypApll
18		I_{C_SYN3} (V_{DD18} 1.8V)		300	320	mA	
19		I_{C_SYN3} (V_{DD} 2.5V)		140	160	mA	2.5V/1.8V bypApll
20		I_{C_SYN3} (V_{DD18} 1.8V)		300	320	mA	
21	Current for Core plus: Syn1 + Syn2	I_{C_SYN12} (V_{DD} 3.3V)		400	450	mA	3.3V/1.8V sysApll
22				340	380	mA	3.3V/1.8V bypApll
23		I_{C_SYN12} (V_{DD18} 1.8V)		480	510	mA	3.3V/1.8V sysApll
24				390	410	mA	3.3V/1.8V bypApll
25		I_{C_SYN12} (V_{DD} 2.5V)		360	410	mA	2.5V/1.8V sysApll
26				300	340	mA	2.5V/1.8V bypApll
27		I_{C_SYN12} (V_{DD18} 1.8V)		480	510	mA	2.5V/1.8V sysApll
28				390	410	mA	2.5V/1.8V bypApll
29	Current for Core plus: Syn1 + Syn2 + Syn3	I_{C_SYN3} (V_{DD} 3.3V)		420	460	mA	3.3V/1.8V bypApll
30		I_{C_SYN3} (V_{DD18} 1.8V)		490	530	mA	
31		I_{C_SYN3} (V_{DD} 2.5V)		380	420	mA	2.5V/1.8V bypApll
32		I_{C_SYN3} (V_{DD18} 1.8V)		490	530	mA	

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO's are programmed to their highest rate; dividers and outputs are disabled
* Current is measured with synthesizer individually enabled/disabled and includes core current

Table 20 · DC Electrical Characteristics* - Current - Core + Synthesizer 1 + HPOUT_DIFF[1:0] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn1DivA + HPOUT_DIFF[0]	I_{CS1_HPD} (V_{DD} 3.3V)		330	370	mA	3.3V/1.8V sysApll
2				270	300	mA	3.3V/1.8V bypApll
3		I_{CS1_HPD} (V_{DD18} 1.8V)		350	370	mA	3.3V/1.8V sysApll
4				260	280	mA	3.3V/1.8V bypApll
5		I_{CS1_HPD} (V_{DD} 2.5V)		300	340	mA	2.5V/1.8V sysApll
6				240	270	mA	2.5V/1.8V bypApll
7		I_{CS1_HPD} (V_{DD18} 1.8V)		350	370	mA	2.5V/1.8V sysApll
8				260	280	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn1DivA + HPOUT_DIFF[0:1]	I_{CS1_HPD} (V_{DD} 3.3V)		380	420	mA	3.3V/1.8V sysApll
10				320	350	mA	3.3V/1.8V bypApll
11		I_{CS1_HPD} (V_{DD18} 1.8V)		350	370	mA	3.3V/1.8V sysApll
12				260	280	mA	3.3V/1.8V bypApll
13		I_{CS1_HPD} (V_{DD} 2.5V)		350	390	mA	2.5V/1.8V sysApll
14				290	320	mA	2.5V/1.8V bypApll
15		I_{CS1_HPD} (V_{DD18} 1.8V)		350	370	mA	2.5V/1.8V sysApll
16				270	290	mA	2.5V/1.8V bypApll
17	Current for Core plus: Syn1DivAC + HPOUT_DIFF[0:1]	I_{CS1_HPD} (V_{DD} 3.3V)		380	420	mA	3.3V/1.8V sysApll
18				320	350	mA	3.3V/1.8V bypApll
19		I_{CS1_HPD} (V_{DD18} 1.8V)		350	370	mA	3.3V/1.8V sysApll
20				260	280	mA	3.3V/1.8V bypApll
21		I_{CS1_HPD} (V_{DD} 2.5V)		350	390	mA	2.5V/1.8V sysApll
22				290	320	mA	2.5V/1.8V bypApll
23		I_{CS1_HPD} (V_{DD18} 1.8V)		350	370	mA	2.5V/1.8V sysApll
24				270	280	mA	2.5V/1.8V bypApll

* Values are over Recommended Operating Conditions
* V_{DDO} and V_{DDPU} are connected to V_{DD} and are included in the V_{DD} measured current value; see Figure 36
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO's are programmed to their highest rate; outputs are at 622.08MHz
* Output drive impedance is set to 25 ohms; output drivel level is set to 0.4V
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current

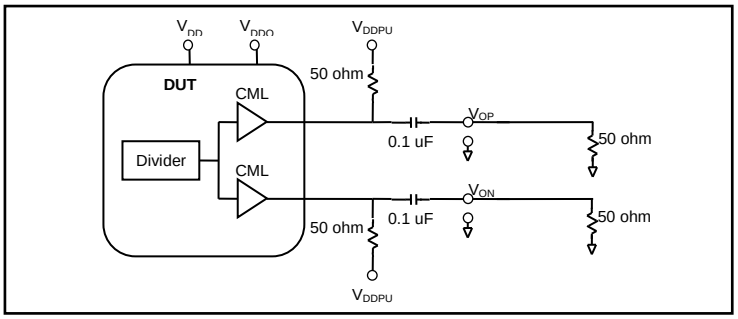


Figure 36. HPOUT_DIFF (CML) Output

Table 21 · DC Electrical Characteristics* - Current - Core + Synthesizer 2 + HPOUT_DIFF[5:2] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn2DivA + HPOUT_DIFF[2]	I_{CS2_HPD} (V_{DD} 3.3V)		270	300	mA	3.3V/1.8V sysApll
2				210	230	mA	3.3V/1.8V bypApll
3		I_{CS2_HPD} (V_{DD18} 1.8V)		400	430	mA	3.3V/1.8V sysApll
4				320	340	mA	3.3V/1.8V bypApll
5		I_{CS2_HPD} (V_{DD} 2.5V)		240	270	mA	2.5V/1.8V sysApll
6				180	200	mA	2.5V/1.8V bypApll
7		I_{CS2_HPD} (V_{DD18} 1.8V)		400	430	mA	2.5V/1.8V sysApll
8				320	340	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn2DivA + HPOUT_DIFF[2:3]	I_{CS2_HPD} (V_{DD} 3.3V)		290	330	mA	3.3V/1.8V sysApll
10				230	260	mA	3.3V/1.8V bypApll
11		I_{CS2_HPD} (V_{DD18} 1.8V)		410	440	mA	3.3V/1.8V sysApll
12				320	350	mA	3.3V/1.8V bypApll
13		I_{CS2_HPD} (V_{DD} 2.5V)		260	300	mA	2.5V/1.8V sysApll
14				200	230	mA	2.5V/1.8V bypApll
15		I_{CS2_HPD} (V_{DD18} 1.8V)		410	440	mA	2.5V/1.8V sysApll
16				320	350	mA	2.5V/1.8V bypApll
17	Current for Core plus: Syn2DivAB + HPOUT_DIFF[2:3]	I_{CS2_HPD} (V_{DD} 3.3V)		290	330	mA	3.3V/1.8V sysApll
18				230	260	mA	3.3V/1.8V bypApll
19		I_{CS2_HPD} (V_{DD18} 1.8V)		420	450	mA	3.3V/1.8V sysApll
20				330	360	mA	3.3V/1.8V bypApll
21		I_{CS2_HPD} (V_{DD} 2.5V)		260	300	mA	2.5V/1.8V sysApll
22				200	230	mA	2.5V/1.8V bypApll
23		I_{CS2_HPD} (V_{DD18} 1.8V)		420	450	mA	2.5V/1.8V sysApll
24				330	360	mA	2.5V/1.8V bypApll
25	Current for Core plus: Syn2DivABCD + HPOUT_DIFF[2:5]	I_{CS2_HPD} (V_{DD} 3.3V)		330	370	mA	3.3V/1.8V sysApll
26		I_{CS2_HPD} (V_{DD18} 1.8V)		480	520	mA	
27		I_{CS2_HPD} (V_{DD} 2.5V)		300	340	mA	2.5V/1.8V sysApll
28		I_{CS2_HPD} (V_{DD18} 1.8V)		480	520	mA	

* Values are over Recommended Operating Conditions
* V_{DDO} and V_{DDPU} are connected to V_{DD} and are included in the V_{DD} measured current value; see Figure 36.
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* Note that Syn2DivCD + HPOUT_DIFF[4:5] should not be used in bypass mode as jitter is significantly higher
* VCO's are programmed to their highest rate; outputs are at 622.08MHz
* Output drive impedance is set to 25 ohms; output drivel level is set to 0.4V
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current

Table 22 · DC Electrical Characteristics* - Current - Core + Synthesizer 3 + HPOUT_DIFF[5:4] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn3DivA + HPOUT_DIFF[4]	I_{CS3_HPD} (V_{DD} 3.3V)		180	210	mA	3.3V/1.8V bypApll
2		I_{CS3_HPD} (V_{DD18} 1.8V)		300	320	mA	
3		I_{CS3_HPD} (V_{DD} 2.5V)		160	190	mA	2.5V/1.8V bypApll
4		I_{CS3_HPD} (V_{DD18} 1.8V)		300	320	mA	
5	Current for Core plus: Syn3DivA + HPOUT_DIFF[4:5]	I_{CS3_HPD} (V_{DD} 3.3V)		200	230	mA	3.3V/1.8V bypApll
6		I_{CS3_HPD} (V_{DD18} 1.8V)		300	330	mA	
7		I_{CS3_HPD} (V_{DD} 2.5V)		180	210	mA	2.5V/1.8V bypApll
8		I_{CS3_HPD} (V_{DD18} 1.8V)		300	330	mA	
9	Current for Core plus: Syn3DivAB + HPOUT_DIFF[4:5]	I_{CS3_HPD} (V_{DD} 3.3V)		200	230	mA	3.3V/1.8V bypApll
10		I_{CS3_HPD} (V_{DD18} 1.8V)		310	340	mA	
11		I_{CS3_HPD} (V_{DD} 2.5V)		180	210	mA	2.5V/1.8V bypApll
12		I_{CS3_HPD} (V_{DD18} 1.8V)		310	340	mA	

* Values are over Recommended Operating Conditions
* V_{DDO} and V_{DDPU} are connected to V_{DD} and are included in the V_{DD} measured current value; see Figure 36**.**
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO's are programmed to their highest rate; outputs are at 622.08MHz
* Output drive impedance is set to 25 ohms; output drivel level is set to 0.4V
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current

Table 23 · DC Electrical Characteristics* - Current - Core + Synthesizer 3:1 + HPOUT_DIFF[5:0] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn1DivA + Syn2DivA + HPOUT_DIFF[0,2]	I_{CS2_HPD} (V_{DD} 3.3V)		450	500	mA	3.3V/1.8V sysApll
2				390	430	mA	3.3V/1.8V bypApll
3		I_{CS2_HPD} (V_{DD18} 1.8V)		480	510	mA	3.3V/1.8V sysApll
4				390	410	mA	3.3V/1.8V bypApll
5		I_{CS2_HPD} (V_{DD} 2.5V)		410	460	mA	2.5V/1.8V sysApll
6				350	400	mA	2.5V/1.8V bypApll
7		I_{CS2_HPD} (V_{DD18} 1.8V)		480	510	mA	2.5V/1.8V sysApll
8				390	420	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn1DivAC + Syn2DivAB + HPOUT_DIFF[0:3]	I_{CS2_HPD} (V_{DD} 3.3V)		520	580	mA	3.3V/1.8V sysApll
10				460	510	mA	3.3V/1.8V bypApll
11		I_{CS2_HPD} (V_{DD18} 1.8V)		490	520	mA	3.3V/1.8V sysApll
12				400	430	mA	3.3V/1.8V bypApll
13		I_{CS2_HPD} (V_{DD} 2.5V)		480	540	mA	2.5V/1.8V sysApll
14				420	470	mA	2.5V/1.8V bypApll
15		I_{CS2_HPD} (V_{DD18} 1.8V)		490	520	mA	2.5V/1.8V sysApll
16				400	430	mA	2.5V/1.8V bypApll
17	Current for Core plus: Syn1DivA + Syn2DivA + Syn3DivA + HPOUT_DIFF[0,2,4]	I_{CS2_HPD} (V_{DD} 3.3V)		490	540	mA	3.3V/1.8V bypApll
18		I_{CS2_HPD} (V_{DD18} 1.8V)		490	530	mA	
19		I_{CS2_HPD} (V_{DD} 2.5V)		440	500	mA	2.5V/1.8V bypApll
20		I_{CS2_HPD} (V_{DD18} 1.8V)		490	530	mA	
21	Current for Core plus: Syn1DivA + Syn2DivA + Syn3DivA + HPOUT_DIFF[0:5]	I_{CS2_HPD} (V_{DD} 3.3V)		580	640	mA	3.3V/1.8V bypApll
22		I_{CS2_HPD} (V_{DD18} 1.8V)		520	560	mA	
23		I_{CS2_HPD} (V_{DD} 2.5V)		530	600	mA	2.5V/1.8V bypApll
24		I_{CS2_HPD} (V_{DD18} 1.8V)		520	560	mA	
25	Current for Core plus: Syn1DivAC + Syn2DivAB + Syn3DivAB + HPOUT_DIFF[0:5]	I_{CS2_HPD} (V_{DD} 3.3V)		580	640	mA	3.3V/1.8V bypApll
26		I_{CS2_HPD} (V_{DD18} 1.8V)		520	560	mA	
27		I_{CS2_HPD} (V_{DD} 2.5V)		530	600	mA	2.5V/1.8V bypApll
28		I_{CS2_HPD} (V_{DD18} 1.8V)		520	560	mA	
29	Current for Core plus: Syn1DivAC + Syn2DivAB + Syn3DivAB + HPOUT_DIFF[0:5] Drive Level = 0.7V	I_{CS2_HPD} (V_{DD} 3.3V)		630	710	mA	3.3V/1.8V bypApll
30		I_{CS2_HPD} (V_{DD18} 1.8V)		520	560	mA	
31		I_{CS2_HPD} (V_{DD} 2.5V)		590	660	mA	2.5V/1.8V bypApll
32		I_{CS2_HPD} (V_{DD18} 1.8V)		520	560	mA	

* Values are over Recommended Operating Conditions
* V_{DDO} and V_{DDPU} are connected to V_{DD} and are included in the V_{DD} measured current value; see Figure 36.
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO's are programmed to their highest rate; outputs are at 622.08MHz
* Output drive impedance is set to 25 ohms; output drivel level is set to 0.4V unless otherwise indicated
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current

Table 24 · DC Electrical Characteristics* - Current - Core + Synthesizer 1 + HPOUT[3:0] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn1DivA + HPOUT[0]	I_{CS1_HPO} (V_{DD} 3.3V)		350	390	mA	3.3V/1.8V sysApll
2				290	330	mA	3.3V/1.8V bypApll
3		I_{CS1_HPO} (V_{DD18} 1.8V)		350	380	mA	3.3V/1.8V sysApll
4				260	290	mA	3.3V/1.8V bypApll
5		I_{CS1_HPO} (V_{DD} 2.5V)		300	340	mA	2.5V/1.8V sysApll
6				240	280	mA	2.5V/1.8V bypApll
7		I_{CS1_HPO} (V_{DD18} 1.8V)		350	380	mA	2.5V/1.8V sysApll
8				260	290	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn1DivA + HPOUT[0:3]	I_{CS1_HPO} (V_{DD} 3.3V)		400	440	mA	3.3V/1.8V sysApll
10				340	370	mA	3.3V/1.8V bypApll
11		I_{CS1_HPO} (V_{DD18} 1.8V)		350	380	mA	3.3V/1.8V sysApll
12				260	290	mA	3.3V/1.8V bypApll
13		I_{CS1_HPO} (V_{DD} 2.5V)		350	390	mA	2.5V/1.8V sysApll
14				290	320	mA	2.5V/1.8V bypApll
15		I_{CS1_HPO} (V_{DD18} 1.8V)		350	380	mA	2.5V/1.8V sysApll
16				270	290	mA	2.5V/1.8V bypApll
17	Current for Core plus: Syn1DivABCD + HPOUT[0:3]	I_{CS1_HPO} (V_{DD} 3.3V)		480	520	mA	3.3V/1.8V sysApll
18				420	450	mA	3.3V/1.8V bypApll
19		I_{CS1_HPO} (V_{DD18} 1.8V)		370	410	mA	3.3V/1.8V sysApll
20				290	320	mA	3.3V/1.8V bypApll
21		I_{CS1_HPO} (V_{DD} 2.5V)		420	460	mA	2.5V/1.8V sysApll
22				360	400	mA	2.5V/1.8V bypApll
23		I_{CS1_HPO} (V_{DD18} 1.8V)		370	410	mA	2.5V/1.8V sysApll
24				290	320	mA	2.5V/1.8V bypApll

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO's are programmed to their highest rate; outputs are at 125MHz
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current
* See Figure 37

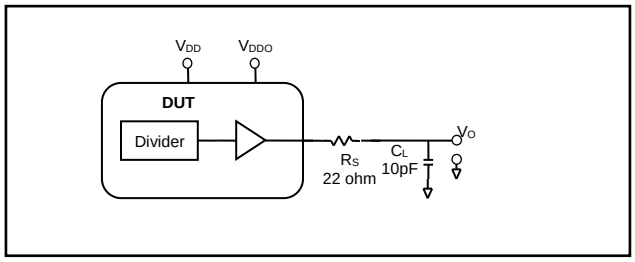


Figure 37. HPOUT & GPOUT (CMOS) Output

Table 25 · DC Electrical Characteristics* - Current - Core + Synthesizer 2 + HPOUT[11:4] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn2DivA + HPOUT[4]	I_{CS2_HPO} (V_{DD} 3.3V)		270	300	mA	3.3V/1.8V sysApll
2				210	230	mA	3.3V/1.8V bypApll
3		I_{CS2_HPO} (V_{DD18} 1.8V)		400	440	mA	3.3V/1.8V sysApll
4				320	350	mA	3.3V/1.8V bypApll
5		I_{CS2_HPO} (V_{DD} 2.5V)		230	260	mA	2.5V/1.8V sysApll
6				170	190	mA	2.5V/1.8V bypApll
7		I_{CS2_HPO} (V_{DD18} 1.8V)		400	440	mA	2.5V/1.8V sysApll
8				320	350	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn2DivA + HPOUT[4:7]	I_{CS2_HPO} (V_{DD} 3.3V)		310	340	mA	3.3V/1.8V sysApll
10				250	280	mA	3.3V/1.8V bypApll
11		I_{CS2_HPO} (V_{DD18} 1.8V)		410	450	mA	3.3V/1.8V sysApll
12				320	350	mA	3.3V/1.8V bypApll
13		I_{CS2_HPO} (V_{DD} 2.5V)		260	290	mA	2.5V/1.8V sysApll
14				200	220	mA	2.5V/1.8V bypApll
15		I_{CS2_HPO} (V_{DD18} 1.8V)		410	450	mA	2.5V/1.8V sysApll
16				320	360	mA	2.5V/1.8V bypApll
17	Current for Core plus: Syn2DivAB + HPOUT[4:7]	I_{CS2_HPO} (V_{DD} 3.3V)		310	340	mA	3.3V/1.8V sysApll
18				250	280	mA	3.3V/1.8V bypApll
19		I_{CS2_HPO} (V_{DD18} 1.8V)		420	460	mA	3.3V/1.8V sysApll
20				330	370	mA	3.3V/1.8V bypApll
21		I_{CS2_HPO} (V_{DD} 2.5V)		260	290	mA	2.5V/1.8V sysApll
22				200	220	mA	2.5V/1.8V bypApll
23		I_{CS2_HPO} (V_{DD18} 1.8V)		420	460	mA	2.5V/1.8V sysApll
24				330	370	mA	2.5V/1.8V bypApll
25	Current for Core plus: Syn2DivABCD + HPOUT[4:11]	I_{CS2_HPO} (V_{DD} 3.3V)		370	410	mA	3.3V/1.8V sysApll
26		I_{CS2_HPO} (V_{DD18} 1.8V)		480	530	mA	
27		I_{CS2_HPO} (V_{DD} 2.5V)		310	340	mA	2.5V/1.8V sysApll
28		I_{CS2_HPO} (V_{DD18} 1.8V)		480	530	mA	

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* Note that Syn2DivCD + HPOUT[8:11] should not be used in bypass mode as jitter is significantly higher
* VCO's are programmed to their highest rate; outputs are at 125MHz
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current
* See Figure 37

Table 26 · DC Electrical Characteristics* - Current - Core + Synthesizer 3 + HPOUT[11:8] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn3DivA + HPOUT[8]	I_{CS3_HPO} (V_{DD} 3.3V)		180	200	mA	3.3V/1.8V bypApll
2		I_{CS3_HPO} (V_{DD18} 1.8V)		300	340	mA	
3		I_{CS3_HPO} (V_{DD} 2.5V)		160	180	mA	2.5V/1.8V bypApll
4		I_{CS3_HPO} (V_{DD18} 1.8V)		300	340	mA	
5	Current for Core plus: Syn3DivA + HPOUT[8:11]	I_{CS3_HPO} (V_{DD} 3.3V)		220	250	mA	3.3V/1.8V bypApll
6		I_{CS3_HPO} (V_{DD18} 1.8V)		300	340	mA	
7		I_{CS3_HPO} (V_{DD} 2.5V)		190	210	mA	2.5V/1.8V bypApll
8		I_{CS3_HPO} (V_{DD18} 1.8V)		310	340	mA	
9	Current for Core plus: Syn3DivAB + HPOUT[8:11]	I_{CS3_HPO} (V_{DD} 3.3V)		220	250	mA	3.3V/1.8V bypApll
10		I_{CS3_HPO} (V_{DD18} 1.8V)		310	350	mA	
11		I_{CS3_HPO} (V_{DD} 2.5V)		190	210	mA	2.5V/1.8V bypApll
12		I_{CS3_HPO} (V_{DD18} 1.8V)		320	350	mA	

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO's are programmed to their highest rate; outputs are at 125MHz
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current
* See Figure 37

Table 27 · DC Electrical Characteristics* - Current - Core + Synthesizer 3:1 + HPOUT[11:0] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn1DivA + Syn2DivA + HPOUT[0,4]	I_{CS2_HPO} (V_{DD} 3.3V)		470	520	mA	3.3V/1.8V sysApll
2				400	460	mA	3.3V/1.8V bypApll
3		I_{CS2_HPO} (V_{DD18} 1.8V)		480	520	mA	3.3V/1.8V sysApll
4				390	430	mA	3.3V/1.8V bypApll
5		I_{CS2_HPO} (V_{DD} 2.5V)		400	450	mA	2.5V/1.8V sysApll
6				340	390	mA	2.5V/1.8V bypApll
7		I_{CS2_HPO} (V_{DD18} 1.8V)		480	520	mA	2.5V/1.8V sysApll
8				390	430	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn1DivABCD + Syn2DivAB + HPOUT[0:7]	I_{CS2_HPO} (V_{DD} 3.3V)		640	690	mA	3.3V/1.8V sysApll
10				580	620	mA	3.3V/1.8V bypApll
11		I_{CS2_HPO} (V_{DD18} 1.8V)		520	560	mA	3.3V/1.8V sysApll
12				430	470	mA	3.3V/1.8V bypApll
13		I_{CS2_HPO} (V_{DD} 2.5V)		560	600	mA	2.5V/1.8V sysApll
14				490	530	mA	2.5V/1.8V bypApll
15		I_{CS2_HPO} (V_{DD18} 1.8V)		520	560	mA	2.5V/1.8V sysApll
16				430	470	mA	2.5V/1.8V bypApll
17	Current for Core plus: Syn1DivA + Syn2DivA + Syn3DivA + HPOUT[0,4,8]	I_{CS2_HPO} (V_{DD} 3.3V)		500	560	mA	3.3V/1.8V bypApll
18		I_{CS2_HPO} (V_{DD18} 1.8V)		500	550	mA	
19		I_{CS2_HPO} (V_{DD} 2.5V)		430	480	mA	2.5V/1.8V bypApll
20		I_{CS2_HPO} (V_{DD18} 1.8V)		500	550	mA	
21	Current for Core plus: Syn1DivA + Syn2DivA + Syn3DivA + HPOUT[0:11]	I_{CS2_HPO} (V_{DD} 3.3V)		640	680	mA	3.3V/1.8V bypApll
22		I_{CS2_HPO} (V_{DD18} 1.8V)		510	560	mA	
23		I_{CS2_HPO} (V_{DD} 2.5V)		550	580	mA	2.5V/1.8V bypApll
24		I_{CS2_HPO} (V_{DD18} 1.8V)		510	560	mA	
25	Current for Core plus: Syn1DivABCD + Syn2DivAB + Syn3DivAB + HPOUT[0:11]	I_{CS2_HPO} (V_{DD} 3.3V)		720	760	mA	3.3V/1.8V bypApll
26		I_{CS2_HPO} (V_{DD18} 1.8V)		550	610	mA	
27		I_{CS2_HPO} (V_{DD} 2.5V)		620	660	mA	2.5V/1.8V bypApll
28		I_{CS2_HPO} (V_{DD18} 1.8V)		550	610	mA	
29	Current for Core plus: Syn1DivABCD + Syn2DivAB + Syn3DivAB + HPOUT[0:11] Outputs are at 100Hz	I_{CS2_HPO} (V_{DD} 3.3V)		590	650	mA	3.3V/1.8V bypApll
30		I_{CS2_HPO} (V_{DD18} 1.8V)		520	580	mA	
31		I_{CS2_HPO} (V_{DD} 2.5V)		520	570	mA	2.5V/1.8V bypApll
32		I_{CS2_HPO} (V_{DD18} 1.8V)		520	580	mA	

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO's are programmed to their highest rate; outputs are at 125MHz unless otherwise indicated
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current
* See Figure 37

Table 28 · DC Electrical Characteristics* - Current - Core + Synthesizer 0 + GPOUT[1:0] Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Current for Core plus: Syn0DivA + GPOUT[0]	I_{CS0_GP} (V_{DD} 3.3V)		160	180	mA	3.3V/1.8V sysApll
2				100	110	mA	3.3V/1.8V bypApll
3		I_{CS0_GP} (V_{DD18} 1.8V)		270	300	mA	3.3V/1.8V sysApll
4				190	220	mA	3.3V/1.8V bypApll
5		I_{CS0_GP} (V_{DD} 2.5V)		140	160	mA	2.5V/1.8V sysApll
6				80	90	mA	2.5V/1.8V bypApll
7		I_{CS0_GP} (V_{DD18} 1.8V)		270	300	mA	2.5V/1.8V sysApll
8				190	220	mA	2.5V/1.8V bypApll
9	Current for Core plus: Syn0DivAB + GPOUT[0:1]	I_{CS0_GP} (V_{DD} 3.3V)		170	180	mA	3.3V/1.8V sysApll
10				110	120	mA	3.3V/1.8V bypApll
11		I_{CS0_GP} (V_{DD18} 1.8V)		270	300	mA	3.3V/1.8V sysApll
12				190	220	mA	3.3V/1.8V bypApll
13		I_{CS0_GP} (V_{DD} 2.5V)		140	160	mA	2.5V/1.8V sysApll
14				80	90	mA	2.5V/1.8V bypApll
15		I_{CS0_GP} (V_{DD18} 1.8V)		270	300	mA	2.5V/1.8V sysApll
16				190	220	mA	2.5V/1.8V bypApll

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* sysApll is “System APLL Mode” and is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO’s are programmed to their highest rate; outputs are at 125MHz
* Output drivel level is set to 4X
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current
* See Figure 37

Table 29 · DC Electrical Characteristics* - Current - Core + Synthesizer 3:0 + HPOUT[11:0] + GPOUT[1:0]

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Current for Core plus: Syn0DivAB + Syn1DivABCD + Syn2DivABCD + GPOUT[0:1] + HPOUT[0:11]	I_{CS012_HPOGP} (V_{DD} 3.3V)		720	760	mA
2		I_{CS012_HPOGP} (V_{DD18} 1.8V)		580	640	mA
3		I_{CS012_HPOGP} (V_{DD} 2.5V)		620	650	mA
4		I_{CS012_HPOGP} (V_{DD18} 1.8V)		580	640	mA
5	Current for Core plus: Syn0DivAB + Syn1DivABCD + Syn2DivABCD + GPOUT[0:1] + HPOUT[0:11] Outputs are at 100Hz	I_{CS012_HPOGP} (V_{DD} 3.3V)		600	650	mA
6		I_{CS012_HPOGP} (V_{DD18} 1.8V)		550	610	mA
7		I_{CS012_HPOGP} (V_{DD} 2.5V)		520	570	mA
8		I_{CS012_HPOGP} (V_{DD18} 1.8V)		550	610	mA
9	Current for Core plus: Syn0DivAB + Syn1DivABCD + Syn2DivAB + Syn3DivAB + GPOUT[0:1] + HPOUT[0:11]	I_{CS0123_HPOGP} (V_{DD} 3.3V)		730	770	mA
10		I_{CS0123_HPOGP} (V_{DD18} 1.8V)		550	610	mA
11		I_{CS0123_HPOGP} (V_{DD} 2.5V)		630	670	mA
12		I_{CS0123_HPOGP} (V_{DD18} 1.8V)		550	610	mA
13	Current for Core plus: Syn0DivAB + Syn1DivABCD + Syn2DivAB + Syn3DivAB + GPOUT[0:1] + HPOUT[0:11] Outputs are at 100Hz	I_{CS0123_HPOGP} (V_{DD} 3.3V)		610	660	mA
14		I_{CS0123_HPOGP} (V_{DD18} 1.8V)		520	580	mA
15		I_{CS0123_HPOGP} (V_{DD} 2.5V)		540	580	mA
16		I_{CS0123_HPOGP} (V_{DD18} 1.8V)		520	580	mA

* Values are over Recommended Operating Conditions
* V_{DDO} is connected to V_{DD} and is included in the V_{DD} measured current value
* sysApll is “System APLL Mode” is when osc input is 49.152MHz and Syn[3] is used for internal clock generation
* bypApll is “Bypass APLL Mode” and is when osc input is 114.285MHz and no synthesizers are used for internal clock generation
* VCO’s are programmed to their highest rate; outputs are at 125MHz unless otherwise indicated
* GPOUT output drivel level is set to 4X
* Current is measured with synthesizer and outputs individually enabled/disabled and includes core current
* See Figure 37

Table 30 · DC Electrical Characteristics* - Reference Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Single ended CMOS high-level input voltage for ref[9:0]	$V_{IH-CMOS}$	$0.7 \cdot V_{DD}$			V	
2	Single ended CMOS low-level input voltage for ref[9:0]	$V_{IL-CMOS}$			$0.3 \cdot V_{DD}$	V	
3	Single ended CMOS input leakage current for ref[9:0]	$I_{IL-CMOS}$	-10		10	µA	Notes 1,2
4	Single ended PECL high-level input voltage for ref[9:0]	$V_{IH-PECL}$	$V_{REF-PECL}$ + 0.2			V	V_{DD} = 3.3V or 2.5V
5	Single ended PECL low-level input voltage for ref[9:0]	$V_{IL-PECL}$			$V_{REF-PECL}$ - 0.2	V	
6	Single ended PECL input reference voltage for ref[9:0]	$V_{REF-PECL}$		$0.55 \cdot V_{DD}$		V	
7	Single ended PECL input leakage current for ref[9:0]	$I_{IL-PECL}$	-10		10	µA	Note 1, $V_I = V_{DD}$ or 0.8 V
8	Differential input common mode voltage for ref[4:0]	V_{CM}	1.1		2.0	V	
9	Differential input voltage difference for ref[4:0]	V_{ID}	0.25		1.0	V	
10	Differential input leakage current for ref[4:0]	I_{IL}	-10		10	µA	Notes 1,2

Note 1 - Leakage current flowing out of the device pin referenced as positive
Note 2 - $V_I = V_{DD}$ or 0 V
* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V, 2.5V & 1.8V)

Table 31 · DC Electrical Characteristics* - Other Inputs and IO (Bi-directional)

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	High-level input voltage for osci[2:0]	V_{IH}	1.26			V	
2	Low-level input voltage for osci[2:0]	V_{IL}			0.54	V	
3	Input leakage current for osci[2:0]	I_{IL}	-10		10	µA	Note 1,2
4	Differential input common mode voltage for mclki[p,n]	V_{CM}	1.4		2.0	V	
5	Differential input voltage difference for mclki[p,n]	V_{ID}	0.25		1.0	V	
6	Differential input leakage current for mclki[p,n]	I_{IL}	-20		10	µA	Notes 1,2
7	CMOS high-level input voltage for gpio[3:0], rst_b	$V_{IH-CMOS}$	$0.7 \cdot V_{DD}$			V	
8	CMOS low-level input voltage for gpio[3:0], rst_b	$V_{IL-CMOS}$			$0.3 \cdot V_{DD}$	V	
9	CMOS input leakage current for gpio[3:0] (75 kohm pulldown)	$I_{IL-CMOS}$	-80		10	µA	Notes 1,2
10	CMOS input leakage current for rst_b (75 kohm pullup)	$I_{IL-CMOS}$	-10		80	µA	Notes 1,2
11	Schmitt high-level input voltage for tdi, tms, tck, trst_b, cs_b_asel0, m_so	$V_{IH-SCHM}$	2.0			V	
12	Schmitt low-level input voltage for tdi, tms, tck, trst_b, cs_b_asel0, m_so	$V_{IL-SCHM}$			0.7	V	
13	Schmitt input leakage current for tdi, tms, tck, trst_b, cs_b_asel0, m_so (33 kohm pullup)	$I_{IL-SCHM}$	-10		160	µA	Note 1,2
14	Bidirectional schmitt high-level input voltage for si_sda, sck_scl, so_asel1, gpio[6:4]	$V_{IH-BIDI}$	2.0			V	
15	Bidirectional schmitt low-level input voltage for si_sda, sck_scl, so_asel1, gpio[6:4]	$V_{SIL-BIDI}$			0.7	V	
16	Bidirectional schmitt input leakage current for si_sda, sck_scl (33 kohm pullup)	$I_{IL-BIDI}$	-10		160	µA	Notes 1,2
17	Bidirectional schmitt input leakage current for so_asel1	$I_{IL-BIDI}$	-10		10	µA	Notes 1,2
18	Bidirectional schmitt input leakage current for gpio[6:4] (33 kohm pulldown)	$I_{IL-BIDI}$	-160		15	µA	Notes 1,2
19	Tri-Level high-level input voltage for cnfgsel	V_{IH-TRI}	2.2			V	
20	Tri-Level mid-level input voltage for cnfgsel	V_{IM-TRI}	1.1		1.8	V	
21	Tri-Level low-level input voltage for cnfgsel	V_{IL-TRI}			0.8	V	
22	Tri-Level input leakage current for cnfgsel (115 kohm pullup, 125 kohm pulldown)	I_{IL-TRI}	-10		50	µA	Notes 1, V_I = V_{DD18} or 0 V

Note 1 - Leakage current flowing out of the device pin referenced as positive
Note 2 - $V_I = V_{DD}$ or 0 V
* Values are over Recommended Operating Conditions

Table 32 · DC Electrical Characteristics* - HPOUT_DIFF Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPOUT_DIFF[0:1] high level output voltage (V_{DDO} 3.3V or 2.5V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	Output Setting 0.7V See Figure 38 and Figure 14
2	HPOUT_DIFF[0:1] low level output voltage (V_{DDO} 3.3V or 2.5V)	V_{OL-CML}	V_{DDO} - 0.92	V_{DDO} - 0.69	V_{DDO} - 0.48	V	
3	HPOUT_DIFF[0:1] high to low output voltage (V_{DDO} 3.3V or 2.5V)	V_{OD-CML}	0.46	0.67	0.90	V	
4	HPOUT_DIFF[0:1] differential output voltage (V_{DDO} 3.3V or 2.5V)	$2*V_{OD-CML}$	0.92	1.34	1.80	V	
5	HPOUT_DIFF[2:3] high level output voltage (V_{DDO} 3.3V or 2.5V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	
6	HPOUT_DIFF[2:3] low level output voltage (V_{DDO} 3.3V or 2.5V)	V_{OL-CML}	V_{DDO} - 0.96	V_{DDO} - 0.74	V_{DDO} - 0.54	V	
7	HPOUT_DIFF[2:3] high to low output voltage (V_{DDO} 3.3V or 2.5V)	V_{OD-CML}	0.50	0.72	0.94	V	
8	HPOUT_DIFF[2:3] differential output voltage (V_{DDO} 3.3V or 2.5V)	$2*V_{OD-CML}$	1.0	1.44	1.88	V	
9	HPOUT_DIFF[4:5] high level output voltage (V_{DDO} 3.3V or 2.5V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	
10	HPOUT_DIFF[4:5] low level output voltage (V_{DDO} 3.3V or 2.5V)	V_{OL-CML}	V_{DDO} - 0.84	V_{DDO} - 0.61	V_{DDO} - 0.43	V	
11	HPOUT_DIFF[4:5] high to low output voltage (V_{DDO} 3.3V or 2.5V)	V_{OD-CML}	0.41	0.59	0.83	V	
12	HPOUT_DIFF[4:5] differential output voltage (V_{DDO} 3.3V or 2.5V)	$2*V_{OD-CML}$	0.82	1.18	1.66	V	
13	HPOUT_DIFF[0:1] high level output voltage (V_{DDO} 3.3V, 2.5V, 1.8V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	Output Setting 0.6V See Figure 38 and Figure 14
14	HPOUT_DIFF[0:1] low level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OL-CML}	V_{DDO} - 0.82	V_{DDO} - 0.61	V_{DDO} - 0.43	V	
15	HPOUT_DIFF[0:1] high to low output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OD-CML}	0.41	0.60	0.81	V	
16	HPOUT_DIFF[0:1] differential output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	$2*V_{OD-CML}$	0.82	1.20	1.62	V	
17	HPOUT_DIFF[2:3] high level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	
18	HPOUT_DIFF[2:3] low level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OL-CML}	V_{DDO} - 0.85	V_{DDO} - 0.66	V_{DDO} - 0.48	V	
19	HPOUT_DIFF[2:3] high to low output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OD-CML}	0.46	0.65	0.84	V	
20	HPOUT_DIFF[2:3] differential output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	$2*V_{OD-CML}$	0.92	1.30	1.68	V	
21	HPOUT_DIFF[4:5] high level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	
22	HPOUT_DIFF[4:5] low level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OL-CML}	V_{DDO} - 0.76	V_{DDO} - 0.55	V_{DDO} - 0.38	V	
23	HPOUT_DIFF[4:5] high to low output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OD-CML}	0.36	0.53	0.74	V	
24	HPOUT_DIFF[4:5] differential output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	$2*V_{OD-CML}$	0.72	1.06	1.48	V	
25	HPOUT_DIFF[0:1] high level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	Output Setting 0.4V See Figure 38 and Figure 14
26	HPOUT_DIFF[0:1] low level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OL-CML}	V_{DDO} - 0.55	V_{DDO} - 0.42	V_{DDO} - 0.28	V	
27	HPOUT_DIFF[0:1] high to low output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OD-CML}	0.27	0.41	0.54	V	
28	HPOUT_DIFF[0:1] differential output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	$2*V_{OD-CML}$	0.54	0.82	1.08	V	
29	HPOUT_DIFF[2:3] high level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	
30	HPOUT_DIFF[2:3] low level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OL-CML}	V_{DDO} - 0.58	V_{DDO} - 0.45	V_{DDO} - 0.31	V	
31	HPOUT_DIFF[2:3] high to low output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OD-CML}	0.31	0.44	0.56	V	
32	HPOUT_DIFF[2:3] differential output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	$2*V_{OD-CML}$	0.62	0.88	1.12	V	
33	HPOUT_DIFF[4:5] high level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OH-CML}	V_{DDO} - 0.11	V_{DDO} - 0.02	V_{DDO}	V	
34	HPOUT_DIFF[4:5] low level output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OL-CML}	V_{DDO} - 0.53	V_{DDO} - 0.37	V_{DDO} - 0.25	V	
35	HPOUT_DIFF[4:5] high to low output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	V_{OD-CML}	0.24	0.36	0.52	V	
36	HPOUT_DIFF[4:5] differential output voltage (V_{DDO} 3.3V, 2.5V or 1.8V)	$2*V_{OD-CML}$	0.48	0.72	1.04	V	

* Values are over Recommended Operating Conditions
* V_{DD} may be 2.5V or 3.3V as specified in Recommended Operating Conditions
* V_{DDO} may be 1.8V, 2.5V or 3.3V as specified in Recommended Operating Conditions
* HPOUT_DIFF for CML outputs
* CML pull-up resistors are R_{PU} = 50 ohm to V_{DDO} and far end termination is 50 ohms to V_{DDO}
* Output drive impedance is set to 25 ohms
* CML drive level can be set to 0.7V, 0.6V or 0.4V when V_{DDO} is 3.3V
* CML drive level can be set to 0.6V or 0.4V when V_{DDO} is 1.8V

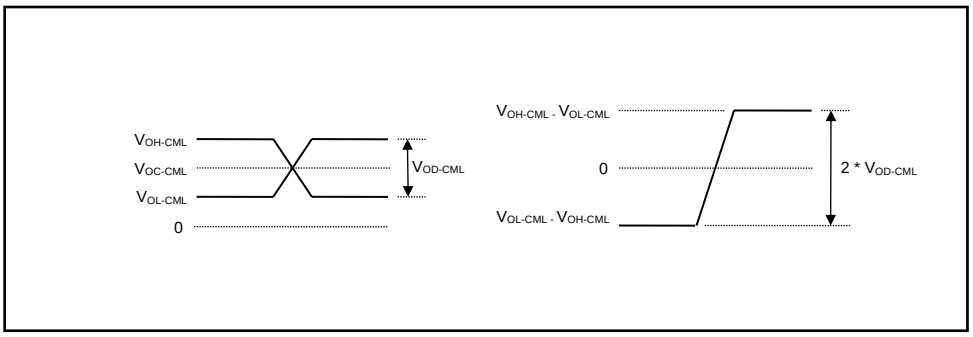


Figure 38. HPOUT_DIFF (CML) DC Output Level

Table 33 · DC Electrical Characteristics* - HPOUT and GPOUT Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPOUT[3:0] high level output voltage (V_{DDO} = 1.8V, I_{OH} = 3mA)	$V_{OH-HPOUT}$	0.8 * V_{DDO}			V	See Figure 37 & Figure 39
2	HPOUT[3:0] low level output voltage (V_{DDO} = 1.8V, I_{OL} = 3mA)	$V_{OL-HPOUT}$			0.2 * V_{DDO}	V	
3	HPOUT[3:0] high level output voltage (V_{DDO} = 2.5V, I_{OH} = 8mA)	$V_{OH-HPOUT}$	0.8 * V_{DDO}			V	
4	HPOUT[3:0] low level output voltage (V_{DDO} = 2.5V, I_{OL} = 8mA)	$V_{OL-HPOUT}$			0.2 * V_{DDO}	V	
5	HPOUT[3:0] high level output voltage (V_{DDO} = 3.3V, I_{OH} = 14mA)	$V_{OH-HPOUT}$	0.8 * V_{DDO}			V	
6	HPOUT[3:0] low level output voltage (V_{DDO} = 3.3V, I_{OL} = 14mA)	$V_{OL-HPOUT}$			0.2 * V_{DDO}	V	
7	HPOUT[11:4] high level output voltage (V_{DDO} = 1.8V, I_{OH} = 5mA)	$V_{OH-HPOUT}$	0.8 * V_{DDO}			V	See Figure 37 & Figure 39
8	HPOUT[11:4] low level output voltage (V_{DDO} = 1.8V, I_{OL} = 5mA)	$V_{OL-HPOUT}$			0.2 * V_{DDO}	V	
9	HPOUT[11:4] high level output voltage (V_{DDO} = 2.5V, I_{OH} = 12mA)	$V_{OH-HPOUT}$	0.8 * V_{DDO}			V	
10	HPOUT[11:4] low level output voltage (V_{DDO} = 2.5V, I_{OL} = 12mA)	$V_{OL-HPOUT}$			0.2 * V_{DDO}	V	
11	HPOUT[11:4] high level output voltage (V_{DDO} = 3.3V, I_{OH} = 21mA)	$V_{OH-HPOUT}$	0.8 * V_{DDO}			V	
12	HPOUT[11:4] low level output voltage (V_{DDO} = 3.3V, I_{OL} = 21mA)	$V_{OL-HPOUT}$			0.2 * V_{DDO}	V	
13	GPOUT high level output voltage (I_{OH} = 1.5mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 1X See Figure 37 & Figure 39
14	GPOUT low level output voltage (I_{OL} = 1.5mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	
15	GPOUT high level output voltage (I_{OH} = 3mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 2X See Figure 37 & Figure 39
16	GPOUT low level output voltage (I_{OL} = 3mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	
17	GPOUT high level output voltage (I_{OH} = 4.5mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 3X See Figure 37 & Figure 39
18	GPOUT low level output voltage (I_{OL} = 4.5mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	
19	GPOUT high level output voltage (I_{OH} = 6mA)	$V_{OH-GPOUT}$	0.8 * V_{DD}			V	Drive Setting = 4X See Figure 37 & Figure 39
20	GPOUT low level output voltage (I_{OL} = 6mA)	$V_{OL-GPOUT}$			0.2 * V_{DD}	V	

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* V_{DD} may be 2.5V or 3.3V as specified in Recommended Operating Conditions
* V_{DDO} may be 1.8V, 2.5V or 3.3V as specified in Recommended Operating Conditions

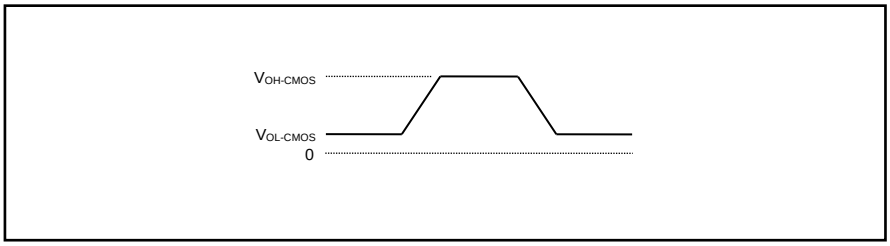


Figure 39. HPOUT and GPOUT (CMOS) Output Termination and DC Output Level

Table 34 · DC Electrical Characteristics* - Other Outputs and IO (Bi-directional)

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level output voltage for m_si, m_cs_b, m_sck	$V_{OH-CMOS}$	0.8 * V_{DD}			V	I_{OH} = 6mA
2	CMOS low-level output voltage for m_si, m_cs_b, m_sck	$V_{OL-CMOS}$			0.2 * V_{DD}	V	I_{OL} = 10mA
3	CMOS high-level output voltage for tdo	$V_{OH-CMOS}$	0.8 * V_{DD}			V	I_{OH} = 3.5mA
4	CMOS low-level output voltage for tdo	$V_{OL-CMOS}$			0.2 * V_{DD}	V	I_{OL} = 5mA
5	Bidirectional high level output voltage for so_asel1, gpio[5]	$V_{OH-BIDI}$	0.8 * V_{DD}			V	I_{OH} = 6mA
6	Bidirectional low level output voltage for so_asel1, gpio[5]	$V_{OL-BIDI}$			0.2 * V_{DD}	V	I_{OL} = 6mA
7	Bidirectional low level output voltage for si_sda, sck_scl	$V_{OL-BIDI}$			0.2 * V_{DD}	V	I_{OL} = 2mA
8	Bidirectional high level output voltage for gpio[6,4]	$V_{OH-BIDI}$	0.8 * V_{DD}			V	I_{OH} = 2.5mA
9	Bidirectional low level output voltage for gpio[6,4]	$V_{OL-BIDI}$			0.2 * V_{DD}	V	I_{OL} = 2.5mA
10	Bidirectional high level output voltage for gpio[3:0]	$V_{OH-BIDI}$	0.8 * V_{DD}			V	I_{OH} = 6mA
11	Bidirectional low level output voltage for gpio[3:0]	$V_{OL-BIDI}$			0.2 * V_{DD}	V	I_{OL} = 6mA

* Values are over Recommended Operating Conditions
* Values are tested over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* V_{DD} may be 2.5V or 3.3V as specified in Recommended Operating Conditions

14.4 AC Electrical Characteristics

Table 35 · AC Electrical Characteristics* - Output Timing Parameters Measurement Voltage Levels

	Characteristics	Sym.	Units	Notes
1	HPOUT_DIFF (CML) threshold voltage	V_T	V	Threshold (V_T) is 50% of output swing Threshold high (V_{HM}) is 80% of output swing Threshold low (V_{LM}) is 20% of output swing
2	HPOUT_DIFF (CML) rise/fall threshold voltage high	V_{HM}	V	
3	HPOUT_DIFF (CML) rise/fall threshold voltage low	V_{LM}	V	
4	HPOUT threshold voltage	V_T	V	
5	HPOUT rise/fall threshold voltage high	V_{HM}	V	
6	HPOUT rise/fall threshold voltage low	V_{LM}	V	
7	GPOUT threshold voltage	V_T	V	
8	GPOUT rise/fall threshold voltage high	V_{HM}	V	
9	GPOUT rise/fall threshold voltage low	V_{LM}	V	

* Values are over Recommended Operating Conditions
* For the threshold voltage drawing see Figure 40

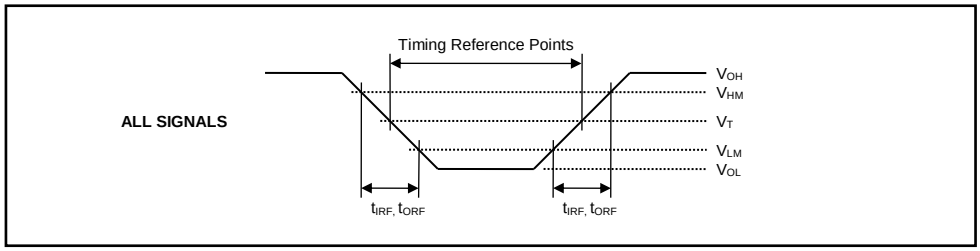


Figure 40. Timing Parameter Measurement Voltage Levels

Table 36 · AC Electrical Characteristics* - Input Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Single ended CMOS input reference frequency for ref[9:0]	$1/T_{TREFP}$			180	MHz	See Figure 41
2	Single ended CMOS input reference pulse width low or high for ref[9:0]	T_{TREFW}	2.7			ns	
3	Single ended PECL input reference frequency for ref[9:0]	$1/T_{TREFP}$			900	MHz	
4	Single ended PECL input reference pulse width low or high for ref[9:0]	T_{TREFW}	0.55			ns	
5	Differential input reference frequency for ref[4:0]	$1/T_{TREFP}$			900	MHz	
6	Differential input reference pulse width low or high for ref[4:0]	T_{TREFW}	0.55			ns	
7	Duty Cycle for osci		40		60	%	
8	Duty Cycle for mclki[p,n]		40		60	%	

* Values are over Recommended Operating Conditions

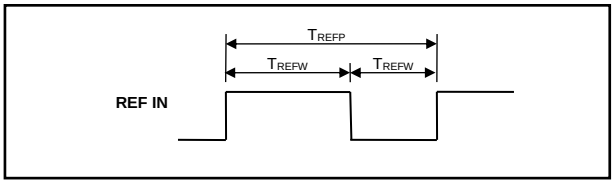


Figure 41. Reference Input Timing

Table 37 · AC Electrical Characteristics* - REF Input to HPOUT_DIFF, HPOUT and GPOUT Output Clock Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Input reference (REF DIFF) to HPOUT_DIFF output delay	$T_{D\text{-}REF\text{-}HPOUT\_DIFF}$	-2.0	0	+2.0	ns	See Figure 36 and Figure 42
2	Input reference (REF) to HPOUT output delay	$T_{D\text{-}REF\text{-}HPOUT}$	-2.0	0	+2.0	ns	See Figure 37 and Figure 42
3	Input reference (REF) to GPOUT output delay	$T_{D\text{-}REF\text{-}GPOUT}$	-2.5	0	+2.5	ns	See Figure 37 and Figure 42

* Values are over Recommended Operating Conditions
* Input and output are at the same frequency
* HPOUT_DIFF output drive impedance is set to 25 ohms and drive level is set to 0.7V
* GPOUT output drive level is set to 4X

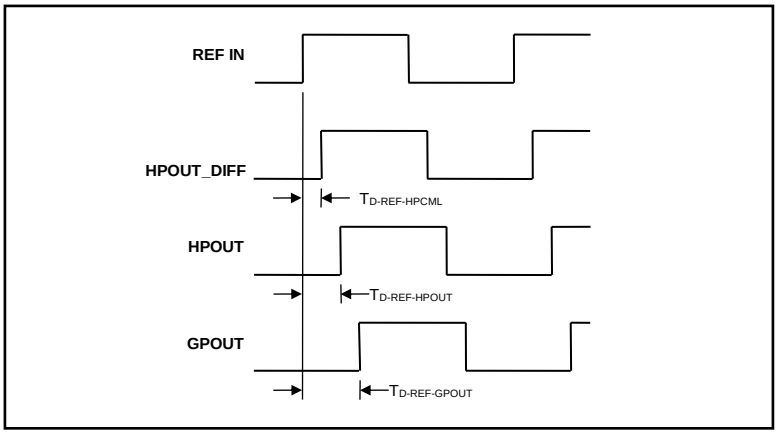


Figure 42. Reference Input to Output Clock Timing

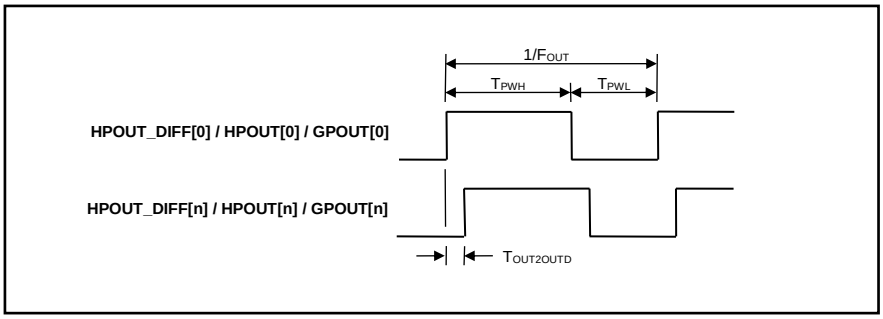


Figure 43. Output to Output Clock Timing

Table 38 · AC Electrical Characteristics* - HPOUT_DIFF Output Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Frequency for HPOUT_DIFF outputs	$F_{OUT-HPOUT\_DIFF}$			900	MHz	
2	Duty cycle for HPOUT_DIFF outputs (drive 0.7V)	T_{PWL}, T_{PWH}	45	50	55	percent	Tested at 707.352MHz and 900MHz
3	Rise & Fall time for HPOUT_DIFF outputs (drive 0.7V)	t_r/ t_f	200	285	450	ps	3.3V & 1.8V supply mode with 3.3V VDDO
4	Rise & Fall time for HPOUT_DIFF outputs (drive 0.7V)	t_r/ t_f	200	310	450	ps	2.5 & 1.8V supply mode with 2.5V VDDO
5	Rise & Fall time for HPOUT_DIFF outputs (drive 0.4V)	t_r/ t_f	200	320	450	ps	2.5V & 1.8V supply mode with 1.8V VDDO

* Values are over Recommended Operating Conditions
* Output drive impedance is set to 25 ohms
* See Figure 40, Figure 44 and Figure 45

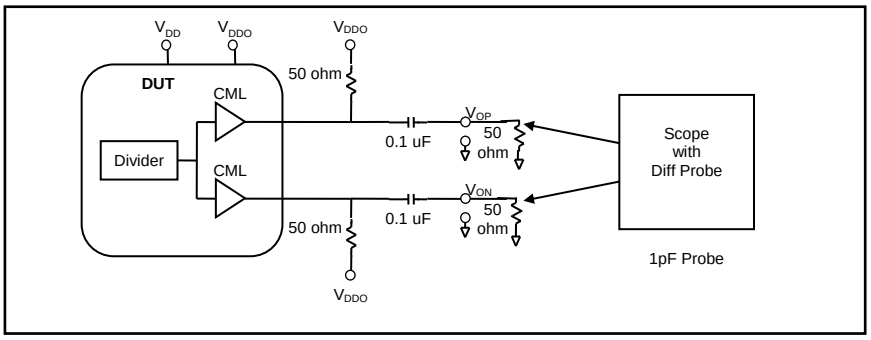


Figure 44. HPOUT_DIFF Output tr and tf Measurement Setup

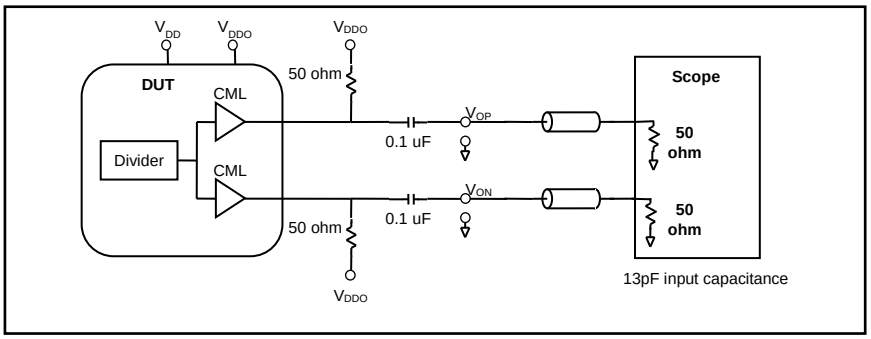


Figure 45. HPOUT_DIFF Output Duty Cycle Measurement Setup

Table 39 · AC Electrical Characteristics* - HPOUT and GPOUT Output Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Frequency for HPOUT outputs	$F_{OUT-HPOUT}$			180	MHz	
2	Frequency for GPOUT outputs	$F_{OUT-GPOUT}$			180	MHz	
3	Duty cycle for HPOUT outputs	T_{PWL}, T_{PWH}	45	50	55	percent	Tested at 77.760MHz, 125MHz, 156.25MHz and 180MHz
4	Duty cycle for GPOUT outputs	T_{PWL}, T_{PWH}	40	50	60	percent	Tested at 125MHz and 180MHz
5	Rise time for HPOUT outputs	t_r	450	700	950	ps	3.3V & 1.8V supply mode with 3.3V VDDO
6	Fall time for HPOUT outputs	t_f	450	700	950	ps	
7	Rise time for HPOUT outputs	t_r	750	1000	2100	ps	2.5V & 1.8V supply mode with 1.8V VDDO
8	Fall time for HPOUT outputs	t_f	750	1000	2100	ps	
9	Rise time for GPOUT outputs (drive 4X)	t_r	800	1500	2500	ps	3.3V & 1.8V supply mode
10	Fall time for GPOUT outputs (drive 4X)	t_f	500	700	1700	ps	
11	Rise time for GPOUT outputs (drive 4X)	t_r	1200	1900	3200	ps	2.5V & 1.8V supply mode
12	Fall time for GPOUT outputs (drive 4X)	t_f	600	900	2200	ps	

* Values are over Recommended Operating Conditions
* See Figure 40 and Figure 46

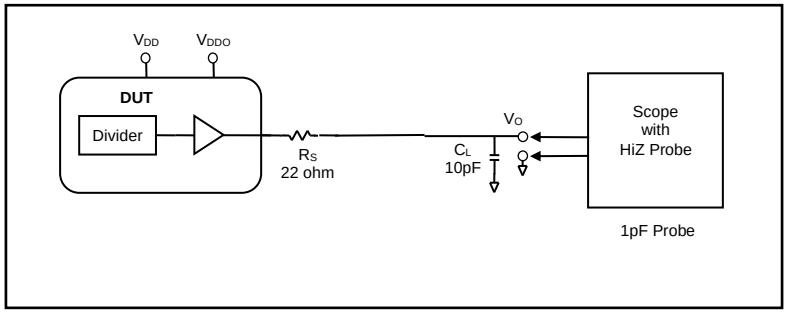


Figure 46. HPOUT and GPOUT Output tr, tf & Duty Cycle Measurement Setup

Table 40 · AC Electrical Characteristics* - SPI (Serial Peripheral Interface) Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	sck period	tcyc	80			ns	See Figure 47& Figure 48
2	sck pulse width low	tclkl	40			ns	
3	sck pulse width high	tclkh	40			ns	
4	si setup (write) from sck rising edge	trxs	8			ns	
5	si hold (write) from sck falling edge	trxh	8			ns	
6	so delay (read) from sck falling edge	txd			25	ns	
7	cs_b to output high impedance	tohz			60	ns	
8	cs_b setup from sck falling edge (LSB first)	tcssi	16			ns	See Figure 47
9	cs_b hold from sck rising edge (LSB first)	tcshi	8			ns	
10	cs_b setup from sck rising edge (MSB first)	tcssm	16			ns	See Figure 48
11	cs_b hold from sck falling edge (MSB first)	tcshm	8			ns	

* Values are over Recommended Operating Conditions
* For LSB first mode timing diagram, refer to Figure 47
* For MSB first mode timing diagram, refer to Figure 48

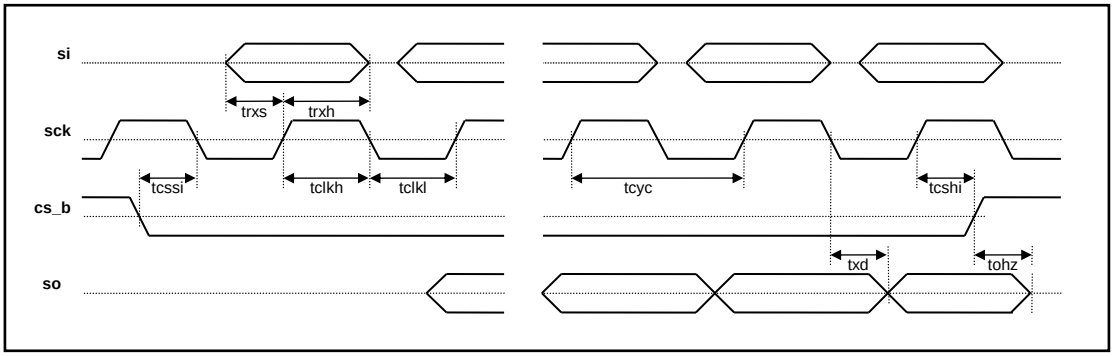


Figure 47. SPI (Serial Peripheral Interface) Timing - LSB First Mode

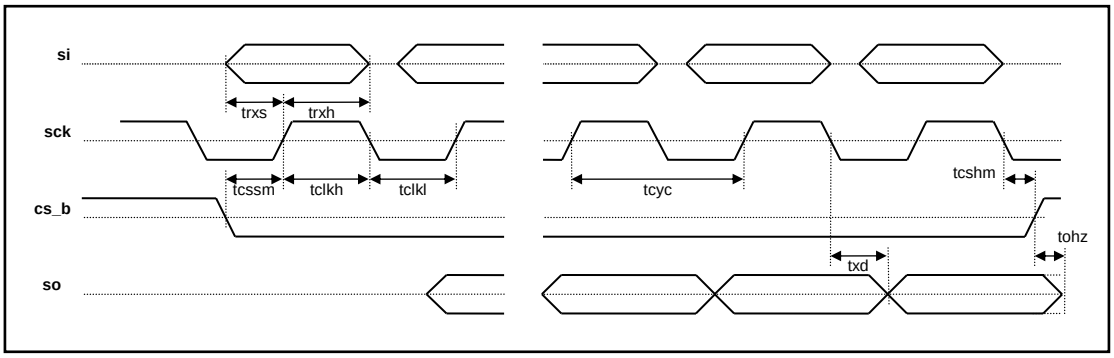


Figure 48. SPI (Serial Peripheral Interface) Timing - MSB First Mode

Table 41 · AC Electrical Characteristics* - I²C Serial Microport Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	SCL clock frequency	f_{SCL}	0		400	kHz	
2	Hold time START condition	$t_{HD:STA}$	0.6			us	
3	Low period SCL	t_{LOW}	1.3			us	
4	Hi period SCL	t_{HIGH}	0.6			us	
5	Setup time START condition	$t_{SU:STA}$	0.6			us	
6	Data hold time	$t_{HD:DAT}$	0		0.9	us	
7	Data setup time	$t_{SU:DAT}$	100			ns	
8	Rise time	t_r	20 + 0.1*Cb		250	ns	
9	Fall time	t_f	20 + 0.1*Cb		250	ns	
10	Setup time STOP condition	$t_{SU:STO}$	0.6			us	
11	Bus free time between STOP/START	t_{BUF}	1.3			us	
12	Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
13	Max capacitance for each I/O pin				10	pF	

* Values are over Recommended Operating Conditions
* For I²C timing diagram, refer to Figure 49

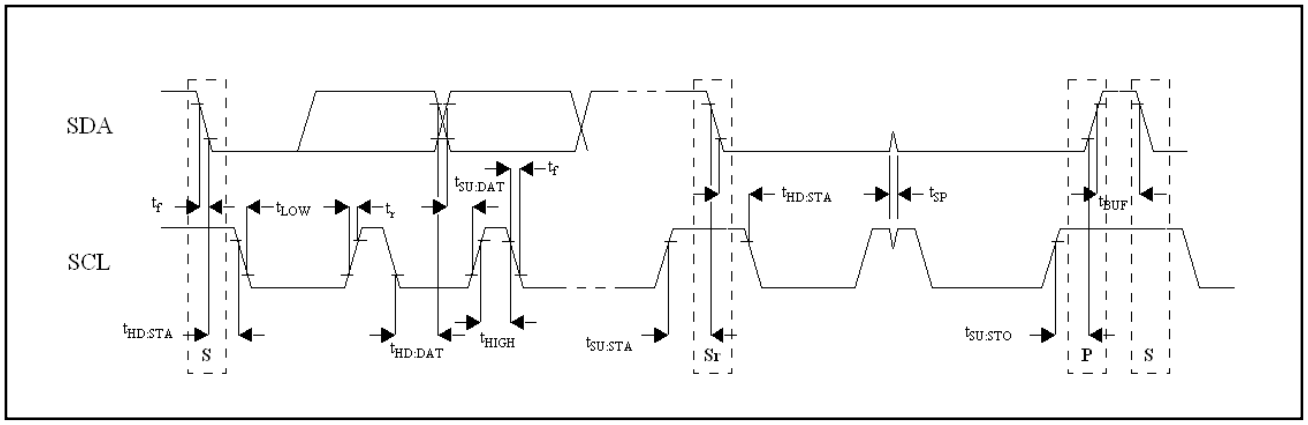


Figure 49. I²C Serial Microport Timing

15 Performance Characteristics

15.1 Output Clocks Jitter Generation

Table 42 · Output Clocks Jitter Generation* - HPOUT_DIFF[0:1] (CML) with 114.285MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[0]	622.08MHz	50kHz - 80MHz	175	250	fs-rms
2			12kHz - 20MHz	185	260	fs-rms
3		625MHz	50kHz - 80MHz	175	250	fs-rms
4			12kHz - 20MHz	180	260	fs-rms
5		156.25MHz	10kHz - 1MHz	160	220	fs-rms
6			50kHz - 8 MHz	185	270	fs-rms
7			12kHz - 20MHz	240	325	fs-rms
8	HPOUT_DIFF[1]	622.08MHz	50kHz - 80MHz	195	270	fs-rms
9			12kHz - 20MHz	190	270	fs-rms
10		625MHz	50kHz - 80MHz	190	270	fs-rms
11			12kHz - 20MHz	190	280	fs-rms
12		156.25MHz	10kHz - 1MHz	160	220	fs-rms
13			50kHz - 8 MHz	190	275	fs-rms
14			12kHz - 20MHz	250	340	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator Vectron VCC1-1537-114M285
* The jitter test circuit is shown in Figure 50

Table 43 · Output Clocks Jitter Generation* - HPOUT_DIFF[2:3] (CML) with 114.285MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[2]	622.08MHz	50kHz - 80MHz	170	230	fs-rms
2			12kHz - 20MHz	185	250	fs-rms
3		625MHz	50kHz - 80MHz	170	230	fs-rms
4			12kHz - 20MHz	185	250	fs-rms
5		156.25MHz	10kHz - 1MHz	165	215	fs-rms
6			50kHz - 8 MHz	175	235	fs-rms
7			12kHz - 20MHz	215	275	fs-rms
8	HPOUT_DIFF[3]	622.08MHz	50kHz - 80MHz	170	230	fs-rms
9			12kHz - 20MHz	185	250	fs-rms
10		625MHz	50kHz - 80MHz	170	230	fs-rms
11			12kHz - 20MHz	185	250	fs-rms
12		156.25MHz	10kHz - 1MHz	165	215	fs-rms
13			50kHz - 8 MHz	180	240	fs-rms
14			12kHz - 20MHz	225	285	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator Vectron VCC1-1537-114M285
* The jitter test circuit is shown in Figure 50

Table 44 · Output Clocks Jitter Generation* - HPOUT_DIFF[4:5] (CML) with 114.285MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[4]	622.08MHz	50kHz - 80MHz	200	310	fs-rms
2			12kHz - 20MHz	200	280	fs-rms
3		625MHz	50kHz - 80MHz	195	290	fs-rms
4			12kHz - 20MHz	200	280	fs-rms
5		156.25MHz	10kHz - 1MHz	165	215	fs-rms
6			50kHz - 8 MHz	190	270	fs-rms
7			12kHz - 20MHz	250	340	fs-rms
8	HPOUT_DIFF[5]	622.08MHz	50kHz - 80MHz	195	280	fs-rms
9			12kHz - 20MHz	190	260	fs-rms
10		625MHz	50kHz - 80MHz	190	280	fs-rms
11			12kHz - 20MHz	195	270	fs-rms
12		156.25MHz	10kHz - 1MHz	165	210	fs-rms
13			50kHz - 8 MHz	185	250	fs-rms
14			12kHz - 20MHz	245	320	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator Vectron VCC1-1537-114M285
* The jitter test circuit is shown in Figure 50

Table 45 · Output Clocks Jitter Generation* - HPOUT_DIFF[0:1] (CML) with 49.152MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[0]	622.08MHz	50kHz - 80MHz	195	270	fs-rms
2			12kHz - 20MHz	210	310	fs-rms
5		156.25MHz	10kHz - 1MHz	195	280	fs-rms
6			50kHz - 8 MHz	205	280	fs-rms
7			12kHz - 20MHz	265	370	fs-rms
8	HPOUT_DIFF[1]	622.08MHz	50kHz - 80MHz	210	290	fs-rms
9			12kHz - 20MHz	220	300	fs-rms
12		156.25MHz	10kHz - 1MHz	195	290	fs-rms
13			50kHz - 8 MHz	215	285	fs-rms
14			12kHz - 20MHz	275	360	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Clock oscillator 49.152MHz = CTS CB3LV10012
* The jitter test circuit is shown in Figure 50

Table 46 · Output Clocks Jitter Generation* - HPOUT_DIFF[2:3] (CML) with 49.152MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[2]	622.08MHz	50kHz - 80MHz	195	240	fs-rms
2			12kHz - 20MHz	210	270	fs-rms
3		625MHz	50kHz - 80MHz	195	240	fs-rms
4			12kHz - 20MHz	215	290	fs-rms
5		156.25MHz	10kHz - 1MHz	190	270	fs-rms
6			50kHz - 8 MHz	190	235	fs-rms
7			12kHz - 20MHz	235	300	fs-rms
8	HPOUT_DIFF[3]	622.08MHz	50kHz - 80MHz	200	240	fs-rms
9			12kHz - 20MHz	215	270	fs-rms
10		625MHz	50kHz - 80MHz	200	240	fs-rms
11			12kHz - 20MHz	215	290	fs-rms
12		156.25MHz	10kHz - 1MHz	190	270	fs-rms
13			50kHz - 8 MHz	195	235	fs-rms
14			12kHz - 20MHz	240	300	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Clock oscillator 49.152MHz = CTS CB3LV10012
* The jitter test circuit is shown in Figure 50

Table 47 · Output Clocks Jitter Generation* - HPOUT_DIFF[4:5] (CML) with 49.152MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[4]	622.08MHz	50kHz - 80MHz	220	260	fs-rms
2			12kHz - 20MHz	225	290	fs-rms
3		625MHz	50kHz - 80MHz	220	260	fs-rms
4			12kHz - 20MHz	225	300	fs-rms
5		156.25MHz	10kHz - 1MHz	195	270	fs-rms
6			50kHz - 8 MHz	220	265	fs-rms
7			12kHz - 20MHz	280	340	fs-rms
8	HPOUT_DIFF[5]	622.08MHz	50kHz - 80MHz	215	260	fs-rms
9			12kHz - 20MHz	220	290	fs-rms
10		625MHz	50kHz - 80MHz	215	260	fs-rms
11			12kHz - 20MHz	220	290	fs-rms
12		156.25MHz	10kHz - 1MHz	190	260	fs-rms
13			50kHz - 8 MHz	210	250	fs-rms
14			12kHz - 20MHz	270	325	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Clock oscillator 49.152MHz = CTS CB3LV10012
* The jitter test circuit is shown in Figure 50

Table 48 · Output Clocks Jitter Generation* - HPOUT_DIFF[0:1] (CML) with 24.576MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[0]	622.08MHz	50kHz - 80MHz	220	295	fs-rms
2			12kHz - 20MHz	240	330	fs-rms
3		156.25MHz	10kHz - 1MHz	225	300	fs-rms
4			50kHz - 8 MHz	230	310	fs-rms
5			12kHz - 20MHz	285	380	fs-rms
6	HPOUT_DIFF[1]	622.08MHz	50kHz - 80MHz	235	315	fs-rms
7			12kHz - 20MHz	245	330	fs-rms
8		156.25MHz	10kHz - 1MHz	225	300	fs-rms
9			50kHz - 8 MHz	240	315	fs-rms
10			12kHz - 20MHz	305	385	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator CTS CB3LV10059
* The jitter test circuit is shown in Figure 50

Table 49 · Output Clocks Jitter Generation* - HPOUT_DIFF[2:3] (CML) with 24.576MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[2]	622.08MHz	50kHz - 80MHz	220	270	fs-rms
2			12kHz - 20MHz	240	310	fs-rms
3		625MHz	50kHz - 80MHz	220	270	fs-rms
4			12kHz - 20MHz	240	300	fs-rms
5		156.25MHz	10kHz - 1MHz	220	280	fs-rms
6			50kHz - 8 MHz	220	265	fs-rms
7			12kHz - 20MHz	260	320	fs-rms
8	HPOUT_DIFF[3]	622.08MHz	50kHz - 80MHz	225	270	fs-rms
9			12kHz - 20MHz	245	310	fs-rms
10		625MHz	50kHz - 80MHz	225	270	fs-rms
11			12kHz - 20MHz	245	310	fs-rms
12		156.25MHz	10kHz - 1MHz	225	280	fs-rms
13			50kHz - 8 MHz	225	270	fs-rms
14			12kHz - 20MHz	270	325	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator CTS CB3LV10059
* The jitter test circuit is shown in Figure 50

Table 50 · Output Clocks Jitter Generation* - HPOUT_DIFF[4:5] (CML) with 24.576MHz XO

	Outputs	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units
1	HPOUT_DIFF[4]	622.08MHz	50kHz - 80MHz	230	280	fs-rms
2			12kHz - 20MHz	250	310	fs-rms
3		625MHz	50kHz - 80MHz	230	280	fs-rms
4			12kHz - 20MHz	250	310	fs-rms
5		156.25MHz	10kHz - 1MHz	225	290	fs-rms
6			50kHz - 8 MHz	235	285	fs-rms
7			12kHz - 20MHz	290	360	fs-rms
8	HPOUT_DIFF[5]	622.08MHz	50kHz - 80MHz	230	280	fs-rms
9			12kHz - 20MHz	250	310	fs-rms
10		625MHz	50kHz - 80MHz	225	280	fs-rms
11			12kHz - 20MHz	245	310	fs-rms
12		156.25MHz	10kHz - 1MHz	220	280	fs-rms
13			50kHz - 8 MHz	230	280	fs-rms
14			12kHz - 20MHz	285	350	fs-rms

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* Output drive impedance is set to 25 ohms
* Output drive levels are set to 0.4V
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator CTS CB3LV10059
* The jitter test circuit is shown in Figure 50

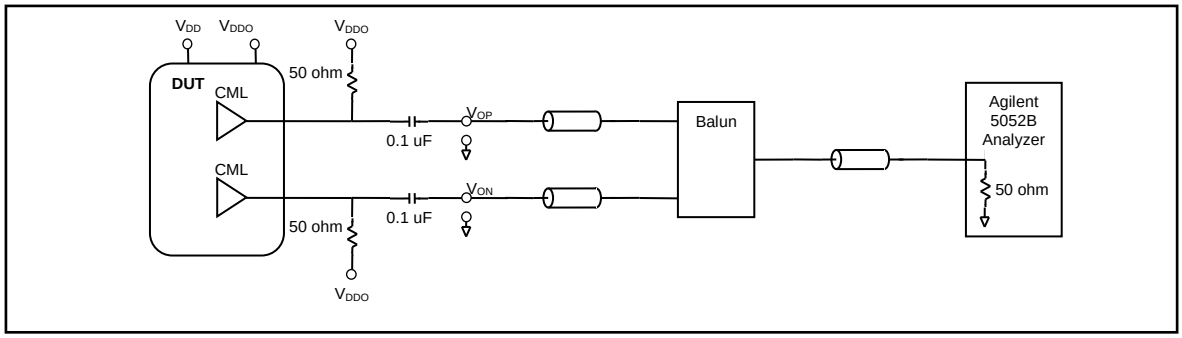


Figure 50. HPOUT_DIFF (CML) Output Jitter Test Circuit

Table 51 · Output Clocks Jitter Generation* - HPOUT (LVCMOS) Output Clock Timing

	Output & Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units	Notes
1	HPOUT[11:0] 125MHz	12 kHz – 20 MHz	0.29	0.55	ps-rms	osci= 49.152MHz osci =24.576MHz osci = 114.285MHz
2	HPOUT[11:0] 25MHz	12 kHz – 5 MHz	0.26	0.52	ps-rms	

* Maximum value shows worst case for all outputs. Individual outputs can have significantly better maximum value.
* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator type and part numbers is as follows:
  24.576MHz = CTS CB3LV10059
  49.152MHz = CTS CB3LV10012
  114.285MHz = Vectron VCC1-1537-114M285
* The jitter test circuit is shown in Figure 51

Table 52 · Output Clocks Jitter Generation* - GPOUT (LVCMOS) Output Clock Timing

	Output Frequency	Jitter Measurement Filter	Typ.	Max.	Units	Notes
1	125 MHz	12 kHz - 20 MHz	17	24	ps-rms	osci = 49.152MHz
2	25 MHz	12 kHz - 5 MHz	12	20	ps-rms	

* Values are over Recommended Operating Conditions
* Values are over both power supply modes (3.3V & 1.8V and 2.5V & 1.8V)
* Values are with V_{DDO} = 3.3V for 3.3V & 1.8V mode; and V_{DDO} = 2.5V for 2.5V & 1.8V mode
* GPOUT output drive levels are set to 4x
* The DPLL is in locked mode with 14Hz bandwidth and reference input at 19.44MHz
* Oscillator type and part numbers is as follows:
  49.152MHz = CTS CB3LV10012
* The jitter test circuit is shown in Figure 51

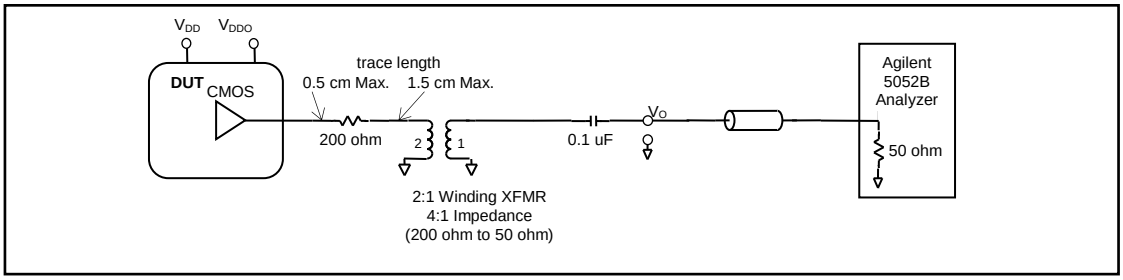


Figure 51. HPOUT (LVCMOS) and GPOUT (LVCMOS) Output Jitter Test Circuit

15.2 DPLL Performance Characteristics

Table 53 · DPLL Performance Characteristics*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in/Hold-in Range	0.1	12	2100	ppm	user programmable
2	Lock Time (Bandwidth > 14Hz)		1.6	2	sec	unlimited phase slope limit 10us/1s lock selection +/-200ppm pull-in/hold range
3	Reference Switching MTIE		0.6		ns	bandwidth = 14Hz jitter free input (1ps rms)
4	Entry into Holdover MTIE		0.6		ns	
5	Exit from Holdover MTIE		0.6		ns	
6	Initial Holdover Accuracy (Bandwidth =14Hz)		2	10	ppb	input frequency = 19.44MHz jitter free input (1ps rms)
7	Damping Factor	1	5	50		user programmable
8	Phase gain in the pass band		0.08	0.1	dB	damping factor set to 5

* Values are over Recommended Operating Conditions
* Jitter free input implies less than 1ps rms jitter

15.3 Package thermal characteristics

Table 54 · Package Thermal Characteristics

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	still air	11.6	°C/W
		1m/s airflow	9.20	
		2m/s airflow	8.50	
Junction to Board Thermal Resistance	θ_{JB}		2.56	°C/W
Junction to Case Thermal Resistance	θ_{JC}		3.84	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.21	°C/W

Note 1: Theta-JA (θJA) is the thermal resistance from junction to ambient when the package is mounted on an 8-layer JEDEC standard test board and dissipating maximum power.

16 Change History

The August 2016 issue is the first release of the production datasheet.

February 2017 changes:

- Modified pin description for pin R2
- Modified section 10.6.5
- Added revision register at address 0x003

July 2017 changes:

- Corrected pull-up/pull-down information in the **General Purpose Input and Output pins** description.
- Added a NOTE to the **GPIO Configuration**
- Added bit mapping descriptions for the mask bits in the **ref_ctrl** register (0x0582:0x0583), **dpll_ctrl** register (0x0602:0x0603), and **synth_ctrl** register (0x0682:0x0683) descriptions.
- Updated the SPI timing diagrams and tables (see section: **AC Electrical Characteristics* - SPI (Serial Peripheral Interface) Timing**)
- Removed ZLAN-526 from the **Companion Documentation**
- Changed bits [6:4] in the **synth_irq_mask** register to reserved bits

October 2017 changes:

- Added Notes to **Table 31 · DC Electrical Characteristics* - Other Inputs and IO (Bi-directional)** and **Table 30 · DC Electrical Characteristics* - Reference Inputs**
- Corrected DC parameters V_{OH-CML} , V_{OL-CML}, V_{OD-CML}, $2*V_{OD-CML}$ in **Table 32 · DC Electrical Characteristics* - HPOUT_DIFF Outputs** section.

January 2018 changes:

- Corrected DC parameters V_{OL-CML}, V_{OD-CML} for HPDIFF[4:5] in **Table 32 · DC Electrical Characteristics* - HPOUT_DIFF Outputs**
- Corrected DC parameters I_{OL}, I_{OH} in **Table 33 · DC Electrical Characteristics* - HPOUT and GPOUT Outputs**
- Corrected DC parameters I_{OL}, I_{OH} in the Notes section in **Table 34 · DC Electrical Characteristics* - Other Outputs and IO (Bi-directional)**

August 2018 changes:

- Replaced text in section 10.1.4 Input Buffers and Figure 7 Input buffers & termination

September 2019 changes:

- Added support for Split-XO mode
- Added 4th DPLL channel
- Add note in register descriptions for the **revision** register (0x0003) and the split_**xo_mode_control** register (0x021D)
- Updated the default value for the **revision** in register 0x0003
- Updated the default value for the **chip_id** in id registers 0x0001 and 0x0002.

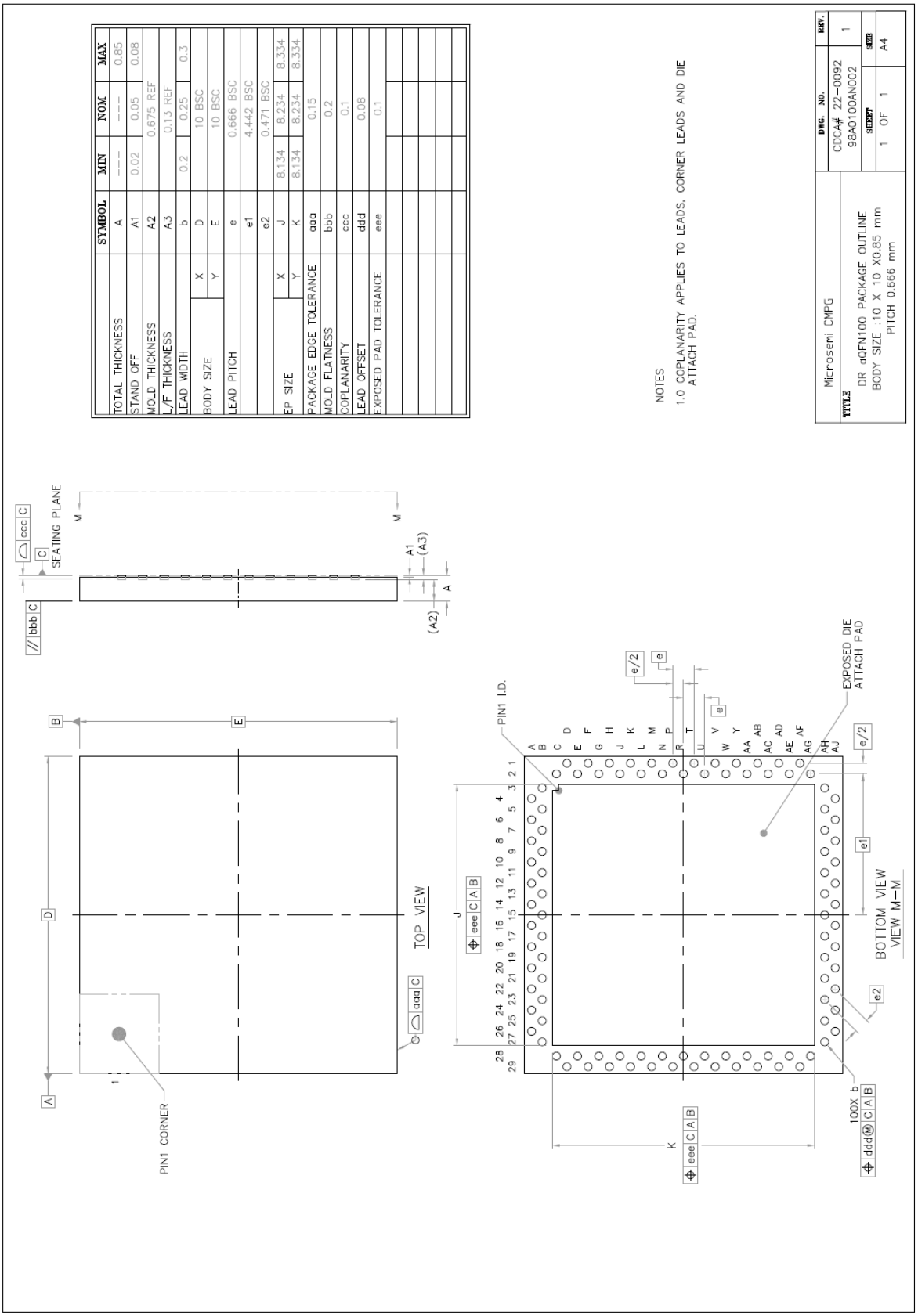
August 2023 changes:

- Updated Table 33 DC Electrical Characteristics* - HPOUT and GPOUT Outputs

17 Acronyms

- CGU: Clock Generation Unit
- DCO: Digitally Controlled Oscillator
- DPLL: Digital Phase Lock Loop
- FCL: Frequency Change Limit
- NCO: Numerically Controlled Oscillator
- OTN: Optical Transport Network
- PLL: Phase Lock Loop
- ppb: Parts per billion (10E-9)
- ppt: Parts per trillion (10E-12)
- PSL: Phase Slope Limit
- SyncE: Synchronous Ethernet
- ZL: Zarlink
- ZLE: Zarlink Evaluation Board

18 Package Outline



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