ZL30250 - ZL30251

4 Input, 3 Output Any-to-Any Clock Multiplier and Frequency Synthesizer ICs

Features

Four Input Clocks

- One Crystal/CMOS Input
- Two Differential/CMOS Inputs
- One Single-Ended/CMOS Input
- Any Input Frequency from 9.72 MHz to 1250 MHz (9.72 MHz to 300 MHz for CMOS)
- Clock Selection by Pin or Register Control

Low-Jitter Fractional-N APLL and 3 Outputs

- Any Output Frequency from <1 Hz to 1035 MHz
- High-Resolution Fractional Frequency Conversion with 0 ppm Error
- Easy-to-Configure, Encapsulated Design Requires No External VCXO or Loop Filter Components
- Each Output has Independent Dividers
- Output Jitter as Low as 0.16 ps RMS (12 kHz to 20 MHz Integration Band)
- Outputs are CML or 2xCMOS, can Interface to LVDS, LVPECL, HSTL, SSTL, and HCSL
- In 2xCMOS Mode, the P and N Pins can be Different Frequencies (e.g. 125 MHz and 25 MHz)
- Per-Output Supply Pin with CMOS Output Voltages from 1.5V to 3.3V
- Precise Output Alignment Circuitry and Per-Output Phase Adjustment
- Per-Output Enable/Disable and Glitchless Start/Stop (Stop High or Low)

General Features

- Automatic Self-Configuration at Power-Up from External (ZL30250) or Internal (ZL30251) EEPROM; up to Four Configs, Pin-Selectable
- SPI or I^2C Processor Interface
- Numerically Controlled Oscillator Mode
- Spread-Spectrum Modulation Mode
- PCIe Gen1 through Gen6 Clock Generation (without Spread Spectrum)
- Tiny 5 mm x 5 mm VQFN Package
- Easy-to-Use Evaluation Software

Applications

- Frequency conversion and frequency synthesis in a wide variety of equipment types

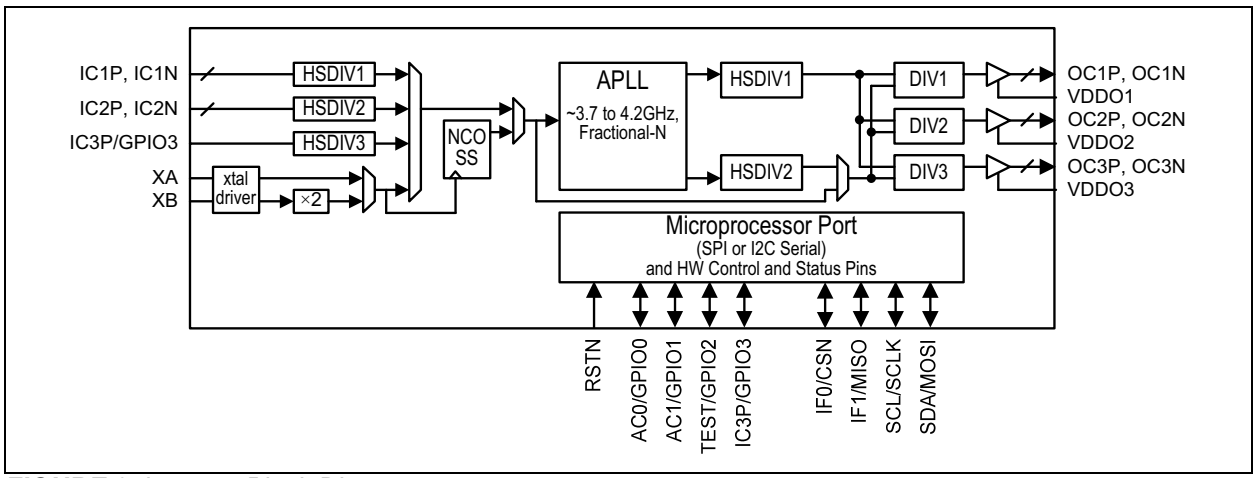

FIGURE 0-1: *Block Diagram.*

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1.0 APPLICATION EXAMPLES

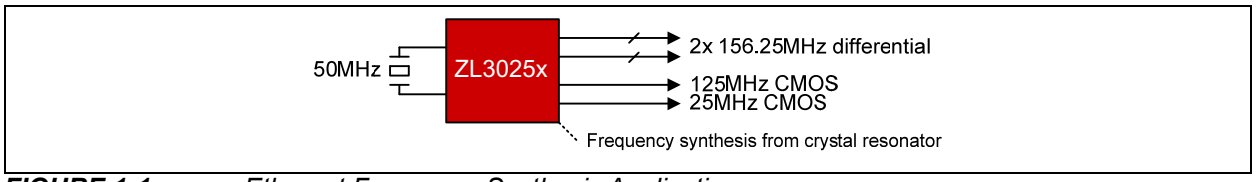


FIGURE 1-1: *Ethernet Frequency Synthesis Application.*

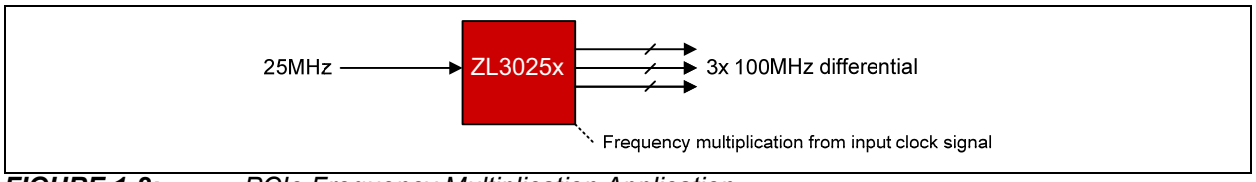


FIGURE 1-2: *PCIe Frequency Multiplication Application.*

2.0 DETAILED FEATURES

2.1 Input Clock Features

- Four input clocks: one crystal/CMOS, two differential/CMOS, one single-ended/CMOS
- Input clocks can be any frequency from 9.72 MHz up to 1250 MHz (differential) or 300 MHz (CMOS)

2.2 APLL Features

- Very high-resolution fractional (i.e. non-integer) multiplication
- Any-to-any frequency conversion with 0 ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Bypass mode supports system testing

2.3 Output Clock Features

- Three low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1 Hz to 1035 MHz (250 MHz max. for CMOS and HSTL outputs)
- Output jitter as low as 0.16 ps RMS (12 kHz to 20 MHz integration band)
- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (example: OC3P 125 MHz, OC3N 25 MHz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL, and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs, and other components
- Can produce PCIe-compliant clocks Gen1 through Gen 6 (non spread-spectrum)
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.4 General Features

- SPI or I^2C serial microprocessor interface
- Automatic self-configuration at power-up from external (ZL30250) or internal (ZL30251) EEPROM memory; pin control to specify one of four stored configurations
- Numerically controlled oscillator (NCO) mode allows system software to steer frequency with resolution better than 0.01 ppb
- Spread-spectrum modulation mode
- Four general-purpose I/O pins each with many possible status and control options
- Reference can be fundamental-mode crystal, low-cost XO or clock signal from elsewhere in the system

2.5 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30250 or ZL30251 quick and easy
- Generates configuration scripts to be stored in external (ZL30250) or internal (ZL30251) EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without a ZL30250 or ZL30251 evaluation board

3.0 PIN DIAGRAM

The device is packaged in a 5 mm x 5 mm 32-lead VQFN

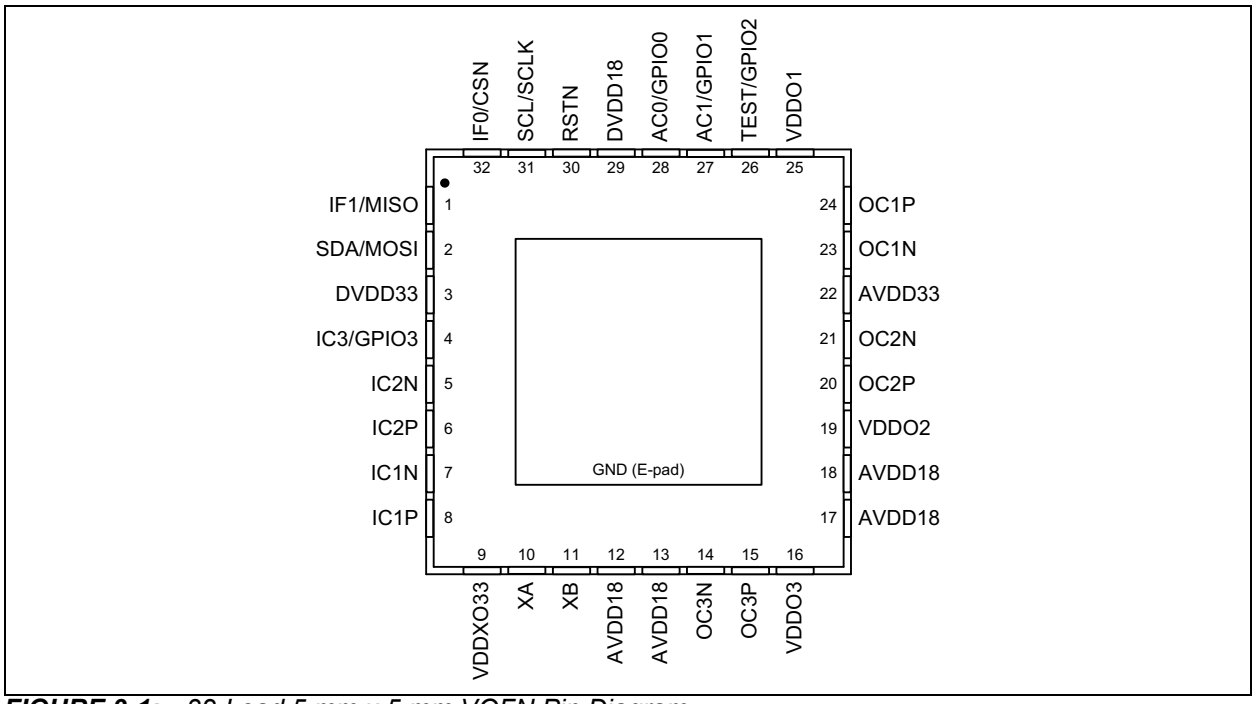


FIGURE 3-1: *32-Lead 5 mm x 5 mm VQFN Pin Diagram.*

4.0 PIN DESCRIPTIONS

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, I_{PU} – input with 50 kΩ internal pull-up resistor, O – output, A – analog, P – power supply pin. All GPIO and SPI/I^2C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

TABLE 4-1: PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Description
8	IC1P	I	**Input Clock Pins** Differential or Single-ended signal format. Programmable frequency. *Differential*: See Table 7-6 for electrical specifications, and see Table 7-2 for recommended external circuitry for interfacing these differential inputs to LVDS, LVPECL, CML or HSCL output pins on neighboring devices. *Single-ended*: For input signal amplitude >2.5V, connect the signal directly to ICxP pin. For input signal amplitude ≤2.5V, AC-coupling the signal to ICxP is recommended. Connect the N pin to a capacitor (0.1 µF or 0.01 µF) to VSS. As shown in Table 7-2, the ICxP and ICxN pins are internally biased to approximately 1.3V. Treat the ICxN pin as a sensitive node; minimize stubs; do not connect to anything else including other ICxN pins. *Unused*: Set ICEN.ICxEN=0. The ICxP and ICxN pins can be left floating. Note that the IC3N pin is not bonded out. A differential signal can be connected to IC3P by AC-coupling the POS trace to IC3P and terminating the signal on the driver side of the coupling cap. If not needed as an input clock pin, IC3P can behave as general-purpose I/O pin GPIO3, which is configured by GPIOCR2. Its state is indicated in GPIOSR.
7	IC1N	I	
6	IC2P	I	
5	IC2N	I	
4	IC3P/GPIO3	I/O	
10	XA	A/I	**Crystal or Input Clock Pins** *Crystal*: MCR1.XAB=01. An on-chip crystal driver circuit is designed to work with an external crystal connected to the XA and XB pins. See Section 5.3.2 for crystal characteristics and recommended external components. *Input Clock*: MCR1.XAB=10. An external local oscillator or clock signal can be connected to the XA pin. The XB pin must be left unconnected.
11	XB		
24	OC1P	O	**Output Clock Pins** CML, HSTL or 1 or 2 CMOS. Programmable frequency and drive strength. See Table 7-7 and Figure 7-4 for electrical specifications and recommended external circuitry for interfacing to LVDS, LVPECL or CML input pins on neighboring devices. See Figure 7-8 for electrical specifications for interfacing to CMOS and HSTL inputs on neighboring devices. See Figure 7-5 for recommended external circuitry for interfacing to HCSL inputs on neighboring devices.
23	OC1N		
20	OC2P		
21	OC2N		
15	OC3P		
14	OC3N		
30	RSTN	I_{PU}	**Reset (Active Low)** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. See Section 5.10.

TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	Type	Description
28	AC0/GPIO0	I/O	**Auto-Configure [1:0]/General Purpose I/O 0 and 1** *Auto-Configure*: On the rising edge of RSTN these pins behave as AC[1:0] and specify one of the configurations stored in EEPROM. See Section 5.2. *General-Purpose I/O*: After reset these pins are GPIO0 and GPIO1. GPIOCR1 configures the pins. Their states are indicated in GPIOSR.
27	AC1/GPIO1		
26	TEST/ GPIO2	I/O	**Factory Test/General Purpose I/O 2** *Factory Test*: On the rising edge of RSTN the pin behaves as TEST. Factory test mode is enabled when TEST is high. For normal operation TEST must be low on the rising edge of RSTN. *General-Purpose I/O*: After reset this pin is GPIO2. GPIOCR2 configures the pin. It state is indicated in GPIOSR.
32	IF0/CSN	I/O	**Interface Mode 0/SPI Chip Select (Active Low)** *Interface Mode*: On the rising edge of RSTN the pin behaves as IF0 and, together with IF1, specifies the interface mode for the device. See Section 5.2. *SPI Chip Select*: After reset this pin is CSN. When the device is configured as a SPI slave, an external SPI master must assert (low) CSN to access device registers. When the device is configured as a SPI master (ZL30250 only), the device asserts CSN to access an external SPI EEPROM during auto-configuration.
31	SCL/SCLK	I/O	**I^2C Clock/SPI Clock** *I^2C Clock*: When the device is configured as an I^2C client, an external I^2C server must provide the I^2C clock signal on the SCL pin. Note that I^2C requires an external pull-up resistor on this signal. See the I^2C specification for details. *SPI Clock*: When the device is configured as an SPI client, an external SPI server must provide the SPI clock signal on SCLK. When the device is configured as a SPI server (ZL30250 only), the device drives SCLK as an output to clock accesses to an external SPI EEPROM during auto-configuration.
1	IF1/MISO	I/O	**Interface Mode 1/SPI Server-In-Client-Out** *Interface Mode*: On the rising edge of RSTN the pin behaves as IF1 and, together with IF0, specifies the interface mode for the device. See Section 5.2. *SPI MISO*: After reset this pin is MISO. When the device is configured as a SPI client, the device outputs data to an external SPI server on MISO during SPI read transactions. When the device is configured as a SPI server (ZL30250 only), the device receives data on MISO from an external SPI EEPROM during auto-configuration. **Note:** On rev A parts, in I^2C interface mode this pin toggles between driving low and high-impedance during register accesses. Therefore, in I^2C mode this pin must not be wired directly to VDD. To implement a static high value on IF1/MISO, wire it to VDD through a resistor (approximately 10 kΩ recommended).

TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	Type	Description
2	SDA/MOSI	I/O	**I²C Data/SPI Server-Out-Client-In** *I²C Data*: When the device is configured as an I²C client, SDA is the bidirectional data line between the device and an external I²C server. Note that I²C requires an external pull-up resistor on this signal. See the I²C specification for details. *SPI MOSI*: When the device is configured as a SPI client, an external SPI server sends commands, addresses, and data to the device on MOSI. When the device is configured as a SPI server (ZL30250 only), the device sends commands, addresses and data on MOSI to an external SPI EEPROM during auto-configuration.
12	AVDD18	P	**Analog Power Supply.** 1.8V ±5%.
13			
17			
18			
22	AVDD33	P	**Analog Power Supply.** 3.3V ±5%.
29	DVDD18	P	**Digital Power Supply.** 1.8V ±5%.
3	DVDD33	P	**Digital Power Supply.** 3.3V ±5%.
25	VDDO1	P	**Output OC1 Power Supply.** 1.5V to 3.3V ±5%.
19	VDDO2	P	**Output OC2 Power Supply.** 1.5V to 3.3V ±5%.
16	VDDO3	P	**Output OC3 Power Supply.** 1.5V to 3.3V ±5%.
9	VDDXO33	P	**Analog Power Supply for Crystal Driver Circuitry.** 3.3V ±5%.
ePad	VSS	P	**Ground.** 0 Volts.

5.0 FUNCTIONAL DESCRIPTION

5.1 Device Identification

The 12-bit read-only ID field and the 4-bit revision field are found in the ID1 and ID2 registers. Contact the factory to interpret the revision value and determine the latest revision.

5.2 Pin-Controlled Automatic Configuration at Reset

The device configuration is determined at reset (i.e. on the rising edge of RSTN) by the signal levels on five device pins: TEST/GPIO2, AC1/GPIO1, AC0/GPIO0, IF1/MISO, and IF0/CSN. For each of these pins, the first name (TEST, AC1, AC0, IF1, IF0) indicates their function when they are sampled by the rising edge of the RSTN pin. The second name refers to their function after reset. The values of these pins are latched into the CFGSR register when RSTN goes high. To ensure the device properly samples the reset values of these pins, the following guidelines should be followed:

1. Any pull-up or pull-down resistors used to set the value of these pins at reset should be 1 kΩ.
2. RSTN must be asserted at least as long as specified in Section 5.10.

The hardware configuration pins are grouped into three sets:

- TEST - Manufacturing test mode
- IF[1:0] – Microprocessor interface mode and I^2C address
- AC[1:0] – Auto-configuration from EEPROM

The TEST pin selects manufacturing test modes when TEST=1 (the AC[1:0] pins specify the test mode). For ZL30251, TEST=1 and AC[1:0]=00 configures the part so that production SPI EEPROM programmers can program the internal EEPROM (see Section 5.12.2). For more information about auto-configuration from EEPROM see Section 5.12.1.

5.2.1 ZL30250: EXTERNAL EEPROM OR NO EEPROM

For the ZL30250 the IF[1:0] pins specify the processor interface mode and the I^2C client address. When IF[1:0]=11 (SPI) two options are available:

- If AC[1:0]=00 the device sets up its processor interface as SPI client through which it can be configured by software running on the SPI server. In this option, the device cannot auto-configure from an external EEPROM.
- If AC[1:0]=01, 10, or 11 the device first sets up its processor interface as a SPI server. It then auto-configures itself by reading the configuration number specified by AC[1:0] from an external SPI EEPROM connected to its SPI pins. After auto-configuration is complete, the device reconfigures its processor interface to be SPI client.

These options are summarized in the following table:

TABLE 5-1: IF[1:0] OPTIONS SUMMARY, EXTERNAL EEPROM OR NO EEPROM

IF1	IF0	AC1	AC0	Processor Interface	External EEPROM	Auto Configuration
0	0	0	0	I^2C, client address 11011 00	No	N/A
0	1	0	0	I^2C, client address 11011 01	No	N/A
1	0	0	0	I^2C, client address 11011 10	No	N/A
1	1	0	0	SPI client	No	N/A
1	1	0	1	SPI server to external EEPROM for auto-configuration then SPI client	Yes	Configuration 1
1	1	1	0		Yes	Configuration 2
1	1	1	1		Yes	Configuration 3

Notes about the device auto-configuring from external EEPROM:

1. The device's CSN pin must have a pull-up resistor to VDD to ensure its processor interface is inactive after auto-configuration is complete. The SCLK, MISO, and MOSI pins should also have pull-up resistors to VDD to keep them from floating.
2. If a processor or similar device will access device registers after the device has auto-configured from external EEPROM, the SPI SCLK, MOSI, and MISO wires can be connected directly to the processor, the device, and the external EEPROM. The processor and device CSN pins can be wired together also. The EEPROM CSN signal must be controlled by the device's CSN pin during device auto-configuration and then held inactive when the processor accesses device registers.

5.2.2 ZL30251: INTERNAL EEPROM

For the ZL30251 the IF[1:0] pins specify the processor interface mode and the I^2C client address. The AC[1:0] pins specify which of four device configurations in the EEPROM to execute after reset.

TABLE 5-2: IF[1:0] CONFIGURATIONS, INTERNAL EEPROM

IF1	IF0	Processor Interface
0	0	I^2C, client address 11011 00
0	1	I^2C, client address 11011 01
1	0	I^2C, client address 11011 10
1	1	SPI Client

TABLE 5-3: AC[1:0] CONFIGURATIONS, INTERNAL EEPROM

AC1	AC0	Auto Configuration
0	0	Configuration 0
0	1	Configuration 1
1	0	Configuration 2
1	1	Configuration 3

5.3 Local Oscillator or Crystal

Section 5.3.1 describes how to connect an external oscillator and the required characteristics of the oscillator. Section 5.3.2 describes how to connect an external crystal to the on-chip crystal driver circuit and the required characteristics of the crystal.

5.3.1 EXTERNAL OSCILLATOR

A signal from an external oscillator can be connected to the XA pin (XB must be left unconnected). Table 7-5 specifies the range of possible frequencies for the XA input. To minimize jitter, the signal must be properly terminated and must have very short trace length. A poorly terminated single-ended signal can greatly increase output jitter, and long single-ended trace lengths are more susceptible to noise. When MCR1.XAB=10, XA is enabled as a single-ended input.

While the stability of the external oscillator can be important, its absolute frequency accuracy is less important because any known frequency inaccuracy of the oscillator can be compensated. When the device is configured for NCO or spread-spectrum operation, the DFREQZ parameter can be used to compensate for oscillator frequency error. When the device is configured for APLL-only mode, the APLL's fractional feedback divider value (AFBDIV) can be adjusted by ppb or ppm to compensate for oscillator frequency error.

The jitter on output clock signals depends on the phase noise and frequency of the external oscillator. For the device to operate with the lowest possible output jitter, the external oscillator should have the following characteristics:

- Phase Jitter: less than 0.1 ps RMS over the 12 kHz to 5 MHz integration band
- Frequency: The higher the better, all else being equal

5.3.2 EXTERNAL CRYSTAL AND ON-CHIP DRIVER CIRCUIT

The on-chip crystal driver circuit is designed to work with a fundamental mode, AT-cut crystal resonator. See Table 5-4 for recommended crystal specifications. To enable the crystal driver, set MCR1.XAB=01.

See Figure 5-1 for the crystal equivalent circuit and the recommended external capacitor connections. To achieve a crystal load (C_L) of 10 pF, an external 16 pF is placed in parallel with the 4 pF internal capacitance of the XA pin, and an external 16 pF is placed in parallel with the 4 pF internal capacitance of the XB pin. The crystal then sees a load of 20 pF in series with 20 pF, which is 10 pF total load. Note that the 16 pF capacitance values in Figure 5-1 include all capacitance on those nodes. If, for example, PCB trace capacitance between crystal pin and IC pin is 2 pF then 14 pF capacitors should be used to make 16 pF total.

The crystal, traces, and two external capacitors should be placed on the board as close as possible to the XA and XB pins to reduce crosstalk of active signals into the oscillator. Also no active signals should be routed under the crystal circuitry.

Note: Crystals have temperature sensitivities that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO or TCXO should be used instead.

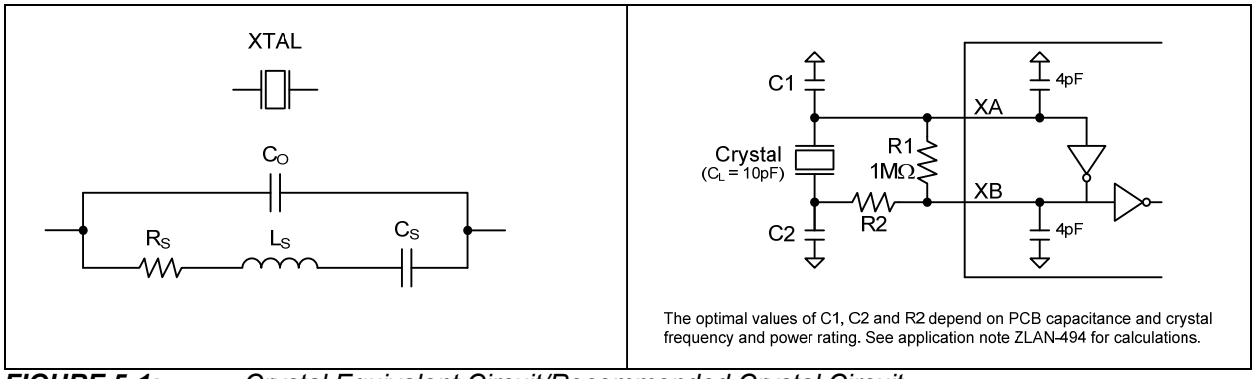


FIGURE 5-1: *Crystal Equivalent Circuit/Recommended Crystal Circuit.*

TABLE 5-4: CRYSTAL SELECTION PARAMETERS

Parameter		Symbol	Min.	Typ.	Max.	Units
Crystal Oscillation Frequency (Note 1)		f_{OSC}	25	—	60	MHz
Shunt Capacitance		C_O	—	2	5	pF
Load Capacitance		C_L	—	10	—	pF
Equivalent Series Resistance (ESR, Note 2)	f_{OSC} <40 MHz	R_S	—	—	60	Ω
	f_{OSC} >40 MHz		—	—	50	Ω
Maximum Crystal Drive Level		—	100	—	—	µW
Crystal Frequency Stability vs. Power Supply		f_{FVD}	—	0.2	0.5	ppm per 10% Δ in V_{DD}

Note 1: Higher frequencies give lower output jitter, all else being equal.

2: These ESR limits are chosen to constrain crystal drive level to less than 100 µW. If the crystal can tolerate a drive level greater than 100 µW then proportionally higher ESR is acceptable.

Any known frequency inaccuracy of the crystal can be compensated in the APLL by adjusting the APLL's fractional feedback divider value (AFBDIV) by ppb or ppm to compensate for crystal frequency error.

5.3.3 CLOCK DOUBLER

Figure 1 shows an optional clock doubler (“x2” block) following the crystal driver block. The doubler, which is enabled by setting MCR1.DBL=1, can be used to double the frequency of the internal crystal driver circuit or an clock signal on the XA pin. The following table shows scenarios when the clock doubler can be used

TABLE 5-5: CLOCK DOUBLER SCENARIOS

Device Mode	With Crystal	With XO or Clock Signal
APLL, Integer Multiply	Maybe (Note 1)	Maybe (Note 1)
APLL, Fractional Multiply	Yes	Yes
NCO	Yes	Yes
Spread-Spectrum	Yes	Yes

Note 1: For APLL integer multiplication, use of the doubler is application-dependent. On the positive side, use of the doubler reduces random jitter. On the negative side, the doubler causes a large spur at the XA frequency (but this spur may be outside the band of interest for the application).

5.3.4 RING OSCILLATOR (FOR SYSTEM START-UP)

To ensure that registers can be written immediately after system start-up, in its power-on reset state the device operates its registers and processor interface from an internal ring oscillator.

When operating the device in NCO mode or spread spectrum mode, as soon as the external oscillator connected to the XA pin has stabilized and is ready to use, the MCR1.MCSEL bit must be set to source the NCO/SS master clock from XA. If the ring oscillator causes undesirable spurs it can be disabled (powered down) by setting MCR1.ROSCD=1.

When operating the part in APLL-only mode, a master clock signal on the XA pin is not required, and the ring oscillator is left enabled to provide a clock for the processor interface logic and registers.

5.4 Input Signal Format Configuration

Input clocks IC1, IC2, and IC3 are enabled by setting the enable bits in the ICEN register. The power consumed by a differential receiver is shown in Table 7-3. The electrical specifications for these inputs are listed in Table 7-6. Each input clock can be configured to accept nearly any differential signal format by using the proper set of external components (see Figure 7-2). To configure these differential inputs to accept single-ended CMOS signals, connect the single-ended signal to the ICxP pin, and connect the ICxN pin to a capacitor (0.1 µF or 0.01 µF) to VSS. Each ICxP and ICxN pin is internally biased to approximately 1.3V. If an input is not used, both ICxP and ICxN pins can be left floating. Note that the IC3N pin is not present. A differential signal can be connected to IC3P by AC-coupling the POS trace to IC3P and terminating the signal on the driver side of the coupling cap. If not needed as an input clock pin, IC3P can behave as general-purpose I/O pin GPIO3.

5.5 Numerically Controlled Oscillator/Spread Spectrum Block (NCO/SS)

The NCO/SS block allows the device to behave as a numerically controlled oscillator and optionally perform spread-spectrum frequency modulation. This block is enabled by setting PLLEN.NCSSEN=1 and is the input reference for the APLL when APLLCR3.APLLMUX=11x. The NCO/SS block requires a clock signal from an external oscillator connected to the XA pin (see Section 5.3.1). Table 7-5 shows the allowable frequency range for the XA signal. Note that device output jitter increases as XA frequency decreases.

5.5.1 NUMERICALLY CONTROLLED OSCILLATOR (NCO) MODE

The NCO/SS block operates in NCO mode when NCSSCR1.MODE=0001. In this mode system software controls the NCO/SS block by controlling the value of the 40-bit FREQZ field in the DFREQZ registers. The resolution of frequency control is better than 0.01 ppb.

The nominal FREQZ value, hereafter referred to as FREQZ0, is computed by the evaluation software for the desired device configuration When the FREQZ field is set to the FREQZ0 value, the device's output clock frequencies have a fractional frequency offset of zero with respect to the NCO master clock signal applied to the XA pin.

(Fractional frequency offset (FFO) is defined as (actual_frequency – nominal_frequency)/nominal_frequency. FFO is a unitless number but is typically expressed in parts per billion (ppb), parts per million (ppm), or percent.)

To control the NCO, system software first reads the FREQZ0 value from the device. FREQZ0 is a 40-bit unsigned integer.

To change the NCO frequency to a specific FFO (in ppm), system software calculates newFREQZ (a 40-bit unsigned integer) as follows:

EQUATION 5-1:

$$newFREQZ = round(FREQZ0 \times (1 + FFO/1e6))$$

System software then writes the newFREQZ value directly to the FREQZ field in the DFREQZ registers.

Note that any subsequent frequency changes are calculated using the same equation from the original FREQZ0 value and are not a function of the previous newFREQZ value. The value of newFREQZ should be kept within ±1000 ppm of FREQZ0 and within ±500 ppm of the previous newFREQZ value to avoid causing the APLL to lose lock. If spread spectrum modulation is also in use, the total frequency change caused by spread spectrum modulation and NCO control should be kept within ±5000 ppm of FREQZ0 to avoid causing the APLL to lose lock.

5.5.2 SPREAD-SPECTRUM MODULATION MODE

For EMI-sensitive applications, the device can perform spread spectrum modulation (SSM). In SSM the frequency of the output clock is continually varied over a narrow frequency range to spread the energy of the signal and thereby reduce EMI. This mode is a special case of NCO mode.

The NCO/SS block operates in spread spectrum mode when NCSSCR1.MODE=0010. In this mode the NCO/SS block performs frequency modulation starting from a base frequency offset specified in the 40-bit FREQZ field in the DFREQZ registers. The frequency modulation is triangle-wave center-spread of up to ±0.5% deviation from the center frequency with modulation rate configurable from 25 kHz to 55 kHz. The nominal value of FREQZ and the spread configuration register values are determined by the evaluation software.

Down-spread applications can be supported by converting them into center-spread. This is done by setting the NCO/SS block's center frequency to be the center of the modulation range rather than the high end of range. For example, 100 MHz with 1% down-spread can be converted into ±0.5% center spread with center frequency of 100 MHz/1.005 = 99.502488 MHz.

5.6 APLL Configuration

5.6.1 APLL INPUT SELECTION AND FREQUENCY

The APLL can lock to any of inputs IC1 through IC3, a clock signal on XA (optionally clock-doubled), or the crystal driver circuit (optionally clock-doubled) when a crystal is connected to XA and XB. The APLL can also lock to the output of the NCO/SS block (see Section 5.5).

The input to the APLL can be controlled by a GPIO pin or by the APLLCR3.APLLMUX register field. When APLLCR3.EXTSW=0, the APLLCR3.APLLMUX register field controls the APLL input mux.

When APLLCR3.EXTSW=1, a GPIO pin controls the APLL input mux. When the GPIO pin is low, the mux selects the input specified by APLLCR3.APLLMUX. When the GPIO pin is high, the mux selects the input specified by APLLCR3.ALTMUX. MCR2.EXTSS specifies which GPIO pin controls this behavior.

In APLL-only mode, the frequencies of all enabled input clocks (ICx and XA) must divide to a common APLL phase-frequency detector (PFD) frequency from 9.72 MHz to 156.25 MHz. In this mode the input high-speed dividers (ICxCR1.HSDIV) can be used to divide the ICx frequencies by 1, 2, 4, or 8. The XA pin does not have an internal divider, and, therefore, if XA is an enabled input clock then the XA frequency sets the APLL common PFD frequency. The polarity of an ICx input signal can be inverted by setting ICxCR1.POL.

5.6.2 APLL OUTPUT FREQUENCY

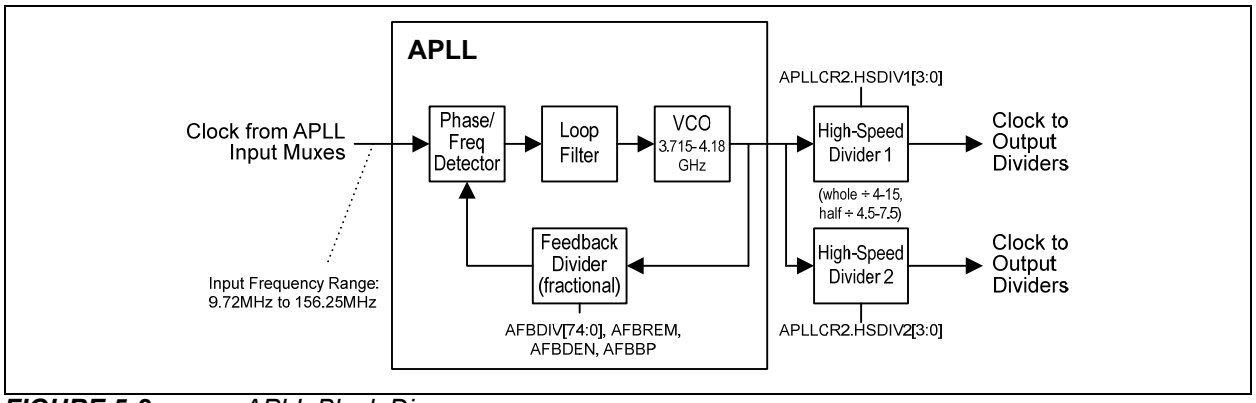


FIGURE 5-2: *APLL Block Diagram.*

The APLL is enabled when PLLEN.APLLEN=1. The APLL has a fractional-N architecture and therefore can produce output frequencies that are either integer or non-integer multiples of the input clock frequency. Figure 5-2 shows a block diagram of the APLL, which is built around an ultra-low-jitter multi-GHz VCO. Register fields AFBDIV, AFBREM, AFBDEN, and AFBBP configure the frequency multiplication ratio of the APLL. The APLLCR2.HSDIV1 and HSDIV2 fields specify how the VCO frequency is divided down by the high-speed dividers. Dividing by six is the typical setting to produce 622.08 MHz for SDH/SONET or 625 MHz for Ethernet applications.

Internally, the exact APLL feedback divider value is expressed in the form AFBDIV + AFBREM/AFBDEN * $2^{-(33-AFBBP)}$. This feedback divider value must be chosen such that APLL_input_frequency * feedback_divider_value is in the operating range of the VCO (as specified in Table 7-9). The AFBDIV term is a fixed-point number with 9 integer bits and a

configurable number of fractional bits (up to 33, as specified by AFBBP). Typically AFBBP is set to 9 to specify that AFBDIV has 33 – 9 = 24 fractional bits. Using more than 24 fractional bits does not yield a detectable benefit. Using less than 12 fractional bits is not recommended.

The following equations show how to calculate the feedback divider values for the situation where the APLL should multiply the APLL input frequency by integer M and also fractionally scale by the ratio of integers N/D. In other words, VCO_frequency = input_frequency * M * N/D. An example of this is multiplying 77.76 MHz by M=48 and scaling by N/D = 255/237 for forward error correction applications.

1. AFBDIV = trunc(M * N/D * 224)
2. lsb_fraction = M * N/D * 224 – AFBDIV
3. AFBDEN = D
4. AFBREM = round(lsb_fraction * AFBDEN)
5. AFBBP = 33 – 24 = 9

The trunc() function returns only the integer portion of the number. The round() function rounds the number to the nearest integer. In Equation (1), AFBDIV is set to the full-precision feedback divider value, M * N/D, truncated after the 24th fractional bit. In Equation (2) the temporary variable 'lsb_fraction' is the fraction that was truncated in Equation (1) and therefore is not represented in the AFBDIV value. In Equation (3), AFBDEN is set to the denominator of the original M * N/D ratio. In Equation (4), AFBREM is calculated as the integer numerator of a fraction (with denominator AFBDEN) that equals the 'lsb_fraction' temporary variable. Finally, in Equation (5) AFBBP is set to 33 – 24 = 9 to correspond with AFBDIV having 24 fractional bits.

When a fractional scaling scenario involves multiplying an integer M times multiple scaling ratios N1/D1 through Nn/Dn, the equations above can still be used if the numerators are multiplied together to get N = N1 x N2 x … x Nn and the denominators are multiplied together to get D = D1 x D2 x … x Dn.

The easiest way to calculate the exact values to write to the APLL registers is to use the ZL3025x evaluation software, available on the Microchip website. This software can be used even when no evaluation board is attached to the computer.

Note: After the APLL's feedback divider settings are configured in register fields AFBDIV, AFBREM, AFBDEN and AFBBP, the APLL enable bit PLLEN.APLLEN should be changed from 0 to 1 to cause the APLL to reacquire lock with the new settings. The real-time lock/unlock status of the APLL is indicated by APLLSR.ALK and ALK2.

5.6.3 APLL PHASE ADJUSTMENT

The phase of the APLL’s output clock can be incremented or decremented by 1/8th of a VCO cycle. This phase step size is 30ps at maximum VCO frequency of 4180 MHz and 33.7 ps at minimum VCO frequency of 3715 MHz. The APLLCR4.PDSS field specifies the phase decrement control signal, which can be the APLLCR4.DECPH bit or any of the four GPIOs. The APLLCR4.PISS field specifies the phase increment control signal, which can be the APLLCR4.INCPH bit or any of the four GPIOs. Phase is adjusted on every rising edge and every falling edge of the control signal. This phase adjustment affects the output of both high-speed dividers.

5.7 Output Clock Configuration

The device has three output clock signal pairs. Each output has individual divider, enable and signal format controls. In CMOS mode each signal pair can become two CMOS outputs, allowing the device to have up to six output clock signals. Also in CMOS mode, the OCxN pin can have an additional divider allowing the OCxN frequency to be an integer divisor of the OCxP frequency (example: OC3P 125 MHz and OC3N 25 MHz). The outputs can be aligned relative to each other and relative to an input signal, and the phases of output signals can be adjusted dynamically with high resolution and infinite range.

5.7.1 OUTPUT ENABLE, SIGNAL FORMAT, VOLTAGE, AND INTERFACING

To use an output, the output driver must be enabled by setting OCxCR2.OCSF≠0, and the per-output dividers must be enabled by setting the appropriate bit in the OCEN register. The per-output dividers include the medium-speed divider, the low-speed divider and the associated phase adjustment/alignment circuitry and start/stop logic.

Using the OCxCR2.OCSF register field, each output pair can be disabled or configured as a CML output, an HSTL output, or one or two CMOS outputs. When an output is disabled it is high impedance, and the output driver is in a low-power state. In CMOS mode, the OCxN pin can be disabled, in phase or inverted vs. the OCxP pin. In CML mode the normal 800 mV V_{OD} differential voltage is available as well as a half-swing 400 mV V_{OD}. All of these options are specified by OCxCR2.OCSF. The clock to the output driver can inverted by setting OCxCR2.POL=1. The CMOS/HSTL output driver can be set to any of four drive strengths using OCxCR2.DRIVE.

Each output has its own power supply pin to allow CMOS or HSTL signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components. If OCSF is set to HSTL mode then a 1.5V power supply voltage should be used to get a standards-compliant HSTL output. Note that differential (CML) outputs must have a power supply of 3.3V.

The differential outputs can be easily interfaced to LVDS, LVPECL, CML, HCSL, HSTL, and other differential inputs on neighboring ICs using a few external passive components. See Figure 7-4 for examples.

5.7.2 OUTPUT FREQUENCY CONFIGURATION

The frequency of each output is determined by the configuration of the APLL, the high-speed dividers and the per-output dividers. Each output can be connected to either high-speed divider 1 (HSDIV1) or 2 (HSDIV2) using the OCxCR3.DIVSEL field.

Each output has two output dividers, a 7-bit medium-speed divider (OCxCR1.MSDIV) and a 25-bit low-speed output divider (LSDIV field in the OCxDIV registers). These dividers are in series, medium-speed divider first then output divider. These dividers produce signals with 50% duty cycle for all divider values including odd numbers. The low-speed divider can only be used if the medium-speed divider is used (i.e. OCxCR1.MSDIV>0). The maximum input frequency to the medium-speed divider is 850 MHz. The maximum input frequency to the low-speed divider is 425 MHz.

Because each output has its own independent dividers, the device can output families of related frequencies that have an APLL HSDIV output frequency as a common multiple. For example, for Ethernet clocks, a 625 MHz HSDIV output clock can be divided by four for one output to get 156.25 MHz, divided by five for another output to get 125 MHz, and divided by 25 for another output to get 25 MHz. Similarly, for SDH/SONET clocks, a 622.08 MHz HSDIV output clock can be divided by 4 to get 155.52 MHz, by 8 to get 77.76 MHz, by 16 to get 38.88 MHz or by 32 to get 19.44 MHz.

Two Different Frequencies in 2xCMOS Mode

When an output is in 2xCMOS mode it can be configured to have the frequency of the OCxN clock be an integer divisor of the frequency of the OCxP clock. Examples of where this can be useful:

- 125 MHz on OCxP and 25 MHz on OCxN for Ethernet applications
- 77.76 MHz on OCxP and 19.44 MHz on OCxN for SONET/SDH applications
- 25 MHz on OCxP and 1 Hz (i.e. 1PPS) on OCxN for telecom applications with Synchronous Ethernet and IEEE1588 timing

An output can be configured to operate like this by setting the LSDIV value in the OCxDIV registers to OCxP_freq/OCxN_freq – 1 and setting OCxCR3.LSSEL=0 and OCxCR3.NEGLSD=1. Here are some notes about this dual-frequency configuration option:

- In this mode only the medium speed divider is used to create the OCxP frequency. The low-speed divider is then used to divide the OCxP frequency down to the OCxN frequency. This means that the lowest OCxP frequency is the high-speed divider output frequency divided by 128.
- An additional constraint is that the medium-speed divider must be configured to divide by 6 or more (i.e. must have OCxCR1.MSDIV≥5).

5.7.3 OUTPUT DUTY CYCLE ADJUSTMENT

For output frequencies less than or equal to 141.666 MHz, the duty cycle of the output clock can be modified using the OCxDC.OCDC register field. This behavior is only available when MSDIV>0 and LSDIV > 1. When OCDC = 0 the output clock is 50%. Otherwise the clock signal is a pulse with a width of OCDC number of MSDIV output clock periods. The range of OCDC can create pulse widths of 1 to 255 MSDIV output clock periods. When OCxCR2.POL=0, the pulse is high and the signal is low the remainder of the cycle. When POL=1, the pulse is low and the signal is high the remainder of the cycle.

Note that duty cycle adjustment is done in the low-speed divider. Therefore, when OCxCR3.LSSEL=0 the duty cycle of the output is not affected. Also, when a CMOS output is configured with OCxCR3.LSSEL=0 and OCxCR3.NEGLSD=1, the OCxN pin has duty cycle adjustment but the OCxP pin does not. This allows a higher-speed 50% duty cycle clock signal to be output on the OCxP pin and a lower-speed frame/phase/time pulse (e.g. 2 kHz, 8 kHz, or 1PPS) to be output on the OCxN pin at the same time.

An output configured for CMOS or HSTL signal format should not be configured to have a duty cycle with high time shorter than 2 ns or low time shorter than 2 ns.

5.7.4 OUTPUT PHASE ADJUSTMENT AND PHASE ALIGNMENT

The device has flexible, high-resolution tools for managing the phases of the output clocks relative to one another. The key register fields for this are found in the PACR1 and PACR2 global configuration registers and the per-output OCxPH register.

Phase alignment and phase adjustment are done in the medium-speed dividers. Resolution is 0.5 periods (also known as unit intervals or UI) of the high-speed divider (HSDIV) output clock. For example, for an HSDIV output frequency of 800 MHz, resolution is 625 ps.

5.7.4.1 Phase Adjustment

A phase adjustment is a phase change for an output relative to that output's most recent phase. To cause the device to perform phase adjustment of an output clock, set PACR1.MODE=1, set OCxCR1.PHEN=1 to enable the output for phase adjustment, and write the phase adjustment amount to the output's OCxPH register. Then an arm/trigger methodology is used to cause the phase adjustment to happen.

The arm step tells the device that it is enabled to perform the phase adjustment when it sees the trigger stimulus. The source of the arm signal is specified by PACR2.ARMSRC. Options include the 0-to-1 transition of the PACR1.ARM bit, APLL transition from unlocked to locked, or a transition on one of the GPIO pins.

The source of the trigger signal is specified by PACR2.TRGSRC. Options include 0-to-1 transition of the PACR1.TRIG bit, APLL transition from unlocked to locked, or a transition on one of the GPIO pins. The trigger signal can be inverted by setting PACR1.TINV. With TINV=1, the same GPIO signal can arm on one edge and trigger on the opposite edge.

Any combination of outputs can be phase adjusted by the same trigger, and each output can be adjusted by a different amount. Only outputs with OCxCR1.PHEN=1 and OCxPH.PHADJ≠0 have their phases adjusted.

There are a few constraints on the range of possible phase adjustments. These have to do with the output's medium-speed divider value.

1. Phase adjustment is not available unless OCxCR1.MSDIV>0.
2. The largest negative phase adjustment magnitude in HSDIV periods is:

   If OCxCR1.MSDIV is odd: (OCxCR1.MSDIV – 1)/2

   If OCxCR1.MSDIV is even: (OCxCR1.MSDIV – 2)/2
3. The largest positive phase adjustment in HSDIV periods is:

   If OCxCR1.MSDIV is odd: (127 – OCxCR1.MSDIV)/2

   If OCxCR1.MSDIV is even: (128 – OCxCR1.MSDIV)/2

The implications of constraints 2) and 3) are shown in this table:

OCxCR1.MSDIV	Largest Negative Phase Adjust, HSDIV periods	Largest Positive Phase Adjust, HSDIV periods	Notes
1 or 2	0	63	No negative adjustment.
3 or 4	1	62	—
5 or 6	2	61	—
...	...	...	—
123 or 124	61	2	—
125 or 126	62	1	—
127	63	0	No positive adjustment.

During a phase adjustment the MSDIV output period is changed for one period. The MSDIV output signal during that period will have longer high time (unless inverted) during a positive phase adjustment and shorter high time (unless inverted) during a negative phase adjustment. With negative phase adjustments care must be taken to not shorten the high time of the output clock signal to be too short for the components that receive the clock. There are several possible ways to avoid this issue including: (1) using small negative adjustments such as –0.5 UI repeatedly instead of one larger negative adjustment, (2) using positive adjustments to “wrap around” to the desired negative adjustment, or (3) holding the components that receive the clock in reset during the phase adjustment.

An armed phase adjustment can be canceled before the trigger occurs by setting the PACR1.RST bit.

The PASR register has real-time status bits indicating whether a phase adjustment is armed and waiting for a trigger (ARMED bit) or in progress (BUSY bit). It also has a latched status bit (ADJL bit) to indicate the adjustment has completed.

Example: +1.0 HSDIV period phase adjustment for output OC1 using ARM and TRIG register bits:

OC1CR1.PHEN=1 (Enable phase adjust on OC1)

OC1PH.PHADJ=00000010 (Specify +1.0 HSDIV period phase adjustment)

PACR1.MODE=1 (Phase adjustment mode)

PACR2.ARMSRC=0001 (arm signal is PACR1.ARM bit)

PACR2.TRGSRC=0000 (trigger signal is PACR1.TRIG bit)

PACR1.RST=1 (reset phase adjust/align state machine after changing ARMSRC)

PACR1.ARM=1 (arm for phase adjust)

PACR1.TRIG=1 (do the phase adjust: add +1.0 UI to output phase)

repeat the next two writes as needed:

PACR1.ARM=1 .TRIG=0 (arm again; clearing the TRIG bit is required when MSDIV period < master clock period because TRIG is not self-clearing in this situation)

PACR1.TRIG=1 (add +1.0 UI to output phase again)

5.7.4.2 Phase Alignment, Output-to-Output

A phase alignment is a special case of phase adjustment where the MSDIV and LSDIV dividers for all participating outputs are reset just before the phase adjustment occurs. For output-to-output alignment the trigger can be the PACR1.TRIG bit or the APLL lock signal.

To avoid glitches (i.e. “runt pulses”) on the output clock it is possible to manually stop the output(s), before triggering the phase alignment, and then restart the output(s) after the alignment (See Section 5.7.5).

When aligning outputs, it is important to note that, by default, the phase of outputs configured as HSTL format or “two CMOS, OCxP inverted vs. OCxN” format is opposite that of CML outputs. For example, consider the case where OC1 is 100MHz CML format and OC2 is 100MHz HSTL format. When OC1 and OC2 are aligned then OC2N is high when OC1P is high. The polarity bit OCxCR2.POL can be used to change this as needed.

There are several rules when alignment is enabled for multiple outputs:

- All participating outputs must come from the same high-speed divider
- All outputs that use both medium-speed and low-speed divider must have the same MSDIV value, the same LSDIV value and PHADJ=0. Subsequent phase adjustment(s) can be used to move the output(s) to other phase(s).
- All outputs that only use medium-speed divider can have PHADJ values smaller than the period of the highest output frequency among them.
- When some outputs use only medium-speed divider and other outputs use both medium-speed and low-speed divider, all MSDIV values must be the same, and those output using low-speed divider must have PHADJ=0.

Contact Microchip Timing Applications Support for help with alignment scenarios that don’t meet the rules listed above.

Example: OC1-to-OC2 alignment (+3.5 HSDIV UI offset) after the APLL locks:

OC1CR1.PHEN=1 (Enable phase adjust on OC1)

OC2CR1.PHEN=1 (Enable phase adjust on OC2)

OC1PH.PHADJ=00000000 (0.0UI)

OC2PH.PHADJ=00000111 (+3.5UI)

PACR1.MODE=0 (Phase alignment mode)

PACR2.ARMSRC=0001 (arm signal is PACR1.ARM bit)

PACR2.TRGSRC=0001 (trigger signal is APLL transition from unlocked to locked)

PACR1.RST=1 (reset phase adjust/align state machine after changing ARMSRC, TRGSRC)

PACR1.ARM=1 (arm for phase alignment)

(Aligns/realigns outputs when the APLL locks or relocks)

5.7.4.3 Phase Alignment, Input-to-Output

The phase alignment tool described in Section 5.7.4.2 can use a GPIO pin as the alignment trigger. However there is some uncertainty associated with sampling the GPIO signal. Therefore the phase alignment tool by itself is not sufficient to achieve input-to-output phase alignment. The procedure is to first do a phase alignment as described in Section 5.7.4.2 but with a GPIO input as the trigger. Then the phase measurement tool described in Section 5.7.6 can be used to determine the phase difference between an output signal and the input signal. Then phase adjustment as described in Section 5.7.4.1 can be used to change the phase of one or more output signals to align with input signal phase.

It is important to note that, by default, outputs that only use the medium-speed divider have their rising edge aligned with the rising edge of the trigger signal. Meanwhile, outputs that use both the medium-speed and low-speed dividers have their rising edge aligned with the falling edge of the trigger signal. Per-output polarity bits (OCxCR2.POL) can be used to invert the polarity of output signals as needed so that all are rising-edge aligned or falling-edge aligned or any combination as needed.

5.7.5 OUTPUT CLOCK START AND STOP

Output clocks can be stopped high or low. One use for this behavior is to ensure “glitchless” output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an OCxSTOP register with fields to control this behavior. The OCxSTOP.MODE field specifies whether the output clock signal stops high, stops low, or does not stop. The OCxSTOP.SRC field specifies the source of the stop signal. Options include the OCxSTOP.STOP bit, assertion of one of the GPIO pins, and the arming of a phase adjustment (which is indicate by PASR.ARMED).

When the stop mode is Stop High (OCxSTOP.MODE=01) and the stop signal is asserted, the output clock is stopped after the next rising edge of the output clock. When the stop mode is Stop Low (OCxSTOP.MODE=10) and the stop signal is asserted, the output clock is stopped after the next falling edge of the output clock. Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on. Low-speed output clocks can take long intervals before being stopped after the stop signal goes active. For example, a 1 Hz output could take up to 1 second to stop.

OCxCR1.MSDIV must be > 0 for this function to operate since MSDIV=0 bypasses the start-stop circuits. Note that when OCxCR3.NEGLSD=1 the start-stop logic is bypassed for the OCxN pin, and OCxN may not start/stop without glitches.

When OCxCR2.POL=1 the output stops on the opposite polarity that is specified by the OCxSTOP.MODE field.

When OCxCR2.STOPDIS=1 the output driver is disabled (high impedance) while the output clock is stopped.

Each output has a status register (OCxSR) with several stop/start status bits. The STOPD bit is a real-time status bit indicating stopped or not stopped. The STOPL bit is a latched status bit that is set when the output clock has stopped. The STARTL bit is a latched status bit that is set when the output clock has started.

5.7.6 A-TO-B PHASE OFFSET MEASUREMENT

The phase or time offset between two signals (A and B) can be measured in units of a timebase clock. This capability can be used to for several purposes, including:

- Keeping output clocks and low-speed output phase/time signals—such as frame sync, multiframe sync, or 1 pulse per second (1PPS) signals—aligned with input phase/time signals. The A-to-B measurement circuitry can detect phase changes in the input signal. Then the output phase adjustment circuitry described in Section 5.7.4 can be used to move phase(s) of output(s) to follow the input phase change.
- Keeping output clock signals and/or low-speed output phase/time signals aligned with one another. The A-to-B measurement circuitry can detect relative phase changes, and the phase adjustment circuitry described in Section 5.7.4 can be used to move phase(s) of output(s) as needed.

The A and B signals can be any ICx input, any OCx output, or any GPIO, as specified by MABCR2.ASRC and MABCR3.BSRC. The timebase signal can be the external oscillator signal (or the output of the crystal driver circuit, optionally doubled by the clock doubler) or the output clock of any of the three medium-speed dividers (MSDIV1, MSDIV2, MSDIV3). The timebase signal is specified by MABCR1.TBSRC.

A new measurement is started by writing MABCR1.START=1. Any previously started measurement must be completed before a new measurement is started. If a measurement has not finished it can be aborted by writing MABCR1.RST=1 before starting a new measurement. The measurement is complete when MABSR1.RDYL is set.

Example: consider an SDH/SONET application where OC1 is a 19.44 MHz output clock and OC2 is an 8 kHz frame sync signal. The goal is to measure the phase offset of OC1 vs. OC2. If they are found to have a phase offset then the phase adjustment circuitry in Section 5.7.4 can be used to slowly change the phase of OC1 to match the phase of OC2 (or vice versa).

MABCR1.TBSRC=001	(MSDIV1 output clock is 311.04 MHz = 3.2 ns period)
MABCR2.ASRC=10001	(OC2 8 kHz sync signal)
MABCR3.BSRC=10000	(OC1 19.44 MHz clock)
MABCR1.START=1	(Start measurement)
Wait for MABSR1.RDYL=1	(Measurement ready)
Read MABSR1.OVFL	(to see if the measurement is valid)
MABSR1.RDYL=1, MABSR1.OVFL=1	(clear latched status bits)
Read MEAS bits from MABSR1 and MABSR2	

If, for example, MEAS = 111 1111 1001 (–8) then the rising edge of OC1 (the ‘B’ signal) precedes the rising edge of OC2 (the ‘A’ signal) by 8 MSDIV1 output clock periods (25.7 ns).

An A-to-B measurement is performed by sampling the A and B signals with the selected timebase clock and detecting the rising or falling edges to measure. The number of timebase clocks between the A and B edges is counted. If the counter doesn’t overflow then the phase difference is reported in the MEAS field in MABSR1 and MABSR2. If the counter does overflow then MABSR1.OVFL is set and the value of MEAS is invalid.

While the measurement is in progress the MABSR1.BUSY bit is set to 1. When the measurement is complete MABSR1.BUSY is set to 0 and MABSR1.RDYL is set to 1. Because the A and B signals are sampled by the timebase signal, this measurement tool is only useful when the timebase signal is much higher frequency than the A and B signals (at least 8-10x). Also, when possible, the timebase signal frequency should be less than or equal to 1000 times faster than the frequencies of the A and B frequencies to avoid measurement counter overflow.

Constraints on A-to-B measurement:

- $f_B = f_A \times N$
  - where f_A is the frequency of signal A, f_B is the frequency of signal B, and N is a positive integer

When measuring from an ICx input or a GPIO (signal A) to an ICx or a GPIO (signal B) and when measuring from an OCx output to an OCx output, the measured value is MEAS * timebase_period. This measurement has a variability of 0 to +1 timebase clock period.

When measuring from an ICx input or a GPIO (signal A) to an OCx output (signal B), the measurement in time units is MEAS * timebase_period + 6 * HSCLK_period, where HSCLK_period is the period of the output of the high-speed divider from which OCx signal is derived. This measurement has a variability of 0 to +1 timebase clock period plus 0 to +1 HSCLK periods.

When measuring from an OCx output (signal A) to an ICx input or a GPIO (signal B), the measurement in time units is MEAS * timebase_period – 6 * HSCLK_period, where HSCLK_period is the period of the output of the high-speed divider from which OCx signal is derived. This measurement has a variability of 0 to +1 timebase clock period plus 0 to +1 HSCLK periods.

Guidance for Use

When the A and B signals are aligned to within one timebase clock cycle, the measurement hardware does not report 0. Instead it reports a measurement value that is equivalent to +1 cycle of signal B.

If the timebase clock is ≤ 1023 times faster than signal B (so that the MEAS field cannot overflow, unless signal B is grossly too slow or not toggling at all) then system software should check the measured phase value. If the measured value is equal to the period of signal B then the A and B signals are aligned.

If the timebase clock is 1024 to 2047 times faster than signal B (and therefore the measurement counter can overflow) then the measurement hardware reports overflow when the A and B signals are aligned to within one timebase clock cycle. This report of overflow can be distinguished from other overflow cases by setting MABCR3.BINV=1 and then remeasuring from signal A to the opposite edge of signal B. If the new measured value is equal to half the period of signal B then the A and B signals are aligned.

If the timebase clock is > 2047 times faster than signal B then the measurement hardware reports overflow when the A and B signals are aligned to within one timebase clock cycle. This report of overflow is not distinguishable from other overflow cases. One way system software could work around this to determine that A and B are aligned is to use phase adjustment to move one of the signals by 2 or more timebase clocks then remeasure. If the new measured value matches the phase adjustment then the signals were aligned before the phase adjustment. Software can then adjust the phase of the signal back to its original position. Not all applications can tolerate such phase adjustments; for those applications it is recommended that the timebase clock be ≤ 2047 times faster than signal B.

5.8 Microprocessor Interface

The device can communicate over a SPI interface or an I^2C interface.

In SPI mode, the ZL30250 can be configured at reset to be a SPI client to a processor server or a SPI server to an external EEPROM client. The ZL30251 can only be configured as a SPI client to a processor server. Both devices are always clients on the I^2C bus.

Section 5.2 describes reset pin settings required to configure the device for these interfaces.

5.8.1 SPI CLIENT

The device can present a SPI client port on the CSN, SCLK, MOSI,, and MISO pins. SPI is a widely used server/client bus protocol that allows a server and one or more clients to communicate over a serial bus. SPI servers are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the server, which also generates the SCLK signal. The device receives serial data on the MOSI (Server Out Client In) pin and transmits serial data on the MISO (Server In Client Out) pin. MISO is high impedance except when the device is transmitting data to the bus server.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MOSI on the rising edge of SCLK and updates data on MISO on the falling edge of SCLK. SCLK does not have to toggle between accesses, i.e., when CSN is high.

Device Selection. Each SPI device has its own chip-select line. To select the device, the bus server drives its CSN pin low.

Command and Address. After driving CSN low, the bus server transmits an 8-bit command followed by a 16-bit register address. The available commands are shown below.

TABLE 5-6: SPI COMMANDS

Command	Hex	Bit Order, Left to Right
Write Enable	0x06	0000 0110
Write	0x02	0000 0010
Read	0x03	0000 0011
Read Status	0x05	0000 0101

Read Transactions. The device registers are accessible when EESEL=0. On a ZL30251, the internal EEPROM memory is accessible when EESEL=1. On a ZL30250, EESEL must be set to 0. After driving CSN low, the bus server transmits the read command followed by the 16-bit address. The device then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the bus server continues to demand data, the device continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the bus server drives CSN high. See Figure 5-3.

Register Write Transactions. The device registers are accessible when EESEL=0. After driving CSN low, the bus server transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device receives the first data byte on MOSI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the server continues to transmit, the device continues to write the data received and increment its address counter. The write transaction is completed when the bus server drives CSN high. See Figure 5-5.

EEPROM Writes (ZL30251 Only). The internal EEPROM memory is accessible when EESEL=1. After driving CSN low, the bus server transmits the write enable command and then drives CSN high to set the internal write enable latch. The bus server then drives CSN low again and transmits the write command followed by the 16-bit address followed by the first data byte to be written. The device first copies the page to be written from EEPROM to its page buffer. The device then receives the first data byte on MOSI, writes it to its page buffer, increments its internal address register, and prepares to receive the next data byte. If the server continues to transmit, the device continues to write the data received to its page buffer and continues to increment its address counter. The address counter rolls over at the 32-byte page boundary (i.e. when the five least-significant address bits are 11111). When the bus server drives CSN high, the device transfers the data in the page buffer to the appropriate page in the EEPROM memory. See Figure 5-4 and Figure 5-5.

EEPROM Read Status (ZL30251 Only). After the bus server drives CSN high to end an EEPROM write command, the EEPROM memory is not accessible for up to 5 ms while the data is transferred from the page buffer. To determine when this transfer is complete, the bus server can use the Read Status command. After driving CSN low, the bus server transmits the Read Status command. The device then responds with the status byte on MISO. In this byte, the least significant bit is set to 1 if the transfer is still in progress and 0 if the transfer has completed.

Early Termination of Bus Transactions. The bus server can terminate SPI bus transactions at any time by pulling CSN high. In response to early terminations, the device resets its SPI interface logic and waits for the start of the next transaction. If a register write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, the data byte is not written. On ZL30251, if an EEPROM write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, none of the bytes in that write transaction are written.

Design Option: Wiring MOSI and MISO Together. Because communication between the bus server and the device is half-duplex, the MOSI and MISO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the MOSI/MISO line when the device is transmitting.

AC Timing. See Table 7-14 and Figure 7-6 for AC timing specifications for the SPI interface.

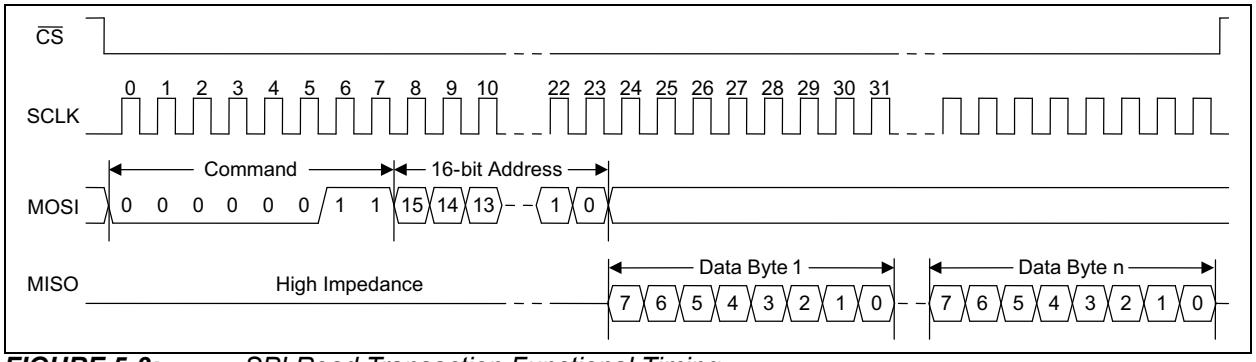


FIGURE 5-3: *SPI Read Transaction Functional Timing.*

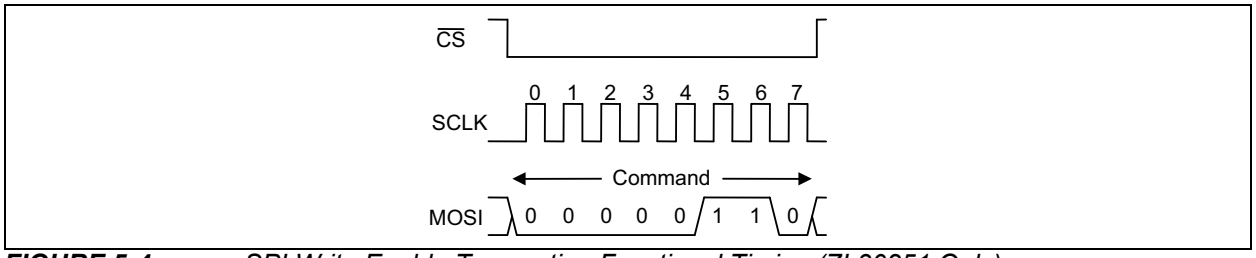


FIGURE 5-4: *SPI Write Enable Transaction Functional Timing (ZL30251 Only).*

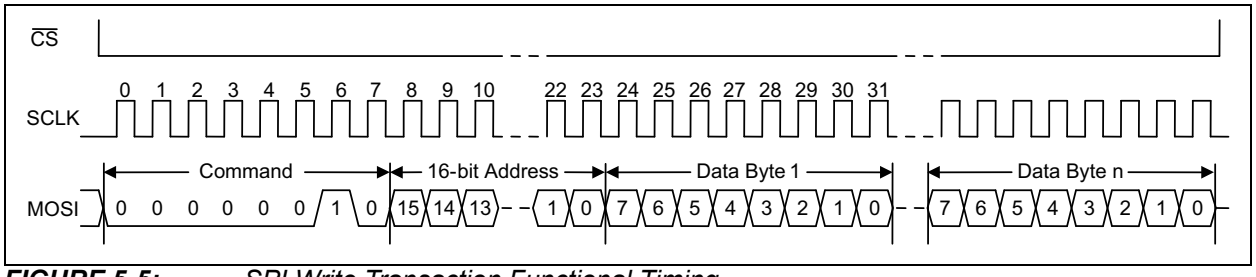


FIGURE 5-5: *SPI Write Transaction Functional Timing.*

5.8.2 SPI SERVER (ZL30250 ONLY)

After reset the ZL30250 can present a SPI server port on the CSN, SCLK, MOSI, and MISO pins for auto-configuration using data read from an external SPI EEPROM. During auto-configuration the device is always the SPI server and generates the CSN and SCLK signals. The device transmits serial data on the MOSI (Server Out Client In) pin and receives serial data on the MISO (Server In Client Out) pin.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MISO on the rising edge of SCLK and updates data on MOSI on the falling edge of SCLK.

Device Selection. Each SPI device has its own chip-select line. To select the external EEPROM, the device drives the CSN signal low.

Command and Address. After driving CSN low, the device transmits an 8-bit read command followed by a 16-bit register address. The read command is shown below.

Command	Hex	Bit Order, Left to Right
Read	0x03	0000 0011

Read Transactions. After driving CSN low, the device transmits the read command followed by the 16-bit register address. The external EEPROM then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the device continues to demand data, the EEPROM continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the device drives CSN high. See Figure 5-3.

Writing the External EEPROM. Due to the small package size and low pin count of the device, there is no way to use the ZL30250 to write the external EEPROM. The auto-configuration data used by the ZL30250 must be pre-programmed into the EEPROM by some other method, such as:

1. The EEPROM manufacturer can write the data to the EEPROM during production testing. This is a service they routinely provide.
2. A contract manufacturer or distributor can write the data to the EEPROM using a production EEPROM programmer before the EEPROM is mounted to the board.

5.8.3 I^2C CLIENT

The device can present a fast-mode (400 kbit/s) I^2C client port on the SCL and SDA pins. I^2C is a widely used server/client bus protocol that allows one or more servers and one or more clients to communicate over a two-wire serial bus. I^2C servers are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the server, which also generates the SCL signal. The device is compliant with version 2.1 of the I^2C specification.

The I^2C interface on the device is a protocol translator from external I^2C transactions to internal SPI transactions. This explains the slightly increased protocol complexity described in the paragraphs that follow.

Read Transactions. The device registers are accessible when EESEL=0. On a ZL30251 the internal EEPROM memory is accessible when EESEL=1. On ZL30250 EESEL must be set to 0. The bus server first does an I^2C write to the device. In this transaction, three bytes are written: the SPI Read command (see Table 5-6), the upper byte of the register address, and the lower byte of the register address. The bus server then does an I^2C read. During each acknowledge (A) bit the device fetches data from the read address and then increments the read address. The device then transmits the data to the bus server during the next 8 SCL cycles. The bus server terminates the read with a not-acknowledge (NA) followed by a STOP condition (P). See Figure 5-6. Note: If the I^2C write is separated in time from the I^2C read by other I^2C transactions then the device only outputs the data value from the first address and repeats that same data value after each acknowledge (A) generated by the bus server.

Register Write Transactions. The device registers are accessible when EESEL=0. The bus server does an I^2C write to the device. The first three bytes of this transaction are the SPI Write command (see Table 5-6), the upper byte of the register address, and the lower byte of the register address. Subsequent bytes are data bytes to be written. After each data byte is received, the device writes the byte to the write address and then increments the write address. The bus master terminates the write with a STOP condition (P). See Figure 5-7.

EEPROM Writes (ZL30251 Only). The EEPROM memory is accessible when EESEL=1. The bus server first does an I^2C write to transmit the SPI Write Enable command (see Table 5-6) to the device. The bus server then does an I^2C write to transmit data to the device as described in the Register Write Transactions paragraph above. See Figure 5-8.

EEPROM Read Status (ZL30251 Only). The bus server first does an I²C write to transmit the SPI Read Status command (see Table 5-6) to the device. The bus server then does an I²C read to get the status byte. In this byte, the least significant bit is set to 1 if the transfer is still in progress and 0 if the transfer has completed. See Figure 5-9.

I²C Features Not Supported by the Device. The I²C specification has several optional features that are not supported by the device. These are: 3.4 Mbit/s high-speed mode (Hs-mode), 10-bit device addressing, general call address, software reset, and device ID. The device does not hold SCL low to force the server to wait.

I²C Client Address. The device's 7-bit client address can be pin-configured for any of three values. These values are show in the table in Section 5.2.

Bit Order. The I²C specification requires device address, register address, and all data bytes to be transmitted most significant bit first on the SDA signal.

Note: as required by the I²C specification, when power is removed from the device, the SDA and SCL pins are left floating so they don't obstruct the bus lines.

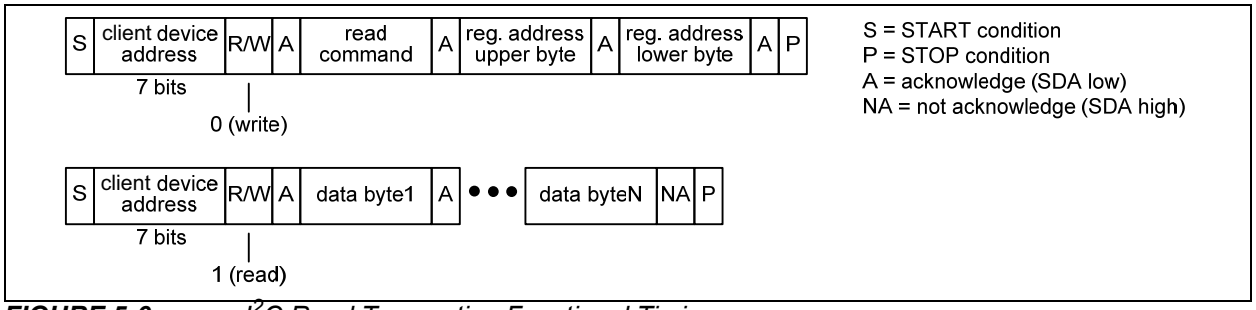


FIGURE 5-6: *I²C Read Transaction Functional Timing.*

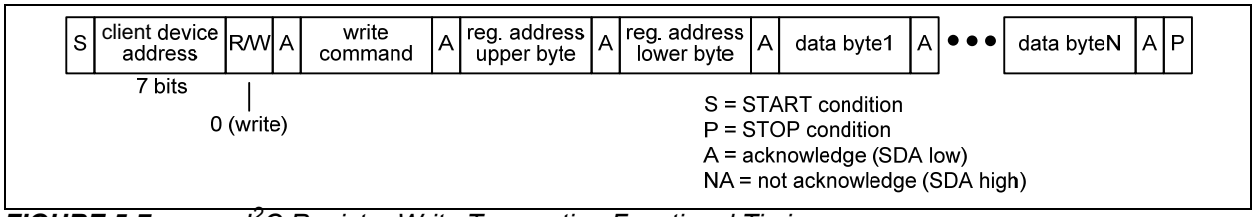


FIGURE 5-7: *I²C Register Write Transaction Functional Timing.*

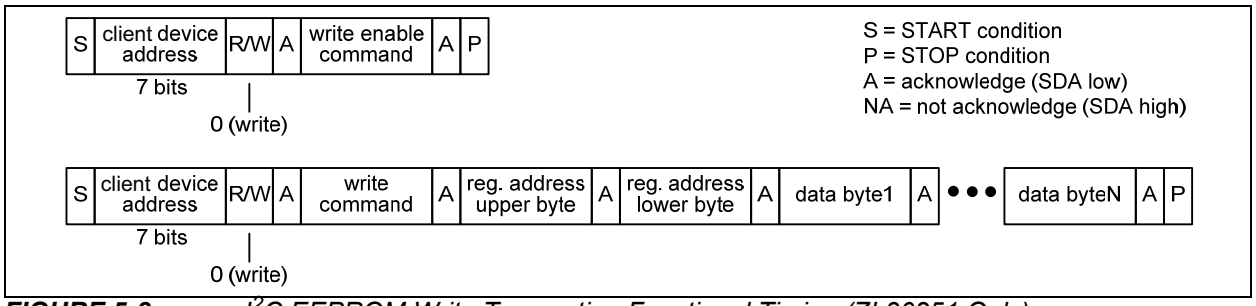


FIGURE 5-8: *I²C EEPROM Write Transaction Functional Timing (ZL30251 Only).*

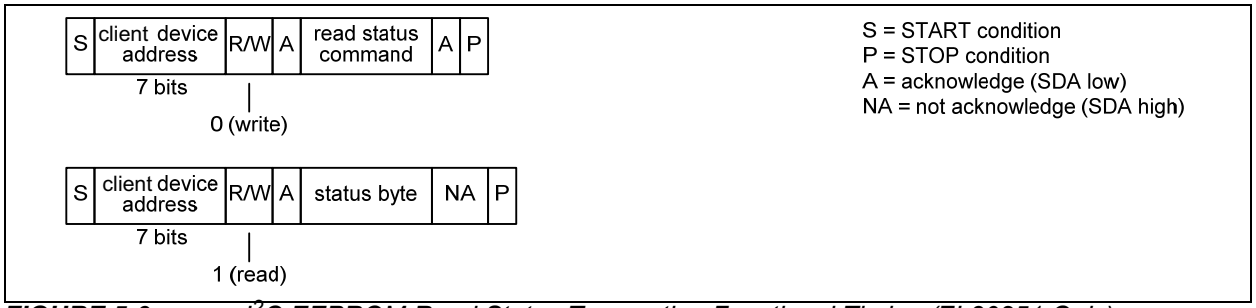


FIGURE 5-9: *I²C EEPROM Read Status Transaction Functional Timing (ZL30251 Only).*

Note: In Figure 5-6 through Figure 5-9, a STOP condition (P) immediately followed by a START condition (S) can be replaced by a repeated START condition (Sr) as described in the I^2C specification.

5.9 Interrupt Logic

Any of the GPIO pins can be configured as an interrupt-request output by setting the appropriate GPIOxC field in the GPIOCR registers to one of the status output options (01xx) and configuring the appropriate GPIOxSS register to follow the INTSR.INT bit. If system software is written to poll rather than receive interrupt requests, then software can read the INTSR.INT bit first to determine if any interrupt requests are active in the device.

Many of the latched status bits in the device can be the source of an interrupt request if their corresponding interrupt enable bits are set. The device's interrupt logic is shown in Figure 5-10. See the register map (Table 6-1) and the status register descriptions in Section 6.3.2 for descriptions of the register bits shown in the figure.

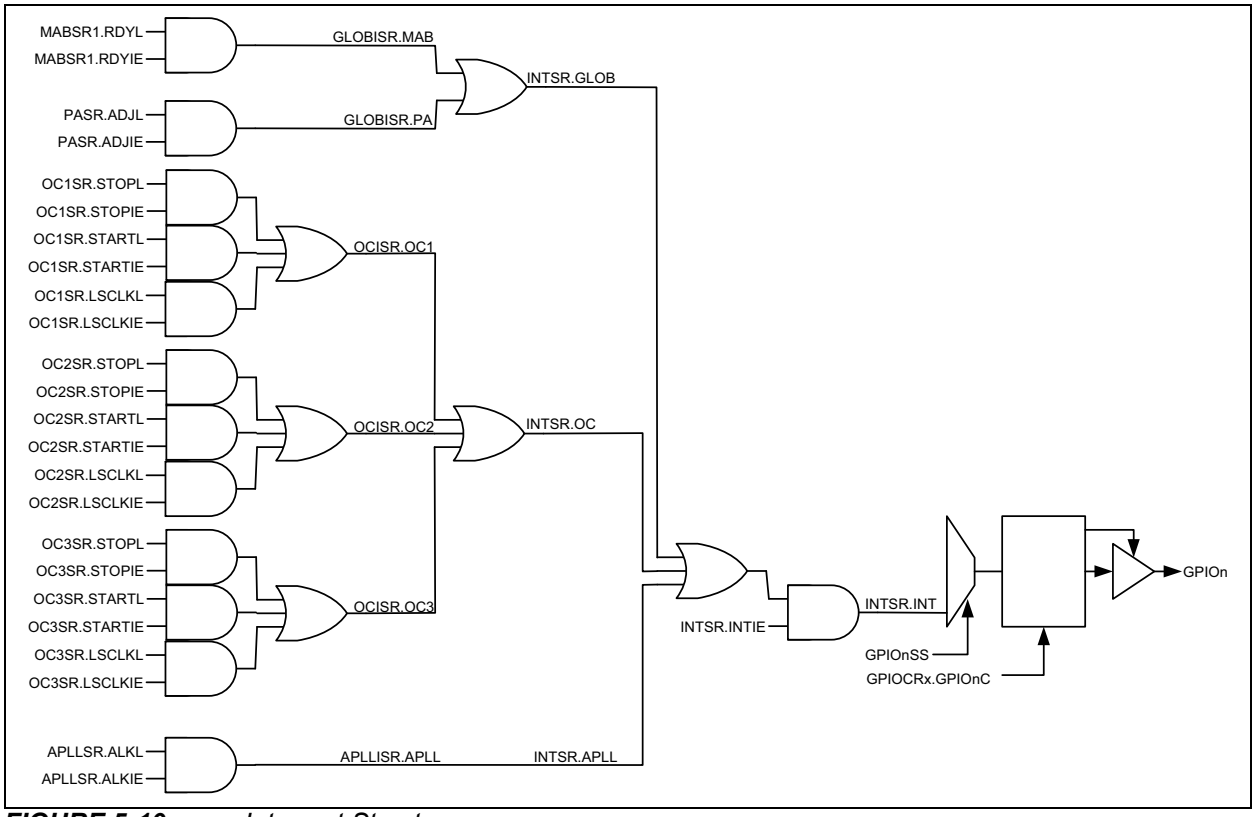


FIGURE 5-10: *Interrupt Structure.*

5.10 Reset Logic

The device has two reset controls: the RSTN pin and the RST bit in MCR1. The RSTN pin asynchronously resets the entire device. When the RSTN pin is low all internal registers are reset to their default values. **The RSTN pin must have one rising edge after power-up.** At initial power-up reset should be asserted for at least 1 µs. During operation, the RSTN assertion time can be as short as 1 µs with one important exception:

> Consider each of these four pins: AC0/GPIO0, AC1/GPIO1, TEST/GPIO2, and IF1/MISO. If (1) the pin could be an output driving high when RSTN is asserted, and (2) an external pull-down resistor is used to set the at-reset value of the pin, then RSTN should be asserted for 100 milliseconds.

The MCR1.RST bit resets the entire device (except for the microprocessor interface and the RST bit itself), but when the RST bit is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead these fields are reset to the default values that were latched when the RSTN pin was last active.

Microchip recommends holding RSTN low while the internal ring oscillator starts up and stabilizes. An incorrect reset condition could result if RSTN is released before the oscillator has started up completely. After the external oscillator or internal crystal driver circuit has been enabled and stabilized, the master clock can be switched from the ring oscillator to the external oscillator using the MCR1.MCSEL bit.

Important: System software must wait at least 100 µs after RSTN is deasserted and wait for GLOBISR.BCDONE=1 before configuring the device.

5.11 Power Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a <3.3V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latch-up. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the <3.3V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop of the <3.3V supply. The second method is to ramp up the 3.3V supply first and then ramp up the <3.3V supply. In some applications VDDOx power supply pins can be at other voltages, such as 2.5V or 1.5V. In these applications the general solution is to ramp up the supplies in order from highest nominal to lowest nominal voltage.

5.12 Auto-Configuration from EEPROM

For the ZL30250, for applications where the device can operate stand-alone without supervision from a processor, the device can configure itself at reset from an external EEPROM connected to its SPI interface. The EEPROM can store up to three configurations, known as configurations 1, 2, and 3. As described in Section 5.2.1, IF[1:0] must be 11 at reset, and the device configuration to be used is specified by the values of the AC[1:0] pins at reset (1, 2, or 3).

For the ZL30251, the internal EEPROM memory can store up to four device configurations, known as configurations 0, 1, 2, and 3. As described in Section 5.2.2, the device configuration to be used is specified by the values of the AC[1:0] pins at reset.

5.12.1 GENERATING DEVICE CONFIGURATIONS

Device configurations must be generated using the evaluation software. This is true for auto-configurations stored in internal or external EEPROM and for configurations that are written to the device by a system processor. The reason for this requirement is that writes to undocumented registers must be done to tune analog circuitry for optimal performance. The writes to be done depend on integer vs. fractional multiplication, device mode and other factors. The registers involved control very low-level device parameters that are difficult to describe and difficult to understand how to use. Instead the evaluation software has all of the expert knowledge built-in to keep configuration easy for the user.

5.12.2 DIRECT EEPROM WRITE MODE (ZL30251 ONLY)

To simplify writing the ZL30251's internal EEPROM during manufacturing, the device has a test mode known as direct EEPROM write mode. The device enters this mode when TEST=1 and AC[1:0]=00 on the rising edge of RSTN. In this mode the EEPROM memory is mapped into the address map and can be written as needed to store configuration scripts in the device. Device registers are not accessible in this mode. The device exits this mode when TEST=0 on the rising edge of RSTN. Note: the device drives the MISO pin continually during this mode. Therefore this mode cannot be used when MOSI and MISO are tied together (as described in the Design Option: Wiring MOSI and MISO Together paragraph in Section 5.8.1).

5.12.3 HOLDING OTHER DEVICES IN RESET DURING AUTO-CONFIGURATION

Using the appropriate GPIOCR and GPIO0SS registers, a GPIO pin can be configured to follow the GLOBISR.BCDONE status bit. This GPIO can then be used as a reset signal to hold other devices (that use clocks from this device) in reset while the device configures itself. As an example, to configure GPIO0 to follow BCDONE with 0=reset add the following writes at the beginning of the configuration file: write 0x1F to GPIO0SS and write 0x04 to GPIOCR1.

5.13 Power Supply Decoupling and Layout Recommendations

Application Note ZLAN-490 describes recommended power supply decoupling and layout practices.

6.0 REGISTER DESCRIPTIONS

The device has an overall address range from 000h to 6FFh. Table 6-1 shows the register map. In each register, bit 7 is the MSb and bit 0 is the LSb. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 6-1.

6.1 Register Types

6.1.1 STATUS BITS

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request if enabled to do so by corresponding interrupt enable bits. Status bits marked "—" are reserved and must be ignored.

6.1.2 CONFIGURATION BITS

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

6.1.3 MULTIREGISTER FIELDS

Multiregister fields—such as FREQZ[39:0] in registers DFREQZ1 through DFREQZ5—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multiregister field is accomplished by writing all the registers of the field in order from smallest address to largest. Writes to registers other than the last register in the field (i.e. the register with the largest address) are stored in a transfer register. When the last register of the field is written, the entire multiregister field is updated simultaneously from the transfer register. If the last register of the field is not written, the field is not updated. Any reads from the multiregister field that occur during the middle of the multiregister write will read the existing value of the field not the new value in the transfer register.

A read access from a multiregister field is accomplished by reading the registers of the field in order from smallest address to largest. When the first register in the field (i.e. the register with the lowest address) is read, the entire multiregister field is copied to the transfer register. During subsequent reads from the other registers in the multiregister field, the data comes from the transfer register. Any writes to the multiregister field that occur during the middle of the multiregister read will overwrite values in the transfer register.

The device has one write transfer register and one read transfer register that it reuses for all multiregister fields. For proper operation system software should be organized such that only one software process accesses the device's registers. If two or more processes are allowed to make uncoordinated accesses to the device's registers, their accesses to multiregister fields could interrupt one another leading to incorrect writes and reads of the multiregister fields.

The multiregister fields are:

Field	Registers	Type
FREQZ[39:0]	DFREQZ1 to DFREQZ5	Read/Write

6.1.4 BANK-SWITCHED REGISTERS (ZL30251 ONLY)

The EESEL register is a bank-select control field that maps the device registers into the memory map at address 0x1 and above when EESEL=0 and maps the EEPROM memory into the memory map at address 0x1 and above when EESEL=1. The EESEL register itself is always in the memory map at address 0x0 for both EESEL=0 and EESEL=1.

6.2 Register Map

TABLE 6-1: REGISTER MAP

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Configuration Registers									
00h	EESEL	—	—	—	—	—	—	—	EESEL
09	MCR1	RST	—	MCSEL1	MCSEL	ROSCD	DBL	XAB[1:0]	
0A	MCR2	—	EXTSS[1:0]		—	—	—	—	—
0B	PLLEN	—	—	—	NCSSEN	—	—	—	APLLEN
0C	ICEN	—	—	—	—	—	IC3EN	IC2EN	IC1EN
0D	OCEN	—	—	—	—	—	OC3EN	OC2EN	OC1EN
0E	GPIOCR1	GPIO1C[3:0]				GPIO0C[3:0]			
0F	GPIOCR2	GPIO3C[3:0]				GPIO2C[3:0]			
12	GPIO0SS	REG[4:0]					BIT[2:0]		
13	GPIO1SS	REG[4:0]					BIT[2:0]		
14	GPIO2SS	REG[4:0]					BIT[2:0]		
15	GPIO3SS	REG[4:0]					BIT[2:0]		
1B	PACR1	RST	TRIG	ARM	—	—	—	TINV	MODE
1C	PACR2	ARMSRC[3:0]				TRGSRC[3:0]			
1D	MABCR1	RST	START	—	—	—	TBSRC[2:0]		
1E	MABCR2	AINV	—	—	ASRC[4:0]				
1F	MABCR3	BINV	—	—	BSRC[4:0]				
Status Registers									
30	ID1	IDU[7:0}							
31	ID2	IDL[3:0]				REV[3:0]			
40	CFGSR	TEST	XOFAIL	—	—	IF[1:0]		AC[1:0]	
41	GPIOSR	—	—	—	—	GPIO3	GPIO2	GPIO1	GPIO0
42	INTSR	—	GLOB	OC	—	—	APLL	INTIE	INT
43	GLOBISR	BCDONE	—	—	—	—	—	PA	MAB
45	OCISR	—	—	—	—	—	OC3	OC2	OC1
46	APLLISR	—	—	—	—	—	—	—	APLL
48	APLLSR	—	ALK2IE	ALK2L	ALK2	—	ALKIE	ALKL	ALK
4B	MABSR1	—	OVFL	RDYIE	RDYL	BUSY	MEAS[10:8]		
4C	MABSR2	MEAS[7:0]							
4D	PASR	—	—	—	—	ADJIE	ADJL	BUSY	ARMED
53	OC1SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
54	OC2SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
55	OC3SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
APLL Configuration Registers									
100	APLLCR1	—	—	—	—	—	ENHS2	BYPHS2	—
101	APLLCR2	HSDIV2[3:0]				HSDIV1[3:0]			
102	APLLCR3	—	EXTSW	ALTMUX[2:0]			APLLMUX[2:0]		
103	APLLCR4	DECPH	PDSS[2:0]			INCPH	PISS[2:0]		
106	AFBDIV1	AFBDIV[7:0]							
107	AFBDIV2	AFBDIV[15:8]							
108	AFBDIV3	AFBDIV[23:16]							
109	AFBDIV4	AFBDIV[31:24]							

TABLE 6-1: REGISTER MAP (CONTINUED)

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
10A	AFBDIV5	AFBDIV[39:32]							
10B	AFBDIV6	—	—	—	—	—	—	AFBDIV[41:40]	
10C	AFBDEN1	AFBDEN[7:0]							
10D	AFBDEN2	AFBDEN[15:8]							
10E	AFBDEN3	AFBDEN[23:16]							
10F	AFBDEN4	AFBDEN[31:24]							
110	AFBREM1	AFBREM[7:0]							
111	AFBREM2	AFBREM[15:8]							
112	AFBREM3	AFBREM[23:16]							
113	AFBREM4	AFBREM[31:24]							
114	AFBBP	AFBBP[7:0]							
Output Clock Configuration Registers									
—	**OC1 Registers**								
200	OC1CR1	PHEN	MSDIV[6:0]						
201	OC1CR2	—	POL	DRIVE[1:0]		STOPDIS	OCSF[2:0]		
202	OC1CR3	SRLSEN	DIVSEL	NEGLSD	LSSEL	—	—	—	LSDIV[24]
203	OC1DIV1	LSDIV[7:0]							
204	OC1DIV2	LSDIV[15:8]							
205	OC1DIV3	LSDIV[23:16]							
206	OC1DC	OCDC[7:0]							
207	OC1PH	PHADJ[7:0]							
208	OC1STOP	STOP	—	SRC[3:0]				MODE[1:0]	
—	**OC2 Registers**								
210	OC2CR1	Same as OC1 Registers							
...	...								
218	OC2STOP								
—	**OC3 Registers**								
220	OC3CR1	Same as OC1 Registers							
...	...								
228	OC3STOP								
Input Clock Configuration									
300	IC1CR1	—	POL	—	—	—	—	HSDIV[1:0]	
320	IC2CR1	—	POL	—	—	—	—	HSDIV[1:0]	
340	IC3CR1	—	POL	—	—	—	—	HSDIV[1:0]	
NCO/SS Configuration Registers									
40B	NCSSCR1	—	—	—	—	MODE[3:0]			
420	DFREQZ1	FREQZ[7:0]							
421	DFREQZ2	FREQZ[15:8]							
422	DFREQZ3	FREQZ[23:16]							
423	DFREQZ4	FREQZ[31:24]							
424	DFREQZ5	FREQZ[39:32]							

6.3 Register Definitions

6.3.1 GLOBAL CONFIGURATION REGISTERS

Register Name:		EESEL						
Register Description:		EEPROM Memory Selection Register						
Register Address:		00h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	—	—	EESEL
Default:	0	0	0	0	0	0	0	0

Bit 0: EEPROM Memory Select (EESEL). This bit is a bank-select that specifies whether device register space or EEPROM memory is mapped into addresses 0x1 and above. This applies only to the ZL30251. The ZL30250 does not have internal EEPROM memory. See Section 5.8 and Section 6.1.4. Note that this bit is write-only; the value read is not reliable.

0 = Device registers

1= EEPROM memory

Register Name:		MCR1						
Register Description:		Master Configuration Register 1						
Register Address:		09h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	RST	—	MCSEL1	MCSEL	ROSCD	DBL	XAB[1:0]	
Default:	0	0	0	0	0	0	0	0

Bit 7: Device Reset (RST). When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is high, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RSTN pin was last active. See Section 5.10.

0 = Normal operation

1 = Reset

Note: For proper sequencing of internal logic, write MCR1 to clear the MCSEL1, MCSEL and ROSCD bits first (without changing the value of the RST bit) then perform a second write to set the RST bit.

(Note: on rev A devices (ID2.REV=0) do not set this bit to 1.)

Bit 5: NCO/SS Master Clock Select IC1 (MCSEL1). This bit overrides the MCSEL bit to specify IC1 as the source of the NCO/SS block's master clock.

0 = Master clock selected by MCSEL bit

1 = Master clock sourced from IC1, which has a divider and a polarity control bit

Bit 4: NCO/SS Master Clock Select (MCSEL). This bit selects the source of the NCO/SS block's master clock. At reset the internal ring oscillator is enabled and selected. When operating the device in NCO mode or spread spectrum mode, this bit must be set to 1 after the external oscillator connected to the XA pin has stabilized and is ready to use. See Section 5.3.4.

0 = Master clock sourced from internal ring oscillator

1 = Master clock sourced from the XA pin (optionally through the clock doubler)

Bit 3: Ring Oscillator Disable (ROSCD). This bit disables the ring oscillator. It can be set to 1 when either MCSEL or MCSEL1 is set 1 so that the ring oscillator does not cause unwanted phase noise spurs in output clock signals. See Section 5.3.4.

0 = Enable

1 = Disable (power-down)

Bit 2: Clock Doubler Enable (DBL). This bit enables the clock doubler for either the output of the crystal driver circuitry or the signal on the XA pin. During power-up, system software must wait at least 5 ms for the crystal driver circuit to stabilize before enabling the clock doubler. See Section 5.3.3.

0 = Disable (power down)

1 = Enable

Bits 1 to 0: XA/XB Pin Mode (XAB[1:0]). This field specifies the behavior of the XA and XB pins. See Section 5.3.

00 = Crystal driver and input disabled / powered down

01 = Crystal driver and input enabled on XA/XB

10 = XA enabled as single-ended input for external oscillator signal; XB must be left floating

11 = {unused value}

Register Name:	MCR2							
Register Description:	Master Configuration Register 2							
Register Address:	0Ah							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	—	EXTSS[1:0]		—	—	—	—	—
Default:	0	0	0	0	0	0	0	0

Bits 6 to 5: External Switch Source Select (EXTSS[1:0]). This field selects the GPIO source for the external switch control signal. It is only valid when APLLCR3.EXTSW=1. See Section 5.6.1.

00 = GPIO0

01 = GPIO1

10 = GPIO2

11 = GPIO3

Register Name:	PLLEN							
Register Description:	APLL Enable Register							
Register Address:	0Bh							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	—	—	—	NCSSEN	—	—	—	APLLEN
Default:	0	0	0	0	0	0	0	0

Bit 4: NCO/SS Block Enable (NCSSEN). This field enables or disables the NCO/SS block. See Section 5.5. Note that the XA clock source must be properly configured and selected to operate the NCO/SS block.

0 = Disable (powered down)

1 = Enable

Bit 0: APLL Enable (APLLEN). This bit enables or disables the APLL. For normal operation the APLL must be enabled. See Section 5.6.2.

0 = Disabled

1 = Enabled

Register Name:		ICEN						
Register Description:		Input Clock Enable Register						
Register Address:		0Ch						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	IC3EN	IC2EN	IC1EN
Default:	0	0	0	0	0	0	0	0

Bit 2: Input Clock 3 Enable (IC3EN). This bit enables and disables the input clock 3 differential receiver and input dividers. See Section 5.4.

0 = Disabled

1 = Enabled

Bit 1: Input Clock 2 Enable (IC2EN). This bit enables and disables the input clock 2 differential receiver and input dividers. See Section 5.4.

0 = Disabled

1 = Enabled

Bit 0: Input Clock 1 Enable (IC1EN). This bit enables and disables the input clock 1 differential receiver and input dividers. See Section 5.4.

0 = Disabled

1 = Enabled

Register Name:		OCEN						
Register Description:		Output Clock Enable Register						
Register Address:		0Dh						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	OC3EN	OC2EN	OC1EN
Default:	0	0	0	0	0	0	0	0

Bit 2: Output Clock 3 Enable (OC3EN). This bit enables and disables the output clock 3 drivers, output dividers, phase adjustment/alignment circuitry and start/stop circuitry. See Section 5.7.1.

0 = Disabled

1 = Enabled

Bit 1: Output Clock 2 Enable (OC2EN). This bit enables and disables the output clock 2 drivers, output dividers, phase adjustment/alignment circuitry and start/stop circuitry. See Section 5.7.1.

0 = Disabled

1 = Enabled

Bit 0: Output Clock 1 Enable (OC1EN). This bit enables and disables the output clock 1 drivers, output dividers, phase adjustment/alignment circuitry and start/stop circuitry. See Section 5.7.1.

0 = Disabled

1 = Enabled

Register Name:	GPIOCR1							
Register Description:	GPIO Configuration Register 1							
Register Address:	0Eh							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	GPIO1C[3:0]				GPIO0C[3:0]			
Default:	0	0	0	0	0	0	0	0

Bits 7 to 4: GPIO1 Configuration (GPIO1C[3:0]). This field configures the GPIO1 pin as a general-purpose input, a general-purpose output driving low or high, or a status output. The current state of the pin can be read from GPIOSR.GPIO1. When GPIO1 is a status output, the GPIO1SS register specifies which status bit is output.

0000 = General-purpose input

0001 = General-purpose input - inverted polarity

0010 = General-purpose output driving low

0011 = General-purpose output driving high

0100 = Status output – non-inverted polarity

0101 = Status output - inverted polarity of the status bit it follows

0110 = Status output – 0 drives low, 1 high impedance

0111 = Status output – 0 high impedance, 1 drives low

1000 to 1111 = {unused values}

Bits 3 to 0: GPIO0 Configuration (GPIO0C[3:0]). This field configures the GPIO0 pin as a general-purpose input, a general-purpose output driving low or high, or a status output. The current state of the pin can be read from GPIOSR.GPIO0. When GPIO0 is a status output, the GPIO0SS register specifies which status bit is output.

0000 = General-purpose input

0001 = General-purpose input - inverted polarity

0010 = General-purpose output driving low

0011 = General-purpose output driving high

0100 = Status output – non-inverted polarity

0101 = Status output - inverted polarity of the status bit it follows

0110 = Status output – 0 drives low, 1 high impedance

0111 = Status output – 0 high impedance, 1 drives low

1000 to 1111 = {unused values}

Register Name:	GPIOCR2							
Register Description:	GPIO Configuration Register 2							
Register Address:	0Fh							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	GPIO3C[3:0]				GPIO2C[3:0]			
Default:	0	0	0	0	0	0	0	0

These fields are identical to those in GPIOCR1 except they control GPIO2 and GPIO3.

Register Name:	GPIO0SS							
Register Description:	GPIO0 Status Select Register							
Register Address:	12h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	REG[4:0]					BIT[2:0]		
Default:	0	0	0	0	0	0	0	0

Bits 7 to 3: Status Register (REG[4:0]). When GPIOCR1.GPIO0C=01xx, this field specifies the register of the status bit that GPIO0 will follow while the BIT field below specifies the status bit within the register. Setting the combination of this field and the BIT field below to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO0 being driven low. The address of the status bit that GPIO0 follows is 0x40 + REG[4:0]

Bits 2 to 0: Status Bit (BIT[2:0]). When GPIOCR1.GPIO0C=01xx, the REG field above specifies the register of the status bit that GPIO0 will follow while this field specifies the status bit within the register. Setting the combination of the REG field and this field to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO1 being driven low. 000=bit 0 of the register. 111=bit 7 of the register.

Note: The device does not allow the GPIO status register bits in GPIOSR to be followed by a GPIO.

Register Name:	GPIO1SS							
Register Description:	GPIO1 Status Select Register							
Register Address:	13h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	REG[4:0]					BIT[2:0]		
Default:	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO0SS except they control GPIO1.

Register Name:	GPIO2SS							
Register Description:	GPIO2 Status Select Register							
Register Address:	14h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	REG[4:0]					BIT[2:0]		
Default:	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO0SS except they control GPIO2.

Register Name:	GPIO3SS							
Register Description:	GPIO3 Status Select Register							
Register Address:	15h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	REG[4:0]					BIT[2:0]		
Default:	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO0SS except they control GPIO3.

Register Name:	PACR1							
Register Description:	Phase Adjust Configuration Register 1							
Register Address:	1Bh							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	RST	TRIG	ARM	—	—	—	TINV	MODE
Default:	0	0	0	0	0	0	0	0

Bit 7: Phase Adjustment Reset Bit (RST). This bit is used to reset the phase adjustment state machine. This is used to abort the phase adjustment after arming but before the trigger occurs. Resetting puts the state machine back to waiting for an arm signal. This bit is self-clearing. See Section 5.7.4.

1 = Reset a phase adjustment event in progress, self clearing

Bit 6: Phase Adjustment Trigger Bit (TRIG). This bit is used to trigger the phase adjustment event when PACR2.TRGSRC=0000 and the phase adjustment has been armed. This bit is self-clearing and must be written again to cause another trigger. When the ARM bit and TRIG bit are selected as the sources for arming and triggering, respectively, the ARM bit must be set first then the TRIG bit can be set in a subsequent register write to initiate a trigger event. See Section 5.7.4.

1 = Trigger a phase adjustment, self clearing

Note: For (1) phase adjustment when any OCx output's MSDIV period is less than server clock period, or (2) phase alignment when device is in APLL-only mode and any OCx output has MSDIV period + 7 x HSDIV period < 15.38 ns, this bit may or may not self-clear depending on exact device configuration and therefore must be cleared by system software for proper operation.

Bit 5: Phase Adjustment Arm Bit (ARM). When PACR2.ARMSRC=0001, setting this bit to 1 while PASR.ARMED=0 arms the phase adjustment. Writing a 0 to this bit has no effect. Changing the value of this bit from 0 to 1 while PASR.ARMED=1 has no effect. See Section 5.7.4.

1 = Arm the phase adjustment, self clearing

Bit 1: Phase Adjustment Trigger Invert (TINV). This bit specifies the polarity of the trigger signal. See Section 5.7.4.

0 = Trigger signal normal polarity

1 = Trigger signal inverted

Bit 0: Phase Adjust/Alignment Mode (MODE). This field sets the mode of the phase change. In output phase alignment mode, the device resets the MSDIV and LSDIV dividers for all participating outputs so that they are all aligned and then adjusts the phase of each participating output as specified in the OCxPH register. In output phase adjustment mode the device does not reset the MSDIV and LSDIV dividers and therefore causes each participating output to have the phase adjustment specified in the OCxPH register relative to that output's previous phase. See Section 5.7.4.

0 = Phase alignment mode

1 = Phase adjustment mode

Register Name:	PACR2							
Register Description:	Phase Adjust Configuration Register 2							
Register Address:	1Ch							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	ARMSRC[3:0]				TRGSRC[3:0]			
Default:	0	0	0	0	0	0	0	0

Bits 7 to 4: Output Phase Adjustment Arm Source (ARMSRC[3:0]). This field selects the source of the phase adjustment arming signal. See Section 5.7.4.

0000 = Always armed (see Note)

0001 = PACR1.ARM bit (one-shot)

0010 = APLL transition from unlocked to locked

0011 to 0111 = {unused values}

1000 = GPIO0 transition (see note below)

1001 = GPIO1 transition

1010 = GPIO2 transition

1011 = GPIO3 transition

1100 to 1111 = {unused values}

Note: When using always armed, any change to the PACR1 or PACR2 registers or any change to the OCxCR1.PHEN bits must be followed by a reset of the phase adjustment state machine (set PACR1.RST=1).

Bits 3 to 0: Output Phase Adjustment Trigger Source (TRGSRC[3:0]). This field selects the source of the phase adjustment trigger signal. The phase adjustment must be armed or the trigger signal is ignored. The trigger source transition initiates the phase adjustment event. See Section 5.7.4.

0000 = PACR1.TRIG bit

0001 = APLL transition from unlocked to locked

0010 to 0111 = {unused values}

1000 = GPIO0 transition (see note below)

1001 = GPIO1 transition

1010 = GPIO2 transition

1011 = GPIO3 transition

1100 to 1111 = {unused values}

Note: In both fields above the GPIO transitions are 0-to-1 when GPIOCR1.GPIOxC=0000 and 1-to-0 when GPIOCR1.GPIOxC=0001.

Register Name:	MABCR1							
Register Description:	Measure A-to-B Configuration Register 1							
Register Address:	1Dh							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	RST	START	—	—	—	TBSRC[2:0]		
Default:	0	0	0	0	0	0	0	0

Bit 7: Measurement Reset (RST). This field stops the current A-to-B phase measurement. This bit is self clearing. See Section 5.7.6.

1 = Stop measurement (self-clearing)

Bit 6: Measurement Start (START). This field starts a new A-to-B phase measurement. This bit is self clearing. See Section 5.7.6.

1= Start new measurement (self-clearing)

Bits 2 to 0: Measurement Time Base Source (TBSRC[2:0]). This field selects the source of the measurement time base. See Section 5.7.6.

000 = {reserved value, do not use}

001 = Medium-speed divider 1 (MSDIV1) output clock

010 = Medium-speed divider 2 (MSDIV2) output clock

011 = Medium-speed divider 3 (MSDIV3) output clock

Register Name:	MABCR2							
Register Description:	Measure A-to-B Configuration Register 2							
Register Address:	1Eh							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	AINV	—	—	ASRC[4:0]				
Default:	0	0	0	0	0	0	0	0

Bit 7: Measurement Input A Invert (AINV). This field inverts the signal of measurement input A. See Section 5.7.6.

0 = Measure to and from rising edge of input A

1 = Measure to and from falling edge of input A

Bits 4 to 0: Measurement Input A Source (ASRC[4:0]). This field selects the source of measurement input A. See Section 5.7.6.

00000 = IC1

00001 = IC2

00010 = IC3

01000 = GPIO0

01001 = GPIO1

01010 = GPIO2

01011 = GPIO3

10000 = OC1

10001 = OC2

10010 = OC3

Register Name:	MABCR3							
Register Description:	Measure A-to-B Configuration Register 3							
Register Address:	1Fh							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	BINV	—	—	BSRC[4:0]				
Default:	0	0	0	0	0	0	0	0

Bit 7: Measurement Input B Invert (BINV). This field inverts the signal of measurement input B. See Section 5.7.6.

0 = Measure to and from rising edge of input B

1 = Measure to and from falling edge of input B

Bits 4 to 0: Measurement Input B Source (BSRC[4:0]). This field selects the source of measurement input B. See Section 5.7.6.

00000 = IC1

00001 = IC2

00010 = IC3

01000 = GPIO0

01001 = GPIO1

01010 = GPIO2

01011 = GPIO3

10000 = OC1

10001 = OC2

10010 = OC3

6.3.2 STATUS REGISTERS

Register Name:	ID1							
Register Description:	Device Identification Register, MSB							
Register Address:	30h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	IDU[7:0]							
Default:	0	0	0	1	1	0	0	1

Bits 7 to 0: Device ID Upper (IDU[7:0]). This field is the upper eight bits of the device ID.

Register Name:	ID2							
Register Description:	Device Identification Register, LSB and Revision							
Register Address:	31h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	IDL[3:0]				REV[3:0]			
Default:	See below.				0	0	0	1

Bits 7 to 4: Device ID Lower (IDL[3:0]). This field is the lower four bits of the device ID.

ZL30250 = 0000

ZL30251 = 0001

Bits 3 to 0: Device Revision (REV[3:0]). These bits are the device hardware revision starting at 0.

Register Name:	CFGSR							
Register Description:	Configuration Status Register							
Register Address:	40h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	TEST	XOFAIL	—	—	IF[1:0]		AC[1:0]	
Default:	See below.	0	0	0	See below.		See below.	

Bit 7: Test Mode (TEST). This read-only bit is the latched state of the TEST/GPIO2 pin when the RSTN pin transitions high. For proper operation it should be 0. See Section 5.2.

Bit 6: XO Fail (XOFAIL). This read-only bit is set when the external oscillator signal on the XA pin fails or when the crystal connected to the XA/XB pins fails to oscillate.

Bits 3 to 2: Interface Mode (IF[1:0]). These read-only bits are the latched state of the IF1/MISO and IF0/CSN pins when the RSTN pin transitions high. See Section 5.2.

Bits 1 to 0: Auto-Configuration (AC[1:0]). These read-only bits are the latched state of the AC1/GPIO1 and AC0/GPIO0 pins when the RSTN pin transitions high. See Section 5.2.

Register Name:	GPIOSR							
Register Description:	GPIO Status Register							
Register Address:	41h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	GPIO3	GPIO2	GPIO1	GPIO0
Default:	0	0	0	0	0	0	0	0

Bit 3: GPIO3 State (GPIO3). This real-time status bit indicates the current state of the GPIO3 pin, not influenced by any inversion that may be specified by GPIOCR2.GPIO3C.

0 = low

1 = high

Bit 2: GPIO2 State (GPIO2). This real-time status bit indicates the current state of the GPIO2 pin, not influenced by inversion that may be specified by GPIOCR2.GPIO2C.

0 = low

1 = high

Bit 1: GPIO1 State (GPIO1). This real-time status bit indicates the current state of the GPIO1 pin, not influenced by inversion that may be specified by GPIOCR1.GPIO1C.

0 = low

1 = high

Bit 0: GPIO0 State (GPIO0). This real-time status bit indicates the current state of the GPIO0 pin, not influenced by inversion that may be specified by GPIOCR1.GPIO0C.

0 = low

1 = high

Register Name:	INTSR							
Register Description:	Interrupt Status Register							
Register Address:	42h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	GLOB	OC	—	—	APLL	INTIE	INT
Default:	0	0	0	0	0	0	0	0

Bit 6: Global Interrupt Status (GLOB). This read-only bit is set if any of the global interrupt status bits are set in the GLOBISR register. See Section 5.9.

Bit 5: Output Clock Interrupt Status (OC). This read-only bit is set if any of the output clock interrupt status bits are set in the OCISR register. See Section 5.9.

Bit 2: APLL Interrupt Status (APLL). This read-only bit is set if any of the APLL interrupt status bits are set in the APLLISR register. See Section 5.9.

Bit 1: Interrupt Enable Bit (INTIE). This is the global interrupt enable bit. When this bit is 0 all interrupt sources are prevented from setting the INT global interrupt status bit (below). See Section 5.9.

0 = Interrupts are disabled at the global level

1 = Interrupts are enabled at the global level

Bit 0: Interrupt Status (INT). This read-only bit is set when any of the GLOB, OC, or APLL bits in this INTSR register are set and the INTIE bit is set. This bit can cause an interrupt request when set by configuring one of the GPIO pins to follow it. See Section 5.9.

0 = No interrupt

1 = An unmasked interrupt source is active

Register Name:		GLOBISR						
Register Description:		Global Functions Interrupt Status Register						
Register Address:		43h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	BCDONE	—	—	—	—	—	PA	MAB
Default:	See below	0	0	0	0	0	0	0

Bit 7: Boot Controller Done (BCDONE). This bit indicates the status of the on-chip boot controller, which performs auto-configuration from EEPROM. It is cleared when the device is reset and set after the boot controller finishes auto-configuration of the device. See Section 5.12.

Bit 1: Phase Adjust Interrupt Status (PA). This bit indicates the current status of the interrupt sources from the phase adjust function (see Section 5.7.4). It is set when any latched status bit in the PASR register is set and the associated interrupt enable bit is also set. See Section 5.9.

Bit 0: Measure AB Interrupt Status (MAB). This bit indicates the current status of the interrupt sources from the A-to-B phase offset measurement function (see Section 5.7.6). It is set when any latched status bit in the MABSR1 register is set and the associated interrupt enable bit is also set. See Section 5.9.

Register Name:		OCISR						
Register Description:		Output Clock Interrupt Status Register						
Register Address:		45h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	OC3	OC2	OC1
Default:	0	0	0	0	0	0	0	0

Bit 2: Output Clock 3 Interrupt Status (OC3). This bit indicates the current status of the interrupt sources for OC3. It is set when any latched status bit in the OC3SR register is set and the associated interrupt enable bit is also set. See Section 5.9.

Bit 1: Output Clock 2 Interrupt Status (OC2). This bit indicates the current status of the interrupt sources for OC2. It is set when any latched status bit in the OC2SR register is set and the associated interrupt enable bit is also set. See Section 5.9.

Bit 0: Output Clock 1 Interrupt Status (OC1). This bit indicates the current status of the interrupt sources for OC1. It is set when any latched status bit in the OC1SR register is set and the associated interrupt enable bit is also set. See Section 5.9.

Register Name:		APLLISR						
Register Description:		APLL Interrupt Status Register						
Register Address:		46h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	—	—	APLL
Default:	0	0	0	0	0	0	0	0

Bit 0: APLL Interrupt Status (APLL). This bit indicates the current status of the interrupt sources for the APLL. It is set when any latched status bit in the APLLSR register is set and the associated interrupt enable bit is also set. See Section 5.9.

Register Name:	APLLSR							
Register Description:	APLL Status Register							
Register Address:	48h							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	—	ALK2IE	ALK2L	ALK2	—	ALKIE	ALKL	ALK
Default:	0	0	0	0	0	0	0	0

Bit 6: APLL Lock 2 Interrupt Enable (ALK2IE). This bit enables the ALK2L latched status bit to send an interrupt request into device's interrupt logic.

0 = Interrupt is disabled

1 = Interrupt is enabled

Bit 5: APLL Lock 2 Latched Status (ALK2L). This latched status bit is set to 1 when the ALK2 status bit changes state (set or cleared). ALK2L is cleared when written with a 1. When ALK2L is set it can cause an interrupt request if the ALK2IE interrupt enable bit is set.

Bit 4: APLL Lock Status 2 (ALK2). This real-time status bit provides one type of APLL lock status. System software should consider the APLL locked when ALK (bit 0) is set to 1 AND ALK2=1. See Section 5.6.

Bit 2: APLL Lock Interrupt Enable (ALKIE). This bit enables the ALKL latched status bit to send an interrupt request into device's interrupt logic.

0 = Interrupt is disabled

1 = Interrupt is enabled

Bit 1: APLL Lock Latched Status (ALKL). This latched status bit is set to 1 when the ALK status bit changes state (set or cleared). ALKL is cleared when written with a 1. When ALKL is set it can cause an interrupt request if the ALKIE interrupt enable bit is set.

Bit 0: APLL Lock Status (ALK). This real-time status bit indicates one type of APLL lock status. System software should consider the APLL locked when ALK=1 AND ALK2 (bit 4) is set to 1. See Section 5.6.

0 = Not locked

1 = Locked

Register Name:	MABSR1							
Register Description:	Measure A to B Status Register 1							
Register Address:	4Bh							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	—	OVFL	RDYIE	RDYL	BUSY	MEAS[10:8]		
Default:	0	0	0	0	0	0	0	0

Bit 6: Measurement Overflow (OVFL). This latched status bit is set when the phase measurement is ready and an overflow has occurred. See Section 5.7.6.

0 = No measurement overflow, MEAS is a valid value

1 = A measurement overflow occurred, MEAS is not a valid value

Bit 5: Measurement Ready Interrupt Enable (RDYIE). This bit enables the RDYL latched status bit to send an interrupt request into device's interrupt logic.

0 = Interrupt is disabled

1 = Interrupt is enabled

Bit 4: Measurement Ready (RDYL). This latched status bit is set when a new phase measurement is ready. See Section 5.7.6.

0 = New measurement not ready

1 = A new measurement in MEAS is ready

Bit 3: Measurement Busy (BUSY). This real-time status bit is set when a new phase measurement is being performed. See Section 5.7.6.

0 = A measurement is not being performed

1 = A measurement is being performed

Bits 2 to 0: Measurement Value (MEAS[10:8]). See the MABSR2 register description.

Register Name:	MABSR2							
Register Description:	Measure A to B Status Register 2							
Register Address:	4Ch							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	MEAS[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Measurement Value (MEAS[7:0]). The full 11-bit MEAS[10:0] field spans this register and the lower bits of MABSR1. The format is two's-complement. This field indicates the result of the A-to-B measurement when BUSY=0, RDYL=1 and OVFL=0. Its value is in units of the selected timebase period and has a range of +1023 to –1024 periods. See Section 5.7.6.

Register Name:	PASR							
Register Description:	Phase Adjust Status Register							
Register Address:	4Dh							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	—	—	—	—	ADJIE	ADJL	BUSY	ARMED
Default:	1	0	0	0	0	1	0	0

Bit 3: Phase Adjustment Finished Interrupt Enable (ADJIE). This bit enables the ADJL latched status bit to send an interrupt request into the device's interrupt logic.

0 = Interrupt is disabled

1 = Interrupt is enabled

Bit 2: Phase Adjustment Finished (ADJL). This latched status bit is set when the output phase adjustment is completed for all participating outputs. Writing a 1 to this bit clears it. See Section 5.7.4.

0 = Output phase adjustment has not completed

1 = Output phase adjustment has completed

Note: For (1) phase adjustment when any OCx output's MSDIV period is less than server clock period, or (2) phase alignment when device is in APLL-only mode and any OCx output has MSDIV period + 7 x HSDIV period < 15.38 ns, this bit may or may not be set depending on exact device configuration and therefore should not be checked by system software. Instead the state of the BUSY real-time bit (bit 1) should be checked.

Bit 1: Phase Adjustment Busy (BUSY). This bit is a real time status that indicates that the output phase adjustment has been triggered and is in progress on the participating outputs. See Section 5.7.4.

0 = Output phase adjustment is not in progress

1 = Output phase adjustment is in progress

Bit 0: Phase Adjustment Armed (ARMED). This bit is a real time status that indicates that the output phase adjustment is armed and waiting for a trigger. It is cleared when the trigger event occurs. See Section 5.7.4.

0 = Output phase adjustment is not armed

1 = Output phase adjustment is armed

Register Name:		OC1SR	OC2SR	OC3SR				
Register Description:		Output Clock x Status Register						
Register Address:		OC1: 53h, OC2: 54h, OC3: 55h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
Default:	0	0	0	0	0	0	See note	See note

Bit 7: (LSCLKIE). This bit enables the LSCLKL latched status bit to send an interrupt request into device's interrupt logic.

0 = Interrupt is disabled

1 = Interrupt is enabled

Bit 6: (LSCLKL). This latched status bit is set when the low-speed divider output clock transitions low-to-high. Writing a 1 to this bit clears it.

0 = Low speed output clock has not transitioned low to high

1 = Low speed output clock has transitioned low to high

Bit 5: (LSCLK). This real-time status bit follows the level of the low-speed divider output clock when the OCx-CR3.SRLSEN bit is set.

0 = LSCLK is high

1 = LSCLK is low

Bit 4: (STARTIE). This bit enables the STARTL latched status bit to send an interrupt request into device's interrupt logic.

0 = Interrupt is disabled

1 = Interrupt is enabled

Bit 3: (STARTL). This latched status bit is set when the output clock signal has been started after being stopped. Writing a 1 to this bit clears it. See Section 5.7.5.

0 = Output clock signal has not resumed from being stopped

1 = Output clock signal has resumed from being stopped

Bit 2: (STOPIE). This bit enables the STOPL latched status bit to send an interrupt request into device's interrupt logic.

0 = Interrupt is disabled

1 = Interrupt is enabled

Bit 1: (STOPL). This latched status bit is set when the output clock signal has been stopped. Writing a 1 to this bit clears it. See Section 5.7.5.

0 = Output clock signal has not stopped

1 = Output clock signal has stopped

Bit 0: (STOPD). This real-time status bit is high when the output clock signal is stopped and low when the output clock is not stopped. See Section 5.7.5.

0 = Output clock signal is not stopped

1 = Output clock signal is stopped

6.3.3 APLL CONFIGURATION REGISTERS

Register Name:	APLLCR1							
Register Description:	APLL Configuration Register 1							
Register Address:	100h							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	—	—	—	—	—	ENHS2	BYPHS2	—
Default:	0	0	0	0	0	0	0	0

Bit 2: Enable High-Speed Divider 2 (ENHS2). This bit is an enable/disable control for HSDIV2. When HSDIV2 is disabled, device power consumption is reduced as shown in Table 7-3. HSDIV2 is enabled when PLLEN.APLLEN=1, ENHS2=1 and APLLCR1.BYPHS2=0.

0 = Disable

1 = Enable

Bit 1: Bypass APLL and High-Speed Divider 2 (BYPHS2). This bit controls the mux immediately to the right of HSDIV2 in the Block Diagram. The mux that provides the bypass signal to this mux is controlled by APLLMUX and related fields in APLLCR3.

0 = No bypass

1 = Bypass

Register Name:	APLLCR2							
Register Description:	APLL Configuration Register 2							
Register Address:	101h							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	HSDIV2[3:0]				HSDIV1[3:0]			
Default:	0	0	0	0	0	0	0	0

Bits 7 to 4: APLL High-Speed Divider 2 (HSDIV2[3:0]). This field controls the APLL's high-speed divider 2 block (see Figure 5-2). See Section 5.6.2.

0000 = Divide by 4 1000 = Divide by 8

0001 = Divide by 4.5 1001 = Divide by 9

0010 = Divide by 5 1010 = Divide by 10

0011 = Divide by 5.5 1011 = Divide by 11

0100 = Divide by 6 1100 = Divide by 12

0101 = Divide by 6.5 1101 = Divide by 13

0110 = Divide by 7 1110 = Divide by 14

0111 = Divide by 7.5 1111 = Divide by 15

Bits 3 to 0: APLL High-Speed Divider 1 (HSDIV1[3:0]). This field controls the APLL's high-speed divider 1 block (see Figure 5-2). See Section 5.6.2.

0000 = Divide by 4 1000 = Divide by 8

0001 = Divide by 4.5 1001 = Divide by 9

0010 = Divide by 5 1010 = Divide by 10

0011 = Divide by 5.5 1011 = Divide by 11

0100 = Divide by 6 1100 = Divide by 12

0101 = Divide by 6.5 1101 = Divide by 13

0110 = Divide by 7 1110 = Divide by 14

0111 = Divide by 7.5 1111 = Divide by 15

Register Name:	APLLCR3							
Register Description:	APLL Configuration Register 3							
Register Address:	102h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	EXTSW	ALTMUX[2:0]			APLLMUX[2:0]		
Default:	0	0	0	0	0	0	0	0

Bit 6: APLL External Switching Mode (EXTSW). This bit enables APLL external reference switching mode. In this mode, if the selected GPIO signal is low the APLL input mux is controlled by APLLCR3.APLLMUX. If the selected GPIO signal is high the APLL input mux is controlled by APLLCR3.ALTMUX. MCR2.EXTSS specifies which GPIO pin controls this behavior. See Section 5.6.1.

Bits 5 to 3: APLL Alternate Mux Control (ALTMUX[2:0]). When APLLCR3.EXTSW=0 this field is ignored. When APLLCR3.EXTSW=1 and the selected GPIO signal is high, this field controls the APLL input muxes. See Section 5.6.1.

000 = Crystal driver circuit if crystal is connected, otherwise XA input

(clock frequency can be 2x if clock doubler enabled by MCR1.DBL=1)

001 = IC1 input

010 = IC2 input

011 = IC3 input

100-111 = {unused values}

Bits 2 to 0: APLL Mux Control (APLLMUX[2:0]). By default this field controls the APLL input muxes. When APLLCR3.EXTSW=1 and the selected GPIO signal is high, this field is ignored, and the APLL's clock source is specified by APLLCR3.ALTMUX. See Section 5.6.1.

000 = Crystal driver circuit if crystal is connected, otherwise XA input

(clock frequency can be 2x if clock doubler enabled by MCR1.DBL=1)

001 = IC1 input

010 = IC2 input

011 = IC3 input

110 = NCO/SS output to the APLL, XA (optionally doubled) sent to the bypass mux

111 = NCO/SS output to the APLL, no signal sent to the bypass mux (set APLLCR1.BYPHS2=0)

The following decodes are for applications where the NCO/SS master clock comes from IC1 rather than XA (MCR1.MCSEL1=1).

100 = NCO/SS output to the APLL, IC1 sent to the bypass mux

101 = NCO/SS output to the APLL, no signal sent to the bypass mux (set APLLCR1.BYPHS2=0)

Register Name:	APLLCR4							
Register Description:	APLL Configuration Register 4							
Register Address:	103h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	DECPH	PDSS[2:0]			INCPH	PISS[2:0]		
Default:	0	0	0	0	0	0	0	0

Bit 7: Decrement Phase (DECPH). When PDSS=000, this bit is the APLL phase decrement control signal. See Section 5.6.3. Decrement moves the signal earlier in time (to the left on a scope).

Bits 6 to 4: Phase Decrement Source Select (PDSS[2:0]). This field specifies the APLL phase decrement control signal. Every low-to-high transition and every high-to-low transition of the signal decrements the APLL's output phase. See Section 5.6.3.

000 = DECPH bit

001 = GPIO0

010 = GPIO1

011 = GPIO2

100 = GPIO3

101 to 111 = {unused values}

Bit 3: Increment Phase (INCPH). When PISS=000, this bit is the APLL phase increment control signal. See Section 5.6.3. Increment moved the signal later in time (to the right on a scope).

Bits 2 to 0: Phase Increment Source Select (PISS[2:0]). This field specifies the APLL phase increment control signal. Every low-to-high transition and every high-to-low transition of the signal increments the APLL's output phase. See Section 5.6.3.

000 = INCPH bit

001 = GPIO0

010 = GPIO1

011 = GPIO2

100 = GPIO3

101 to 111 = {unused values}

Register Name:	AFBDIV1							
Register Description:	APLL Feedback Divider Register 1							
Register Address:	106h							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	AFBDIV[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[7:0]). The full 42-bit AFBDIV[41:0] field spans the AFBDIV1 through AFBDIV6 registers. AFBDIV is an unsigned number with 9 integer bits (AFBDIV[41:33]) and up to 33 fractional bits. AFBDIV specifies the fixed-point term of the APLL's fractional feedback divide value. The value AFBDIV=0 is undefined. Unused least significant bits must be written with 0. See Section 5.6.2.

Register Name:	AFBDIV2							
Register Description:	APLL Feedback Divider Register 2							
Register Address:	107h							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	AFBDIV[15:8]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[15:8]). See the AFBDIV1 register description.

Register Name:	AFBDIV3							
Register Description:	APLL Feedback Divider Register 3							
Register Address:	108h							
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	AFBDIV[23:16]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[23:16]). See the AFBDIV1 register description.

Register Name:	AFBDIV4							
Register Description:	APLL Feedback Divider Register 4							
Register Address:	109h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBDIV[31:24]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[31:24]). See the AFBDIV1 register description.

Register Name:	AFBDIV5							
Register Description:	APLL Feedback Divider Register 5							
Register Address:	10Ah							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBDIV[39:32]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[39:32]). See the AFBDIV1 register description.

Register Name:	AFBDIV6							
Register Description:	APLL Feedback Divider Register 6							
Register Address:	10Bh							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	—	AFBDIV[41:40]	
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Register (AFBDIV[41:40]). See the AFBDIV1 register description.

Register Name:	AFBDEN1							
Register Description:	APLL Feedback Divider Denominator Register 1							
Register Address:	10Ch							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBDEN[7:0]							
Default:	0	0	0	0	0	0	0	1

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[7:0]). The full 32-bit AFBDEN[31:0] field spans AFBDEN1 through AFBDEN4 registers. AFBDEN is an unsigned integer that specifies the denominator of the APLL's fractional feedback divide value. The value AFBDEN=0 is undefined. When AFBBP=0, AFBDEN must be set to 1. See Section 5.6.2.

Register Name:	AFBDEN2							
Register Description:	APLL Feedback Divider Denominator Register 2							
Register Address:	10Dh							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBDEN[15:8]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[15:8]). See the AFBDEN1 register description.

Register Name:	AFBDEN3							
Register Description:	APLL Feedback Divider Denominator Register 3							
Register Address:	10Eh							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBDEN[23:16]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[23:16]). See the AFBDEN1 register description.

Register Name:	AFBDEN4							
Register Description:	APLL Feedback Divider Denominator Register 4							
Register Address:	10Fh							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBDEN[31:24]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Denominator Register (AFBDEN[31:24]). See the AFBDEN1 register description.

Register Name:	AFBREM1							
Register Description:	APLL Feedback Divider Remainder Register 1							
Register Address:	110h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBREM[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[7:0]). The full 32-bit AFBDEN[31:0] field spans AFBREM1 through AFBREM4 registers. AFBREM is an unsigned integer that specifies the remainder of the APLL's fractional feedback divider value. When AFBBP=0, AFBREM must be set to 0. See Section 5.6.2.

Register Name:	AFBREM2							
Register Description:	APLL Feedback Divider Remainder Register 2							
Register Address:	111h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBREM[15:8]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[15:8]). See the AFBREM1 register description.

Register Name:	AFBREM3							
Register Description:	APLL Feedback Divider Remainder Register 3							
Register Address:	112h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBREM[23:16]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[23:16]). See the AFBREM1 register description.

Register Name:	AFBREM4							
Register Description:	APLL Feedback Divider Remainder Register 4							
Register Address:	113h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBREM[31:24]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Remainder Register (AFBREM[31:24]). See the AFBREM1 register description.

Register Name:	AFBBP							
Register Description:	APLL Feedback Divider Truncate Bit Position							
Register Address:	114h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	AFBBP[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: APLL Feedback Divider Truncate Bit Position (AFBBP[7:0]). This unsigned integer specifies the number of fractional bits that are valid in the AFBDIV value. There are 33 fractional bits in AFBDIV. The value in this AFBBP field specifies 33 – number_of_valid_AFBDIV_fractional_bits. When AFBBP=0 all 33 AFBDIV fractional bits are valid. When AFBBP=9, the most significant 24 AFBDIV fractional bits are valid and the least significant 9 bits must be set to 0. This register field is only used when the feedback divider value is expressed in the form AFBDIV + AFBREM/AFBDEN. AFBBP values greater than 33 are invalid. When AFBBP=0, AFBREM must be set to 0 and AFBDEN must be set to 1. See Section 5.6.2.

6.3.4 OUTPUT CLOCK CONFIGURATION REGISTERS

Register Name:	OC1CR1	OC2CR1	OC3CR1					
Register Description:	Output Clock x Configuration Register 1							
Register Address:	OC1: 200h, OC2: 210h, OC3: 220h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	PHEN	MSDIV[6:0]						
Default:	0	0	0	0	0	0	0	0

Bit 7: Phase Adjust Enable (PHEN). This bit enables this output to participate in phase adjustment/alignment. See Section 5.7.4.

0 = Phase adjustment/alignment disabled for this output

1 = Phase adjustment/alignment enabled for this output

Bits 6 to 0: Medium-Speed Divider Value (MSDIV[6:0]). This field specifies the setting for the output clock's medium-speed divider. The divisor is MSDIV+1. Note that if MSDIV is not set to 0 (bypass) then MSDIV must be set to a value that causes the output clock of the medium-speed divider to be 425 MHz or less. When MSDIV=0, the medium-speed divider, phase adjust, low-speed divider, start/stop and output duty cycle adjustment circuits are bypassed and the high-frequency clock signal is directly sent to the output driver. See Section 5.7.2.

Register Name:		OC1CR2	OC2CR2	OC3CR2				
Register Description:		Output Clock x Configuration Register 2						
Register Address:		OC1: 201h, OC2: 211h, OC3: 221h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	POL	DRIVE[1:0]		STOPDIS	OCSF[2:0]		
Default:	0	0	0	0	0	0	0	0

Bit 6: Clock Path Polarity (POL). The clock path to the CML, HSTL, and CMOS outputs is inverted when this bit set. This does not invert the LSDIV path to the CMOS OCxN pin if that path is enabled. See Section 5.7.1.

Bits 5 to 4: CMOS/HSTL Output Drive Strength (DRIVE[1:0]). The CMOS/HSTL output drivers have four equal sections that can be enabled or disabled to achieve four different drive strengths from 1x to 4x. When the output power supply VDDOx is 3.3V or 2.5V, the user should start with 1x and only increase drive strength if the output is highly loaded and signal transition time is unacceptable. When VDDOx is 1.8V or 1.5V the user should start with 4x and only decrease drive strength if the output signal has unacceptable overshoot. See Section 5.7.1.

00 = 1x

01 = 2x

10 = 3x

11 = 4x

Bit 3: Stop Disable (STOPDIS). This bit causes the output to become disabled (high impedance) while the output clock is stopped. See Section 5.7.5.

0 = Do not disable the output while stopped

1 = Disable the output while stopped

Bits 2 to 0: Output Clock Signal Format (OCSF[2:0]). Note that OCEN.OCxEN=0 forces the output driver to be high-impedance regardless of the value of the OCSF register field. See Section 5.7.1.

000 = Disabled (high-impedance, low power mode)

001 = CML, standard swing (V_{OD} =800 mV_{P-P} typical)

010 = CML, narrow swing (V_{OD} =400 mV_{P-P} typical)

011 = HSTL (Set OCxCR2.DRIVE=11 (4x) to meet JESD8-6)

100 = Two CMOS: OCxP in phase with OCxN

101 = One CMOS: OCxP high impedance, OCxN enabled

110 = One CMOS: OCxP enabled, OCxN high impedance

111 = Two CMOS: OCxP inverted vs. OCxN

Register Name:		OC1CR3	OC2CR3	OC3CR3				
Register Description:		Output Clock x Configuration Register 3						
Register Address:		OC1: 202h, OC2: 212h, OC3: 222h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	SRLSEN	DIVSEL	NEGLSD	LSSEL	—	—	—	LSDIV[24]
Default:	0	0	0	0	0	0	0	0

Bit 7 Enable LSDIV Statuses (SRLSEN). This bit enables the OCxSR.LSCLK real-time status bit and its associated latched status bit OCxSR.LSCLKL.

0 = LSCLK status bit is not enabled (low)

1 = LSCLK status bit is enabled

Bit 6: High Speed Divider Select (DIVSEL). This bit selects which high-speed divider is the source of the clock for the output. See Section 5.7.2.

0 = HSDIV1

1 = HSDIV2

Bit 5: OCxN Low Speed Divider (NEGLSD). This bit selects the source of the clock on the OCxN pin in CMOS mode. See Section 5.7.2.

0 = Same as OCxP

1 = Output of the LSDIV divider

Note: NEGLSD should only be set to one in two-CMOS mode (OCxCR2.OCSF=100 or 111) and when OCx-CR2.POL=0.

Bit 4: LSDIV Select (LSSEL). This bit selects the source of the output clock. When the MSDIV divider is selected (LSSEL=0) the LSDIV divider output can be independently selected as the source for the OCxN pin (in CMOS output mode) or monitored by the OCxSR.LSCLK status bit. This bit is only valid when OCxCR1.MSDIV > 0. See Section 5.7.2.

0 = The output clock is sourced from the MSDIV divider.

1 = The output clock is sourced from the LSDIV divider.

Bit 0: Low-Speed Divider Value (LSDIV[24]). See the OCxDIV1 register description.

Register Name:		OC1DIV1	OC2DIV1	OC3DIV1				
Register Description:		Output Clock x Divider Register 1						
Register Address:		OC1: 203h, OC2: 213h, OC3: 223h						
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	LSDIV[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Low-Speed Divider Value (LSDIV[7:0]). The full 25-bit LSDIV[24:0] field spans this register, OCxDIV2, OCxDIV3. and bit 0 of OCxCR3. LSDIV is an unsigned integer. The frequency of the clock from the medium-speed divider is divided by LSDIV+1. The OCxCR3.LSSEL and NEGLSD bits control when the output of the low-speed divider is present on the OCxP and OCxN output pins. OCxCR1.MSDIV must be > 0 for the low-speed divider to operate. See Section 5.7.2.

Register Name:		OC1DIV2	OC2DIV2	OC3DIV2				
Register Description:		Output Clock x Divider Register 2						
Register Address:		OC1: 204h, OC2: 214h, OC3: 224h						
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	LSDIV[15:8]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Low-Speed Divider Value (LSDIV[15:8]). See the OCxDIV1 register description.

Register Name:		OC1DIV3	OC2DIV3	OC3DIV3				
Register Description:		Output Clock x Divider Register 3						
Register Address:		OC1: 205h, OC2: 215h, OC3: 225h						
—	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name:	LSDIV[23:16]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Low-Speed Divider Value (LSDIV[23:16]). See the OCxDIV1 register description.

Register Name:		OC1DC	OC2DC	OC3DC				
Register Description:		Output Clock x Duty Cycle Register						
Register Address:		OC1: 206h, OC2: 216h, OC3: 226h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	OCDC[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Output Clock Duty Cycle (OCDC[7:0]). This field controls the output clock signal duty cycle when MSDIV>0 and LSDIV>1. When OCDC = 0 the output clock is 50%. Otherwise the clock signal is a pulse with a width of OCDC number of MSDIV output clock periods. The range of OCDC can create pulse widths from 1 to 255 MSDIV output clock periods. When OCxCR2.POL=0, the pulse is high and the signal is low the remainder of the cycle. When POL=1, the pulse is low and the signal is high the remainder of the cycle. See Section 5.7.3.

Note: Rev A devices require MSDIV>5.

Register Name:		OC1PH	OC2PH	OC3PH				
Register Description:		Output Clock x Phase Adjust Register						
Register Address:		OC1: 207h, OC2: 217h, OC3: 227h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	PHADJ[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Phase Adjust Value (PHADJ[7:0]). When OCxCR1.PHEN=1, this field specifies the phase adjustment of the output clock during a phase adjustment event. When OCxCR1.PHEN=0, this field is ignored. The specified phase adjustment occurs once during a phase adjustment event. The format of the field is 2's-complement with the LSB being one half of an HSDIV output clock period. Positive values move the signal later in time (to the right on a scope). See Section 5.7.4.

00000000 = 0.0 UI

00000001 = +0.5 UI

00000010 = +1.0 UI

00000011 = +1.5 UI

…

01111110 = +63.0 UI

01111111 = +63.5 UI

10000000 = –64.0 UI

10000001 = –63.5 UI

…

11111101 = –1.5 UI

11111110 = –1.0 UI

11111111 = –0.5 UI

Register Name:		OC1STOP	OC2STOP	OC3STOP				
Register Description:		Output Clock x Start Stop Register						
Register Address:		OC1: 208h, OC2: 218h, OC3: 228h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	STOP	—	SRC[3:0]				MODE[1:0]	
Default:	0	0	0	0	0	0	0	0

Bit 7: Output Clock Stop (STOP). When SRC=0000, this bit is used to stop the output clock high or low. The output stays stopped while this bit is high. See Section 5.7.5.

0 = Do not stop the output clock

1 = Stop the output clock

Bits 5 to 2: Output Clock Stop Source (SRC[3:0]). This field specifies the source of the stop signal. See Section 5.7.5.

0000 = STOP bit

0001 = The arming of a phase adjustment (signal stopped when PASR.ARMED is asserted; signal started when PASR.ADJL is asserted)

0010 to 0111 = {unused values}

1000 = GPIO0

1001 = GPIO1

1010 = GPIO2

1011 = GPIO3

1100 to 1111 = {unused values}

Bits 1 to 0: Output Clock Stop Mode (MODE[1:0]). This field selects the mode of the start-stop function. See Section 5.7.5.

00 = Never stop

01 = Stop High: stop after rising edge of output clock, start after falling edge of output clock

10 = Stop Low: stop after falling edge of output clock, start after rising edge of output clock

11 = {unused value}

The following table shows which pin(s) stop high or low as specified above for each output signal format:

Signal Format	OCxCR2.OCSF	Pins that Stop as Specified
CML	001 or 010	OCxP
HSTL	011	OCxN
Two CMOS, OCxP in phase with OCxN	100	OCxP and OCxN
One CMOS, OCxN enabled	101	OCxN
One CMOS, OCxP enabled	110	OCxP
Two CMOS, OCxP inverted vs. OCxN	111	OCxN

Note 1: The highest priority condition for an output is when it is stopped and OCxCR2.STOPDIS=1. When this condition occurs both OCxP and OCxN become high-impedance regardless of the state of the control bits mentioned below.

2: When the output is not stopped or when OCxCR2.STOPDIS=0, OCxCR3.NEGLSD=1 causes the OCxN pin to follow the output clock of the low-speed divider uninverted regardless of the signal format, regardless of the state of OCxCR2.POL, and regardless of whether the output is stopped.

3: When the above situations do not apply, OCxCR2.POL=1 changes Stop High to Stop Low and vice versa.

6.3.5 INPUT CLOCK CONFIGURATION REGISTERS

Register Name:		IC1CR1	IC2CR1	IC3CR1				
Register Description:		Input Clock x Configuration Register 1						
Register Address:		IC1: 300h, IC2: 320h, IC3: 340h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	POL	—	—	—	—	HSDIV[1:0]	
Default:	0	0	0	0	0	0	0	0

Bit 6: Locking Polarity (POL). This field specifies which input clock signal edge the APLL will lock to. See Section 5.6.1.

0 = Rising edge

1 = Falling edge

Bits 1 to 0: Input Clock High-Speed Divider (HSDIV[1:0]). This field specifies the divide value for the input clock high-speed divider. See Section 5.6.1.

00 = Divide by 1

01 = Divide by 2

10 = Divide by 4

11 = Divide by 8

6.3.6 NCO/SPREAD SPECTRUM CONFIGURATION REGISTERS

Register Name:		NCSSCR1						
Register Description:		NCO/SS Configuration Register 1						
Register Address:		40Bh						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	MODE[3:0]			
Default:	0	0	0	0	0	0	0	0

Bits 3 to 0: NCO/SS Mode (MODE[3:0]). This field selects the operational mode of the NCO/SS block. See Section 5.5.

0000: Reset

0001: NCO

0010: Spread-spectrum

All other values are invalid.

Register Name:		DFREQZ1						
Register Description:		Digital Frequency Tuning Word Register 1						
Register Address:		420h						
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	FREQZ[7:0]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Digital Frequency Tuning Word (FREQZ[7:0]). The full 40-bit DFREQZ[39:0] field spans this register and the DFREQZ2 to DFREQZ5 registers and is a multi-register field (see Section 6.1.3). This unsigned coefficient is the frequency tuning word value that sets the frequency the NCO/SS block generates in NCO mode. It is also the base frequency to which the NCO/SS adds a dynamic offset during spread spectrum mode. The nominal value of this field is set by the evaluation software. In NCO mode, system software can change this value by any fraction (less than 1 ppb to multiple ppm) to cause a fractional change in the device's output frequency. See Section 5.5.1.

Register Name:	DFREQZ2							
Register Description:	Digital Frequency Tuning Word Register 2							
Register Address:	421h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	FREQZ[15:8]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Digital Frequency Tuning Word (FREQZ[15:8]). See the DFREQZ1 register description.

Register Name:	DFREQZ3							
Register Description:	Digital Frequency Tuning Word Register 3							
Register Address:	422h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	FREQZ[23:16]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Digital Frequency Tuning Word (FREQZ[23:16]). See the DFREQZ1 register description.

Register Name:	DFREQZ4							
Register Description:	Digital Frequency Tuning Word Register 4							
Register Address:	423h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	FREQZ[31:24]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Digital Frequency Tuning Word (FREQZ[31:24]). See the DFREQZ1 register description.

Register Name:	DFREQZ5							
Register Description:	Digital Frequency Tuning Word Register 5							
Register Address:	424h							
—	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	FREQZ[39:32]							
Default:	0	0	0	0	0	0	0	0

Bits 7 to 0: Digital Frequency Tuning Word (FREQZ[39:32]). See the DFREQZ1 register description.

7.0 ELECTRICAL CHARACTERISTICS

TABLE 7-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, nominal 1.8V	VDD18	–0.3	+1.98	V
Supply Voltage, nominal 3.3V	VDD33	–0.3	+3.63	V
Supply voltage, VDDOx (x = 1, 2, 3)	VDDOx	–0.3	+3.63	V
Voltage on XA, any ICxP/N, any OCxP/N pin	VANAPIN	–0.3	+3.63	V
Voltage on any digital I/O pin	VDIGPIN	–0.3	+5.5	V
Storage Temperature Range	T_{ST}	–55	+125	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
*Voltages are with respect to ground (VSS) unless otherwise stated.

Note 1: The typical values listed in the tables of Section 7 are at nominal voltage and room temperature and are not production tested.

2: Specifications to –40°C and +85°C are ensured by design or characterization and not production tested.

TABLE 7-2: RECOMMENDED DC OPERATING CONDITIONS

Min. and max. values in all electrical tables below are over these operating conditions.					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**
Supply Voltage 3.3V	VDD33	3.135	3.3	3.465	V
Supply Voltage 1.8V	VDD18	1.71	1.8	1.89	V
Supply Voltage, VDDOx (x = 1, 2, 3)	VDDOx	1.425	1.5	1.575	V
		1.71	1.8	1.89	
		2.375	2.5	2.625	
		3.135	3.3	3.465	
Operating Temperature	T_A	–40	—	+85	°C

TABLE 7-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units	Notes
Total power, one input and one normal-swing CML output enabled, XA/XB disabled	P_{DISS}	—	0.57	—	W	—
Total current, all 1.8V supply pins, NCO and SSM modes	I_{DD18}	—	242	297	mA	Note 2
Total current, all 3.3V supply pins, NCO and SSM modes	I_{DD33}	—	184	225	mA	Note 2
Total current, all 1.8V supply pins, APLL-only mode	I_{DD18}	—	208	251	mA	Note 2
Total current, all 3.3V supply pins, APLL-only mode	I_{DD33}	—	168	206	mA	Note 2
3.3V supply current change from enabling or disabling the crystal driver circuit	$\Delta I_{DD33XTAL}$	—	16	—	mA	—
3.3V supply current change from enabling or disabling high-speed divider 2	$\Delta I_{DD33HSD}$	—	20	—	mA	—

TABLE 7-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS (CONTINUED)

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units	Notes
1.8V supply current from enabling/disabling per-output mux and dividers using OCEN.OCxEN bit	$\Delta I_{DD18ODIV}$	—	28	—	mA	—
1.8V supply current change from enabling or disabling a CML output, standard swing	$\Delta I_{DD18CML}$	—	10	—	mA	—
3.3V supply current change from enabling or disabling a CML output, standard swing	$\Delta I_{DD33CML}$	—	17	—	mA	—
1.8V supply current change from enabling or disabling a CML output, narrow swing	$\Delta I_{DD18CMLN}$	—	10	—	mA	—
3.3V supply current change from enabling or disabling a CML output, narrow swing	$\Delta I_{DD33CMLN}$	—	9	—	mA	—
1.8V supply current change from enabling or disabling a pair of single-ended outputs	$\Delta I_{DD18CMOS}$	—	2	—	mA	—
VDDOx supply current change from enabling or disabling a pair of single-ended outputs	$\Delta I_{DD33CMOS}$	—	16	—	mA	Note 3
1.8V supply current change from enabling or disabling an input clock	ΔI_{DD18IN}	—	13	—	mA	—

Note 1: Typical values measured at nominal supply voltages and 25°C ambient temperature.

2: Max I_{DD} measurements made with all blocks enabled, 650 MHz signals on IC1 and IC2 inputs, 187.5 MHz signal on IC3, VCO frequency of 3750 MHz, both HSDIV enabled and dividing by 6, all MSDIV dividing by 2, all LSDIV dividing by 2, and all outputs enabled as full-swing CML outputs driving 156.25 MHz signals. NCO or SSM modes: 114.285M XO master clock on XA. APLL-only mode: Crystal driver and doubler off, ensured by design.

3: VDDOx=3.3V, 1x drive strength, f_O = 250 MHz, 2 pF load.

TABLE 7-4: ELECTRICAL CHARACTERISTICS: NON-CLOCK CMOS PINS

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, SCL and SDA	V_{IH}	0.7 x V_{DD33}	—	—	V	—
Input low voltage, SCL and SDA	V_{IL}	—	—	0.3 x V_{DD33}	V	—
Input high voltage, all other digital inputs	V_{IH}	2.0	—	—	V	—
Input low voltage, all other digital inputs	V_{IL}	—	—	0.8	V	—
Input leakage current, RSTN pin	I_{ILPU}	–85	—	10	µA	Note 1
Input leakage current, GPIO3/IC3P pin	I_{ILGP3}	–20	—	20	µA	Note 1
Input leakage current, all other digital inputs	I_{IL}	–10	—	10	µA	Note 1
Input capacitance	C_{IN}	—	3	10	pF	—
Input capacitance, SCL/SCLK, SDA/MOSI	C_{IN}	—	3	11	pF	—
Input hysteresis, SCL and SDA in I^2C Bus Mode	—	0.05 x V_{DD33}	—	—	mV	—

TABLE 7-4: ELECTRICAL CHARACTERISTICS: NON-CLOCK CMOS PINS

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output leakage (when high impedance)	I_{LO}	–10	—	10	µA	Note 1
Output high voltage	V_{OH}	2.4	—	—	V	I_O = –3.0 mA
Output low voltage	V_{OL}	—	—	0.4	V	I_O = 3.0 mA

Note 1: $0V < V_{IN} < V_{DD33}$ for all other digital inputs.

2: V_{OH} does not apply for SCL and SDA in I^2C interface mode because they are open-drain.

TABLE 7-5: ELECTRICAL CHARACTERISTICS: XA CLOCK INPUT

This table covers the case when there is no external crystal connected and an external oscillator or clock signal is connected to the XA pin.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, XA	V_{IH}	1.2	—	—	V	—
Input low voltage, XA	V_{IL}	—	—	0.8	V	—
Input frequency on XA pin, master clock for NCO mode, clock doubler disabled	f_{IN}	80	—	130	MHz	—
Input frequency on XA pin, internally doubled to make master clock for NCO mode	f_{IN}	40	—	65	MHz	—
Input frequency on XA pin, master clock for Spread Spectrum mode, clock doubler disabled	f_{IN}	80	—	130	MHz	—
Input frequency on XA pin, internally doubled to make master clock for Spread Spectrum mode	f_{IN}	55	—	65	MHz	—
Input frequency, XA pin to APLL mux	f_{IN}	9.72	—	156.25	MHz	—
Input frequency, XA pin to HSDIV2 bypass mux	f_{IN}	—	—	156.25	MHz	—
Input leakage current	I_{IL}	–10	—	10	µA	—
Input duty cycle	—	40	—	60	%	—

TABLE 7-6: ELECTRICAL CHARACTERISTICS: CLOCK INPUTS, ICxP/N

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input voltage tolerance (each pin, single-ended)	V_{TOL}	0	—	V_{DD33}	V	Note 1
Input differential voltage	$\|V_{ID}\|$	0.1	—	1.4	V	Note 2
Input DC bias voltage (internally biased)	V_{CMI}	—	1.3	—	V	—
Input frequency, ICx pins	f_{IN}	9.72	—	1250	MHz	Differential, Note 3
		9.72	—	300	MHz	Single-Ended, Note 4
Minimum input clock high, low time	t_H,t_L	—	smaller of 3 ns or 0.3 x 1/ f_{IN}	—	ns	f_{IN} ≤ 250 MHz, Note 5
Minimum input clock high, low time	t_H,t_L	0.4	—	—	ns	f_{IN} > 250 MHz, Note 6
Input resistance, single-ended to VDD18, ICxP or ICxN	$R_{INVDD18}$	—	50	—	kΩ	—
Input resistance, single-ended to VSS, ICxP or ICxN	R_{INVSS}	—	80	—	kΩ	—

Note 1: The device can tolerate voltages as specified in V_{TOL} w.r.t. VSS on its ICxP and ICxN pins without being damaged. For differential input signals, proper operation of the input circuitry is only guaranteed when the other specifications in this table, including $|V_{ID}|$, are met.

2: For inputs IC1P/N and IC2P/N $V_{ID} = V_{ICxP} – V_{ICxN}$. For input IC3P, $V_{ID} = V_{IC3P} – V_{CMI}$. The max. V_{ID} spec only applies when a differential signal is applied on ICxP/N; it does not apply when a single-ended signal is applied on ICxP.

3: **Differential signals.** The differential inputs can easily be interfaced to neighboring ICs driving LVDS, LVPECL, CML, HCSL, HSTL, or other differential signal formats using a few external passive components. In general, Microchip recommends terminating the signal with the termination/load recommended in the neighboring component's data sheet and then AC-coupling the signal into the ICxP/ICxN pins. See Figure 7-2 for details. To connect a differential signal to IC3, AC-couple one side of the signal to IC3P and AC-couple the other side to VSS. For DC-coupling, treat the input as 1.8V CML.

4: **Single-ended signals** can be connected to ICxP pins. Signals with amplitude greater than 2.5V must be DC-coupled. For signals with amplitudes less than 2.5V, Microchip recommends AC-coupling but DC-coupling can also be used. When a single-ended signal is connected to ICxP, ICxN should be connected to a capacitor (0.1 µF or 0.01 µF) to VSS.

5: If MCR1.MCSEL1=1 then IC1 is the NCO/SS block's master clock source and therefore the duty cycle spec in Table 7-5 applies to IC1 rather than the t_H, t_L spec in this table.

6: The input high-speed divider must be used to divide the frequency by 2 or more.

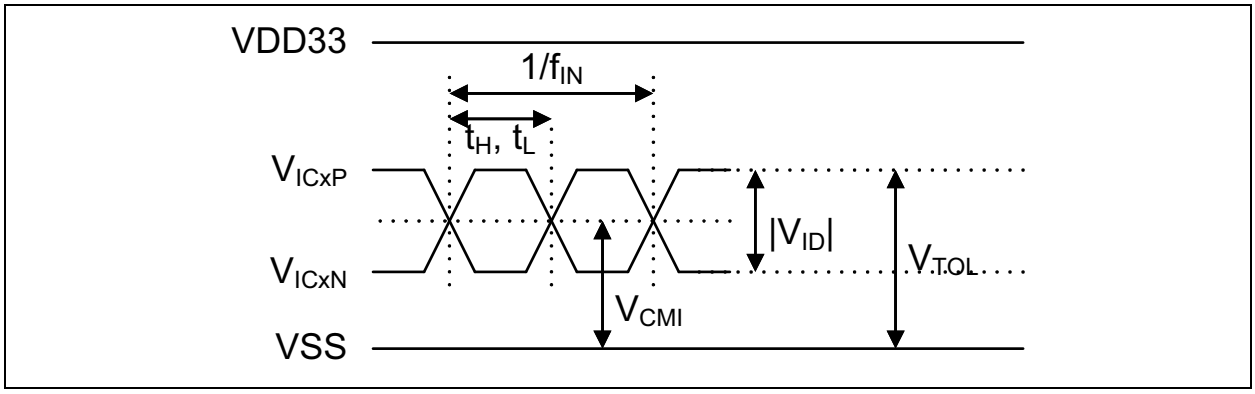


FIGURE 7-1: *Electrical Characteristics: Clock Inputs.*

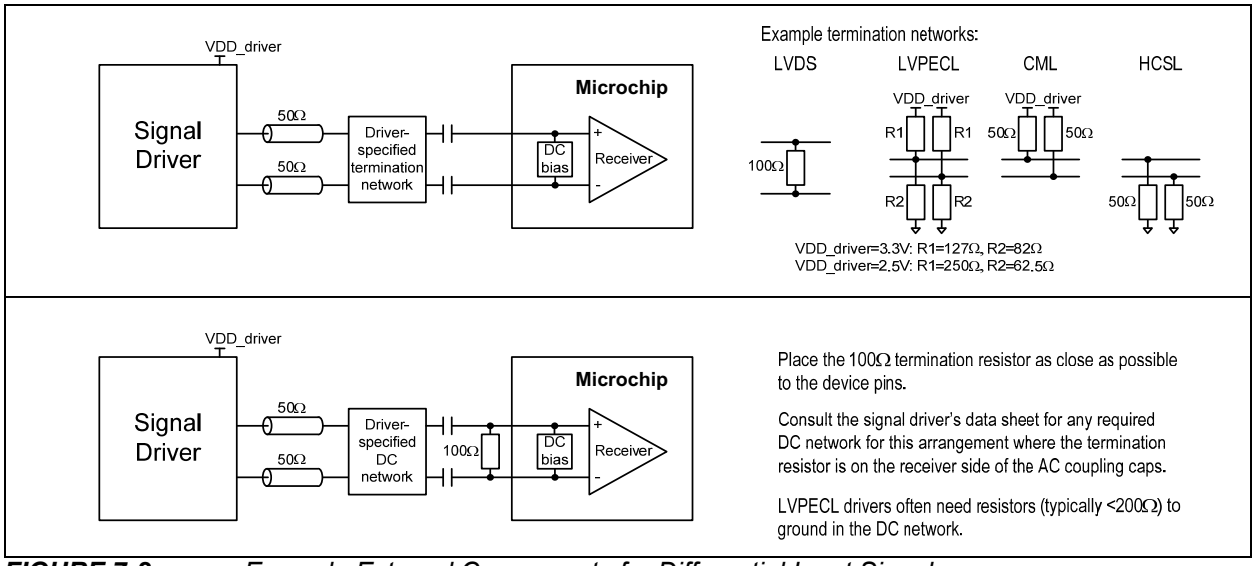


FIGURE 7-2: *Example External Components for Differential Input Signals.*

TABLE 7-7: ELECTRICAL CHARACTERISTICS: CML CLOCK OUTPUTS

VDDOx = 3.3V±5% for CML operation.						
Characteristics	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Output frequency	f_{OCML}	—	—	1035	MHz	—
Output frequency from medium-speed divider	$f_{OCML, MSDIV}$	—	—	425	MHz	—
Output high voltage, single-ended, OCxP or OCxN	$V_{OH,S}$	—	VDDOx – 0.2	—	V	Standard Swing (OCx-CR2.OCSF=1), AC-coupled to 50Ω termination
Output low voltage, single-ended, OCxP or OCxN	$V_{OL,S}$	—	VDDOx – 0.6	—	V	
Output common mode voltage	$V_{CM,S}$	—	VDDOx – 0.4	—	V	
Output differential voltage	$\|V_{OD,S}\|$	320	400	500	mV	
Output differential voltage, peak-to-peak	$\|V_{OD,S,PP}\|$	640	800	1000	mV_{PP}	
Output high voltage, single-ended, OCxP or OCxN	$V_{OH,N}$	—	VDDOx – 0.1	—	V	Narrow Swing (half the power) (OCx-CR2.OCSF=2), AC-coupled to 50Ω termination
Output low voltage, single-ended, OCxP or OCxN	$V_{OL,N}$	—	VDDOx – 0.3	—	V	
Output common mode voltage	$V_{CM,N}$	—	VDDOx – 0.2	—	V	
Output differential voltage	$\|V_{OD,N}\|$	160	200	250	mV	
Output differential voltage, peak-to-peak	$\|V_{OD,N,PP}\|$	320	400	500	mV_{PP}	
Difference in Magnitude of Differential Voltage for Complementary States	V_{DOS}	—	—	50	mV	—

TABLE 7-7: ELECTRICAL CHARACTERISTICS: CML CLOCK OUTPUTS (CONTINUED)

VDDOx = 3.3V±5% for CML operation.						
Characteristics	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Output Rise/Fall Time	t_R, t_F	—	150	—	ps	20% to 80%
Output Duty Cycle	—	45	50	55	%	Note 2
Output Duty Cycle	—	40	—	60	%	Note 3
Output Impedance	R_{OUT}	—	50	—	Ω	Single-Ended, to VDDOx
Mismatch in a pair	ΔR_{OUT}	—	—	10	%	—

Note 1: The differential CML outputs can easily be interfaced to LVDS, LVPECL, CML and other differential inputs on neighboring ICs using a few external passive components. See Figure 7-3 for details.

2: For all HSDIV, MSDIV and LSDIV combinations other than those specified in Note 3.

3: For the case when APLLCR1.HSDIV specifies a half divide and OCxCR1.MSDIV=0 and OCxDIV=0.

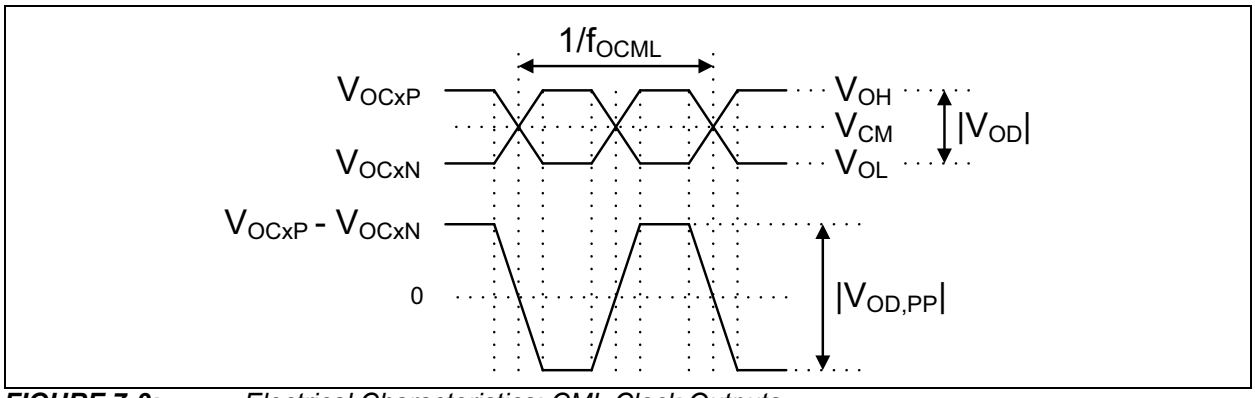


FIGURE 7-3: *Electrical Characteristics: CML Clock Outputs.*

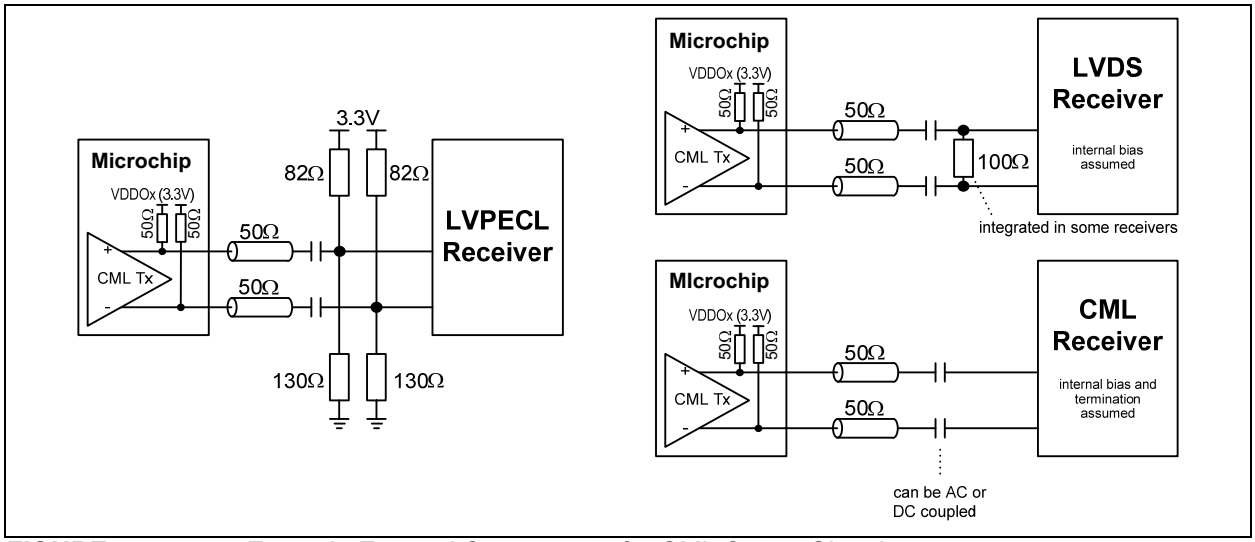


FIGURE 7-4: *Example External Components for CML Output Signals.*

TABLE 7-8: ELECTRICAL CHARACTERISTICS: CMOS AND HSTL (CLASS I) CLOCK OUTPUTS

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCMOS}	<<1 Hz	—	250	MHz	Note 1
Output high voltage	V_{OH}	VDDOx – 0.4	—	VDDOx	V	Note 3, Note 4
Output low voltage	V_{OL}	0	—	0.4	V	Note 3, Note 4
Output rise/fall time, VCCOx = 1.8V, OCxCR2.DRIVE = 4x	t_R, t_F	—	0.4	—	ns	2 pF load
Output rise/fall time, VCCOx = 1.8V, OCxCR2.DRIVE = 4x		—	1.2	—		15 pF load
Output rise/fall time, VCCOx = 3.3V, OCxCR2.DRIVE = 1x		—	0.7	—		2 pF load
Output rise/fall time, VCCOx = 3.3V, OCxCR2.DRIVE = 1x		—	2.2	—		15 pF load
Output duty cycle	—	45	50	55	%	Note 5
Output duty cycle	—	42	50	58	%	Note 6, Note 7
Output duty cycle, OCxNEG single-ended	—	—	50	—	%	Note 6
Output duty cycle, OCxPOS single-ended	—	—	46	—	%	Note 6
Output current when output disabled	—	—	10	—	µA	OCxCR2.OCSF=0

Note 1: Minimum output frequency is a function of VCO frequency and output divider values and is ensured by design.

2: Measured with a series resistor of 33Ω and a 5 pF load capacitance unless otherwise specified.

3: For HSTL Class I, V_{OH} and V_{OL} apply for both unterminated loads and for symmetrically terminated loads, i.e. 50Ω to VDDOx/2.

4: For VDDOx = 3.3V and OCxCR2.DRIVE = 1x, I_O = 4 mA. For VDDOx = 1.5V and OCxCR2.DRIVE = 4x, I_O = 8 mA.

5: Output clock frequency ≤ 160 MHz or VDDOx ≥ 1.8V.

6: Output clock frequency > 160 MHz and VDDOx < 1.8V.

7: Measured differentially.

7.1 Interfacing to HCSL Components

Outputs in HSTL mode with VDDOx = 1.5V or VDDOx = 1.8V can provide an HCSL signal (V_{OH} typ. 0.75V) to a neighboring component when configured as shown in Figure 7-5. For VDDOx = 1.5V the value of R_S should be set to 30Ω and OCxCR2.DRIVE should be set to 4x. For VDDOx = 1.8V the value of R_S should be set to 20Ω and OCxCR2.DRIVE should be set to 2x.

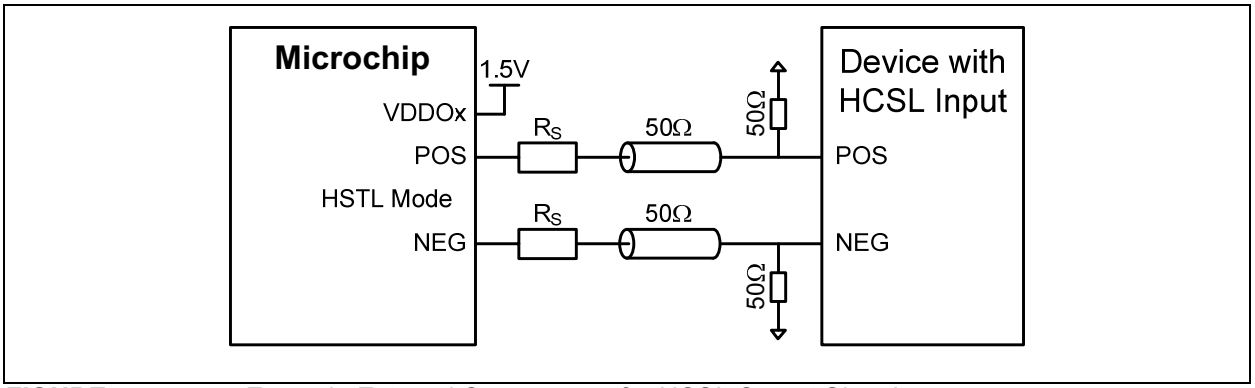


FIGURE 7-5: *Example External Components for HCSL Output Signals.*

TABLE 7-9: ELECTRICAL CHARACTERISTICS: APLL FREQUENCIES

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
APLL VCO frequency range	f_{VCO}	3715	—	4180	MHz	—
APLL PFD input frequency	f_{PFD}	9.72	—	156.25	MHz	—

TABLE 7-10: ELECTRICAL CHARACTERISTICS: JITTER SPECIFICATIONS

Characteristics	Min.	Typ.	Max.	Units	Notes
Output Phase Jitter, 622.08 MHz	—	0.16	0.225	ps_{RMS}	Note 1, Note 2
Output Phase Jitter, 625 MHz, (1.875 MHz to 20 MHz)	—	0.06	—	ps_{RMS}	Note 4
Output Period Jitter	—	8	—	ps_{PP}	N = 10,000, Note 5
Output Half-Period Jitter	—	14	—	ps_{PP}	N = 10,000, Note 5
Output Cycle-to-Cycle Jitter	—	7.5	—	ps_{PK}	N = 10,000, Note 5
Jitter Transfer Bandwidth	—	600	—	kHz	Note 3
Bypass Path Additive Jitter, 100 MHz in/out	—	0.18	—	ps_{RMS}	12 kHz to 20 MHz

Note 1: Jitter calculated from integrated phase noise from 12 kHz to 20 MHz.

2: Tested with 155.52 MHz XO (Vectron VCC1) connected to IC1, APLL VCO frequency 3732.48 MHz, HSDIV1=6, OC1 frequency 622.08 MHz.

3: APLL bandwidth and damping factor can be field configured over a limited range. Contact the factory for details.

4: With 50 MHz crystal doubled as APLL input. Jitter calculated from integrated phase noise from 1.875 MHz to 20 MHz.

5: Outputs from a half-divide (e.g. 4.5) in the high-speed divider followed by only an odd divide in the medium-speed divider can have higher jitter values. Example: 100 MHz from VCO = 3750 MHz, HSDIV1=7.5, MSDIV=5 has typical period jitter of 16 ps, typical cycle-to-cycle jitter of 15 ps and typical half-period jitter of 58 ps.

TABLE 7-11: ELECTRICAL CHARACTERISTICS: TYPICAL OUTPUT JITTER PERFORMANCE

Output Frequency	Output Jitter, ps_{RMS} 125 MHz XO Reference (Note 1)	Output Jitter, ps_{RMS} 50 MHz Crystal Reference (Note 2)
625 MHz	0.155	0.185
156.25 MHz	0.18	0.21
125 MHz	0.19	0.21
25 MHz CMOS	0.26	0.28
622.08 MHz	0.25	0.27
155.52 MHz	0.27	0.315
622.08 MHz * 255/237	0.26	0.29
155.52 MHz * 255/237	0.275	0.30
614.4 MHz	0.25	0.28
153.6 MHz	0.28	0.32

Note 1: APLL locked to external 125 MHz XO (Vectron VCC1-1535-125M000).

2: APLL locked to external 50 MHz crystal (TXC 7M50070021), internal doubler enabled when multiplication is fractional.

3: All signals are differential unless otherwise stated. Jitter is integrated 12 kHz to 5 MHz for 25 MHz output frequency and 12 kHz to 20 MHz for all other output frequencies.

TABLE 7-12: ELECTRICAL CHARACTERISTICS: TYPICAL INPUT-TO-OUTPUT CLOCK DELAY

Mode	Delay, Input Clock Edge to Output Clock Edge
All Modes	Non-deterministic but constant as long as the APLL remains locked and output clock phases are not adjusted as described in Section 5.7.4.1.

TABLE 7-13: ELECTRICAL CHARACTERISTICS: TYPICAL OUTPUT-TO-OUTPUT CLOCK DELAY

Mode	Delay, Output Clock Edge to Output Clock Edge
All Modes	<100ps Requires phase adjustment and phase alignment capability described in Section 5.7.4.

TABLE 7-14: ELECTRICAL CHARACTERISTICS: SPI CLIENT INTERFACE TIMING, DEVICE REGISTERS

Characteristics (Note 1 to Note 3)	Symbol	Min.	Typ.	Max.	Units	Notes
SCLK frequency	f_{BUS}	—	—	10	MHz	—
SCLK cycle time	t_{CYC}	100	—	—	ns	—
CSN setup to first SCLK edge	t_{SUC}	50	—	—	ns	—
CSN hold time after last SCLK edge	t_{HDC}	50	—	—	ns	—
CSN high time	t_{CSH}	50	—	—	ns	—
SCLK high time	t_{CLKH}	40	—	—	ns	—
SCLK low time	t_{CLKL}	40	—	—	ns	—
MOSI data setup time	t_{SUI}	10	—	—	ns	—
MOSI data hold time	t_{HDI}	10	—	—	ns	—
MISO enable time from SCLK edge	t_{EN}	0	—	—	ns	—
MISO disable time from CSN high	t_{DIS}	—	—	80	ns	—
MISO data valid time	t_{DV}	—	—	40	ns	—
MISO data hold time from SCLK edge	t_{HDO}	0	—	—	ns	—
CSN, MOSI input rise time, fall time	t_R, t_F	—	—	10	ns	—

Note 1: All timing is specified with 100 pF load on all SPI pins.

2: All parameters in this table are ensured by design or characterization.

3: See timing diagram in Figure 7-6.

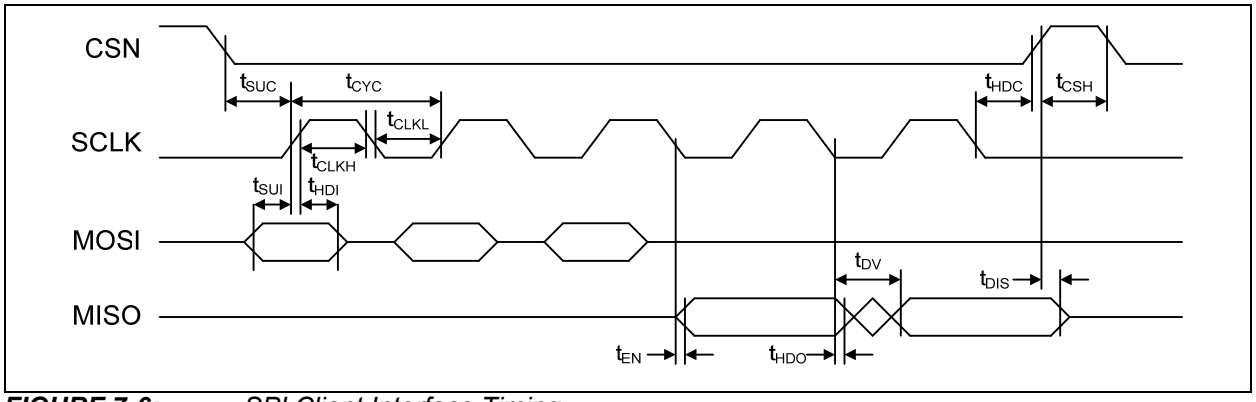


FIGURE 7-6: *SPI Client Interface Timing.*

TABLE 7-15: ELECTRICAL CHARACTERISTICS: SPI CLIENT INTERFACE TIMING, INTERNAL EEPROM (ZL30251 ONLY)

Characteristics (Note 1 to Note 4)	Symbol	Min.	Typ.	Max.	Units	Notes
SCLK frequency	f_{BUS}	—	—	10	MHz	—
SCLK cycle time	t_{CYC}	100	—	—	ns	—
CSN setup to first SCLK edge	t_{SUC}	50	—	—	ns	—
CSN hold time after last SCLK edge	t_{HDC}	51	—	—	ns	—
CSN high time	t_{CSH}	51	—	—	ns	—
SCLK high time	t_{CLKH}	41	—	—	ns	—
SCLK low time	t_{CLKL}	41	—	—	ns	—
MOSI data setup time	t_{SUI}	11	—	—	ns	—
MOSI data hold time	t_{HDI}	11	—	—	ns	—
MISO enable time from SCLK edge	t_{EN}	0	—	—	ns	—
MISO disable time from CSN high	t_{DIS}	—	—	90	ns	—
MISO data valid time	t_{DV}	—	—	60	ns	—
MISO data hold time from SCLK edge	t_{HDO}	0	—	—	ns	—
CSN, MOSI input rise time, fall time	t_R, t_F	—	—	10	ns	—

Note 1: This timing applies (a) when EESEL=1 and (b) in direct EEPROM write mode (see Section 5.12.2).

2: All timing is specified with 100 pF load on all SPI pins.

3: All parameters in this table are ensured by design or characterization.

4: See timing diagram in Figure 7-6.

TABLE 7-16: ELECTRICAL CHARACTERISTICS: SPI SERVER INTERFACE TIMING (ZL30250 ONLY)

Characteristics (Note 1 to Note 3)	Symbol	Min.	Typ.	Max.	Units	Notes
SCLK output frequency	f_{BUS}	—	—	5	MHz	—
SCLK output cycle time	t_{CYC}	200	—	—	ns	—
SCLK output duty cycle	t_{CLKH}/t_{CYC}	45	50	55	%	—
CSN output setup to first SCLK rising edge	t_{SUC}	200	—	—	ns	—
CSN output hold after last SCLK falling edge	t_{HDC}	200	—	—	ns	—
CSN output high time	t_{CSH}	200	—	—	ns	—
MISO input setup time to SCLK rising edge	t_{SU}	15	—	—	ns	—
MISO input hold time from SCLK rising edge	t_{HD}	5	—	—	ns	—
MOSI output valid from SCLK falling edge	t_{DV}	—	—	10	ns	—
SCLK, CSN, MOSI output rise time, fall time	t_R, t_F	—	—	15	ns	—
MISO input rise time, fall time	t_R, t_F	—	—	10	ns	—

Note 1: All timing is specified with 100 pF load on all SPI pins.

2: All parameters in this table are ensured by design or characterization.

3: See timing diagram in Figure 7-7.

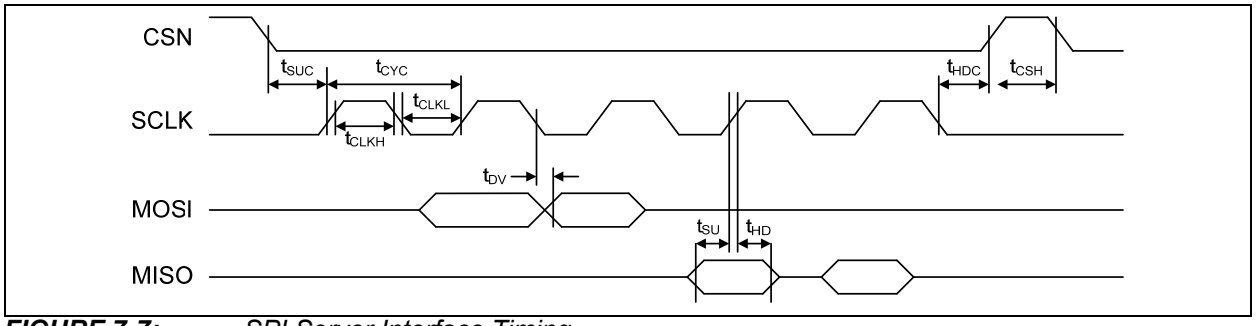


FIGURE 7-7: *SPI Server Interface Timing.*

TABLE 7-17: ELECTRICAL CHARACTERISTICS: I²C CLIENT INTERFACE TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
SCL clock frequency	f_{SCL}	—	—	400	kHz	—
Hold time, START condition	$t_{HD:STA}$	0.6	—	—	µs	—
Low time, SCL	t_{LOW}	1.3	—	—	µs	—
High time, SCL	t_{HIGH}	0.6	—	—	µs	—
Setup time, START condition	$t_{SU:STA}$	0.6	—	—	µs	—
Data hold time	$t_{HD:DAT}$	0	—	0.9	µs	Note 2, Note 3
Data setup time	$t_{SU:DAT}$	100	—	—	ns	—
Rise time	t_R	—	—	—	ns	Note 4
Fall time	t_F	20 + 0.1C_b	—	300	ns	C_b is the capacitor of one bus line
Setup time, STOP condition	$t_{SU:STO}$	0.6	—	—	µs	—
Bus free time between STOP/ START	t_{BUF}	1.3	—	—	µs	—
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	—	50	ns	—

Note 1: The timing parameters in this table are specifically for 400 kbps Fast Mode. Fast Mode devices are downward-compatible with 100 kbps Standard Mode I²C bus timing. All parameters in this table are guaranteed by design or characterization. All values referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels (see Table 7-4).

2: The device internally provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.

3: The I²C specification indicates that the maximum $t_{HD:DAT}$ spec only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. The device does not stretch the low period of the SCL signal.

4: Determined by choice of pull-up resistor.

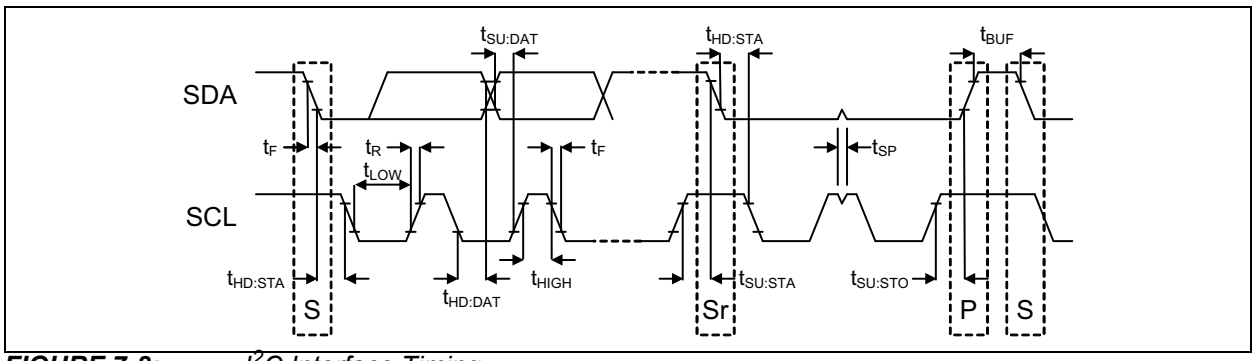


FIGURE 7-8: *I²C Interface Timing.*

TABLE 7-18: 5 MM X 5 MM VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Conditions	Value
Maximum Ambient Temperature	T_A	—	85°C
Maximum Junction Temperature	$T_{J(MAX)}$	—	125°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	Still Air	29.6°C/W
		1 m/s Airflow	23.3°C/W
		2.5 m/s Airflow	20.6°C/W
Junction to Board Thermal Resistance	θ_{JB}	—	9.8°C/W
Junction to Case Thermal Resistance	θ_{JC}	—	17.5°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	Still Air	3.4°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still Air	0.2°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

3: For all numbers in the table, the exposed pad is connected to the ground plane with a 5 mm x 5 mm array of thermal vias; via diameter 0.33 mm; via pitch 0.76 mm.

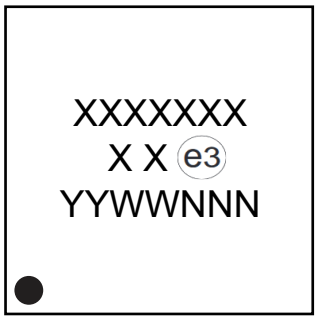
8.0 ACRONYMS AND ABBREVIATIONS

- APLL: analog phase locked loop
- CML: current mode logic
- GbE: gigabit Ethernet
- HCSL: high-speed current steering logic
- HSTL: high-speed transceiver logic
- I/O: input/output
- LVDS: low-voltage differential signal
- LVPECL: low-voltage positive emitter-coupled logic
- PFD: phase/frequency detector
- PLL: phase locked loop
- ppb: parts per billion
- ppm: parts per million
- pk-pk: peak-to-peak
- RMS: root-mean-square
- RO: read-only
- R/W: read/write
- SS or SSM: spread spectrum modulation
- TCXO: temperature-compensated crystal oscillator
- UI: unit interval
- UIPP or UIP-P: unit interval, peak to peak
- XO: crystal oscillator

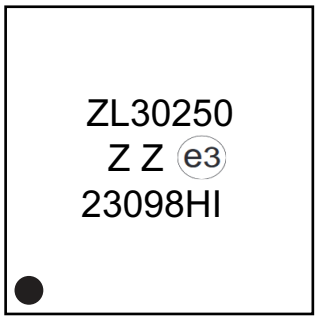
9.0 PACKAGE OUTLINE

9.1 Package Marking Information

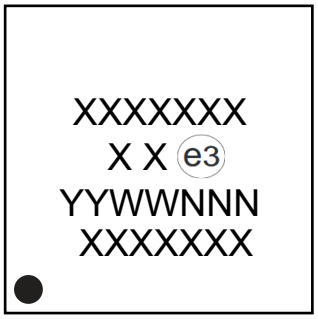
32-Lead VQFN*
(Standard Device)



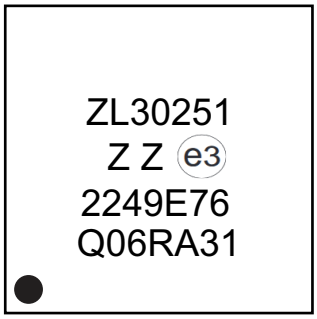
Example



32-Lead VQFN*
(Custom Device)



Example



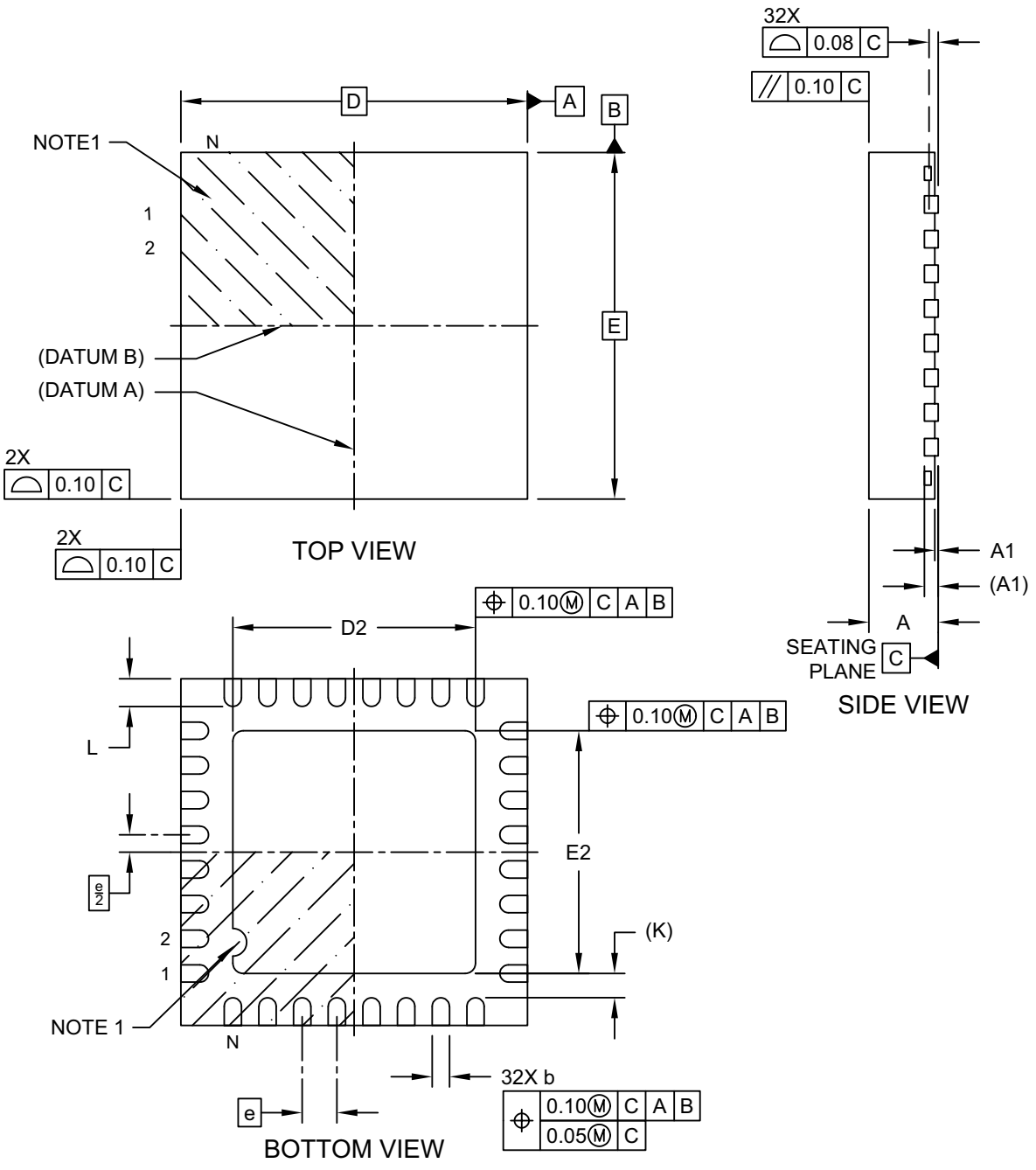
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

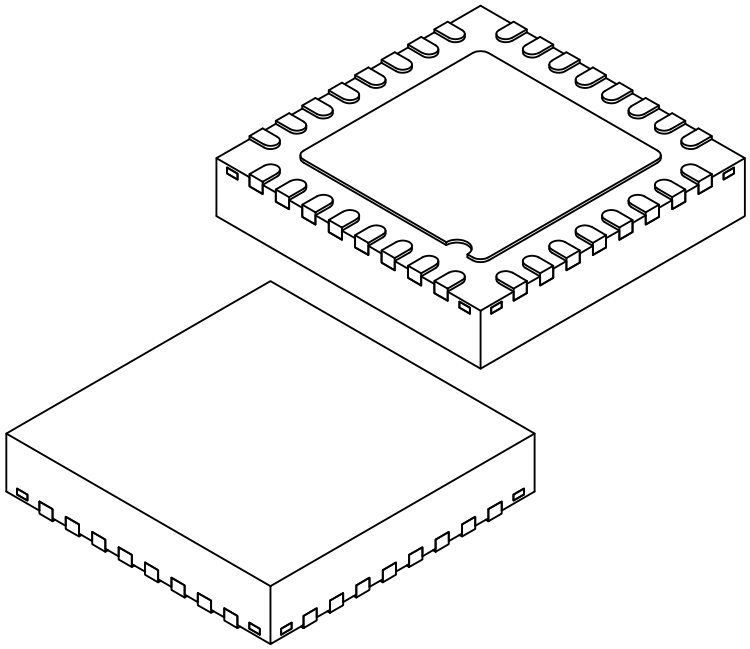
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25401 Rev A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.40	3.50	3.60
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.40	3.50	3.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.35 REF	

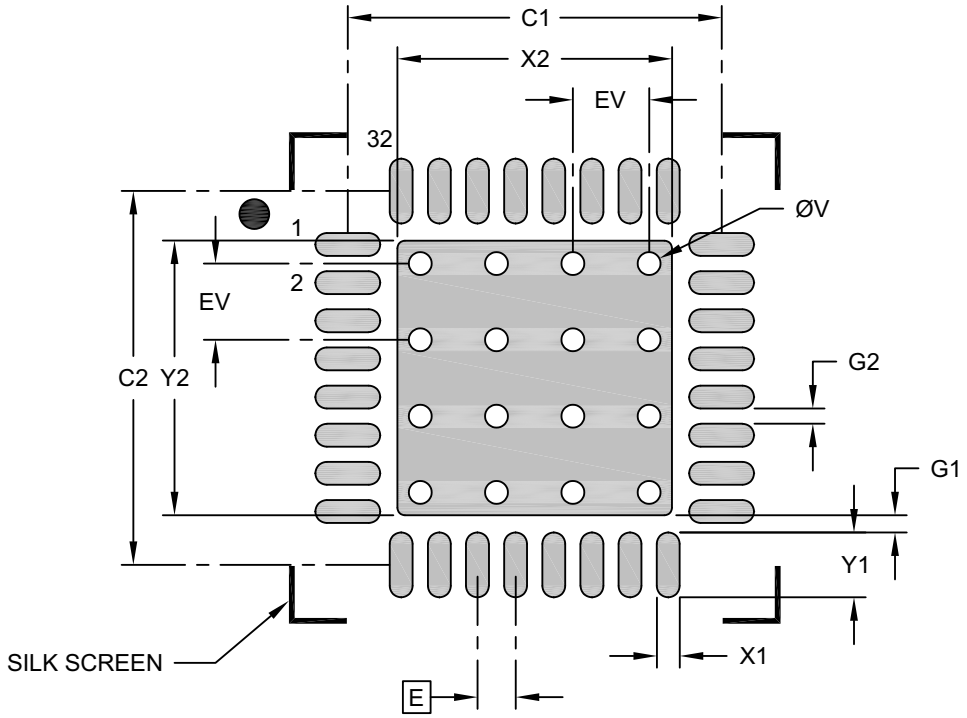
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25401 Rev A Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.60
Optional Center Pad Length	Y2			3.60
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27401 Rev A

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006780A (04-28-23)	—	Converted Microsemi data sheet ZL30250/ZL30251 to Microchip DS20006780A. Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL30250: 4-Input, 3-Output Any-to-Any Clock Multiplier and Frequency Synthesizer, External EEPROM ZL30251: 4-Input, 3-Output Any-to-Any Clock Multiplier and Frequency Synthesizer, Internal EEPROM
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 32-Lead 5 mm x 5 mm VQFN
Media Type:	G = 490/Tray F = 4000/Reel
Finish:	1 = Pb-Free, Matte Tin (Sn) Finish

Examples:

a) ZL30250LDG1:

4-Input, 3-Output Any-to-Any Clock Multiplier and Frequency Synthesizer, External EEPROM, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 490/Tray, Pb-Free Matte Tin (Sn) Finish

b) ZL30250LDF1:

4-Input, 3-Output Any-to-Any Clock Multiplier and Frequency Synthesizer, External EEPROM, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 4000/Reel, Pb-Free Matte Tin (Sn) Finish

c) ZL30251LDG1:

4-Input, 3-Output Any-to-Any Clock Multiplier and Frequency Synthesizer, Internal EEPROM, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 490/Tray, Pb-Free Matte Tin (Sn) Finish

d) ZL30251LDF1:

4-Input, 3-Output Any-to-Any Clock Multiplier and Frequency Synthesizer, Internal EEPROM, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 4000/Reel, Pb-Free Matte Tin (Sn) Finish

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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