



ZL30270 - ZL30271

6- or 10-Output, 5-Synthesizer Clock Generators

Features

Highlights

- Any-to-any frequency conversion
- Five output frequency synthesizers
- Inputs: crystal or CMOS input clock
- Outputs: up to 10 differential, up to 20 CMOS
- Output jitter $100 f_{s_{RMS}}$ typical for 156.25 MHz
12 kHz to 20 MHz
- Core power consumption <0.9W

Input Clocks

- Crystal: 24 MHz to 60 MHz
- OSCB: CMOS 10 MHz to 400 MHz

Output Clocks

- Any frequency 0.5 Hz to 750 MHz
- Each OUTP/N pair can be LVDS, LVPECL, 2xC-MOS, Low- V_{CM} , or programmable differential
- In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125 MHz and 25 MHz)
- VDD per output pair, CMOS voltages 1.8V to 3.3V
- Per-synth phase adjustment, 1 ps resolution
- Per-output duty cycle adjustment
- Precise output alignment circuitry and per-output phase adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)

General Features

- Automatic self-configuration at power-up from internal Flash memory, 7 configurations
- Numerically controlled oscillator behavior in each synthesizer
- Easy-to-configure design requires no external VCXO or loop filter components
- 5 GPIO pins with many possible behaviors, each OUT can be GPO
- SPI or I²C processor Interface
- 1.8V and 3.3V core VDD voltages
- 48-Lead 7 mm x 7 mm VQFN Package (ZL30270)
- 64-Lead 9 mm x 9 mm VQFN Package (ZL30271)
- Easy-to-use evaluation/programming software

Applications

- Frequency conversion and frequency synthesis in a wide variety of equipment types

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1.0 BLOCK DIAGRAM

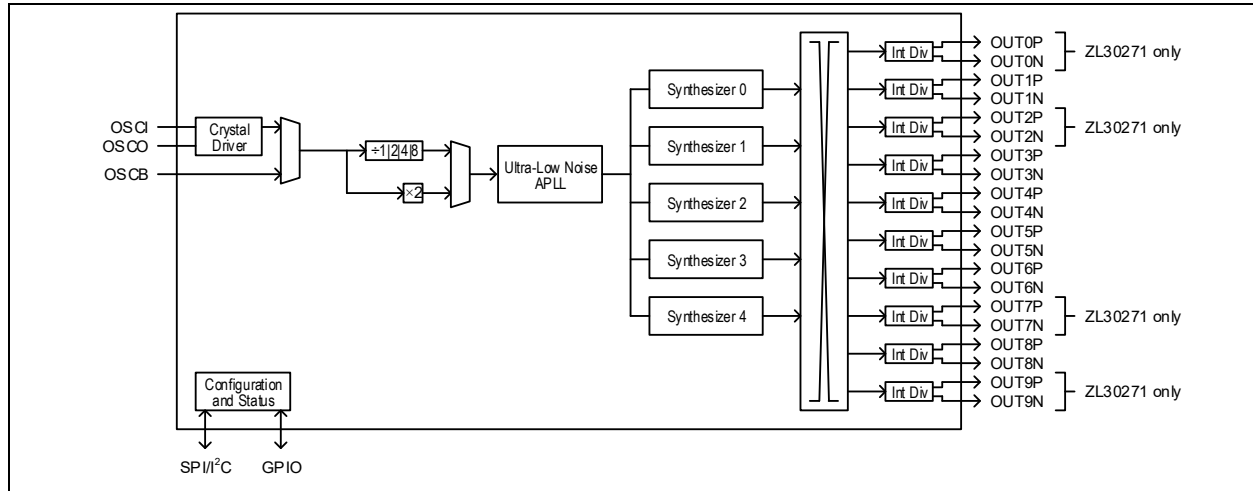


FIGURE 1-1: Functional Block Diagram.

2.0 DETAILED FEATURES

2.1 General

- Operates from a single crystal resonator or clock oscillator
 - ≥48 MHz for lowest jitter
 - 9.72 MHz to 400 MHz total frequency range
- Configurable via SPI or I²C interface
- Internal nonvolatile memory
 - Factory-configurable power-on configuration
 - Multiple time writeable/re-writeable
- Default settings can be overridden using SPI/I²C

2.2 Synthesizer Features

- Five next-generation low-jitter, low-power, any-frequency synthesizers
- A total of five output frequency families
- Any-to-any frequency conversion with 0 ppm error
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Jitter suitable for OC-192, STM-64, and 1G, 10G, 40G, 100G, and 400G Ethernet jitter requirements

2.3 Output Clock Features

- ZL30270: Up to 12 single-ended outputs, up to 6 differential outputs, from any synthesizer
- ZL30271: Up to 20 single-ended outputs, up to 10 differential outputs, from any synthesizer
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 0.5 Hz to 750 MHz (250 MHz max for CMOS)
- Output jitter 100 fs_{RMS} typical for 156.25 MHz and many other frequencies (12 kHz to 20 MHz)
- In CMOS mode, the OUTxN frequency can be an integer divisor of the OUTxP frequency (Example 1: OUT3P 125 MHz, OUT3N 25 MHz. Example 2: OUT2P 25 MHz, OUT2N 1 Hz)
- Outputs directly interface (DC-coupled) with LVDS, LVPECL, HCSL, and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs, and other components
- Can produce PCIe Gen 1 to 5 clocks

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- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1 ps resolution
- Per-output phase adjustment to accommodate trace delays or compensate for system routing paths
- Per-output duty cycle/pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)
- Each OUT pin can be a GPO (general-purpose output)

2.4 General Features

- Automatic self-configuration at power-up from internal Flash memory
- Generates output SYNC signals: 1PPS (IEEE 1588), 2 kHz or 8 kHz (SONET/SDH), or other frequency
- JESD204B clocking: clock and SYSREF signal generation with skew adjustment
- Numerically controlled oscillator (NCO) behavior allows system software to steer synthesizer frequency with resolution better than 0.005 ppt
- Spread-spectrum modulation available in each synthesizer (PCIe compliant)
- Five general-purpose I/O pins each with many possible status and control options
- SPI or I²C serial microprocessor interface

2.5 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts
- Works with or without an evaluation board

3.0 PIN DIAGRAMS

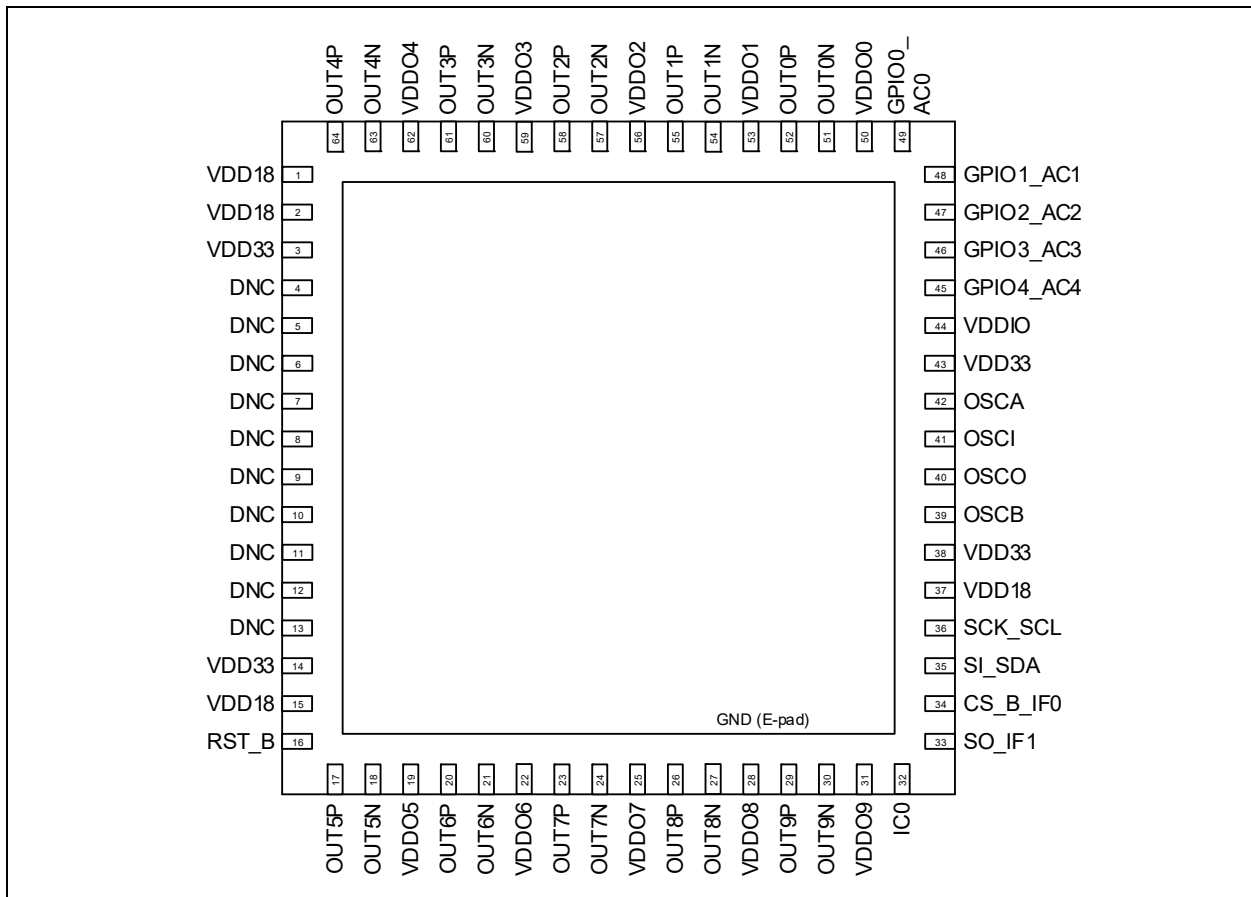


FIGURE 3-1: 64-Lead 9 mm x 9 mm VQFN (0.5 mm pitch) for ZL30271.

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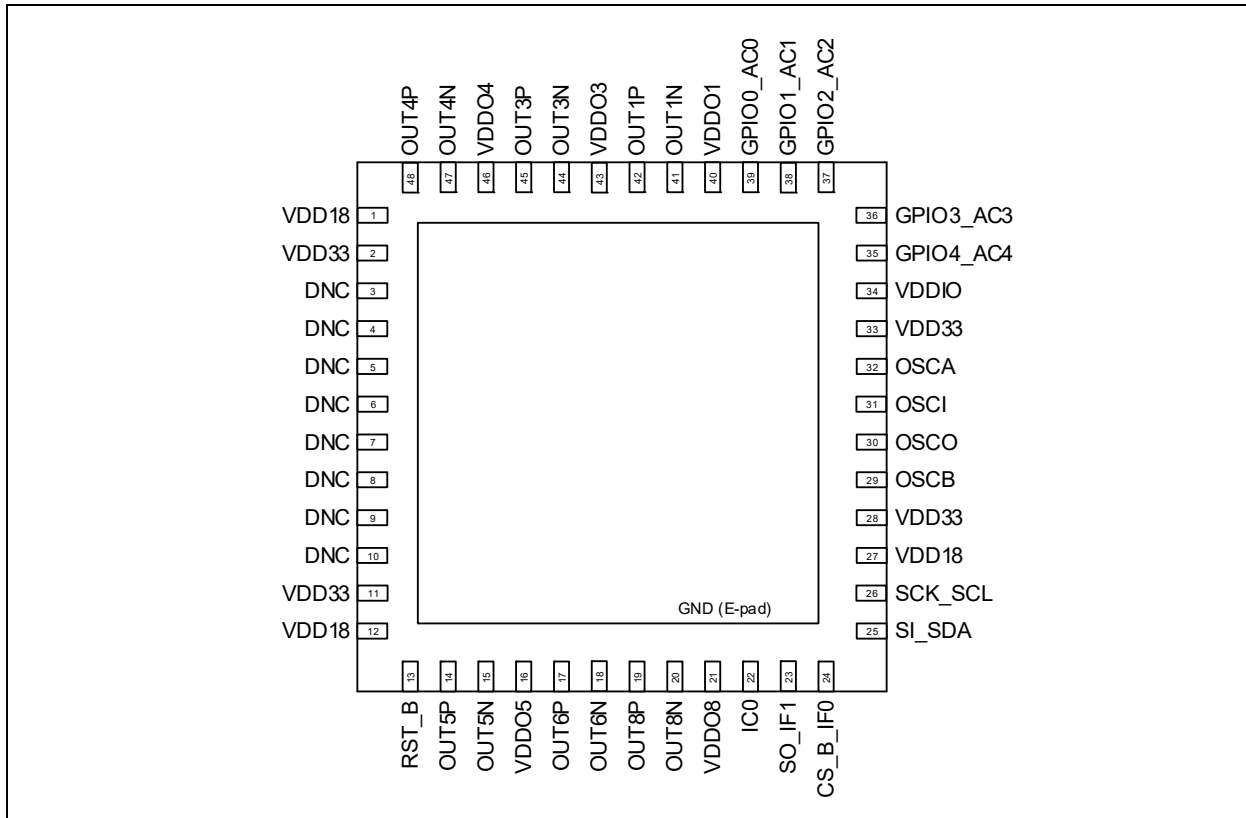


FIGURE 3-2: 48-Lead 7 mm x 7 mm VQFN (0.5 mm pitch) for ZL30270.

4.0 PIN DESCRIPTIONS

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, I_{PU} – input with internal pull-up resistor, I_{OPD} – input/output with internal pull-down resistor, O – output, A – analog, P – power supply pin. All GPIO and SPI/I²C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

TABLE 4-1: PIN DESCRIPTIONS

| 7x7 Pin Number | 9x9 Pin Number | Pin Name | Type | Description |
|---------------------------|----------------|----------|-----------------|--|
| Output Clocks | | | | |
| — | 52 | OUT0P | O | <p>Outputs Clocks LVDS, LVPECL, programmable differential, Low-V_{CM} differential (HCSL-like) or 1 or 2 CMOS. Programmable frequency and drive strength. Programmable common-mode voltage and signal amplitude in programmable differential mode. See Figure 5-1 for example external interface circuitry.</p> <p>See Table 9-6, Table 9-7, and Table 9-8 for electrical specifications for LVDS, LVPECL, and Low-V_{CM} signal format, respectively.</p> <p>See Table 9-9 for electrical specifications for interfacing to CMOS inputs on neighboring devices.</p> <p>Microchip does not recommend using an output clock from this device as a system clock for the processor that controls this device. In some scenarios output clocks are not available from the device, such as during device reset after firmware upgrade.</p> <p>For the 7 mm x 7 mm VQFN package only: OUT6P/N and OUT8P/N share power supply pin VDDO8 which makes crosstalk worse between these outputs when they are different frequencies. When OUT6 and OUT8 must be low jitter Microchip recommends they follow the same synthesizer and are the same frequency or the frequency of one is an integer divide of the other.</p> |
| — | 51 | OUT0N | | |
| 42 | 55 | OUT1P | | |
| 41 | 54 | OUT1N | | |
| — | 58 | OUT2P | | |
| — | 57 | OUT2N | | |
| 45 | 61 | OUT3P | | |
| 44 | 60 | OUT3N | | |
| 48 | 64 | OUT4P | | |
| 47 | 63 | OUT4N | | |
| 14 | 17 | OUT5P | | |
| 15 | 18 | OUT5N | | |
| 17 | 20 | OUT6P | | |
| 18 | 21 | OUT6N | | |
| — | 23 | OUT7P | | |
| — | 24 | OUT7N | | |
| 19 | 26 | OUT8P | | |
| 20 | 27 | OUT8N | | |
| — | 29 | OUT9P | | |
| — | 30 | OUT9N | | |
| Control and Status | | | | |
| 13 | 16 | RST_B | I _{PU} | <p>Power-on Reset. A logic low at this input resets the device. To ensure proper operation, the device must be reset <u>after</u> power-up by <u>driving</u> the RST_B pin low. The RST_B pin should be held low for at least 2 ms. This pin has an internal 85 kΩ pull-up to VDD33 (not VDDIO). Device registers can be accessed either 500 ms after RST_B goes high or after bit 7 in register at address 0x00 goes high. Note that the supply rail for RST_B is VDD33 not VDDIO.</p> <p>When the host interface is I²C, Microchip recommends RST_B be wired to a general-purpose output pin on an FPGA, microcontroller or other software-controlled component.</p> |

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TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

| 7x7 Pin Number | 9x9 Pin Number | Pin Name | Type | Description |
|---|----------------|-----------|------------------|---|
| 39 | 49 | GPIO0_AC0 | IO _{PD} | <p>General Purpose I/O / Auto-Configuration</p> <p>General-Purpose I/O: These are general-purpose pins with many possible uses, including:</p> <ul style="list-style-type: none"> • Status indicators • Interrupt Output: indicates changes of device status prompting system software to read the interrupt service registers (ISR). <p>These pins have internal pull-down resistors (80 kΩ typical). Each pull-down can be disabled by a register field. If not used, GPIO can be left unconnected.</p> <p>Auto-Configuration: On the rising edge of RST_B GPIO3_AC3 and GPIO4_AC4 must be 0 for normal operation, and GPIO0_AC0 to GPIO2_AC2 behave as auto-configuration pins to specify a custom configuration stored in internal Flash.</p> <p>000 = configuration 0 001 = configuration 1 010 = configuration 2 011 = configuration 3 100 = configuration 4 101 = configuration 5 110 = configuration 6 111 = factory default state (no configuration)</p> <p>If the specified configuration is empty in internal flash then the device powers up in factory default state.</p> <p>Legacy recommendation: When the host interface is I²C, Microchip recommends GPIO3 be wired to a 1 kΩ resistor to ground and to a general-purpose output pin on an FPGA, microcontroller or other software-controlled component.</p> <p>Latest recommendation: Regardless of host interface type, Microchip recommends all five GPIO pins be wired to GPIO pins on an FPGA, microcontroller or other software-controlled component.</p> |
| 38 | 48 | GPIO1_AC1 | | |
| 37 | 47 | GPIO2_AC2 | | |
| 36 | 46 | GPIO3_AC3 | | |
| 35 | 45 | GPIO4_AC4 | | |
| Host Interface (SPI or I²C) | | | | |
| 26 | 36 | SCK_SCL | I/O | <p>SPI Clock/I²C Clock</p> <p><i>SPI Clock:</i> An external SPI controller must provide the SPI clock signal on SCK.</p> <p><i>I²C Clock:</i> An external I²C controller must provide the I²C clock signal on the SCL pin. This pin should be externally pulled high by 1 kΩ to 5 kΩ resistor. See the I²C bus specification for sizing guidance for this resistor, referred to as RP in that specification.</p> <p>This pin has an internal pull-up (typical 85 kΩ) to VDDIO.</p> |
| 25 | 35 | SI_SDA | I/O | <p>SPI Data In/I²C Data</p> <p><i>SPI Data In:</i> An external SPI controller sends commands, addresses and data to the device on SI.</p> <p><i>I²C Data:</i> SDA is the bidirectional data line between the device and an external I²C controller. This pin should be externally pulled high by 1 kΩ to 5 kΩ resistor. See the I²C bus specification for sizing guidance for this resistor, referred to as RP in that specification.</p> <p>This pin has an internal pull-up (typical 85 kΩ) to VDDIO.</p> |

TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

| 7x7 Pin Number | 9x9 Pin Number | Pin Name | Type | Description |
|-------------------------------|----------------|----------|-----------------|---|
| 23 | 33 | SO_IF1 | I/O | SPI Data Out/Interface Mode 1 <i>SPI Data Out:</i> After reset this pin is SO. The device outputs data to an external SPI controller on SO during SPI read transactions. <i>Interface Mode:</i> On the rising edge of RST_B this pin behaves as IF1. In I ² C interface mode IF1 specifies bit 0 of the I ² C device address. In SPI interface mode IF1 is ignored. The interface mode is set by the CS_B_IF0 pin state on the rising edge of RST_B. See Section 7.0, "Host Interface" . |
| 24 | 34 | CS_B_IF0 | I _{PU} | SPI Chip Select (Active Low)/Interface Mode 0 <i>SPI Chip Select:</i> After reset this pin is CS_B. An external SPI controller must assert (low) CS_B to access device registers. CS_B should not be allowed to float. <i>Interface Mode:</i> On the rising edge of RST_B this pin behaves as IF0: 0=I ² C, 1=SPI. This pin has an internal pull-up (typical 85 kΩ) to VDDIO. |
| Crystal or Input Clock | | | | |
| 31 | 41 | OSCI | A-I | Crystal Pins (Jitter Reference) <i>Crystal:</i> An on-chip crystal driver circuit is designed to work with an external crystal connected to the OSCI and OSCO pins. See Section 5.3.2 for crystal characteristics and recommended external components. <i>Input Clock:</i> Wire OSCI to a 1 kΩ resistor to ground. Leave OSCO unconnected. |
| 30 | 40 | OSCO | A-O | |
| 32 | 42 | OSCA | P | Crystal Oscillator Guard Pin This pin is internally connected to crystal driver circuit ground. <i>Crystal:</i> Wire OSCA to a top-layer ring around the external crystal and a layer-2 island under the ring, the crystal and the OSCA, OSCI, OSCO, and OSCB pins. Void all other PCB layers under the layer-2 island. See Section 5.3.2 for details. <i>Input Clock:</i> Leave OSCA unconnected. |
| 29 | 39 | OSCB | A-I | System Clock Input (Jitter Reference) <i>Crystal:</i> When a crystal is connected to the OSCI and OSCO pins, wire OSCB to the ring and layer-2 island that are connected to OSCA. <i>Input Clock:</i> An external single-ended local oscillator or clock signal can be connected to the OSCB pin. This is a design alternative instead of a crystal connected to OSCI and OSCO. Only one crystal or clock signal should be wired to the OSC* pins at a time. |
| Miscellaneous | | | | |
| 22 | 32 | IC0 | A-I/O | Internal Connection. Leave unconnected. Do not attach to any routing. |
| Power and Ground | | | | |
| 1 | 1 | VDD18 | P | Core Power Supply. 1.8V ±5%. |
| — | 2 | | | |
| 12 | 15 | | | |
| 27 | 37 | | | |
| 2 | 3 | VDD33 | P | Core Power Supply. 3.3V ±5%. |
| 11 | 14 | | | |
| 28 | 38 | | | |
| 33 | 43 | | | |
| 34 | 44 | VDDIO | P | Digital I/O Supply. 1.8V±5% to VDD33. Supply pin for SPI/I ² C and GPIO[4:0] pins. |
| — | 50 | VDDO0 | P | OUT0P/N Power Supply. 1.8V±5% to VDD33. |
| 40 | 53 | VDDO1 | P | OUT1P/N Power Supply. 1.8V±5% to VDD33. |

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TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

| 7x7 Pin Number | 9x9 Pin Number | Pin Name | Type | Description |
|----------------------|---------------------------------|----------|------|---|
| - | 56 | VDDO2 | P | OUT2P/N Power Supply. 1.8V±5% to VDD33. |
| 43 | 59 | VDDO3 | P | OUT3P/N Power Supply. 1.8V±5% to VDD33. |
| 46 | 62 | VDDO4 | P | OUT4P/N Power Supply. 1.8V±5% to VDD33. |
| 16 | 19 | VDDO5 | P | OUT5P/N Power Supply. 1.8V±5% to VDD33. |
| — | 22 | VDDO6 | P | OUT6P/N Power Supply. 1.8V±5% to VDD33. For the 7 mm x 7 mm VQFN package only: OUT6P/N is on VDDO8 with OUT8P/N |
| — | 25 | VDDO7 | P | OUT7P/N Power Supply. 1.8V±5% to VDD33. |
| 21 | 28 | VDDO8 | P | OUT8P/N Power Supply. 1.8V±5% to VDD33. |
| — | 31 | VDDO9 | P | OUT9P/N Power Supply. 1.8V±5% to VDD33. |
| — | — | NC | — | Not connected Not internally connected. |
| 3,4,5,6, 7,8,9,10 | 4,5,6,7,8 ,9,10,11, 12,13 | DNC | — | Do Not Connect. Do not wire anything to these pins. Leave unconnected. |
| E-pad | E-pad | VSS | P | Ground. 0 volts. |

5.0 FUNCTIONAL DESCRIPTION

5.1 Output Frequency Synthesizers

5.1.1 SYNTHESIZER ENABLE

A synthesizer is enabled by setting `synth_ctrl_x::en=1`.

5.1.2 SYNTHESIZER NOMINAL FREQUENCY

The synthesizers can each generate any clock frequency from just above the APLL frequency divided by 64 up to APLL frequency divided by 16. For a typical case of APLL frequency being 12.0 GHz, this range is from just above 187.5 MHz up to and including 750 MHz.

The frequency for a synthesizer is programmed as $B * K * M / N$ Hz where B, M, and N are 16-bit registers and K is a 32-bit register. The `synth_freq_base`, `synth_freq_mult`, `synth_freq_m` and `synth_freq_n` mailbox registers specify B, K, M, and N respectively.

5.1.3 SYNTHESIZER FREQUENCY OFFSET AND NCO BEHAVIOR

The frequency offset of a synthesizer can be adjusted with resolution of 2^{-48} (~0.0000035 ppb or $3.5E-15$) in the `synth_df_offset_manual_x` register. The adjustment affects all outputs configured to follow the synthesizer. This register can be written as fast as once every 600 μ s.

5.1.4 SPREAD-SPECTRUM MODULATION

For applications that require 100 MHz PCI Express clocks, the device can perform spread spectrum modulation (SSM) in any synthesizer. In SSM the frequency of the output clock is continually varied over a narrow frequency range to spread the energy of the signal and thereby reduce EMI. Spread-spectrum is enabled by setting `synth_ctrl_x::spread_spectrum_en=1`.

For center-spread applications, the frequency modulation is triangle-wave center-spread up to $\pm 5\%$ deviation from the center frequency with modulation rate configurable from 10 kHz to 100 kHz. (Values outside of these ranges are often achievable as well.)

For down-spread applications, such as PCI Express Refclk, the frequency modulation is triangle-wave down-spread of up to -10% deviation from the nominal frequency with modulation rate configurable from 10 kHz to 100 kHz. (Values outside of these ranges are often achievable as well.)

See the `synth_spread_spectrum_cfg`, `synth_spread_spectrum_rate` and `synth_spread_spectrum_spread` registers.

5.1.5 SYNTHESIZER PHASE ADJUSTMENT

The phase of a synthesizer when enabled is set by the `synth_phase_compensation` mailbox register with 1 ps step size.

5.2 Output Clocks

The device has ten OUTxP/N output clock signal pairs that each can be internally connected to any synthesizer. Each output pair has individual enable, signal format, divider, pulse width, and start/stop controls. In CMOS mode, each signal pair can become two CMOS outputs, allowing the device to have up to 20 output clock signals. Also in CMOS mode, the OUTxN pin can have an additional divider that allows the OUTxN frequency to be an integer divisor of the OUTxP frequency (example: OUT3P 125 MHz and OUT3N 25 MHz). The outputs can be aligned relative to each other and the phases of output signals can be adjusted dynamically with fine resolution.

5.2.1 OUTPUT ENABLE, SIGNAL FORMAT, VOLTAGE AND INTERFACING

To use an output, the output driver must be enabled in `output_mode::signal_format` and the per-output divider must be enabled by setting `output_ctrl_x::en`. The per-output dividers include the per-output phase adjustment/alignment circuitry and start/stop logic.

Each output pair can be disabled or configured as LVDS, LVPECL, programmable differential, Low- V_{CM} (HCSL-like), or one or two CMOS outputs. When an output is disabled, it is high impedance, and the output driver is in a low-power state. In CMOS mode, the OUTxN pin can be disabled, in-phase, or inverted vs. the OUTxP pin. Also the OUTxP pin can be disabled while the OUTxN pin is enabled. The clock to the output driver can be inverted by setting `output_mode::polarity`. The CMOS output driver can be set to any of four drive strengths in the `output_driver_level::drive` mailbox register field.

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When the output driver is in LVDS mode, V_{OD} is forced to 400 mV. V_{CM} can be configured in `output_driver_config::vcm` mailbox register field, but the default value is typically used to get $V_{CM}=1.2V$ for LVDS.

When the output driver is in programmable differential mode the output swing (V_{OD}) can be configured in the `output_driver_level::vod` mailbox register field to any value from 300 mV to 900 mV in 100 mV steps, and the common-mode voltage can be configured to any voltage from 1.0V to 2.1V in 0.1V steps in the `output_driver_level::vcm` mailbox register field. Together these fields allow the output signal to be customized to meet the requirements of the clock receiver and minimize the need for external components. By default, programmable differential mode provides 800 mV LVPECL signal swing with a 1.2V common mode voltage. This gives a signal that can be AC-coupled to receivers that are LVPECL or that require a larger signal swing than LVDS. The output driver can also be configured for LVPECL output with standard 2.0V common-mode voltage.

In both LVDS mode and programmable differential mode, the output driver requires a DC path between OUTxP and OUTxN for proper operation. This DC path is often a 100 Ω termination resistor placed as close as possible to the receiver inputs to terminate the differential signal as shown in Figure 5-1 parts a) and b). If the receiver requires a common-mode voltage that cannot be matched by the output driver then the POS and NEG signals can be AC-coupled to the receiver after the 100 Ω resistor as shown in Figure 5-1 part b). For the case where the receiver already has a 100 Ω termination resistor and AC-coupling is required, a resistor can be placed between OUTxP and OUTxN as close as possible to the device to provide the required DC path as shown in Figure 5-1 part c). This resistor can be 100 Ω for double-termination of the signal or it can be up to 200 Ω , in which case the signal is single-terminated by the 100 Ω resistor at the receiver and the signal amplitude at the receiver is larger than the double-termination case. The device provides an optional internal 200 Ω that can be enabled by setting `output_driver_config::rbias=1`.

When the output driver is in Low- V_{CM} mode the output format is HCSL-like with electrical specs as shown in Table 9-8.

Each output has its own power supply pin, VDDO0 through VDDO9, to allow CMOS signal swing from 1.8V to 3.3V for glueless interfacing to neighboring components.

Note that LVPECL signal formats must have a VDDOx power supply of 2.5V or 3.3V and LVDS must have a VDDOx power supply of 1.8V, 2.5V, or 3.3V.

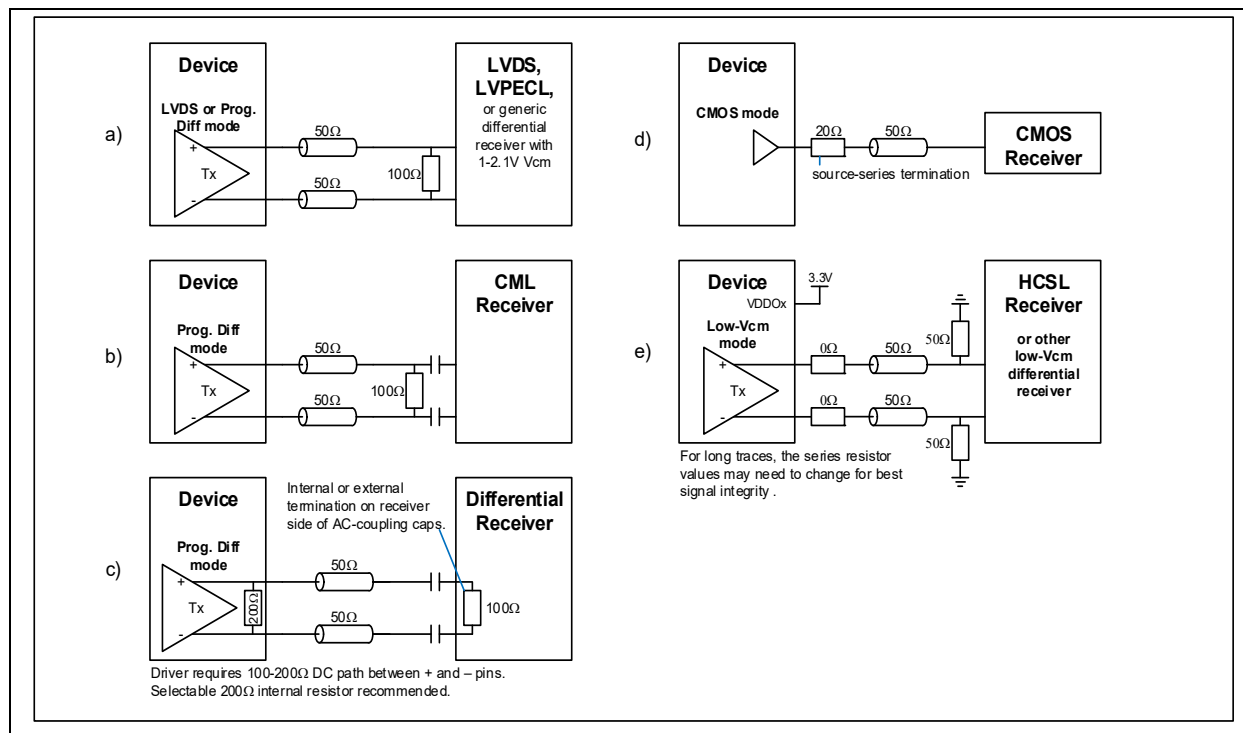


FIGURE 5-1: Output Signal External Component Examples.

5.2.2 OUTPUT FREQUENCY CONFIGURATION

The frequency of each output is determined by the configuration of the source synthesizer and the output divider. Each OUTxP/N pair can be connected to any synthesizer using `output_ctrl_x::synth_sel`. The output divider (`output_div` mailbox register) can produce signals with 50% duty cycle for all divider values including odd numbers. The maximum input frequency for the output divider is 750 MHz.

Because each output pair has its own independent divider, the device can output families of related frequencies that have a synthesizer divider frequency as a common multiple. For example, for Ethernet clocks, a 625 MHz clock from a synthesizer can be divided by four for one output to get 156.25 MHz, divided by five for another output to get 125 MHz, and divided by 25 for another output to get 25 MHz. Similarly, for SDH/SONET clocks, a 622.08 MHz clock can be divided by 4 to get 155.52 MHz, by 8 to get 77.76 MHz, by 16 to get 38.88 MHz or by 32 to get 19.44 MHz.

Two Different Frequencies in 2xCMOS Mode

When an output is in 2xCMOS mode it can be configured, using the 1100 and 1111 decodes of `output_mode::signal_` format, for N-pin divide mode. In this mode, an additional divider allows the OUTxN frequency to be an integer divide of the OUTxP frequency. Examples of where this can be useful:

- 125 MHz on OUTxP and 25 MHz on OUTxN for Ethernet applications
- 77.76 MHz on OUTxP and 19.44 MHz on OUTxN for SONET/SDH applications
- 25 MHz on OUTxP and 1 Hz (i.e. 1PPS) on OUTxN for telecom applications with IEEE1588 timing

In N-pin divide mode, the `output_esync_period` register specifies the additional divide value.

Note that the per-output divider must be configured to divide by 2 or more in N-pin divide mode.

5.2.3 OUTPUT PHASE ALIGNMENT AND PHASE ADJUSTMENT

The device automatically maintains alignment of enabled outputs. The default behavior is rising-edge alignment of all outputs. The phase of an output signal can be shifted by 180° by inverting the polarity (`output_mode::polarity`). In addition, the phase of an output signal can be shifted using the `output_phase_compensation` register with a step size equal to ½ of the source synthesizer clock period. For example, if the synthesizer is 625 MHz then one synthesizer period is 1.6 ns and the smallest phase adjustment is 0.8 ns.

In addition to the per-output controls mentioned above, the phase of all outputs derived from the same synthesizer can be controlled with 1 ps resolution. See [Section 5.1.5](#) for details.

5.2.4 OUTPUT DUTY CYCLE/PULSE WIDTH ADJUSTMENT

The duty cycle of the output clock can be modified using the `output_width` mailbox register. For normal polarity outputs, the pulse is high and the signal is low the remainder of the cycle. For inverse polarity outputs, the pulse is low and the signal is high the remainder of the cycle.

When an OUTxP/N pair is configured for two different frequencies using N-pin divide mode, the OUTxN duty cycle can be modified using the `output_esync_width` mailbox register.

5.2.5 OUTPUT CLOCK START/STOP AND SQUELCH

5.2.5.1 Output Start/Stop

Output clocks can be stopped high or low or high-impedance. One use for this behavior is to ensure “glitchless” output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an `output_ctrl_x` register with bits to control this behavior. When bit `stop_high`=1 and the `stop` bit is asserted, the output clock is stopped after the next rising edge of the output clock. When `stop_high`=0 and the `stop` bit is asserted, the output clock is stopped after the next falling edge of the output clock. When the output is stopped, the output driver goes high-impedance if bit `stop_hz`=1. Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on. Low-speed output clocks can take long intervals before being stopped after the stop signal goes active. For example, a 1 Hz output could take up to 1 second to stop.

When the output polarity is inverted the output stops on the opposite polarity that is specified by the stop mode field.

The output divider must be dividing by 2 or more (`output_div` mailbox register ≥ 2) to use start/stop behavior because divider set to 1 bypasses the start-stop circuits.

Note that when the OUTxP/N pair is configured for two frequencies using N-pin divide mode the start-stop logic controls both OUTxP and OUTxN simultaneously. This is glitchless (no short high or low times) for the OUTxP signal, but the lower-frequency OUTxN signal can have high time or low time as short as one OUTxP cycle.

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5.2.6 OUTPUT CLOCK PINS AS GENERAL-PURPOSE OUTPUTS

When an output pair is configured for a CMOS signal format, the OUTxP pin and the OUTxN pin each can be individually configured as a general-purpose output with similar behaviors to the GPIO pins (see [Section 6.3](#)). Setting `output_gpo_en::out_p=1` configures the OUTxP pin as a GPO. Setting `output_gpo_en::out_n=1` configures the OUTxN pin as a GPO. Note that the pin must be enabled in the `output_mode::signal_format` register field to be a GPO. For example if `signal_format="0101 – One CMOS, OCxP Enabled, OCxN High impedance"` then OCxN is disabled even when `output_gpo_en::out_n=1`. When an output is configured as a GPO, its behavior can be output-high, output-low, or status as specified by the `output_gpo_config_out_p` or `output_gpo_config_out_n` register. When an output is a *status* GPO it can be configured to follow an internal status bit specified by `output_gpo_select_out_p` or `output_gpo_select_out_n`.

5.3 Crystal or Input Clock

All output clocks are generated from a crystal wired to the OSCI and OSCO pins or from an oscillator wired to the OSCB pin. For a list of reference oscillators, refer to ZLAN-442.

5.3.1 EXTERNAL OSCILLATOR

When using a clock oscillator as the device's clock source, connect the oscillator's output clock to the OSCB pin and set `xo_config::xtal_en=0`.

The jitter on output clock signals depends on the phase noise and frequency of the oscillator. For the device to operate with the lowest possible output jitter, the external oscillator should have the following characteristics:

- Phase Jitter: less than 0.1 ps_{RMS} over the 12 kHz to 5 MHz integration band
- Frequency: The higher the better, all else being equal

Several vendors offer XO products with the required jitter. Three good choices from Vectron are the 114.285 MHz VCC1-9004-114M285, the 49.152 MHz VCC1-1545-49M152, and the 48 MHz Vectron VCC1-9003-48M0000. Each of these is a standard VCC1 XO but with a max jitter specification of 0.1 ps_{RMS} over the 12 kHz to 5 MHz integration band.

5.3.2 EXTERNAL CRYSTAL

The on-chip crystal driver circuit is designed to work with a fundamental mode, AT-cut crystal resonator. See [Table 5-1](#) for recommended crystal specifications. To enable the crystal driver, set `xo_config::xtal_en=1`.

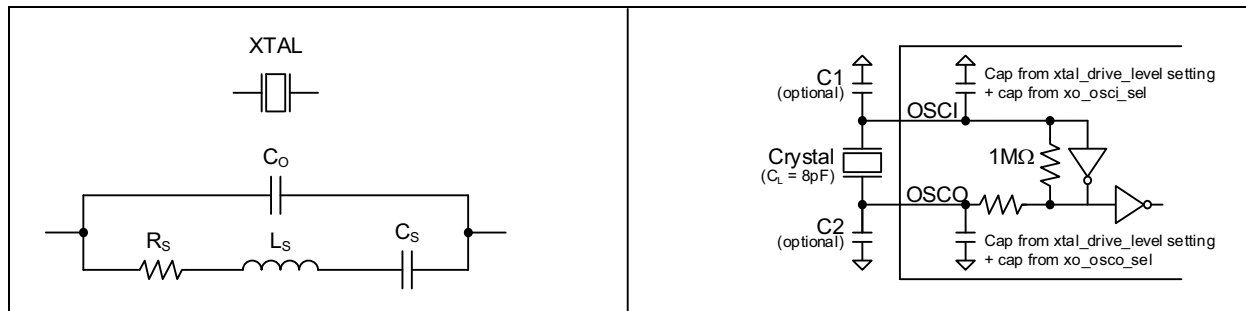


FIGURE 5-2: Crystal Equivalent Circuit/Recommended Crystal Circuit.

See [Figure 5-2](#) for the crystal equivalent circuit and the recommended external component connections. The driver circuit design includes configurable internal load capacitors. For an 8 pF crystal the total capacitance on each of OSCI and OSCO should be $2 \times 8 \text{ pF} = 16 \text{ pF}$. To achieve these loads without external capacitors, first an appropriate crystal drive level should be set in `xo_amp_sel::xtal_drive_level`. This sets baseline internal capacitance numbers for OSCI and OSCO as described in the `xtal_drive_level` description. Then register field `xo_osc*_sel` should be set to 16 pF minus the baseline internal OSCI capacitance minus the actual external OSCI board trace capacitance. Register field `xo_osco_sel` should be set in a similar manner for OSCO load capacitance. Crystals with nominal load capacitance other than 8 pF usually can be supported with only internal load capacitance. If the `xo_osc*_sel` and `xo_osco_sel` fields do not have sufficient range for the application, capacitance can be increased by using external caps C1 and C2.

Users should also note that on-chip capacitors are not nearly as accurate as discrete capacitors (which can have 1% accuracy). If tight frequency accuracy is required for the crystal driver circuit, then set `xo_osc*_sel` and `xo_osco_sel` both to 0 and choose appropriate C1 and C2 external capacitors with 1% tolerance.

The crystal and traces (and two external capacitors sites C1 and C2, if included) should be placed on the board as close as possible to the OSCI and OSCO pins to reduce crosstalk of active signals into the oscillator. No active signals should be routed under the crystal circuitry. A ground ring should surround the crystal (and optional C1 and C2) from the OSCA

pin to the OSCB pin. Layer 2 below the crystal (and optional C1 and C2) should have a ground island that is connected to the layer 1 ground ring with multiple vias along the layer-1 ground ring. All other board layers should be void in the area inside the ground ring.

Note: Crystals have temperature sensitivities that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO or TCXO should be used instead.

TABLE 5-1: CRYSTAL SELECTION PARAMETERS

| Parameter | Symbol | Min. | Typ. | Max. | Units | |
|--|--------------------|-------|---------------------|------|-----------------------------------|----------|
| Crystal Oscillation Frequency, (Note 1) | f_{OSC} | 25 | — | 60 | MHz | |
| Shunt Capacitance | C_O | — | 2 | 5 | pF | |
| Load Capacitance | C_L | — | 8 | — | pF | |
| Equivalent Series Resistance (ESR), (Note 2) | $f_{OSC} < 40$ MHz | R_S | — | — | 60 | Ω |
| | $f_{OSC} > 40$ MHz | R_S | — | — | 50 | Ω |
| Maximum Crystal Drive Level | — | 100 | 100, 200, 300 | — | μ W | |
| Crystal Frequency Stability vs. Power Supply | f_{FVD} | — | 0.2 | 0.5 | ppm per 10% Δ in VDD | |

Note 1: Higher frequencies give lower output jitter, all else being equal.

Note 2: These ESR limits are chosen to constrain crystal drive level to less than 100 μ W. If the crystal can tolerate a drive level greater than 100 μ W then proportionally higher ESR is acceptable.

5.3.3 INPUT CLOCK FREQUENCY SELECTION

The frequency of the device's input clock on the OSCI/OSCO pins or the OSCB pin is set with the following procedure:

1. Reset the device by asserting then deasserting the RST_B pin as described in [Section 5.5](#).
2. Set `xo_config::xtal_en` to 0 for clock signal on OSCB, or to 1 for crystal on OSCI/OSCO
3. Set `xo_config::simple_doubler_en=1` if enabling the internal crystal doubler
4. Set `sys_apll_primary_div_int`, `sys_apll_primary_div_frac`, and `sys_apll_secondary_div` so that: $VCO_freq = [OSC_freq * 2^{double} * (sys_apll_primary_div_int + sys_apll_primary_div_frac / 2^{36}) * sys_apll_secondary_div]$ is within 1% of 12 GHz. The variable double is 1 when `simple_doubler_en=1` and 0 otherwise. The GUI has preloaded options for each of these register fields to support commonly used XO frequencies such as 48 MHz, 49.152 MHz, and 114.285 MHz.
5. Set the `central_freq_offset` register appropriately whenever the APLL VCO frequency is not exactly 12.0 GHz. See the register description for calculations and examples. The GUI automatically calculates this value.
6. Set `master_clk_cfg_ready=1`.
7. Verify the setup is good by reading the `master_clk_status` register. Bit 3 (`sys_apll_lock`) should be 0 to indicate the APLL is locked. Bits 1:0 (state) should be 11 to indicate 'ready'. Also read the `info` register and verify bit 7 (ready) is 1.

5.3.3.1 Crystal Doubler

When operating with a crystal as the input clock source, it is usually beneficial to enable the crystal doubler (`xo_config::simple_doubler_en=1`). This doubles the input clock frequency to the APLL, which reduces random jitter with little or no adverse effect for most frequency plans. Note that the doubler causes a spur at the OSCI frequency. If this spur falls within the output jitter band of interest then the doubler can be disabled if needed.

5.4 Power Supplies

Most of the device is powered from VDD33 (3.3V) and VDD18 (1.8V). Each OUTxP/N output pair can be independently powered with 1.5V, 1.8V, 2.5V, or 3.3V on a VDDOx supply. (The 1.5V option only applies for CMOS output signal formats. The 1.8V option only applies for CMOS and LVDS.) Digital I/O (SPI/I²C interface pins, GPIOs) are powered from VDDIO.

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5.4.1 POWER UP/DOWN SEQUENCE

There are no sequence requirements for power-up or power-down on these devices.

5.4.2 POWER SUPPLY FILTERING

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3V and 1.8V supply pins. Microchip application note ZLAN-810 provides power supply filtering recommendations.

5.4.3 POWER CALCULATOR

The GUI software for the device includes a useful power calculator that estimates power utilization for a specific configuration or application.

5.5 Reset and Configuration Pins

To ensure proper operation, the device must be reset after power-up by driving the RST_B pin low. The RST_B pin should be held low for at least 2 ms after all power supplies are within 5% of nominal voltage. Following reset, the device operates under specified default settings.

The RST_B input has Schmidt trigger properties to prevent level bouncing.

Pin SO_IF1 and CS_B_IF0 are used to configure the device on power up. These pins must be held at the desired level for at least 550 ms after RST_B goes high. Then they can be used for normal functions as described in [Section 7.0](#).

By default all outputs are disabled to allow programming of required frequencies before enabling the outputs.

6.0 CONFIGURATION AND CONTROL

The SPI/I²C host interface allows field programmability of the device's configuration registers. As an example, the user might start the device at nominal synchronous Ethernet rate and then switch to an OTN FEC rate after the link's FEC rate is negotiated.

6.1 Pre-Configured Default Values on Power-Up

Upon power up, device registers have values as described in the Register Map section. If the device should start up with settings different from default, it can be pre-configured (pre-programmed) by Microchip. The device can be pre-configured with up to seven different custom configurations. Any of the custom configurations can be selected just after reset using the GPIO0_AC0, GPIO1_AC1, and GPIO2_AC2 pins. The values of these pins are ignored at reset if the device is not pre-configured.

6.2 Configuration Sequence

After power-up or reset the device has sequence requirements for configuration. The required sequence is as follows:

1. Poll for device ID in the `id` register. During initial boot the device does not respond to SPI or I²C accesses until it is ready. System software can poll the `id` register to wait for the end of this interval. While not ready, the device returns 0 for SPI read accesses and NACK over the I²C interface. When ready the device returns the device ID value.
2. Configure the APLL. See [Section 5.3](#) and its subsections, especially the procedure in [Section 5.3.3](#).
3. Configure the rest of the device in all other registers.

Note that the device does not accept writes to mailbox registers before `master_clk_status::sys_apll_lock=1` and `info::ready=1`.

Configurations saved by the evaluation board GUI follow this sequence. Microchip recommends creating configuration files using the GUI. System software can follow the write sequence in the configuration files after system power-up or reset.

6.3 GPIO Configuration

The device GPIO are configured using the SPI/I²C. Each GPIO pin can be programmed independently in the `gpio_config_x` register to be:

General Input: In this mode, system software can read the logic level of the corresponding pin (either high or low). For example, the logic level of GPIO0 is reflected in the register [gpio_in_status](#), bit 0.

General Output: In this mode, system software can configure a GPIO pin to drive either high or low. For example, GPIO0 would drive the value specified in register [gpio_out_4_0](#), bit 0.

Control Inputs: In this mode, the user can control the device function via GPIOs. For example, the function controlled by GPIO0 is selected by configuring [gpio_select_0](#). Nearly any device function that is controllable through the device registers can be controlled via GPIO. A small subset of control functions is shown below:

- Enable/disable differential and single ended outputs
- Stop/start output clocks

Status Outputs: In this mode the device can connect a status value from any of the device status registers to the corresponding GPIO pin. For example GPIO0 mirrors a bit from the status register specified in register [gpio_select_0](#).

The GPIO outputs are updated and the GPIO inputs are read by the device approximately every 10 ms to 25 ms.

7.0 HOST INTERFACE

A host processor controls and receives status from the device using either a SPI or I²C interface.

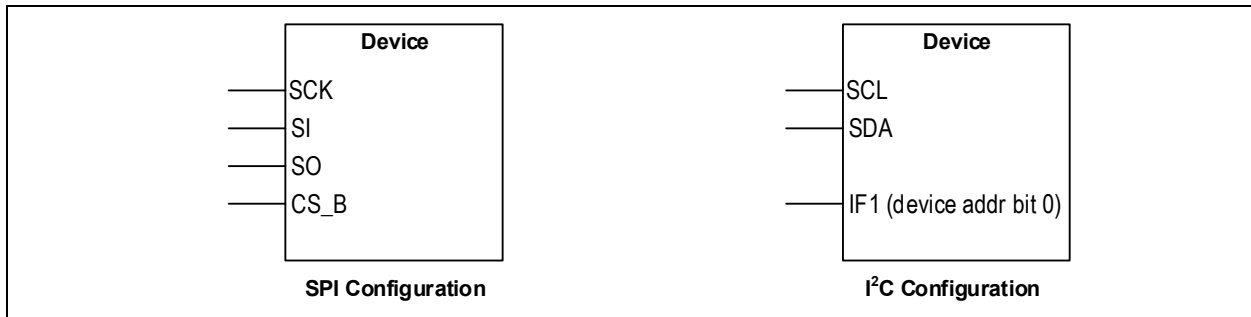


FIGURE 7-1: Host Interface Pins for SPI and I²C.

The selection between I²C and SPI interfaces is performed at start-up using the CS_B_IF0 pin. This pin must be held at the required level for 550 ms after the de-assertion of the RST_B pin, after which time it can be released and used as the SPI chip-select signal if SPI mode is selected at reset.

TABLE 7-1: SERIAL INTERFACE SELECTION

| CS_B_IF0 | Serial Interface |
|----------|------------------|
| 0 | I ² C |
| 1 | SPI |

Both interfaces use a seven-bit address field. The device register space is divided into multiple pages of 127 registers each. Page 0 has addresses 0x000 to 0x07E, Page 1 has addresses 0x080 to 0x0FE and so on. The host selects between the pages by writing to the Page Select register (address 0x7F on each page). For example, writing a 0x03 to the page select register makes registers 0x180 to 0x1FE available through the host interface.

The device registers are divided into direct-access and indirect-access (mailbox) registers. The direct-access registers (Pages 0 to 9) are accessed simply by reading or writing specific memory locations. The mailbox access registers (Pages 10+) have shared address space. For example, Page 14 is shared among all outputs. To initialize one of the outputs, the user needs to specify which output needs to be updated ([output_mb_mask](#) register) and then read the mailbox by setting the rd bit high in [output_mb_sem](#) (output mailbox semaphore). The user then changes register values in the mailbox as needed and then issues the write command by setting the wr bit high in [output_mb_sem](#). The device then transfers values from the mailbox to internal registers for that output. The behavior of other mailbox register pages is similar.

7.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the device's registers.

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The SPI interface operates in half-duplex processor mode. During the data-out portion of a read cycle, the **SI_SDA** pin is ignored by the device. During a write cycle, the driver on the **SO_IF1** pin remains disabled. The SPI interface is compatible with both 4-pin and 3-pin SPI controllers. In 3-pin configuration, when externally connecting **SI_SDA** and **SO_IF1**, a 1 kΩ series resistor is recommended on the **SO_IF1** pin to limit current during bus turnaround and possible contention due to programming errors. The **SO_IF1** driver is enabled on the rising edge of **SCK_SCL** that latches the final read address bit and disabled on the rising edge of **CS_B_IF0**.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission and Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK_SCL** pin when the **CS_B_IF0** pin is active. If the **SCK_SCL** pin is low during **CS_B_IF0** activation, then MSb-first timing is selected. If the **SCK_SCL** pin is high during **CS_B_IF0** activation, then LSb-first timing is assumed.

The SPI port expects 1 bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS_B_IF0** pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **CS_B_IF0** low after a read or a write. The register address is automatically incremented after each data byte is read or written.

Functional waveforms for the LSb-first and MSb-first modes, and burst mode are shown in [Figure 7-2](#), [Figure 7-3](#), and [Figure 7-4](#). Timing characteristics are shown in [Table 9-12](#), [Figure 9-2](#), and [Figure 9-3](#).

7.1.1 LEAST SIGNIFICANT BIT (LSb) FIRST TRANSMISSION MODE

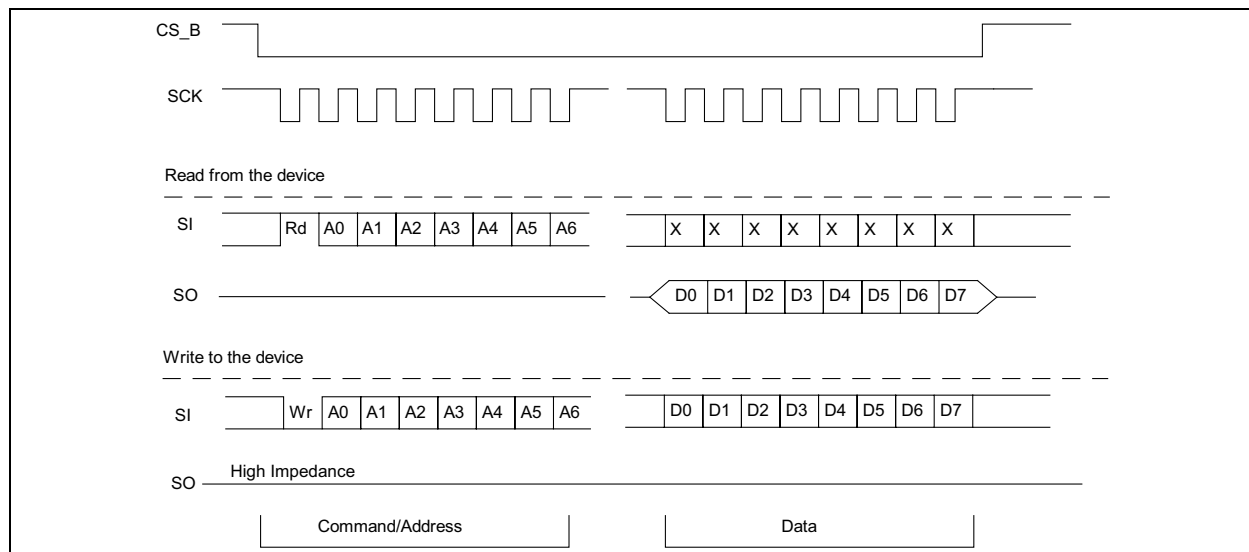


FIGURE 7-2: Serial Peripheral Interface Functional Waveform - LSB First Mode.

7.1.2 MOST SIGNIFICANT BIT (MSb) FIRST TRANSMISSION MODE

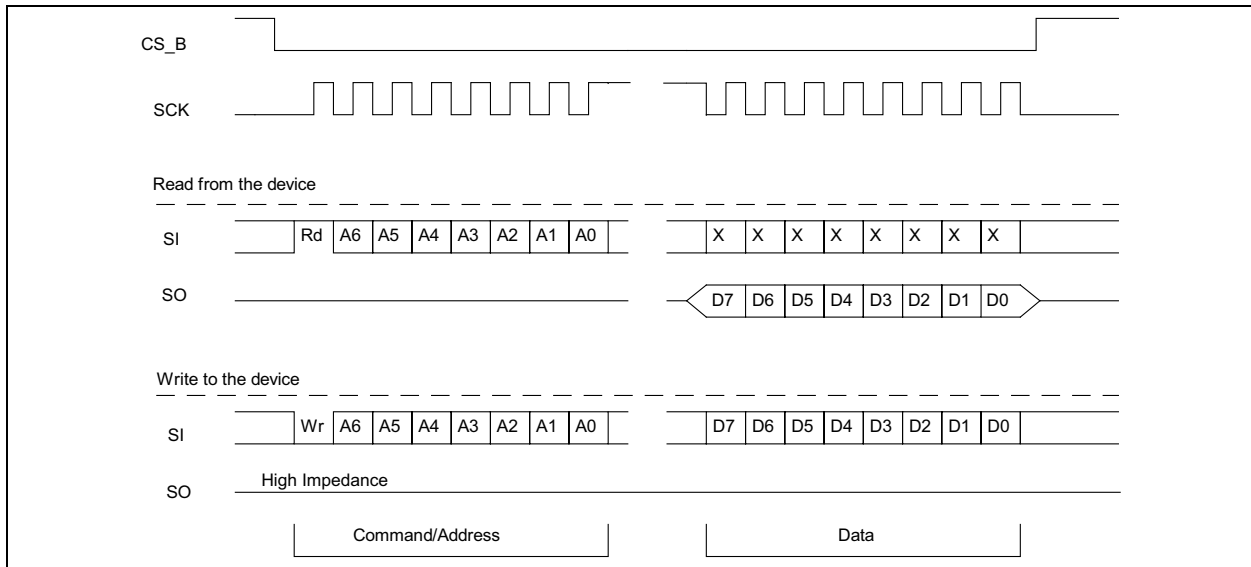


FIGURE 7-3: Serial Peripheral Interface Functional Waveform - MSB First Mode.

7.1.3 SPI BURST MODE OPERATION

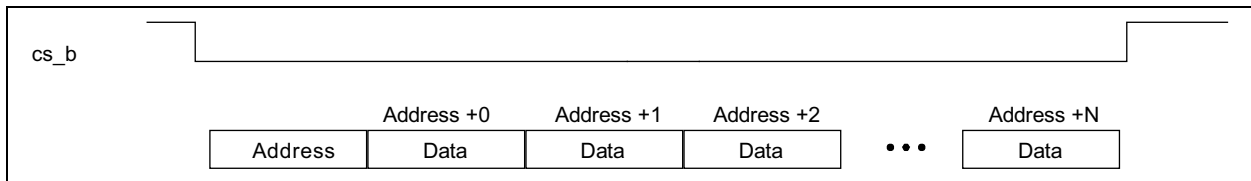


FIGURE 7-4: Example of the Burst Mode Operation.

7.1.4 INTERFACING TO A 1.8V, 2.5V, OR 3.3V SPI BUS

The supply voltage for the SPI interface pins is the VDDIO pin. This pin should be wired to the desired supply voltage for the SPI interface. Note that VDDIO is also the supply pin for the GPIO0 through GPIO4 pins.

7.2 I²C Interface

The I²C interface supports version 2.1 (January 2000) of the Philips I²C bus specification. The device cannot control the bus, it can only respond to an external controller. The device uses 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) modes. Burst mode is supported in both standard and fast modes.

Data is transferred MSb first and occurs in 1 byte blocks. As shown in Figure 7-5, a write command consists of a 7-bit device address, a R/W indicator bit, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

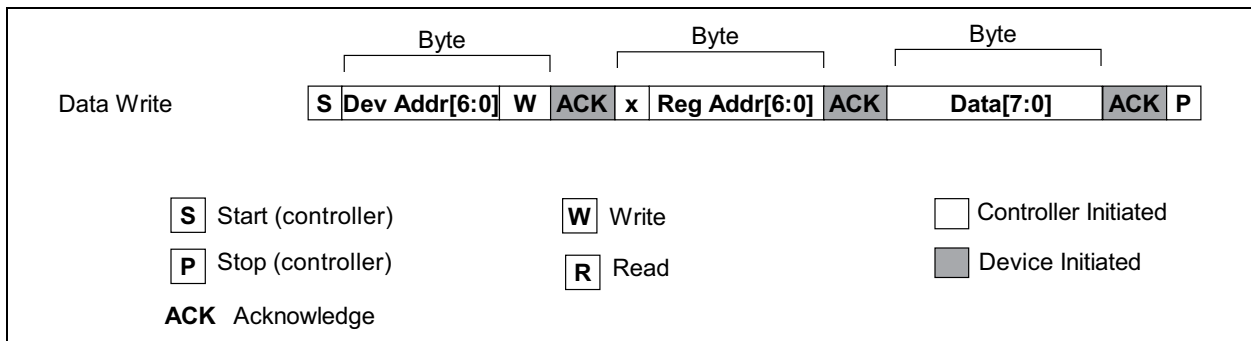


FIGURE 7-5: I²C Data Write Protocol.

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A read is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in following figure.

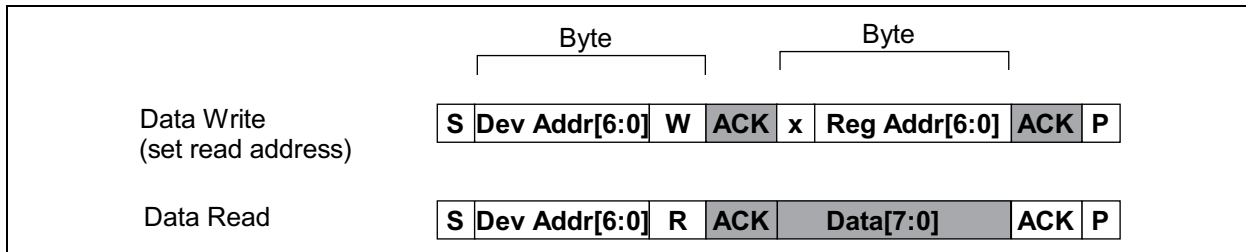


FIGURE 7-6: I²C Data Read Protocol.

The 7-bit device address has 6 fixed address bits plus the least-significant address set by the SO_IF1 pin at reset. This allows multiple devices to share the same I²C bus. The address configuration is shown in following figure.

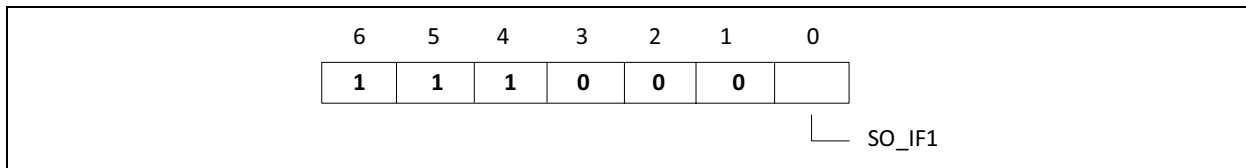


FIGURE 7-7: I²C 7-Bit Device Address.

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 7-8 (write) and Figure 7-6 (read). The first data byte is written/read to/from the specified address, and subsequent data bytes are written/read using an automatically incremented address. The maximum auto increment address of a burst operation is 0x7F and operations beyond this limit are ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

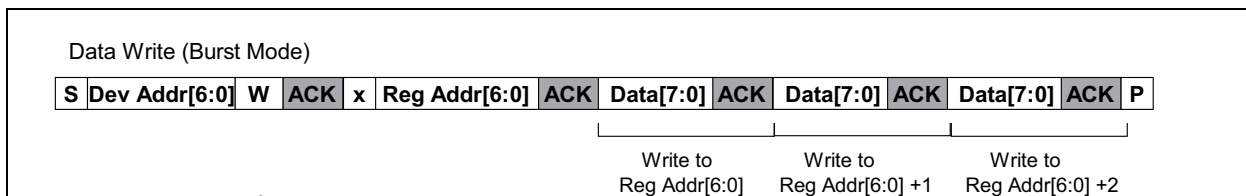


FIGURE 7-8: I²C Data Write Burst Mode.

8.0 REGISTER MAP

The device is controlled by accessing registers through the serial interface (SPI or I²C). The device can be configured to operate in unmanaged (automatic) mode, which minimizes its interaction with system software, or it can operate in a managed (manual) mode where the system software controls operation of the device.

The register map is big-endian format.

A simple way to generate configuration for the device is to use the evaluation software (GUI), which can operate connected to an evaluation board or standalone (without an evaluation board). Through the GUI, the user can quickly set all required parameters and save the configuration to a text file which can then be used by the system processor to load and configure the device.

8.1 Multi-Byte Register Values

The device register map is based on 8-bit register access. Therefore, register values that require more than 8 bits are spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in [Figure 8-1](#). When writing a multi-byte value, the value is latched when the LSB is written.

In this example the [central_freq_offset](#) register has the value 0x046AAAAB, a 32-bit value spread over four 8-bit registers. The MSB is contained in address 0x000B and the LSB in 0x000E. When reading or writing this multi-byte value, the MSB must be accessed first, then the middle bytes, and the LSB last.

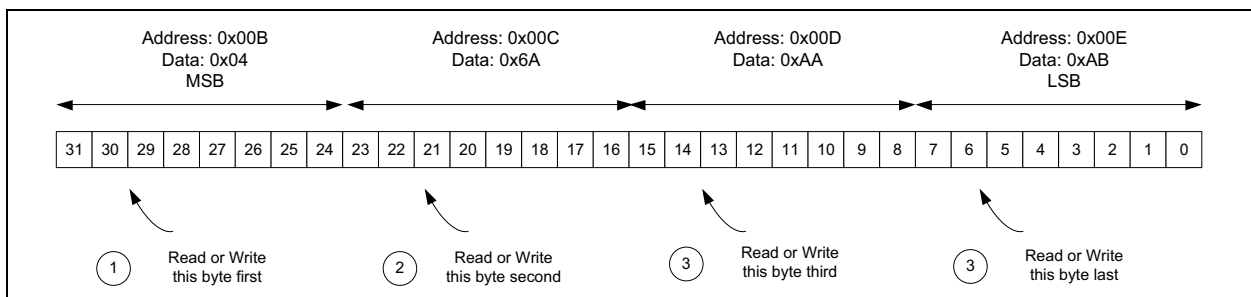


FIGURE 8-1: Accessing Multi-Byte Register Value.

8.1.1 TIME BETWEEN TWO WRITE ACCESSES TO THE SAME REGISTER

The user should not write to the same register faster than 25 ms. Some registers that control APLL operation require larger delays after writing in order for the state and configurations to be updated. One example is the register [central_freq_offset](#) requires much longer time, but this register should not be changed dynamically.

For the page selection register (at addresses 0x07F, 0x0FF, 0x17F, etc.), there is no waiting time required between write accesses.

8.1.2 TIME AFTER CHANGE TO APLL RELATED CONFIGURATION

The user should wait for appropriate time after configuration of APLL related configuration prior to updating other registers. One example is the register [central_freq_offset](#).

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8.2 Register Map List Summary

The following tables provides a summary of the registers available for status and configuration of the device.

Note that devices do not respond to mailbox register accesses after power-up or reset until system software configures the APLL registers and sets [master_clk_cfg_ready](#) to 1 and the device responds by setting the **ready** bit in the [info](#) register.

TABLE 8-1: TOP-LEVEL REGISTER MAP

| Address | Register Map Page |
|---------|---|
| 0x000 | Register Map Page 0, General |
| 0x080 | Register Map Page 1, GPIOs |
| 0x100 | Register Map Page 2, Status |
| 0x480 | Register Map Page 9, Synth and Output |
| 0x680 | Register Map Page 13, Synth Mailbox |
| 0x700 | Register Map Page 14, Output Mailbox |

Register Map Page 0, General

| Address | Name | Default | Type |
|---------------|---|-------------------|------|
| 0x0000 | info | 0x21 | R |
| 0x0001:0x0002 | id | see description | R |
| 0x0003 | revision | 0x03 | R |
| 0x0005:0x0006 | fw_ver | contact Microchip | R |
| 0x0007:0x000A | custom_config_ver | 0xFFFFFFFF | R/W |
| 0x000B:0x000E | central_freq_offset | 0x02769140 | R/W |
| 0x0018 | reset_status | 0x00 | R/W |
| 0x0019:0x001A | gpio_at_startup | 0x0000 | R |
| 0x0021 | xo_amp_sel | 0x00 | R/W |
| 0x0022 | xo_osci_sel | 0x00 | R/W |
| 0x0023 | xo_osco_sel | 0x00 | R/W |
| 0x0025 | xo_tst_ctrl | 0x00 | R/W |
| 0x0026 | xo_config | 0x00 | R/W |
| 0x0029 | sys_apll_source_config | 0x00 | R/W |
| 0x002A | sys_apll_primary_div_int | 0x34 | R/W |
| 0x002B:0x002F | sys_apll_primary_div_frac | 0x0000000000 | R/W |
| 0x0030 | sys_apll_secondary_div | 0x02 | R/W |
| 0x0032 | master_clk_status | 0x00 | R |
| 0x0033 | master_clk_cfg_ready | 0x00 | R/W |
| 0x003E | i2c_device_addr | 0x38 | R |
| 0x0050:0x006F | available for customer use | 0x00 | R/W |
| 0x007E | uport | 0x00 | R/W |
| 0x007F | page_sel | 0x00 | R/W |

Register Map Page 1, GPIOs

| Address | Name | Default | Type |
|---------------|-------------------------------|---------|------|
| 0x00E0:0x00E1 | gpio_select_0 | 0x0000 | R/W |
| 0x00E2 | gpio_config_0 | 0x00 | R/W |
| 0x00E3:0x00E4 | gpio_select_1 | 0x0000 | R/W |

Register Map Page 1, GPIOs (Continued)

| Address | Name | Default | Type |
|---------------|---------------------------------|---------|------|
| 0x00E5 | gpio_config_1 | 0x00 | R/W |
| 0x00E6:0x00E7 | gpio_select_2 | 0x0000 | R/W |
| 0x00E8 | gpio_config_2 | 0x00 | R/W |
| 0x00E9:0x00EA | gpio_select_3 | 0x0000 | R/W |
| 0x00EB | gpio_config_3 | 0x00 | R/W |
| 0x00EC:0x00ED | gpio_select_4 | 0x0000 | R/W |
| 0x00EE | gpio_config_4 | 0x00 | R/W |
| 0x00EF | gpio_out_4_0 | 0x00 | R/W |
| 0x00F0 | gpo_out_7_0 | 0x00 | R/W |
| 0x00F1 | gpo_out_15_8 | 0x00 | R/W |
| 0x00F2 | gpo_out_19_16 | 0x00 | R/W |
| 0x00F3 | gpio_freeze_4_0 | 0x00 | R/W |
| 0x00FE | uport | 0x00 | R/W |
| 0x00FF | page_sel | 0x00 | R/W |

Register Map Page 2, Status

| Address | Name | Default | Type |
|---------|--------------------------------|---------|------|
| 0x0140 | gpio_in_status | 0x00 | R |
| 0x017E | uport | 0x00 | R/W |
| 0x017F | page_sel | 0x00 | R/W |

Register Map Page 9, Synth and Output

| Address | Name | Default | Type |
|---------------|--|--------------|------|
| 0x0480 | synth_ctrl_0 | 0x00 | R/W |
| 0x0481 | synth_ctrl_1 | 0x00 | R/W |
| 0x0482 | synth_ctrl_2 | 0x00 | R/W |
| 0x0483 | synth_ctrl_3 | 0x00 | R/W |
| 0x0484 | synth_ctrl_4 | 0x00 | R/W |
| 0x0485:0x0489 | synth_df_offset_manual_0 | 0x0000000000 | R/W |
| 0x048A:0x048E | synth_df_offset_manual_1 | 0x0000000000 | R/W |
| 0x048F:0x0493 | synth_df_offset_manual_2 | 0x0000000000 | R/W |
| 0x0494:0x0498 | synth_df_offset_manual_3 | 0x0000000000 | R/W |
| 0x0499:0x049D | synth_df_offset_manual_4 | 0x0000000000 | R/W |
| 0x04A8 | output_ctrl_0 | 0x01 | R/W |
| 0x04A9 | output_ctrl_1 | 0x01 | R/W |
| 0x04AA | output_ctrl_2 | 0x01 | R/W |
| 0x04AB | output_ctrl_3 | 0x01 | R/W |
| 0x04AC | output_ctrl_4 | 0x01 | R/W |
| 0x04AD | output_ctrl_5 | 0x01 | R/W |
| 0x04AE | output_ctrl_6 | 0x01 | R/W |
| 0x04AF | output_ctrl_7 | 0x01 | R/W |
| 0x04B0 | output_ctrl_8 | 0x01 | R/W |
| 0x04B1 | output_ctrl_9 | 0x01 | R/W |

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Register Map Page 9, Synth and Output (Continued)

| Address | Name | Default | Type |
|---------|--------------------------|---------|------|
| 0x04FE | uport | 0x00 | R/W |
| 0x04FF | page_sel | 0x00 | R/W |

Register Map Page 13, Synth Mailbox

| Address | Name | Default | Type |
|---------------|--|------------|------|
| 0x0682:0x0683 | synth_mb_mask | 0x0001 | R/W |
| 0x0684 | synth_mb_sem | 0x00 | R/W |
| 0x0686:0x0687 | synth_freq_base | 0x0001 | R/W |
| 0x0688:0x068B | synth_freq_mult | 0x12A05F20 | R/W |
| 0x068C:0x068D | synth_freq_m | 0x0001 | R/W |
| 0x068E:0x068F | synth_freq_n | 0x0001 | R/W |
| 0x0690:0x0691 | synth_phase_compensation | 0x0000 | R/W |
| 0x0694 | synth_spread_spectrum_cfg | 0x00 | R/W |
| 0x0695:0x0696 | synth_spread_spectrum_rate | 0x0000 | R/W |
| 0x0697 | synth_spread_spectrum_spread | 0x00 | R/W |
| 0x06FE | uport | 0x00 | R/W |
| 0x06FF | page_sel | 0x00 | R/W |

Register Map Page 14, Output Mailbox

| Address | Name | Default | Type |
|---------------|---|------------|------|
| 0x0702:0x0703 | output_mb_mask | 0x0001 | R/W |
| 0x0704 | output_mb_sem | 0x00 | R/W |
| 0x0705 | output_mode | 0x00 | R/W |
| 0x0706 | output_driver_level | 0x52 | R/W |
| 0x0707:0x0708 | output_driver_config | 0x0000 | R/W |
| 0x070C:0x070F | output_div | 0x00000002 | R/W |
| 0x0710:0x0713 | output_width | 0x00000002 | R/W |
| 0x0714:0x0717 | output_esync_period | 0x00000002 | R/W |
| 0x0718:0x071B | output_esync_width | 0x00000002 | R/W |
| 0x0720:0x0723 | output_phase_compensation | 0x00000000 | R/W |
| 0x0724 | output_gpo_en | 0x00 | R/W |
| 0x0725:0x0726 | output_gpo_select_out_p | 0x0000 | R/W |
| 0x0727 | output_gpo_config_out_p | 0x01 | R/W |
| 0x0728:0x0729 | output_gpo_select_out_n | 0x0000 | R/W |
| 0x072A | output_gpo_config_out_n | 0x01 | R/W |
| 0x077E | uport | 0x00 | R/W |
| 0x077F | page_sel | 0x00 | R/W |

REGISTER LIST PAGE 0, GENERAL

| Address: | 0x0000 | |
|-----------|---------------|--|
| Name: | info | |
| Default: | 0x21 | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 7 | ready | The device sets this status bit after the APLL (and crystal driver if in use) have been successfully configured and the APLL is locked. This bit indicates that the device is fully ready and mailbox registers can be read and written. |
| 6:0 | reserved | — |

| Address: | 0x0001:0x0002 | |
|-----------|---------------|---|
| Name: | id | |
| Default: | see below | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 15:0 | — | Chip identification number. ZL30270 = 0x8CC6 ZL30271 = 0x0CC7 |

| Address: | 0x0003 | |
|-----------|---------------|---|
| Name: | revision | |
| Default: | 0x03 | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 15:0 | — | Chip revision number. 0x02 = Revision B 0x03 = Revision C |

| Address: | 0x0005:0x0006 | |
|-----------|-------------------|---|
| Name: | fw_ver | |
| Default: | contact Microchip | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 15 | fw_dirty | Firmware dirty indicator. This bit is set when the firmware is built from source code that has not been checked-in to the firmware repository. This bit should never be set in released firmware. |
| 15:0 | — | Firmware revision number. This field indicates the firmware revision of the source code used to build this image. |

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| Address: | 0x0007:0x000A | |
|-----------|-------------------|---|
| Name: | custom_config_ver | |
| Default: | 0xFFFFFFFF | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | This register is intended (but not limited) to be used as configuration version number. Up to 7 custom register configurations can be programmed into the device. |

| Address: | 0x000B:0x000E | |
|-----------|---------------------|---|
| Name: | central_freq_offset | |
| Default: | 0x02769140 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | <p>2's complement binary value of these bits represent central frequency offset for the device. This value indicates the fractional frequency offset of the actual VCO frequency vs. 12.0 GHz. Expressed in steps of $\pm 2^{-32}$ of nominal setting.</p> <p>The actual VCO frequency (f_{vco}) is the product of the XO frequency, the primary divider specified in <code>sys_apll_primary_div_int</code> (0x002A) and <code>sys_apll_primary_div_frac</code> (0x002B to 0x002F), and the secondary divider specified in <code>sys_apll_secondary_div</code> (0x0030). The nominal VCO frequency (f_{nom}) is always 12.0 GHz.</p> <p>The value to be programmed in this register should satisfy the following relationships: $1 + X * 2^{-32} = f_{nom} / f_{vco}$, if $f_{vco} < f_{nom}$ $X * 2^{-32} = f_{nom} / f_{vco}$, if $f_{vco} > f_{nom}$.</p> <p>Equivalently, if X is treated as a signed number, the following equation always holds: $1 + X * 2^{-32} = f_{nom} / f_{vco}$.</p> <p>When the VCO frequency is lower than the 12.0 GHz nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa.</p> <p>Example 1: if VCO frequency offset is -0.1% ($f_{vco} = 11.988$ GHz); $X = (12.0/11.988 - 1) * 2^{32} = 4299267 = 0x00419A03$</p> <p>Example 2: if XO is 49.152 MHz, the primary divider is 244 and the secondary divider is 1 ($f_{vco} = 11.993088$ GHz); $X = (12.0/11.993088 - 1) * 2^{32} = 2475327 = 0x0025C53F$</p> <p>Example 3: if VCO inaccuracy is +0.1% ($f_{vco} = 12.012$ GHz); $X = (12/12.012) * 2^{32} = 4290676619 = 0xFFBE878B$</p> <p>Note: <code>central_freq_offset</code> should not be programmed to exceed $\pm 1\%$ because the APLL VCO range is $12\text{ GHz} \pm 1\%$.</p> |

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| Address: | 0x0018 | |
|-----------|---------------|---|
| Name: | reset_status | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:1 | reserved | — |
| 0 | reset | This field can be used to detect when a reset has occurred. During reset, this bit is cleared. The host controller can write a one to this bit, and then periodically read the register to check for a reset. |

| Address: | 0x0019:0x001A | |
|-----------|-----------------|---|
| Name: | gpio_at_startup | |
| Default: | 0x0000 | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 15:5 | reserved | — |
| 4 | gpio4 | The value of GPIO4 latched at device reset. |
| 3 | gpio3 | The value of GPIO3 latched at device reset. |
| 2 | gpio2 | The value of GPIO2 latched at device reset. |
| 1 | gpio1 | The value of GPIO1 latched at device reset. |
| 0 | gpio0 | The value of GPIO0 latched at device reset. |

| Address: | 0x0021 | |
|-----------|---------------|---|
| Name: | xo_amp_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:5 | reserved | — |
| 4 | dis_hyst | Disables the normal hysteresis circuits of the OSCB pin receiver |
| 3 | en_fdbk | Disables hysteresis and connects a 250 k Ω resistor to 1.25V to the OSCB pin for DC-bias. This allows AC-coupling a clock signal. Enabling this bit is not recommended for rail-to-rail CMOS signals $\geq 1.8V$. This feature and external AC-coupling are only for signal amplitudes $< 1.8V$. |

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| | | |
|-----|------------------|---|
| 2:0 | xtal_drive_level | <p>Controls the XTAL driver strength on OSCO pin and selects the external XO on the OSB pin.</p> <p>000 - disables the XTAL driver and selects the signal on the OSCB pin. 001 – drive 1 010 – drive 2 011 – drive 3 100 – driver 4--recommended 101 – drive 5 110 – drive 6 111 – drive 7</p> |
|-----|------------------|---|

| Address: | 0x0022 | |
|-----------|---------------|---|
| Name: | xo_osci_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Affects the capacitive loading of the OSCI pin. Used to select the total XTAL loading (which affects the oscillation frequency). Resolution is 0.25 pF and range is 0 pF to 11.75 pF. |

| Address: | 0x0023 | |
|-----------|---------------|---|
| Name: | xo_osco_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Affects the capacitive loading of the OSCO pin. Used to select the total XTAL loading (which affects the oscillation frequency), Resolution is 0.25 pF and range is 0 pF to 11.75 pF. |

| Address: | 0x0025 | |
|-----------|---------------|---|
| Name: | xo_tst_ctrl | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | — | The bits in this register control the crystal driver circuit series resistance for OSCO. Each bit controls a resistor, and the resistors are arranged in parallel. All-ones enables 72 k Ω . 0 = Enable 562.6 Ω resistor |
| 6 | — | 0 = Enable 1.125 k Ω resistor |
| 5 | — | 0 = Enable 2.25 k Ω resistor |
| 4 | — | 0 = Enable 4.5 k Ω resistor |
| 3 | — | 0 = Enable 9 k Ω resistor |
| 2 | — | 0 = Enable 18 k Ω resistor |

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| | | |
|---|---|---------------------------|
| 1 | — | 0 = Enable 36 kΩ resistor |
| 0 | — | 0 = Enable 72 kΩ resistor |

| Address: | 0x0026 | |
|-----------|-------------------|---|
| Name: | xo_config | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:6 | reserved | — |
| 5 | xtal_en | 0 = Disable crystal oscillator. The XO clock comes from an external XO connected to the OSCB pin. 1 = Enable crystal oscillator. (Must also set xtal_drive_level > 1 at in xo_amp_sel register (0x0021). |
| 4:2 | reserved | — |
| 1 | simple_doubler_en | Enable the simple crystal doubler. Only appropriate when using a crystal as input clock source. Not for use with an XO. 0 = Disable 1 = Enable |
| 0 | passclk | When this bit is set, the XO clock is passed directly to the APLL, bypassing inversion, division selection and the simple doubler. The simple doubler should be disabled in this case. |

| Address: | 0x0029 | |
|-----------|------------------------|--|
| Name: | sys_apll_source_config | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6 | pfd_gain_boost | When the doubler is disabled, setting this bit minimizes output jitter in most cases. 0 = Disable 1 = Enable |
| 5:4 | div | Divide the source clock for the APLL 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 |
| 3 | invert | APLL source invert 0 = Not inverted 1 = Inverted |
| 2:0 | reserved | — |

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| Address: | 0x002A | |
|-----------|--------------------------|---|
| Name: | sys_apll_primary_div_int | |
| Default: | 0x34 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | System APLL primary divider (integer part). Range is 16 to 67. If any other value is written to this register, the default value 0x34 (52) is used. The value must be ≥ 20 if sys_apll_primary_div_frac (0x002B-0x002F) register is non-zero. |

| Address: | 0x002B:0x002F | |
|-----------|---------------------------|--|
| Name: | sys_apll_primary_div_frac | |
| Default: | 0x0000000000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | System APLL primary divider (fractional part). Only 36 bits are used. The 4 most significant bits are ignored. |

| Address: | 0x0030 | |
|-----------|------------------------|---|
| Name: | sys_apll_secondary_div | |
| Default: | 0x02 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:6 | reserved | — |
| 5:0 | div | System APLL secondary divider. Range is 1 to 63. If any other value is written to this register, the divider value is set to 1. |

| Address: | 0x0032 | |
|-----------|-------------------|---|
| Name: | master_clk_status | |
| Default: | 0x00 | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 7:4 | reserved | — |
| 3 | sys_apll_lock | 0 = APLL is locked. 1 = APLL lost lock. |
| 2 | cfg_invalid | Invalid host system clock info 0 = Valid 1 = Invalid |
| 1:0 | state | System clock state: 00 = Not started 01 = Waiting for host config information 10 = In progress 11 = Ready |

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| Address: | 0x0033 | |
|-----------|----------------------|--|
| Name: | master_clk_cfg_ready | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:1 | reserved | — |
| 0 | ready | 0 = System clock configuration is not ready 1 = System clock configuration is ready Whenever changing system clock configuration, set this bit to 0 first, then apply the changes and finally set the bit to 1. The device only latches system clock configuration into hardware on the first 0-to-1 transition of this bit after reset. |

| Address: | 0x003E | |
|-----------|-----------------|--|
| Name: | i2c_device_addr | |
| Default: | 0x38 | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 7:0 | — | Indicate I ² C device address upper six bits (bit[6:1]) if uPort is configured to I ² C. |

| Address: | 0x007E | |
|-----------|---------------|--|
| Name: | uport | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | lockout | When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing. |
| 6:1 | reserved | — |
| 0 | status | This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful. |

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| Address: | 0x007F | |
|-----------|---------------|---|
| Name: | page_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Unsigned binary value of these bits represents selected page for SPI/I ² C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved |

REGISTER LIST PAGE 1, GPIOs

| Address: | 0x00E0:0x00E1 | |
|-----------|---------------|---|
| Name: | gpio_select_0 | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | bit | Note: The fields in this register are only useful when GPIO0 is configured as a Status or Control. This field works with the page and offset field to select a single bit in the host register map. This field selects the bit position of the selected register byte. |
| 11:8 | page | This field works with the bit and offset fields to select a single bit in the host register map. This field selects the page. |
| 7 | reserved | — |
| 6:0 | offset | When GPIO0 is configured as a Status or Control, then this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page. |

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gpio_config_x

| Address: | 0x00E2 | |
|-----------|---------------|---|
| Name: | gpio_config_0 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:3 | reserved | — |
| 2:0 | ctrl | <p>This field determines the mode of operation for GPIO0. Register 0x0E0-0x0E1 (gpio_select_0) should be set before writing this register, if the mode being set requires additional configuration. However, the new gpio_select value must refer to a register that is also valid for the old mode because GPIO0 would still be in the old mode before this register is written. Therefore, it is much safer to first set GPIO0 to input or output mode, then change gpio_select_0, and then set GPIO0 to the new mode.</p> <p>000 = Input The logic value sensed on GPIO0 is reflected in register 0x140, bit 0 (gpio_in_status::gpio0).</p> <p>001 = Output GPIO0 actively drives the value specified in register 0x0EF, bit 0 (gpio_out::gpio0).</p> <p>010 = Control Certain device functions can be actively controlled via GPIO0. The device function to be controlled is selected by configuring register gpio_select_0. Whenever a change is detected on GPIO0 or the selected host register bit, then the device ORs together the GPIO and register bit values before applying the corresponding configuration. In this mode, the selected host register bit must satisfy the following requirements:</p> <ol style="list-style-type: none"> 1) It must be R/W type; 2) It cannot be one of the GPIO control registers (including gpio_select_x, gpio_config_x, and gpio_freeze_4_0); 3) It cannot be one of the mailbox registers. <p>011 = Status The device status can be actively supervised via GPIO0. The device mirrors the host register bit specified in register gpio_select_0, onto GPIO0. Typically, the selected host register bit is a status bit (either R or S type) in this mode.</p> |

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| Address: | 0x00E3:0x00E4 | |
|-----------|---------------|--|
| Name: | gpio_select_1 | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | bit | See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit). |
| 11:8 | page | See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page). |
| 7 | reserved | — |
| 6:0 | offset | See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset). |

| Address: | 0x00E5 | |
|-----------|---------------|--|
| Name: | gpio_config_1 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:3 | reserved | — |
| 2:0 | ctrl | See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl). |

| Address: | 0x00E6:0x00E7 | |
|-----------|---------------|--|
| Name: | gpio_select_2 | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | bit | See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit). |
| 11:8 | page | See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page). |
| 7 | reserved | — |
| 6:0 | offset | See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset). |

| Address: | 0x00E8 | |
|-----------|---------------|--|
| Name: | gpio_config_2 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:3 | reserved | — |
| 2:0 | ctrl | See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl). |

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| Address: | 0x00E9:0x00EA | |
|-----------|---------------|--|
| Name: | gpio_select_3 | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | bit | See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit). |
| 11:8 | page | See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page). |
| 7 | reserved | — |
| 6:0 | offset | See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset). |

| Address: | 0x00EB | |
|-----------|---------------|--|
| Name: | gpio_config_3 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:3 | reserved | — |
| 2:0 | ctrl | See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl). |

| Address: | 0x00EC:0x00ED | |
|-----------|---------------|--|
| Name: | gpio_select_4 | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | bit | See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit). |
| 11:8 | page | See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page). |
| 7 | reserved | — |
| 6:0 | offset | See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset). |

| Address: | 0x00EE | |
|-----------|---------------|--|
| Name: | gpio_config_4 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:3 | reserved | — |
| 2:0 | ctrl | See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl). |

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| Address: | 0x00EF | |
|-----------|---------------|---|
| Name: | gpio_out_4_0 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:5 | reserved | — |
| 4 | gpio4 | Sets the output value on pin GPIO4. See gpio0 description. |
| 3 | gpio3 | Sets the output value on pin GPIO3. See gpio0 description. |
| 2 | gpio2 | Sets the output value on pin GPIO2. See gpio0 description. |
| 1 | gpio1 | Sets the output value on pin GPIO1. See gpio0 description. |
| 0 | gpio0 | Sets the output value on pin GPIO0. When the ctrl field of gpio_config_0 is set to 001 = Output then this gpio0 bit specifies the GPIO0 output logic value. |

| Address: | 0x00F0 | |
|-----------|---------------|---|
| Name: | gpo_out_7_0 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | gpo7 | Sets the output value on pin OUT3N. See gpo0 description. |
| 6 | gpo6 | Sets the output value on pin OUT3P. See gpo0 description. |
| 5 | gpo5 | Sets the output value on pin OUT2N. See gpo0 description. |
| 4 | gpo4 | Sets the output value on pin OUT2P. See gpo0 description. |
| 3 | gpo3 | Sets the output value on pin OUT1N. See gpo0 description. |
| 2 | gpo2 | Sets the output value on pin OUT1P. See gpo0 description. |
| 1 | gpo1 | Sets the output value on pin OUT0N. See gpo0 description. |
| 0 | gpo0 | Sets the output value on pin OUT0P. When the OUT0P pin is configured as a general-purpose output (GPO) and the ctrl field in the corresponding output_gpo_config_out_p or output_gpo_config_out_n mailbox register is set to 001 = Output then this bit specifies the OUT0P output logic value. |

| Address: | 0x00F1 | |
|-----------|---------------|---|
| Name: | gpo_out_15_8 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | gpo15 | Sets the output value on pin OUT7N. See gpo0 description. |
| 6 | gpo14 | Sets the output value on pin OUT7P. See gpo0 description. |
| 5 | gpo13 | Sets the output value on pin OUT6N. See gpo0 description. |
| 4 | gpo12 | Sets the output value on pin OUT6P. See gpo0 description. |
| 3 | gpo11 | Sets the output value on pin OUT5N. See gpo0 description. |
| 2 | gpo10 | Sets the output value on pin OUT5P. See gpo0 description. |
| 1 | gpo9 | Sets the output value on pin OUT4N. See gpo0 description. |
| 0 | gpo8 | Sets the output value on pin OUT4P. See gpo0 description. |

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| Address: | 0x00F2 | |
|-----------|---------------|---|
| Name: | gpo_out_19_16 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:4 | reserved | — |
| 3 | gpo19 | Sets the output value on pin OUT9N. See gpo0 description. |
| 2 | gpo18 | Sets the output value on pin OUT9P. See gpo0 description. |
| 1 | gpo17 | Sets the output value on pin OUT8N. See gpo0 description. |
| 0 | gpo16 | Sets the output value on pin OUT8P. See gpo0 description. |

| Address: | 0x00F3 | |
|-----------|-----------------|---|
| Name: | gpio_freeze_4_0 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:5 | reserved | — |
| 4 | gpio4 | See description for gpio0. |
| 3 | gpio3 | See description for gpio0. |
| 2 | gpio2 | See description for gpio0. |
| 1 | gpio1 | See description for gpio0. |
| 0 | gpio0 | Freeze the value in register 0x140 bit 0 (gpio_in_status_4_0::gpio0) if GPIO0 is configured as input or control mode. |

| Address: | 0x00FE | |
|-----------|---------------|--|
| Name: | uport | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | lockout | When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing. |
| 6:1 | reserved | — |
| 0 | status | This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful. |

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| Address: | 0x00FF | |
|-----------|---------------|---|
| Name: | page_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Unsigned binary value of these bits represents selected page for SPI/I ² C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved |

REGISTER LIST PAGE 2, STATUS

| Address: | 0x0140 | |
|-----------|----------------|---|
| Name: | gpio_in_status | |
| Default: | 0x00 | |
| Type: | R | |
| Bit Field | Function Name | Description |
| 7:5 | reserved | — |
| 4 | gpio4 | See description for gpio0. |
| 3 | gpio3 | See description for gpio0. |
| 2 | gpio2 | See description for gpio0. |
| 1 | gpio1 | See description for gpio0. |
| 0 | gpio0 | Logic value seen on pin GPIO0 if it is configured as input or control mode in the ctrl field of register gpio_config_0. |

| Address: | 0x017E | |
|-----------|---------------|--|
| Name: | uport | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | lockout | When set, this field causes all other uport registers to be host read-only. When zero, all registers are open for writing. |
| 6:1 | reserved | — |

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| | | |
|---|--------|--|
| 0 | status | This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful. |
|---|--------|--|

| Address: | 0x017F | |
|-----------|---------------|---|
| Name: | page_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Unsigned binary value of these bits represents selected page for SPI/I ² C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved |

REGISTER LIST PAGE 9, SYNTH AND OUTPUT

synth_ctrl_x

| Address: | 0x0480 | |
|-----------|--------------------|---|
| Name: | synth_ctrl_0 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |
| 1 | spread_spectrum_en | Enable or disable spread spectrum for this synthesizer 0 = Disable |
| 0 | en | Enable or disable the synthesizer: 0 = Disable 1 = Enable |

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| Address: | 0x0481 | |
|-----------|--------------------|--|
| Name: | synth_ctrl_1 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |
| 1 | spread_spectrum_en | See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en). |
| 0 | en | See description for register at address 0x480, bit 0 (synth_ctrl_0::en). |

| Address: | 0x0482 | |
|-----------|--------------------|--|
| Name: | synth_ctrl_2 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |
| 1 | spread_spectrum_en | See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en). |
| 0 | en | See description for register at address 0x480, bit 0 (synth_ctrl_0::en). |

| Address: | 0x0483 | |
|-----------|--------------------|--|
| Name: | synth_ctrl_3 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |
| 1 | spread_spectrum_en | See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en). |
| 0 | en | See description for register at address 0x480, bit 0 (synth_ctrl_0::en). |

| Address: | 0x0484 | |
|-----------|--------------------|--|
| Name: | synth_ctrl_4 | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |
| 1 | spread_spectrum_en | See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en). |
| 0 | en | See description for register at address 0x480, bit 0 (synth_ctrl_0::en). |

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synth_df_offset_manual_x

| Address: | 0x0485:0x0489 | |
|-----------|--------------------------|--|
| Name: | synth_df_offset_manual_0 | |
| Default: | 0x0000000000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 39:0 | — | <p>Manual delta frequency offset adjustment for Synth0. This register contains a 2's complement binary value in steps of 2^{-48}.</p> <p>The frequency offset should be calculated as per formula: $f_{\text{offset}} = -(X/2^{48}) * f_{\text{nom}}$ where, X is 2's complement number specified in this register, f_{nom} is the nominal frequency set by Bs, Ks, Ms, Ns for the synthesizer and f_{offset} is the desired frequency for the output.</p> <p>Note 1: This register can be written as fast as once per 600 μs, but no faster. Note 2: The offset frequency is based on the system clock from the APLL. If the system clock experiences frequency drift, the offset frequency is affected.</p> |

| Address: | 0x048A:0x048E | |
|-----------|--------------------------|---|
| Name: | synth_df_offset_manual_1 | |
| Default: | 0x0000000000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 39:0 | — | See description for register at address 0x485-0x489 (synth_df_offset_manual_0). |

| Address: | 0x048F:0x0493 | |
|-----------|--------------------------|---|
| Name: | synth_df_offset_manual_2 | |
| Default: | 0x0000000000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 39:0 | — | See description for register at address 0x485-0x489 (synth_df_offset_manual_0). |

| Address: | 0x0494:0x0498 | |
|-----------|--------------------------|---|
| Name: | synth_df_offset_manual_3 | |
| Default: | 0x0000000000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 39:0 | — | See description for register at address 0x485-0x489 (synth_df_offset_manual_0). |

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| Address: | 0x0499:0x049D | |
|-----------|--------------------------|---|
| Name: | synth_df_offset_manual_4 | |
| Default: | 0x0000000000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 39:0 | — | See description for register at address 0x485-0x489 (synth_df_offset_manual_0). |

output_ctrl_x

| Address: | 0x04A8 | |
|-----------|---------------|---|
| Name: | output_ctrl_0 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | This field selects the synthesizer that drives this output. 0=Synth0, 1=Synth2, etc. |
| 3 | stop_hz | This is a configuration bit that does not trigger action. 0 = After the output stops, it stays low or high as set by the stop_high field (bit 2). 1 = After the output stops, the output driver is disabled and the output goes high-impedance This bit does not affect the N-divided clock under the N-divider mode. The N-divided clock could stop at either high or low. |
| 2 | stop_high | This is a configuration bit that does not trigger action. 0 = Stop low. When the output clock is stopped by the stop field (bit 1), the output stops after a falling edge. 1 = Stop high. When the output clock is stopped by the stop field (bit 1), the output stops after a rising edge. This bit does not affect the N-divided clock under the N-divider mode. The N-divided clock could stop at either high or low. |
| 1 | stop | 0 = Restart the output clock cleanly. Wait until the proper edge and start the output clock signal. 1 = Stop the output clock cleanly. Wait until the proper edge and stop the output clock signal at 1 or 0 based on the stop_high bit. |
| 0 | en | Enable or disable the output module. 0 = Disable. 1 = Enable. |

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| Address: | 0x04A9 | |
|-----------|---------------|---|
| Name: | output_ctrl_1 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04AA | |
|-----------|---------------|---|
| Name: | output_ctrl_2 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04AB | |
|-----------|---------------|---|
| Name: | output_ctrl_3 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |

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| | | |
|---|------|---|
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04AC | |
|-----------|---------------|---|
| Name: | output_ctrl_4 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04AD | |
|-----------|---------------|---|
| Name: | output_ctrl_5 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04AE | |
|-----------|---------------|---|
| Name: | output_ctrl_6 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |

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| | | |
|---|-----------|--|
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04AF | |
|-----------|---------------|---|
| Name: | output_ctrl_7 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04B0 | |
|-----------|---------------|---|
| Name: | output_ctrl_8 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

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| Address: | 0x04B1 | |
|-----------|---------------|---|
| Name: | output_ctrl_9 | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | reserved | — |
| 6:4 | synth_sel | See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel). |
| 3 | stop_hz | See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz). |
| 2 | stop_high | See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high). |
| 1 | stop | See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop). |
| 0 | en | See description for register at address 0x4A8, bit 0 (output_ctrl_0::en). |

| Address: | 0x04FE | |
|-----------|---------------|--|
| Name: | uport | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | lockout | When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing. |
| 6:1 | reserved | — |
| 0 | status | This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful. |

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| Address: | 0x04FF | |
|-----------|---------------|---|
| Name: | page_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Unsigned binary value of these bits represents selected page for SPI/I ² C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved |

REGISTER LIST PAGE 13, SYNTH MAILBOX

| Address: | 0x0682:0x0683 | |
|-----------|---------------|---|
| Name: | synth_mb_mask | |
| Default: | 0x0001 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15:5 | reserved | — |
| 4:0 | mask | For a write operation (see synth_mb_sem::wr bit), this field determines which synth's configuration is modified. Multiple bits can be set to affect multiple synths in a single operation. For a read operation (see synth_mb_sem::rd bit), this field determines which synth configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 for Synth0, bit 1 for Synth1, etc. |

| Address: | 0x0684 | |
|-----------|---------------|-------------|
| Name: | synth_mb_sem | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |

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| | | |
|---|----|---|
| 1 | rd | <p>When this bit is written to a one by the host controller, the device performs a read of the masked synth mailbox (see synth_mb_mask register). Only one mask bit should be set in this case.</p> <p>When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding synth configuration.</p> |
| 0 | wr | <p>When this bit is written to a one by the host controller (and the read bit is zero), the device performs a write of the masked synth mailbox(es) (see synth_mb_mask register). All of the configuration options on this page are applied to each of the synth indicated by synth_mb_mask. The write is complete when this register reads back a zero.</p> |

| Address: | 0x0686:0x0687 | |
|-----------|-----------------|---|
| Name: | synth_freq_base | |
| Default: | 0x0001 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15:0 | — | <p>Sets the synthesizer base frequency (Bs), in Hz. The final frequency is given by: $fsynth = Bs \times Ks \times Ms / Ns$</p> <p>Valid values for this registers must satisfy the rule 500 MHz divided by value is an integer.</p> <p>The synthesizer clock frequency has to satisfy the following range: $187.5 \text{ MHz} \leq fsynth \leq 750 \text{ MHz}$. If the central frequency offset (central_freq_offset register) is non-zero, the range is affected accordingly. In addition, some margin is needed to accommodate any frequency variations, such as crystal or input clock frequency variation.</p> <p>Typically this register can be left at its default value of 1 Hz and the synthesizer frequency can be fully specified by the synth_freq_mult, synth_freq_m and synth_freq_n registers.</p> |

| Address: | 0x0688:0x068B | |
|-----------|-----------------|--|
| Name: | synth_freq_mult | |
| Default: | 0x12A05F20 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | <p>Sets the synthesizer frequency multiplier (Ks). See synth_freq_base description for more information.</p> |

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| Address: | 0x068C:0x068D | |
|-----------|---------------|--|
| Name: | synth_freq_m | |
| Default: | 0x0001 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15:0 | — | Sets the synthesizer frequency numerator (Ms). See synth_freq_base description for more information. |

| Address: | 0x068E:0x068F | |
|-----------|---------------|--|
| Name: | synth_freq_n | |
| Default: | 0x0001 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15:0 | — | Sets the synthesizer frequency numerator (Ns). See synth_freq_base description for more information. |

| Address: | 0x0690:0x0691 | |
|-----------|--------------------------|---|
| Name: | synth_phase_compensation | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15:0 | — | <p>Specifies the amount of initial phase shift that is applied to this synthesizer when the synthesizer is turned on. This number is a 16-bit signed integer with LSB of 1 ps.</p> <p>After the first time a non-zero value is written to this register, the actual synthesizer phase has an offset, in ps, of $389000/vco*(12-vco)/vco$ where vco is the actual VCO frequency in GHz. For example 303ps for 12114.21MHz. This offset is consistent and can be compensated by adding the offset to the desired phase and writing the result to the register.</p> <p>Note that this offset is not present when the device is first configured from flash after power-up or reset. or when the device is configured by loading a config file using the GUI after power-up or reset. In those cases it will only be present if a new value is written to this register.</p> |

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| Address: | 0x0694 | |
|-----------|---------------------------|---|
| Name: | synth_spread_spectrum_cfg | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:1 | reserved | — |
| 0 | mode | <p>Spread spectrum mode: 0 - Center mode 1 - Down mode</p> <p>In both modes, the synthesizer frequency starts at the nominal frequency configured for the synthesizer. In the center mode, the frequency linearly sweeps down half of the peak-to-peak spread, then up the whole peak-to-peak spread then back to the nominal frequency. In the down mode, the frequency linearly sweeps down the whole peak-to-peak spread then back to the nominal frequency. The peak-to-peak spread is specified by the synth_spread_spectrum_spread register (0x0697). The period of this frequency modulation is specified by the synth_spread_spectrum_rate register (0x0695 to 0x0696).</p> |

| Address: | 0x0695:0x0696 | |
|-----------|----------------------------|--|
| Name: | synth_spread_spectrum_rate | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15:0 | — | Spread spectrum modulate rate in 250Hz units. The valid range is 25 kHz to 55 kHz (100 to 220 decimal for the register value). |

| Address: | 0x0697 | |
|-----------|------------------------------|---|
| Name: | synth_spread_spectrum_spread | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Peak-to-peak spread of synthesizer frequency, in 0.025% units. The valid range is 0.025% to 5% (1 to 200 decimal for the register value). |

| Address: | 0x06FE | |
|-----------|---------------|---|
| Name: | uport | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | lockout | When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing. |
| 6:1 | reserved | — |

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| | | |
|---|--------|--|
| 0 | status | This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful. |
|---|--------|--|

| Address: | 0x06FF | |
|-----------|---------------|---|
| Name: | page_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Unsigned binary value of these bits represents selected page for SPI/I ² C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved |

REGISTER LIST PAGE 14, OUTPUT MAILBOX

| Address: | 0x0702:0x0703 | |
|-----------|----------------|--|
| Name: | output_mb_mask | |
| Default: | 0x0001 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15:10 | reserved | — |
| 9:0 | mask | For a write operation (see output_mb_sem::wr bit), this field determines which output's configuration is modified. Multiple bits can be set to affect multiple outputs in a single operation. For a read operation (see output_mb_sem::rd bit), this field determines which output configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 for OUT0, bit 1 for OUT1, etc. |

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| Address: | 0x0704 | |
|-----------|---------------|---|
| Name: | output_mb_sem | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |
| 1 | rd | When this bit is written to a one by the host controller, the device performs a read of the masked output mailbox (see output_mb_mask register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding output configuration. |
| 0 | wr | When this bit is written to a one by the host controller (and the read bit is zero), the device performs a write of the masked output mailbox(es) (see output_mb_mask register). All of the configuration options on this page are applied to each of the outputs indicated by the mask. The write is complete when this register reads back a zero. |

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| Address: | 0x0705 | |
|-----------|---------------|--|
| Name: | output_mode | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:4 | signal_format | <p>0000 = Disabled (High Impedance, Low Power Mode)</p> <p>0001 = LVDS mode (V_{OD} internally set to 400 mV, output_driver_level::vod ignored, V_{CM} set by output_driver_config::vcm which defaults to 1.2V)</p> <p>0010 = Differential mode (V_{OD} set by output_driver_level::vod, V_{CM} set by output_driver_config::vcm)</p> <p>0011 = Low-V_{CM} mode (approx. 0.375V V_{CM}, approx. 0.75V V_{OD})</p> <p>Must set output_driver_level::vod to 0x9, 0xA, 0xB, or 0xC (0xC recommended), output_driver_config::vcm to 0xF, and output_driver_config::regv to 0xD.</p> <p>0100 = Two CMOS, OCxN in phase with OCxP</p> <p>0101 = One CMOS, OCxP Enabled, OCxN High impedance</p> <p>0110 = One CMOS, OCxP High impedance, OCxN Enabled</p> <p>0111 = Two CMOS, OCxN inverted vs. OCxP</p> <p>10xx = Reserved</p> <p>1100 = Two CMOS, N-pin divide mode, OCxN in phase with OCxP</p> <p>1101 = Reserved</p> <p>1110 = Reserved</p> <p>1111 = Two CMOS, N-pin divide mode, OCxN inverted vs. OCxP</p> <p>CMOS signal amplitude for OUTx is set by VDDx supply voltage (1.5V, 1.8V, 2.5V, or 3.3V).</p> |
| 3 | polarity | <p>1 = Inverted</p> <p>0 = Normal</p> <p>Not applicable to N-pin divide modes.</p> |
| 2:0 | clock_type | <p>000 = Normal clock</p> <p>Other values reserved</p> |

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| Address: | 0x0706 | |
|-----------|---------------------|---|
| Name: | output_driver_level | |
| Default: | 0x52 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:4 | vod | <p>This field specifies the differential output voltage (V_{OD}) for the differential output driver. In the device this field actually controls driver output current: 0000 = 3 mA, 0001 = 4 mA, etc. When the specified current is driven into the required external 100Ω termination resistor, the voltage across the termination resistor is the desired V_{OD}. V_{OD} is equivalent to the single-ended voltage swing of the OUT0P pin or the OUT0N pin. This field is ignored for CMOS signal formats.</p> <p>Programmable differential signal format, DC-coupled, internal 200Ω bias resistor disabled, 100Ω termination at receiver: 0000 = 330 mV 0001 = 440 mV 0010 = 550 mV 0011 = 660 mV 0100 = 770 mV (recommended for LVPECL) 0101 = 880 mV (default) 0110 = 990 mV 0111-1111 = Do not use</p> <p>Programmable differential signal format, AC-coupled, internal 200Ω bias resistor enabled, 100Ω termination at receiver: 000x = Do not use 0010 = 367 mV 0011 = 440 mV 0100 = 513 mV 0101 = 587 mV (default) 0110 = 660 mV 0111 = 733 mV 1000 = 807 mV 1001 = 880 mV 1010-1111 = Do not use</p> <p>When output_mode::signal_format=0001 (LVDS), V_{OD} is internally set to 440 mV and this field is ignored.</p> <p>When output_mode::signal_format=0011 (Low-V_{CM}), set this vod field to 0x9, 0xA, 0xB, or 0xC (0xC recommended).</p> <p>The bias resistor is enabled/disabled by output_driver_config::rbias (0x0707:0x0708).</p> |

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| | | |
|-----|-------|---|
| 3:2 | vddo | <p>This field specifies the power supply voltage externally applied to the VDDOx pin (where x is the OUTx number, 0 to 9). The device does not do anything with this value, but the GUI and system software can use this field to indicate the VDDOx voltage and then compare it to the internal regulator voltage (output_driver config::regv). In general, GUI and system software must ensure regulator voltage \leq VDDOx voltage – 0.5V. For the special case of LVDS signal format with VDDOx = 1.8V, the 0.5V term can be reduced to 0.3V. VDDOx of 1.5V is only valid for CMOS signal formats. VDDOx of 1.8V is only valid for LVDS and CMOS signal formats</p> <p>00 = 3.3V 01 = 2.5V 10 = 1.8V 11 = 1.5V</p> |
| 1:0 | drive | <p>Output driver CMOS level.</p> <p>00 = 1x 01 = 2x 10 = 3x 11 = 4x</p> <p>The 3x and 4x settings are recommended for lowest-jitter applications. This field is ignored for non-CMOS signal formats. Typical output impedances of the CMOS driver are listed below. The trace impedance and parasitics must be taken into account when choose an external source series resistor value</p> <p>VDDO = 3.3V, Drive = 4x: 18Ω VDDO = 3.3V, Drive = 3x: 23Ω VDDO = 3.3V, Drive = 2x: 33Ω VDDO = 3.3V, Drive = 1x: 65Ω VDDO = 2.5V, Drive = 4x: 20Ω VDDO = 2.5V, Drive = 3x: 27Ω VDDO = 2.5V, Drive = 2x: 39Ω VDDO = 2.5V, Drive = 1x: 80Ω VDDO = 1.8V, Drive = 4x: 28Ω VDDO = 1.8V, Drive = 3x: 37Ω VDDO = 1.8V, Drive = 2x: 55Ω VDDO = 1.8V, Drive = 1x: not recommended VDDO = 1.5V, Drive = 4x: 29Ω VDDO = 1.5V, Drive = 3x 2x 1x: not recommended</p> |

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| Address: | 0x0707:0x0708 | |
|-----------|----------------------|--|
| Name: | output_driver_config | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | vreg1p1_vsel | Output pad 1.1V regulator voltage select. Leave this field at its default value unless recommended by Microchip. 000 = 1.10V (default) 001 = 0.95V 010 = 1.00V 011 = 1.05V 100 = 0.90V 101 = 1.15V 110 = 1.20V 111 = 1.25V |
| 11:8 | rbias | This field enables/disables an internal bias resistor between OUTxP and OUTxN. When the output driver is in LVDS or programmable differential mode and the device is AC-coupled to the receiver, the output driver requires a DC path between OUTxP and OUTxN. This resistor can provide that DC path. This field should be set to 0 for CMOS and Low- V_{CM} signal formats. 0000 = None 0001 = approx. 200 Ω 0002 to 1111 = None |
| 7:4 | regv | Output driver regulator voltage. This value must be $> V_{CM} + 0.5V_{OD} + 0.5V$ except for the case of LVDS with $V_{DDOx} = 1.8V$ for which this field should be set to 0. This field should be set to 0 for CMOS signal formats. 0000 = Center voltage close to 2.2V (default) 1000 = 2.28V 1001 = 2.37V 1010 = 2.45V 1011 = 2.56V 1100 = 2.67V 1101 = 2.79V (Use this value when signal format = Low- V_{CM}) |
| 3:0 | vcm | Output driver common mode voltage 0000 = 1.2V (default) - recommended for LVDS and AC-coupled 0100 = 1.0V 0101 = 1.1V 0110 = 1.3V 0111 = 1.4V 1000 = 1.5V 1001 = 1.6V 1010 = 1.8V 1011 = 1.9V 1100 = 2.0V - typical for DC-coupled LVPECL 1101 = 2.1V 1110 = 2.2V 1111 = Use this decode only if signal format = Low- V_{CM} This field is ignored for CMOS signal formats. |

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| Address: | 0x070C:0x070F | |
|-----------|---------------|---|
| Name: | output_div | |
| Default: | 0x00000002 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | The divider of the output clock. Expressed as the number of synthesizer clock cycles. The value 0 is undefined. The value 1 bypasses the output divider and pulse width logic and passes the synthesizer frequency directly to the output driver. |

| Address: | 0x0710:0x0713 | |
|-----------|---------------|---|
| Name: | output_width | |
| Default: | 0x00000002 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | The pulse width of the output clock. Expressed as the number of 1/2 synthesizer clock cycles. Valid range has a minimum of 2 (half cycles, i.e. 1 cycle) and a maximum of $\text{output_div} * 2 - 1$ (half cycles). This field is ignored when output_div (0x70C-0x70F) is less than 2. |

| Address: | 0x0714:0x0717 | |
|-----------|---------------------|--|
| Name: | output_esync_period | |
| Default: | 0x00000002 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | For N-pin divide modes, the period of the N-pin clock. Expressed as the number of output divider clock cycles. The values 0 and 1 are undefined. This field is ignored when output_div (0x70C-0x70F) is less than 2. |

| Address: | 0x0718:0x071B | |
|-----------|--------------------|--|
| Name: | output_esync_width | |
| Default: | 0x00000002 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | For N-pin divide modes, the pulse width of the N-pin divided clock. Expressed as the number of 1/2 output clock cycles (instead of synthesizer clock cycles). This field is ignored when output_div (0x70C-0x70F) is less than 2. |

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| Address: | 0x0720:0x0723 | |
|-----------|---------------------------|--|
| Name: | output_phase_compensation | |
| Default: | 0x00000000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 31:0 | — | Output phase shift, expressed in $\frac{1}{2}$ synth clock cycles. Two-complement signed integer. A positive value moves the phase of the output later in time (more to the right on a scope). A negative value moves the phase earlier in time (more to the left on a scope). Note: non-zero values are not supported when output_mode::signal_format is one of the CMOS N-pin divided modes. To make an output pair with this configuration later than other outputs, consider moving the other outputs earlier instead. Another option is to put the output pair on its own synthesizer and use synthesizer phase adjustment (synth_phase_compensation register). |

| Address: | 0x0724 | |
|-----------|---------------|--|
| Name: | output_gpo_en | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:2 | reserved | — |
| 1 | out_n | 0 = The output is driven by the divided clock. 1 = The output is driven according to Register 0x72A (output_gpo_config_out_n). |
| 0 | out_p | 0 = The output is driven by the divided clock. 1 = The output is driven by according to Register 0x727 (output_gpo_config_out_p). |

| Address: | 0x0725:0x0726 | |
|-----------|-------------------------|---|
| Name: | output_gpo_select_out_p | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | bit | This field works with the page and offset fields to select a single bit in the host register map. Specifically, this field selects the bit position in the selected register byte. |
| 11:8 | page | This field works with the bit and offset fields to select a single bit in the host register map. Specifically, this field selects the page. |
| 7 | reserved | — |
| 6:0 | offset | When this GPO is configured to the status mode, this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page. |

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| Address: | 0x0727 | |
|-----------|-------------------------|--|
| Name: | output_gpo_config_out_p | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:3 | reserved | — |
| 2:0 | ctrl | <p>This field determines the mode of operation for this GPO. If the GPO is to be set to status mode, Register 0x725-0x726 (gpo_select) should be set in the previous or in the same mailbox write.</p> <p>001 = Output GPOx actively drives the value specified in register gpo_out (0xF0-0xF2), where x = output index * 2.</p> <p>011 = Status The device status can be actively supervised via GPOx. The device mirrors the host register bit, specified in register output_gpo_select_out_p, onto GPOx. Typically, the selected host register bit is a status bit (either R or S type) in this mode.</p> <p>Other values = Reserved</p> <p>Note: To use the above modes, the output must be set to CMOS (Register 0x705, bit 7:4, output_mode: signal_format) with GPO enabled (Register 0x724, bit 0, output_gpo_en.out_p).</p> |

| Address: | 0x0728:0x0729 | |
|-----------|-------------------------|---|
| Name: | output_gpo_select_out_n | |
| Default: | 0x0000 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 15 | reserved | — |
| 14:12 | bit | This field works with the page and offset fields to select a single bit in the host register map. Specifically, this field selects the bit position in the selected register byte. |
| 11:8 | page | This field works with the bit and offset fields to select a single bit in the host register map. Specifically, this field selects the page. |
| 7 | reserved | — |
| 6:0 | offset | When this GPO is configured to the status mode, this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page. |

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| Address: | 0x072A | |
|-----------|-------------------------|---|
| Name: | output_gpo_config_out_n | |
| Default: | 0x01 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:3 | reserved | — |
| 2:0 | ctrl | <p>This field determines the mode of operation for this GPO. If the GPO is to be set to status mode, Register 0x728-0x729 (output_gpo_select_out_n) should be set in the previous or in the same mailbox write.</p> <p>001 = Output GPOx actively drives the value specified in register gpo_out (0xF0-0xF2), where x = output index * 2 + 1.</p> <p>011 = Status The device status can be actively supervised via GPOx. The device mirrors the host register bit, specified in register output_gpo_select_out_n, onto GPOx. Typically, the selected host register bit is a status bit (either R or S type) in this mode.</p> <p>Other values = Reserved</p> <p>Note: To use the above modes, the output must be set to CMOS (Register 0x705, bit 7:4, output_mode: signal_format) with GPO enabled (Register 0x724, bit 1, output_gpo_en:out_n).</p> |

| Address: | 0x077E | |
|-----------|---------------|--|
| Name: | uport | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7 | lockout | When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing. |
| 6:1 | reserved | — |
| 0 | status | This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful. |

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| Address: | 0x077F | |
|-----------|---------------|---|
| Name: | page_sel | |
| Default: | 0x00 | |
| Type: | R/W | |
| Bit Field | Function Name | Description |
| 7:0 | — | Unsigned binary value of these bits represents selected page for SPI/I ² C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved |

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9.0 ELECTRICAL CHARACTERISTICS

TABLE 9-1: ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min. | Max. | Units |
|---|-----------------|------|-------|-------|
| Supply Voltage, nominal 1.8V | VDD18 | -0.3 | +1.98 | V |
| Supply Voltage, nominal 3.3V | VDD33 | -0.3 | +3.6 | V |
| Supply voltage, nominal 1.8V, 2.5V, or 3.3V | VDDIO | -0.3 | +3.6 | V |
| Supply voltage, nominal 1.5V, 1.8V, 2.5V, or 3.3V | VDDOx | -0.3 | +3.6 | V |
| Voltage on any pin | VPIN | -0.3 | +3.6 | V |
| Storage Temperature Range | T _{ST} | -55 | +125 | °C |

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

*Voltages are with respect to ground (VSS) unless otherwise stated.

Note 1: The typical values listed in the tables of Section 9 are at nominal voltage and room temperature and are not production tested.

2: Specifications to -40°C and +85°C are guaranteed by design or characterization and not production tested.

TABLE 9-2: RECOMMENDED DC OPERATING CONDITIONS

| Min. and max. values in all electrical tables below are over these operating conditions. | | | | | |
|--|----------------|-------|------|-------|-------|
| Parameter | Symbol | Min. | Typ. | Max. | Units |
| Supply Voltage 3.3V | VDD33 | 3.135 | 3.3 | 3.465 | V |
| Supply Voltage 1.8V | VDD18 | 1.71 | 1.8 | 1.89 | V |
| Output Supply Voltage | VDDOx | 1.425 | 1.5 | 1.575 | V |
| | | 1.71 | 1.8 | 1.89 | |
| | | 2.375 | 2.5 | 2.625 | |
| | | 3.135 | 3.3 | 3.465 | |
| Digital I/O Supply Voltage | VDDIO | 1.71 | 1.8 | 1.89 | V |
| | | 2.375 | 2.5 | 2.625 | |
| | | 3.135 | 3.3 | 3.465 | |
| Operating Temperature | T _A | -40 | — | +85 | °C |

TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS

| Characteristics | Symbol | Min. | Typ. (Note 1) | Max. | Units | Notes | |
|--|-------------------|------------------------|---------------|------|-------|--------|--------|
| Total power, Synth1 and six LVDS outputs enabled | P _{DISS} | — | 0.8 | — | W | — | |
| Total current, 3.3V supply (VDD33+VDDOx pins) | I _{DD33} | — | 160 | 322 | mA | Note 2 | |
| Total current, 1.8V supply (VDD18 pins) | I _{DD18} | — | 207 | 519 | mA | Note 2 | |
| Supply current change from enabling or disabling: | | | | | | | |
| the crystal driver circuit | VDD33 | ΔI _{DD33_XO} | — | 3 | — | mA | — |
| | VDD18 | ΔI _{DD18_XO} | — | 7 | — | mA | — |
| the crystal doubler | VDD33 | ΔI _{DD33_DBL} | — | 0 | — | mA | — |
| | VDD18 | ΔI _{DD18_DBL} | — | 2 | — | mA | — |
| a synthesizer | VDD33 | ΔI _{DD33_SYN} | — | 0.5 | — | mA | — |
| | VDD18 | ΔI _{DD18_SYN} | — | 27 | — | mA | Note 7 |

TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS (CONTINUED)

| Characteristics | | Symbol | Min. | Typ. (Note 1) | Max. | Units | Notes |
|---|-------|-------------------|------|------------------|------|-------|------------------------------------|
| an OUTxP/N output pair, LVDS | VDDOx | ΔI_{DDOL} | — | 12 | — | mA | 156.25 MHz, Note 5 |
| | | | — | 18 | — | mA | 700 MHz, Note 6 |
| an OUTxP/N output pair, LVPECL | VDDOx | ΔI_{DDOL} | — | 14 | — | mA | 156.25 MHz, Note 5 |
| | | | — | 21 | — | mA | 700 MHz, Note 6 |
| an OUTxP/N output pair, Low-V _{cm} | VDDOx | ΔI_{DDOL} | — | 25 | — | mA | 156.25 MHz, Note 8 |
| an OUTxP/N output pair, CMOS | VDDOx | ΔI_{DDOC} | — | 3 | — | mA | 25 MHz, Note 3 |
| an OUTxP/N output pair, CMOS | VDDOx | ΔI_{DDOC} | — | 29 | — | mA | 250 MHz, Note 4 |

Note 1: Typical values measured at nominal supply voltages and 25°C ambient temperature.

- 2:** Max I_{DD} measurements made with all blocks enabled, 49.152 MHz crystal doubled as input clock, all synthesizers enabled, all output dividers dividing by 4, all outputs enabled as LVPECL outputs (with `output_driver_level::vod=0x5`) driving 156.25 MHz signals, all VDDO at 3.3V, and 200Ω differential bias resistors enabled for all output pairs. Typical I_{DD} measurements made with same setup as max. I_{DD} but two synthesizers enabled, six outputs enabled with LVDS signal format, and 200Ω differential bias resistors disabled.
- 3:** VDDOx=3.3V, 1x drive strength, $f_O=25$ MHz, 18 pF load per pin. Specifies the current for the OUTxP/N pair. Divide by 2 for per-pin current.
- 4:** VDDOx=3.3V, 1x drive strength, $f_O=250$ MHz, 18 pF load per pin. Specifies the current for the OUTxP/N pair. Divide by 2 for per-pin current.
- 5:** Tested at 156.25 MHz. With internal 200Ω bias resistor disabled or enabled (driver is constant current).
- 6:** Tested at 700 MHz. With internal 200Ω bias resistor disabled or enabled (driver is constant current).
- 7:** Tested with all synthesizers at 312.5 MHz.
- 8:** Tested with 50Ω to ground load on each of OUTxP and OUTxN. Internal 200Ω bias resistor must be disabled for Low-V_{CM} mode.

TABLE 9-4: ELECTRICAL CHARACTERISTICS: OSCB CLOCK INPUT

This table covers the case when there is no external crystal connected and an external oscillator or clock signal is connected to OSCB.

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|---------------------------------------|----------|------|------|------|-------|------------------------|
| Single-ended input high voltage, OSCB | V_{IH} | 1.3 | — | — | V | — |
| Single-ended input low voltage, OSCB | V_{IL} | — | — | 0.75 | V | — |
| Input frequency, OSCB | f_{IN} | 9.72 | — | 200 | MHz | Note 2 |
| Input frequency, OSCB | f_{IN} | 200+ | — | 400 | MHz | Note 3 |
| Input leakage current | I_{IL} | -10 | — | 10 | μA | — |
| Input duty cycle | — | 40 | — | 60 | % | Note 1 |

Note 1: 1.1V threshold.

- 2:** OSCB frequencies below 48 MHz cause higher output jitter all else being equal.
- 3:** Must have `sys_apll_source_config::div` set to divide by 2 or more for OSCB frequencies > 200 MHz.

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TABLE 9-5: ELECTRICAL CHARACTERISTICS: OTHER INPUTS AND I/O (BIDIRECTIONAL)

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|--|-----------------|--------------------------|------|-------------------------|-------|--|
| Input high voltage, SCK_SCL and SI_SDA in I ² C Mode | V _{IH} | 0.7 x V _{DDIO} | — | — | V | — |
| Input low voltage, SCK_SCL and SI_SDA in I ² C Mode | V _{IL} | — | — | 0.3 x V _{DDIO} | V | — |
| Input high voltage, RST_B | V _{IH} | 2.0 | — | 3.6 | V | — |
| Input low voltage, RST_B | V _{IL} | -0.3 | — | 0.8 | V | — |
| Input high voltage, all other digital inputs, SCK_SCL and SI_SDA (in SPI mode), SO_IF1, CS_B_IF0, all GPIOx_ACx | V _{IH} | 2.0 | — | 3.6 | V | V _{DDIO} = 3.3V±5% |
| | | 1.7 | — | 3.6 | V | V _{DDIO} = 2.5V±5% |
| | | 1.3 | — | 3.6 | V | V _{DDIO} = 1.8V±5% |
| Input low voltage, all other digital inputs, SCK_SCL and SI_SDA (in SPI mode), SO_IF1, CS_B_IF0, all GPIOx_ACx | V _{IL} | -0.3 | — | 0.8 | V | V _{DDIO} = 3.3V±5% |
| | | -0.3 | — | 0.7 | V | V _{DDIO} = 2.5V±5% |
| | | -0.3 | — | 0.55 | V | V _{DDIO} = 1.8V±5% |
| Input leakage current, RST_B | I _{IL} | -100 | — | 10 | µA | V _I = 0 - V _{DD33} , Note 1 |
| Input leakage current, CS_B_IF0 | I _{IL} | -100 | — | 10 | µA | V _I = 0 - V _{DDIO} , Note 1 |
| Input leakage current, SCK_SCL, SI_SDA, SO_IF1 | I _{IL} | -10 | — | 10 | µA | V _I = 0 - V _{DDIO} , Note 1 |
| Input leakage current, all GPIOx_ACx | I _{IL} | -10 | — | 100 | µA | V _I = 0 - V _{DDIO} , Note 1 |
| Input capacitance | C _{IN} | — | 3 | 10 | pF | — |
| Input hysteresis, SCK_SCL and SI_SDA in I ² C Mode | — | 0.05 x V _{DDIO} | — | — | mV | — |
| Input hysteresis, all other digital inputs: RST_B, SCK_SCL and SI_SDA (in SPI mode), SO_IF1, CS_B_IF0, all GPIOx_ACx | — | — | 50 | — | mV | — |
| Output leakage (when high impedance) | I _{LO} | -10 | — | 10 | µA | V _I = 0 - V _{DDIO} , Note 1 |
| GPIOx_ACx, CSB_IF0 and SO_IF1 to RST_B setup time | t _{SU} | 50 | — | — | ns | — |
| GPIOx_ACx, CSB_IF0 and SO_IF1 to RST_B hold time | t _{HD} | — | — | 0 | ns | — |

Note 1: Positive leakage is current flowing into the device.

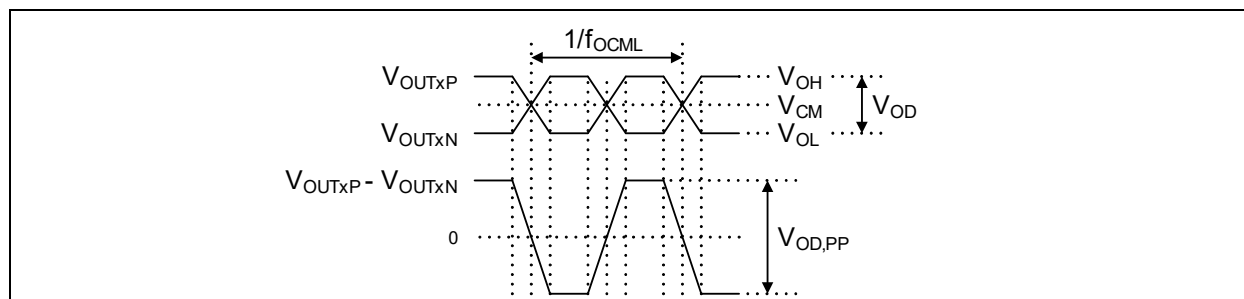


FIGURE 9-1: Electrical Characteristics: Differential Clock Outputs.

TABLE 9-6: ELECTRICAL CHARACTERISTICS: OUTP/N LVDS CLOCK OUTPUTS

VDDOx = 1.8V±5% or 2.5V±5% or 3.3V±5% for LVDS operation.

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes | |
|---|---------------------------------|-------------------|------|------|------------------|---|--|
| Output frequency | f _{OCD} | — | — | 750 | MHz | — | |
| Output common-mode voltage | V _{CM} | VDDO=2.5V or 3.3V | 1.1 | 1.2 | 1.3 | V | Note 1, Note 2, Note 3 See Figure 9-1 |
| | | VDDO=1.8V | 0.7 | 0.9 | 1.1 | V | |
| Output differential voltage | V _{OD} | 320 | 430 | 537 | mV | Note 1, Note 2, Note 3, See Figure 9-1 | |
| Output differential swing, peak-to-peak | V _{OD,PP} | 640 | 860 | 1074 | mV _{PP} | Note 1, Note 2 See Figure 9-1 | |
| Output rise/fall time | t _R , t _F | — | 175 | — | ps | 20% to 80% | |
| Output duty cycle | — | 45 | 50 | 55 | % | — | |

- Note 1:** Measured with 100Ω between OUTxP and OUTxN. Application notes: Output must have 100Ω to 200Ω DC path between OUTxP and OUTxN for proper operation. See Figure 5-1 for recommended external components. When the output signal is AC-coupled an internal 200Ω bias resistor can be switched into the circuit using `output_driver_config::rbias` to meet this requirement. When this 200Ω resistor is in parallel with 100Ω differential termination at the receiver, the actual V_{OD} amplitude is 2/3 of the number shown above. If larger amplitude is needed, the output should be configured for programmable differential mode where V_{OD} is configurable and V_{CM}=1.2V.
- 2:** With `output_mode::signal_format=1` (LVDS) and `output_driver_config::vcm=0x0`. Differential output common-mode voltage is programmable. See Section 5.2.1.
- 3:** Must have `output_driver_config::regv=0` for LVDS with VDDOx=1.8V. Power supply noise rejection may not be as good for LVDS with VDDOx=1.8V compared with VDDOx=2.5V or 3.3V

TABLE 9-7: ELECTRICAL CHARACTERISTICS: OUTP/N LVPECL CLOCK OUTPUTS

VDDOx = 2.5V±5% or 3.3V±5% for LVPECL operation.

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|---|---------------------------------|------|------|------|------------------|----------------------------|
| Output frequency | f _{OCD} | — | — | 750 | MHz | — |
| Output common-mode voltage, VDDOx=3.3V | V _{CM} | 1.80 | 1.90 | 2.05 | V | Note 1, Note 2, Figure 9-1 |
| Output common-Mode voltage, VDDOx=2.5V | V _{CM} | 1.1 | 1.2 | 1.3 | V | Note 1, Note 2, Figure 9-1 |
| Output differential voltage | V _{OD} | 600 | 780 | 1000 | mV | Note 1, Note 2, Figure 9-1 |
| Output differential swing, peak-to-peak | V _{OD} | 1200 | 1560 | 2000 | mV _{PP} | Note 1, Note 2, Figure 9-1 |
| Output rise/fall time | t _R , t _F | — | 185 | — | ps | 20% - 80% |
| Output duty cycle | — | 45 | 50 | 55 | % | — |

- Note 1:** Measured with 100Ω between OUTxP and OUTxN. Application notes: Output must have 100Ω to 200Ω DC path between OUTxP and OUTxN for proper operation. See Figure 5-1 for recommended external components. When the output signal is AC-coupled an internal 200Ω bias resistor can be switched into the circuit using `output_driver_config::rbias` to meet this requirement. When this 200Ω resistor is in parallel with 100Ω differential termination at the receiver, the actual V_{OD} amplitude is 2/3 of the number shown above. If larger amplitude is needed, the output should be configured for programmable differential mode where V_{OD} is configurable.
- 2:** With `output_mode::signal_format=2` (programmable differential) and `output_driver_level::vod=0x4`. With `output_driver_config::vcm=0x0` for 2.5V and `0xC` for 3.3V. Differential output common-mode voltage and differential voltage (i.e. signal amplitude) are programmable. See Section 5.2.1

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TABLE 9-8: ELECTRICAL CHARACTERISTICS: OUTP/N LOW-V_{CM} CLOCK OUTPUTS

VDDOx = 3.3V±5% for Low-V_{CM} operation.

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|-----------------------------|-----------------------------------|----------------------|------|------|-------|--------------------|
| Output frequency | f _{OCD} | — | — | 160 | MHz | — |
| Output common-mode voltage | V _{CM} | V _{OD} / 2 | | | V | Note 1, Figure 9-1 |
| Output differential voltage | V _{OD} | 600 | 810 | 1000 | mV | Note 1, Figure 9-1 |
| Output rise/fall time | t _R , t _F | — | 310 | — | ps | 20% to 80% |
| Output duty cycle | — | 45 | 50 | 55 | % | Note 2 |

Note 1: Each of OUTxP and OUTxN with 50Ω termination resistor to ground. With `output_mode::signal_format=0x3`, `output_driver_level::vod=0xC`, `output_driver_config::vcm=0xF` and `output_driver_config::regv=0xD`.

2: Duty cycle measured differentially.

TABLE 9-9: ELECTRICAL CHARACTERISTICS: OUTP/N CMOS CLOCK OUTPUTS

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|---|-----------------------------------|----------------|------|------|-------|--------------------|
| Output frequency | f _{OCMOS} | — | — | 250 | MHz | Note 1 |
| Output high voltage | V _{OH} | VDDOx – 0.4 | — | — | V | Note 2 |
| Output low voltage | V _{OL} | — | — | 0.4 | V | Note 2 |
| Output rise/fall time, VDDOx=1.8V, 4x drive strength | t _R , t _F | — | 0.4 | — | ns | 2 pF load, Note 3 |
| Output rise/fall time, VDDOx=1.8V, 4x drive strength | | — | 1.2 | — | ns | 15 pF load, Note 3 |
| Output rise/fall time, VDDOx=3.3V, 1x drive strength | | — | 0.7 | — | ns | 2 pF load, Note 3 |
| Output rise/fall time, VDDOx=3.3V, 1x drive strength | | — | 2.2 | — | ns | 15 pF load, Note 3 |
| Output duty cycle | — | 45 | 50 | 55 | % | — |
| Output current when output disabled | I _{OH} | — | 660 | — | μA | — |

Note 1: For VDDOx=1.5V, maximum CMOS output frequency is 160 MHz for a 10 pF load and 125 MHz for a 15 pF load.

2: For VDDOx=3.3V and 1x drive strength, I _O=3.5 mA. For VDDOx=1.8V and 4x drive strength, I _O=7 mA.

3: Measured 20% to 80%.

TABLE 9-10: ELECTRICAL CHARACTERISTICS: OTHER OUTPUTS AND I/O (BIDIRECTIONAL)

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|--|----------------------|------|------|-------------------------|-------|--|
| Bidirectional output high voltage for SO_IF1 and GPIO[4:0]_AC[4:0] pins | V _{OH-BIDI} | 2.4 | — | — | V | V _{DDIO} = 3.3V±5% I _{OH} = 18 mA |
| | | 1.7 | — | — | V | V _{DDIO} = 2.5V±5% I _{OH} = 13 mA |
| | | 1.35 | — | — | V | V _{DDIO} = 1.8V±5% I _{OH} = 4 mA |
| Bidirectional output low voltage for SO_IF1 and GPIO[4:0]_AC[4:0] pins | V _{OL-BIDI} | — | — | 0.4 | V | V _{DDIO} = 3.3V±5% I _{OL} = 12 mA |
| | | — | — | 0.7 | V | V _{DDIO} = 2.5V±5% I _{OL} = 14 mA |
| | | — | — | 0.45 | V | V _{DDIO} = 1.8V±5% I _{OL} = 6 mA |
| Bidirectional output low voltage for SI_SDA (I ² C mode) V _{DDIO} = 3.3V or V _{DDIO} = 2.5V | V _{OL1} | — | — | 0.4 | V | I _{OL} = 3 mA |
| Bidirectional output low voltage for SI_SDA (I ² C mode) V _{DDIO} = 1.8V | V _{OL2} | — | — | 0.2 x V _{DDIO} | V | I _{OL} = 2 mA |
| Bidirectional output low current for SI_SDA (I ² C mode) | I _{OL} | 3 | — | — | mA | V _{OL} = 0.4V |
| | | 5.1 | — | — | mA | V _{OL} = 0.6V |

TABLE 9-11: ELECTRICAL CHARACTERISTICS: OUTPUT-TO-OUTPUT TIMING

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes | |
|---|--------------|----------------------|------|------|-------|-----------|-----------------|
| Initial Skew | | | | | | Note 1, 4 | |
| Synthx OUTa to Synthx OUTb skew | Differential | t _{OO-S} | — | 40 | 100 | ps | Note 1, 3, 4, 7 |
| | CMOS | | — | 50 | 170 | ps | Note 1, 3, 4, 6 |
| Synthx OUTa to SynthY OUTb skew | Differential | t _{OO-S-S} | — | 50 | 105 | ps | Note 1, 3, 4, 7 |
| | CMOS | | — | 50 | 180 | ps | Note 1, 3, 4, 6 |
| Skew Variation | | | | | | Note 1, 5 | |
| SynthX OUTa to SynthX OUTb skew variation | Differential | t _{OOV-S} | — | 8 | 30 | ps | Note 1, 3, 5, 7 |
| | CMOS | | — | 13 | 60 | ps | Note 1, 3, 5, 6 |
| | Diff-CMOS | | — | 30 | 110 | ps | Note 1, 5, 6, 7 |
| SynthX OUTa to SynthY OUTb skew variation | Differential | t _{OOV-S-S} | — | 8 | 35 | ps | Note 1, 3, 5, 7 |
| | CMOS | | — | 13 | 60 | ps | Note 1, 3, 5, 6 |

- Note 1:** All specs in this table tested with 25 MHz output frequencies.
- 2:** Only applies for outputs that have the same load/termination.
- 3:** Only applies for outputs that have the same signal format, VDDO voltage, drive strength, and loading/termination. For 2xCMOS outputs, only measured for OUTxP.
- 4:** Initial delay and skew numbers indicate the timing relationships among the signals just after the device has been configured. Measurement is done at the same temperature and voltage used for configuration.
- 5:** Delay and skew variation numbers indicate how the timing relationships among the signals change as the already-configured device is exposed to all combinations of min., typ., and max. V_{DD} (all supplies varied at the same time) and min., room, and max. temperature without resetting or reconfiguring the device. The values shown are zero-to-peak numbers, i.e. half the peak-to-peak value of max. measurement minus min. measurement. Max. is largest zero-to-peak number over devices. Typ. is average zero-to-peak number over devices.
- 6:** Tested with output configured as 2xCMOS with 3x drive strength and VDDOx = 3.3V.
- 7:** Tested with output configured as programmable differential format with 1.2V V_{CM} and 800 mV V_{OD}.

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TABLE 9-12: ELECTRICAL CHARACTERISTICS: SPI INTERFACE TIMING

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|--|-------------|------|------|------|-------|-----------------------------|
| SCLK frequency | f_{SCLK} | — | — | 12.5 | MHz | See Figure 9-2 & Figure 9-3 |
| SCLK period | t_{cyc} | 80 | — | — | ns | |
| SCLK high time | t_{clkh} | 40 | — | — | ns | |
| SCLK low time | t_{clkl} | 40 | — | — | ns | |
| SI setup time to SCLK rising edge | t_{rxs} | 8 | — | — | ns | |
| SI hold time from SCLK rising edge | t_{rxh} | 8 | — | — | ns | |
| SO data valid time from SCLK falling edge | t_{xd} | — | — | 25 | ns | |
| CS_B rise to output high impedance | t_{ohz} | — | — | 60 | ns | See Figure 9-2 |
| CS_B setup to SCLK falling edge (LSB first) | t_{cssi} | 16 | — | — | ns | |
| CS_B hold from SCLK rising edge (LSB first) | t_{cshi} | 8 | — | — | ns | See Figure 9-3 |
| CS_B setup to SCLK rising edge (MSB first) | t_{cssm} | 16 | — | — | ns | |
| CS_B hold from SCLK falling edge (MSB first) | t_{cshsm} | 8 | — | — | ns | |

Note 1: Values are over Recommended Operating Conditions.

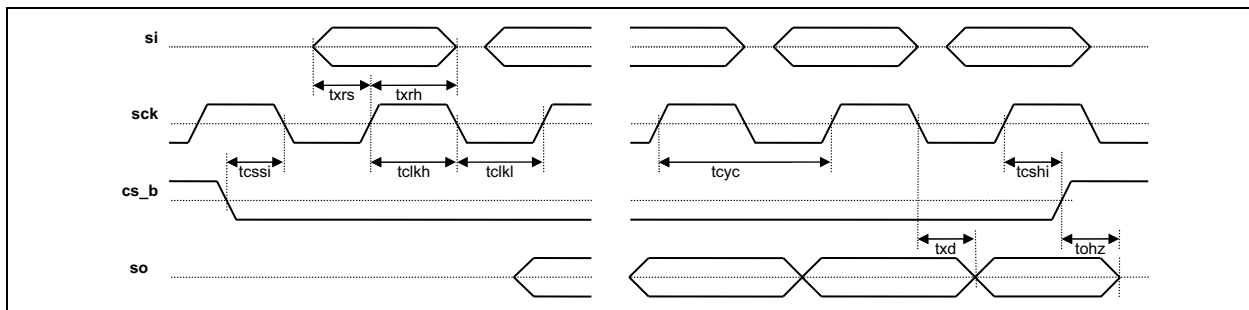


FIGURE 9-2: SPI Interface Timing, LSB First Mode.

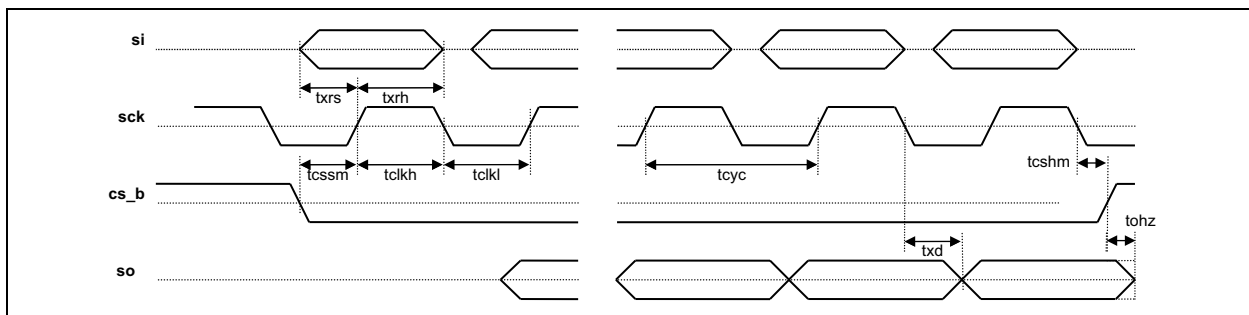


FIGURE 9-3: SPI Interface Timing, MSB First Mode.

TABLE 9-13: ELECTRICAL CHARACTERISTICS: I²C INTERFACE TIMING

VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Notes |
|---------------------------------------|---------------------|----------------------------------|------|------|-------|--------|
| SCL clock frequency | f _{SCL} | — | — | 400 | kHz | Note 1 |
| Hold time, START condition | t _{HD:STA} | 0.6 | — | — | µs | — |
| Low time, SCL | t _{LOW} | 1.3 | — | — | µs | — |
| High time, SCL | t _{HIGH} | 0.6 | — | — | µs | — |
| Setup time, START condition | t _{SU:STA} | 0.6 | — | — | µs | — |
| Data hold time | t _{HD:DAT} | 0 | — | — | µs | Note 2 |
| Data valid time | t _{VD:DAT} | — | — | 0.9 | µs | — |
| Data valid acknowledge time | t _{VD:ACK} | — | — | 0.9 | µs | — |
| Data setup time | t _{SU:DAT} | 100 | — | — | ns | — |
| Rise time, SCL and SDA | t _r | — | — | 300 | ns | — |
| Fall time, SCL and SDA input | t _f | 20 x (V _{DDIO} /5.5) | — | 300 | ns | — |
| Fall time, SDA output | t _{of} | 20 x (V _{DDIO} /5.5) | — | 250 | ns | — |
| Setup time, STOP condition | t _{SU:STO} | 0.6 | — | — | µs | — |
| Bus free time between STOP/START | t _{BUF} | 1.3 | — | — | µs | — |
| Spike suppression, SCL and SDA inputs | t _{SP} | 0 | — | 50 | ns | — |
| Pin capacitance, SCL and SDA | C _p | — | — | 10 | pF | — |
| Bus capacitance, SCL and SDA | C _b | — | — | 400 | pF | — |

- Note 1:** Characteristics in this table apply to Fast-mode with f_{SCL} ≤ 400 kHz. The device may be used in a Standard-mode system with f_{SCL} ≤ 100 kHz and t_r ≤ 1000 ns. The device does not stretch SCL. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 9-5).
- 2:** The device internally provides an output hold time of at least 300 ns for SDA (with respect to the V_{IHmin} of the SCL) to bridge the undefined region (V_{IHmin} to V_{ILmax}) of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.

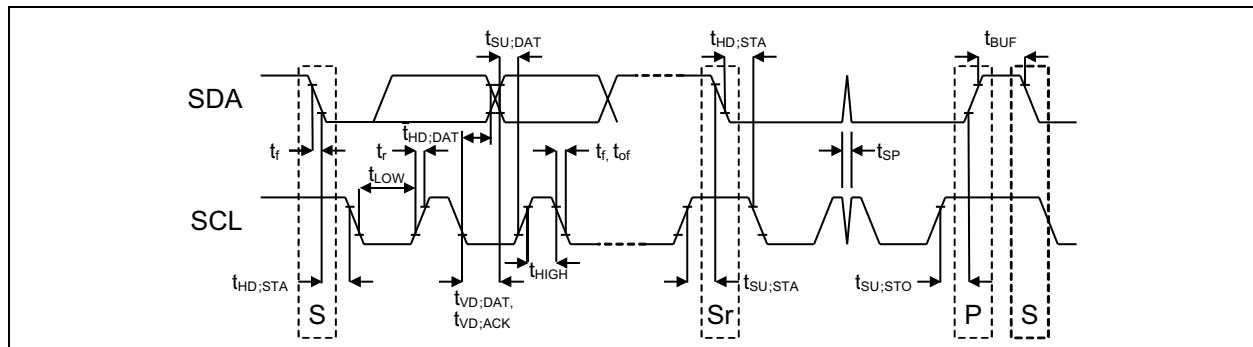


FIGURE 9-4: I²C Interface Timing.

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10.0 PERFORMANCE CHARACTERISTICS

TABLE 10-1: OUTPUT CLOCK JITTER GENERATION – OUTXP/N DIFFERENTIAL

| Characteristics | Test Conditions | Min. | Typ. | Max. | Units |
|--|--|------|------|------|-------------------|
| Phase Jitter, 156.25 MHz (114.285 MHz XO) | 10 kHz to 1 MHz, Note 1 , Note 2 | — | 75 | 120 | fs _{RMS} |
| | 12 kHz to 20 MHz, Note 1 , Note 2 | — | 102 | 145 | fs _{RMS} |
| Phase Jitter, 156.25 MHz (49.152 MHz crystal doubled) | 10 kHz to 1 MHz, Note 1 , Note 4 | — | 68 | — | fs _{RMS} |
| | 12 kHz to 20 MHz, Note 1 , Note 4 | — | 101 | — | fs _{RMS} |
| Phase Jitter, 156.25 MHz (49.152 MHz crystal not doubled) | 10 kHz to 1 MHz, Note 1 , Note 4 | — | 89 | — | fs _{RMS} |
| | 12 kHz to 20 MHz, Note 1 , Note 4 | — | 119 | — | fs _{RMS} |
| Phase Jitter, 156.25 MHz (49.152 MHz XO) | 10 kHz to 1 MHz, Note 1 , Note 3 | — | 99 | — | fs _{RMS} |
| | 12 kHz to 20 MHz, Note 1 , Note 3 | — | 128 | — | fs _{RMS} |
| Period Jitter, 100 MHz | Note 1 , Note 2 , Note 5 | — | 10 | — | ps _{pp} |
| Phase Jitter, 312.5 MHz (114.285 MHz XO) | 12 kHz to 20 MHz, Note 1 , Note 2 | — | 87 | — | fs _{RMS} |
| Phase Jitter, 625 MHz (114.285 MHz XO) | 12 kHz to 20 MHz, Note 1 , Note 6 | — | 82 | — | fs _{RMS} |
| Cycle-to-Cycle Jitter, 100 MHz | Note 1 , Note 2 , Note 5 | — | 10 | — | ps |

- Note 1:** Tested with VDDOx = 3.3V and programmable differential mode with V_{OD} = 800 mV and V_{CM} = 1.2V.
- 2:** With Vectron VCC1-9004-114M285 XO connected to OSCB pin and +2 ppm frequency offset for the output signal w.r.t. the XO. APLL dividers set for 53x2=106 and [xo_config::passclk=1](#), synth frequency 312.5 MHz.
- 3:** With Vectron VCC1-1545-49M152 XO connected to OSCB pin and +2 ppm frequency offset for the output signal w.r.t. the XO. APLL dividers set for 27x9=243 and [xo_config::passclk=1](#), synth frequency 312.5 MHz.
- 4:** With Vectron VXM7-1361-49M1520000 crystal connected to OSCI/OSCO pins and +2 ppm frequency offset for the output signal w.r.t. the crystal. For crystal doubled case, APLL dividers set for 41x3=123. For the not-doubled case, [xo_config::passclk=1](#), synth frequency 312.5 MHz.
- 5:** N=10000. Measured using Tektronix MSO71604C, Mixed Signal Oscilloscope with DPOJET software.
- 6:** With Vectron VCC1-9004-114M285 XO connected to OSCB pin and +2 ppm frequency offset for the output signal w.r.t. the XO. APLL dividers set for 53x2=106 and [xo_config::passclk=1](#), synth frequency 625 MHz.

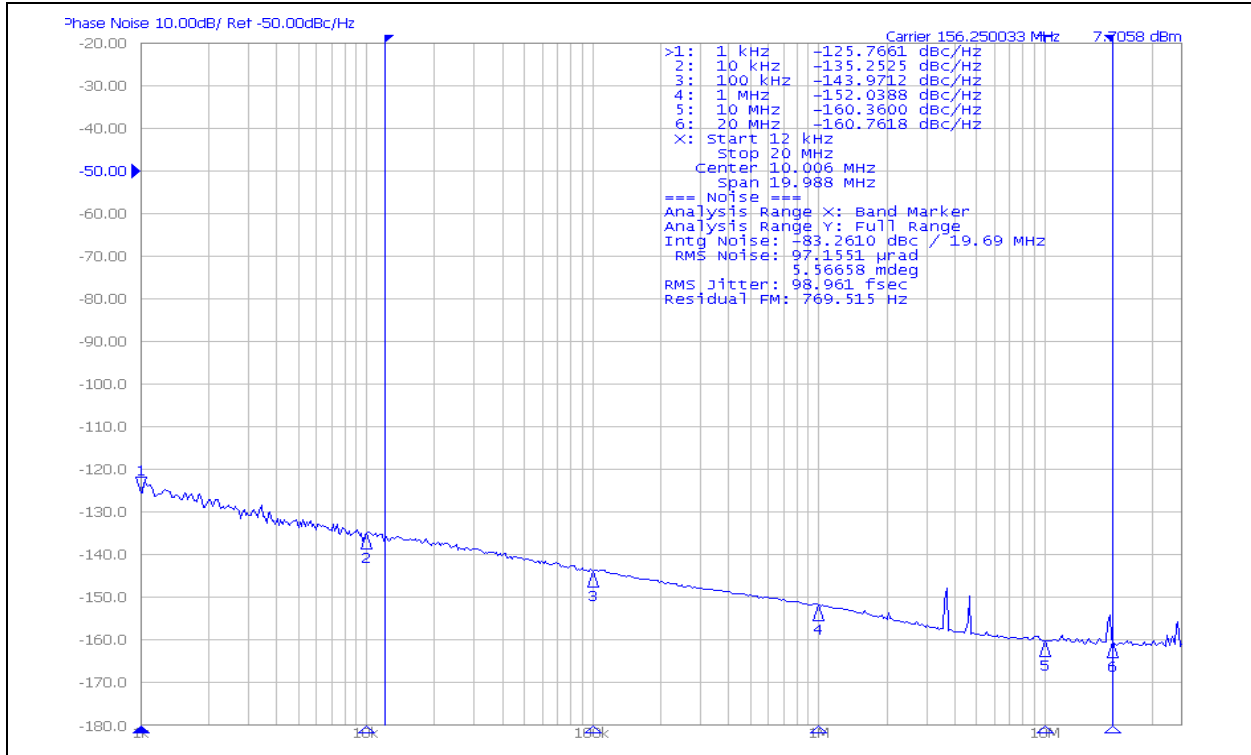


FIGURE 10-1: Typical Phase Noise, 156.25 MHz.

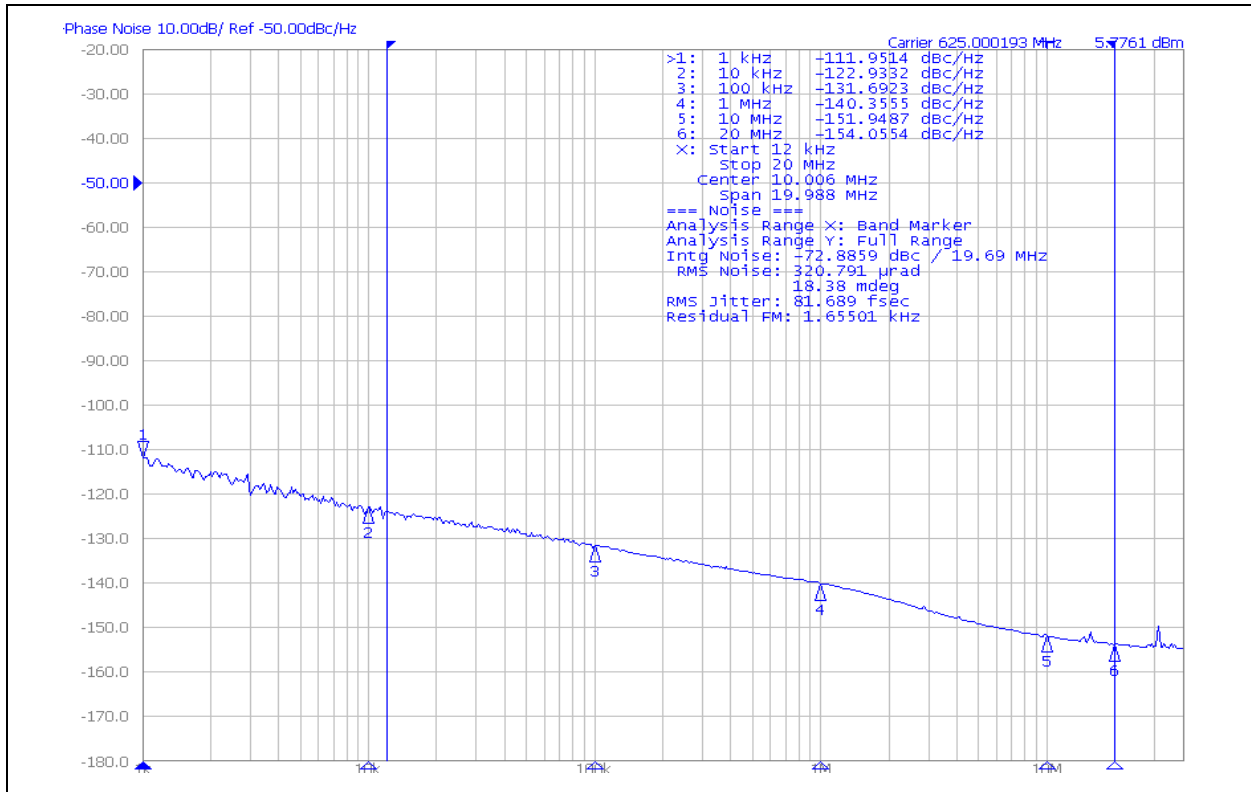


FIGURE 10-2: Typical Phase Noise, 625 MHz.

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11.0 PACKAGE AND THERMAL INFORMATION

The device is fully functional at junction temperatures from T_{JMIN} to T_{JMAX} , but long-term exposure to junction temperatures above 110°C may eventually affect device performance.

TABLE 11-1: 9X9 VQFN PACKAGE THERMAL PROPERTIES

| Parameter | Symbol | Conditions | Value | Units |
|---|---------------|-----------------|-------|-------|
| Maximum Ambient Temperature | T_A | — | +85 | °C |
| Minimum Junction Temperature | T_{JMIN} | — | -40 | °C |
| Maximum Junction Temperature | T_{JMAX} | — | +125 | °C |
| Junction to Ambient Thermal Resistance (Note 1) | θ_{JA} | still air | 16.8 | °C/W |
| | | 1 m/s airflow | 13.6 | |
| | | 2.5 m/s airflow | 11.8 | |
| Junction to Board Thermal Resistance | θ_{JB} | — | 4.5 | °C/W |
| Junction to Case Thermal Resistance | θ_{JC} | — | 8.3 | °C/W |
| Junction to Pad Thermal Resistance (Note 2) | θ_{JP} | — | 1.1 | °C/W |
| Junction to Top-Center Thermal Characterization Parameter | Ψ_{JT} | — | 0.1 | °C/W |

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 8-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

TABLE 11-2: 7X7 VQFN PACKAGE THERMAL PROPERTIES

| Parameter | Symbol | Conditions | Value | Units |
|---|---------------|-----------------|-------|-------|
| Maximum Ambient Temperature | T_A | — | +85 | °C |
| Minimum Junction Temperature | T_{JMIN} | — | -40 | °C |
| Maximum Junction Temperature | T_{JMAX} | — | +125 | °C |
| Junction to Ambient Thermal Resistance (Note 1) | θ_{JA} | still air | 16.8 | °C/W |
| | | 1 m/s airflow | 13.5 | |
| | | 2.5 m/s airflow | 11.7 | |
| Junction to Board Thermal Resistance | θ_{JB} | — | 5.5 | °C/W |
| Junction to Case Thermal Resistance | θ_{JC} | — | 9.3 | °C/W |
| Junction to Pad Thermal Resistance (Note 2) | θ_{JP} | — | 1.1 | °C/W |
| Junction to Top-Center Thermal Characterization Parameter | Ψ_{JT} | — | 0.1 | °C/W |

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 8-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

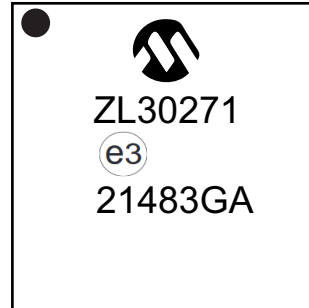
12.0 PACKAGE OUTLINE

12.1 Package Marking Information

64-Lead VQFN



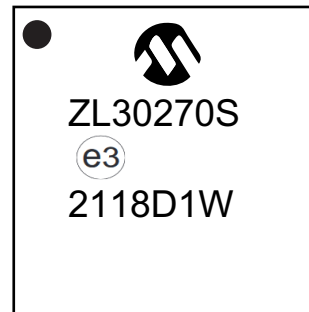
Example



48-Lead VQFN



Example



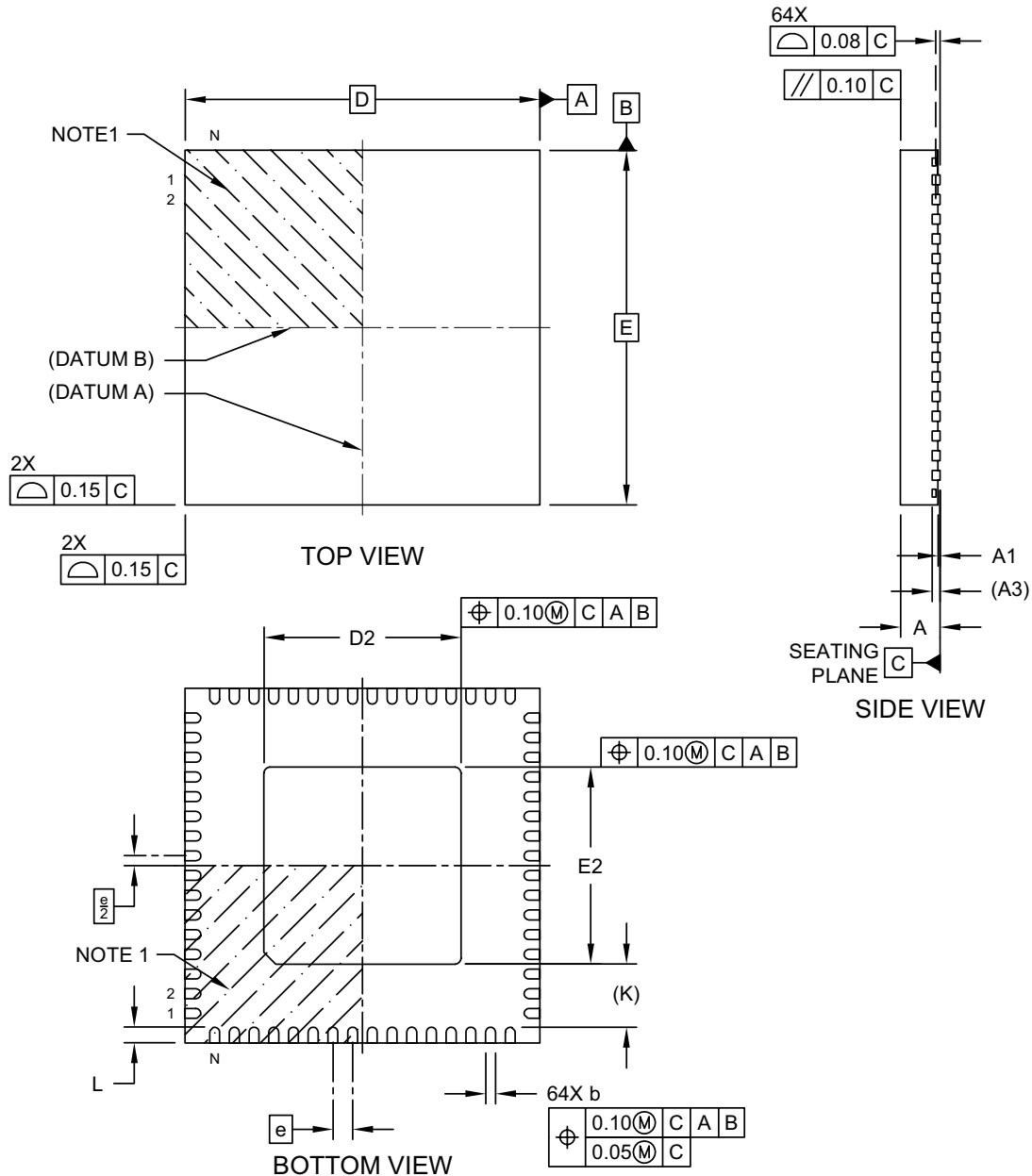
| | |
|--|---|
| <p>Legend:</p> <p>XX...X Product code or customer-specific information</p> <p>Y Year code (last digit of calendar year)</p> <p>YY Year code (last 2 digits of calendar year)</p> <p>WW Week code (week of January 1 is week '01')</p> <p>NNN Alphanumeric traceability code</p> <p>(e3) Pb-free JEDEC[®] designator for Matte Tin (Sn)</p> <p>* This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.</p> <p>•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).</p> | <p>Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.</p> <p>Underbar (_) and/or Overbar (¯) symbol may not be to scale.</p> |
|--|---|

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64-Lead 9 mm x 9 mm VQFN Package Outline and Recommended Land Pattern

64-Lead Very Thin Plastic Quad Flat, No Lead Package (MGC) - 9x9x1 mm Body [VQFN] With 5.0 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

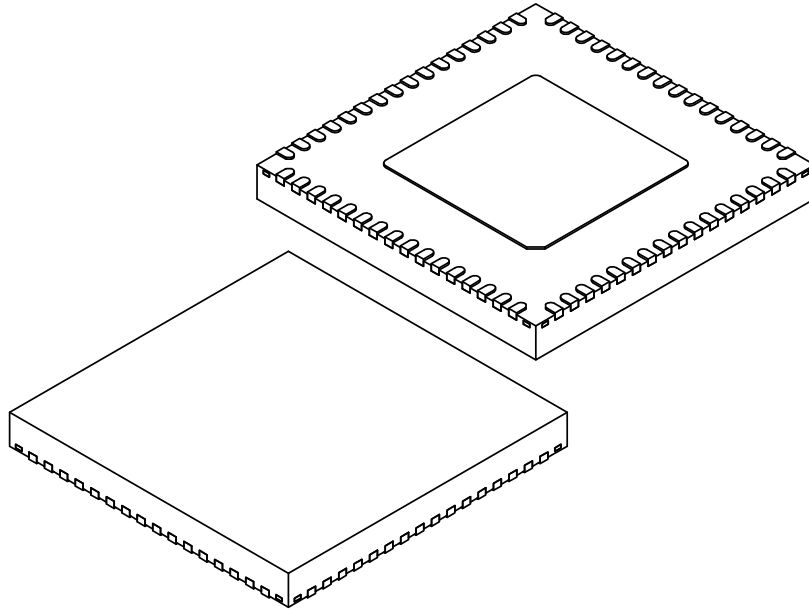


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64-Lead Very Thin Plastic Quad Flat, No Lead Package (MGC) - 9x9x1 mm Body [VQFN] With 5.0 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Terminals | N | 64 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 9.00 BSC | | |
| Exposed Pad Length | D2 | 4.90 | 5.00 | 5.10 |
| Overall Width | E | 9.00 BSC | | |
| Exposed Pad Width | E2 | 4.90 | 5.00 | 5.10 |
| Terminal Width | b | 0.18 | 0.25 | 0.30 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 1.61 REF | | |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

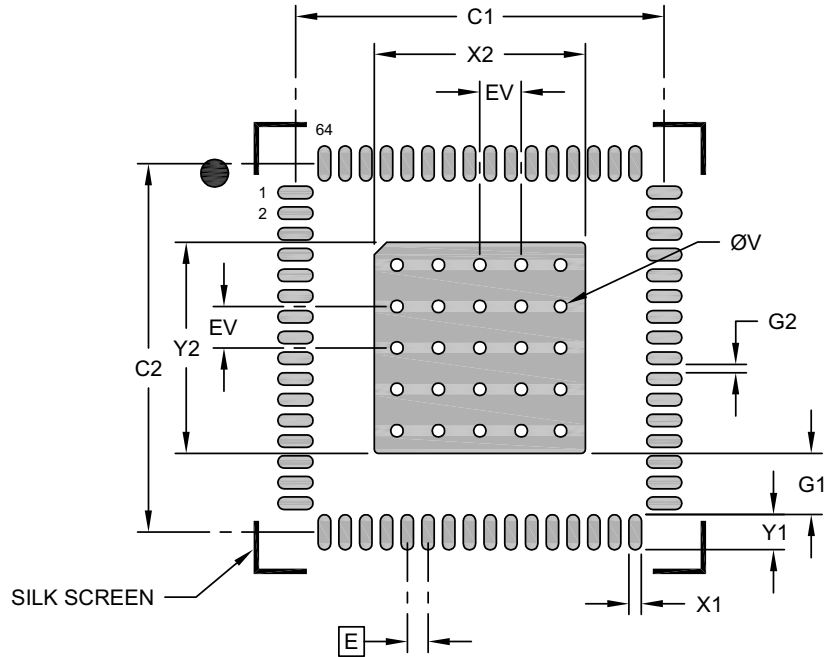
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64-Lead Very Thin Plastic Quad Flat, No Lead Package (MGC) - 9x9x1 mm Body [VQFN] With 5.0 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | X2 | | | 5.10 |
| Optional Center Pad Length | Y2 | | | 5.10 |
| Contact Pad Spacing | C1 | | 8.90 | |
| Contact Pad Spacing | C2 | | 8.90 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X64) | G1 | 1.48 | | |
| Contact Pad to Contact Pad (X60) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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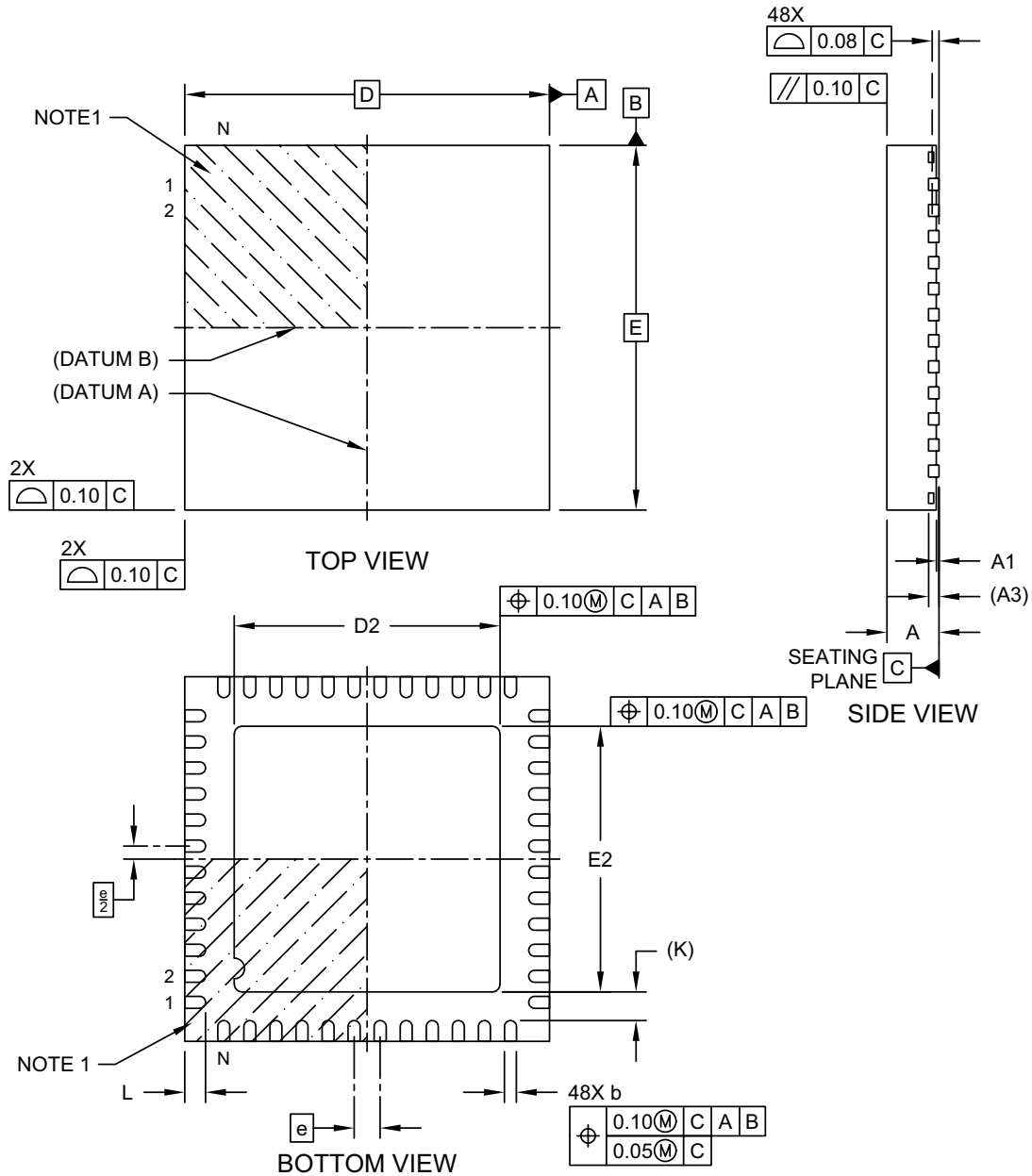
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ZL30270 - ZL30271

48-Lead 7 mm x 7 mm VQFN Package Outline and Recommended Land Pattern

48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

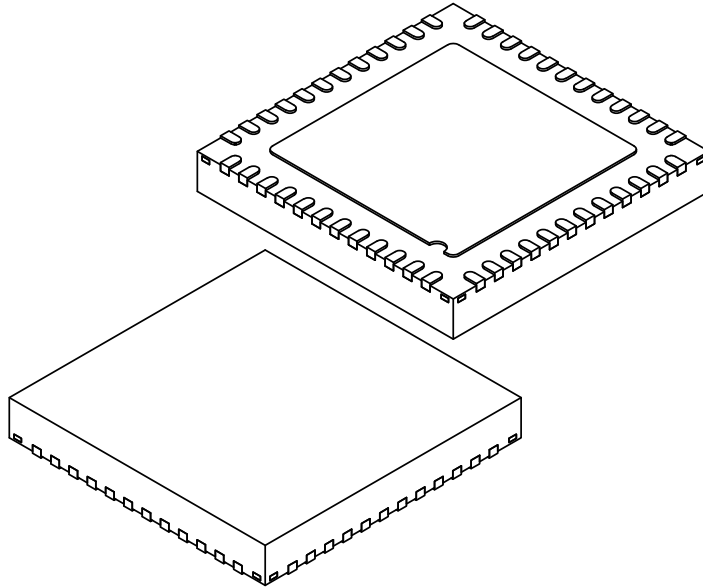


Microchip Technology Drawing C04-25407 Rev B Sheet 1 of 2

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48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | MILLIMETERS | | |
|-------------------------|----|-------|-------------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Terminals | N | | 48 | | |
| Pitch | e | | 0.50 BSC | | |
| Overall Height | A | | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | | |
| Overall Length | D | | 7.00 BSC | | |
| Exposed Pad Length | D2 | | 5.00 | 5.10 | 5.20 |
| Overall Width | E | | 7.00 BSC | | |
| Exposed Pad Width | E2 | | 5.00 | 5.10 | 5.20 |
| Terminal Width | b | | 0.16 | 0.23 | 0.30 |
| Terminal Length | L | | 0.35 | 0.40 | 0.45 |
| Terminal-to-Exposed-Pad | K | | 0.55 REF | | |

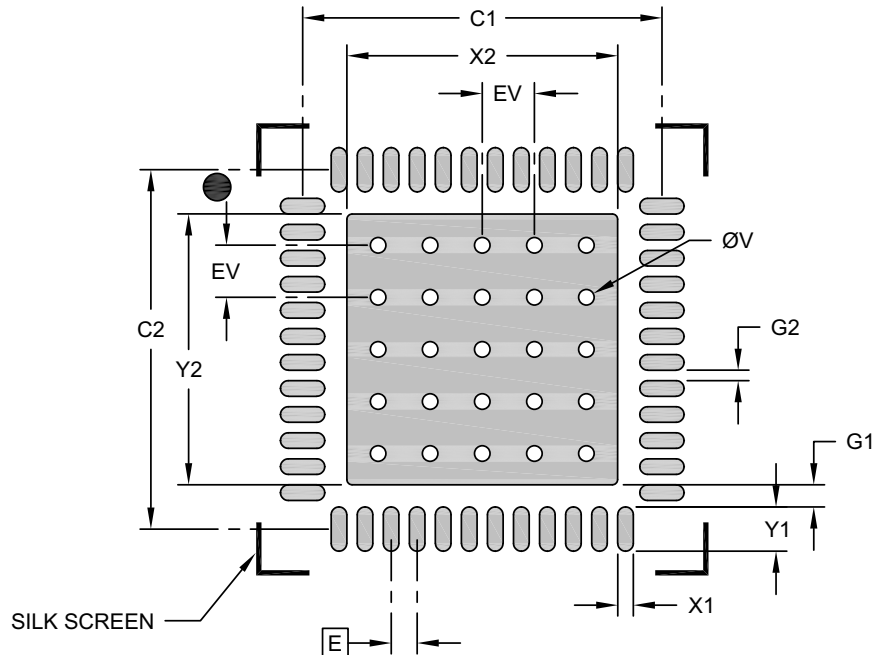
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25407 Rev B Sheet 2 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|----------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Optional Center Pad Width | X2 | | | 5.20 |
| Optional Center Pad Length | Y2 | | | 5.20 |
| Contact Pad Spacing | C1 | | 6.90 | |
| Contact Pad Spacing | C2 | | 6.90 | |
| Contact Pad Width (Xnn) | X1 | | | 0.30 |
| Contact Pad Length (Xnn) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (Xnn) | G1 | 0.43 | | |
| Contact Pad to Contact Pad (Xnn) | G2 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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13.0 ACRONYMS AND ABBREVIATIONS

| | |
|---------------------------------------|--|
| APLL | analog phase locked loop |
| CML | current mode logic |
| GbE | gigabit Ethernet |
| HCSL | high-speed current steering logic |
| I/O | input/output |
| LOS | loss of signal |
| LVDS | low-voltage differential signal |
| LVPECL | low-voltage positive emitter-coupled logic |
| PFD | phase/frequency detector |
| pk-pk | peak-to-peak |
| PLL | phase locked loop |
| ppb | parts per billion |
| ppm | parts per million |
| RMS | root-mean-square |
| RO | read-only |
| R/W | read/write |
| SS or SSM | spread spectrum modulation |
| TCXO | temperature-compensated crystal oscillator |
| UI | unit interval |
| UI _{PP} or UI _{P-P} | unit interval, peak-to-peak |
| XO | crystal oscillator |

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

| Revision | Section/Figure/Entry | Correction |
|------------------------|--|--|
| DS20006639A (12-07-21) | — | Converted Microsemi data sheet ZL30271 to Microchip DS20006639A. Minor text changes throughout. |
| DS20006639B (02-28-22) | — | Documented ZL30270 |
| | Figure 3-2 | Added pin diagram for 48-lead 7 mm x 7 mm package. |
| | Table 4-1 | Add pin numbers for 7 mm x 7 mm package. |
| | Table 11-2 | Added 7 mm x 7 mm package thermal specs. |
| | Section 12.0 | Added package outline and recommended land pattern for 48-lead 7 mm x 7 mm VQFN package. |
| DS20006639C (05-10-22) | Product Identification System | Added S=48-Lead 7 mm x 7 mm package. |
| | xo_amp_sel | Corrected the xtal_drive_level description to what it should be. Previously it was accidentally the same text as the xo_osci_sel description. |
| | Table 4-1 | In the GPIO description added new recommendation. |
| | Figure 5-1 | Added a footnote to part e). |
| | Section 5.1.4, synth_spread_spectrum_cfg, synth_spread_spectrum_rate, synth_spread_spectrum_spread | Documented these registers. |
| | Figure 9-1 | Corrected VOC to VOUT in several places. |
| DS20006639C (05-10-22) | Section 5.2.1 | Correct last paragraph about voltages allowed for LVDS and LVPECL. |
| | output_ctrl_0 | In the stop_high bit description, clarified the 0 decode is stop low and the 1 decode is stop high. Also corrected rising edge to falling edge in the 0 decode. |
| DS20006639D (11-04-22) | Table 4-1 | Added content in OUT and VDDO6 rows to say that in 7x7 package devices OUT6 is powered from VDDO8 along with OUT8. Added recommendation to the output clock pin description. |
| | output_phase_compensation | Added note. |
| | synth_phase_compensation | Added note. |

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| Device | X | X | X | X | X |
|--|-------------------|----------|------------|----------|----------|
| Part Number | Chip Carrier Type | Package | Media Type | Finish | Size |
| <p>Device: ZL30270: 6-Output 5-Synthesizer Clock Generator ZL30271: 10-Output 5-Synthesizer Clock Generator</p> <p>Chip Carrier Type: L = Leadless Chip Carrier</p> <p>Package: D = VQFN</p> <p>Media Type: G = 260/Tray</p> <p>Finish: 1 = Pb-Free, Matte Tin (Sn) Finish</p> <p>Size: <blank> = 64-Lead 9 mm x 9 mm S = 48-Lead 7 mm x 7 mm</p> | | | | | |
| <p>Examples:</p> <p>a) ZL30271LDG1: 10-Output 5-Synthesizer Clock Generator, Leadless Chip Carrier, VQFN, 260/Tray, Pb-Free Matte Tin (Sn) Finish, 64-Lead 9 mm x 9 mm</p> <p>Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p> | | | | | |

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