ZL30272 - ZL30274

1- and 2-Channel Jitter Attenuators with up to 20 Outputs

Features

Highlights

- One (ZL30272, ZL30273) or two (ZL30274) independent clock channels
- Any-to-any frequency conversion per channel
- Inputs: up to 8, differential or single-ended
- Outputs: up to 10 differential, up to 20 CMOS (ZL30272: up to 6 differential, up to 12 CMOS)
- Output jitter 100 fs_{RMS} typical for 156.25 MHz 12 kHz to 20 MHz
- Core power consumption <0.9W

Input Clocks

- Accepts up to 6 (ZL30272, ZL30273) or 8 (ZL30274) differential or CMOS inputs
- Any input frequency from 1 kHz to 1250 MHz
- Per-input activity and frequency monitoring
- Automatic or manual reference switching
- Revertive or nonrevertive switching
- Any input can be a 0.5 Hz to 8 kHz Sync input for Ref-Sync frequency/phase/time locking
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution

DPLLs

- One (ZL30272-273) or two (ZL30274) DPLLs
- Hitless reference switching
- Per-DPLL phase adjustment, 1 ps resolution
- Programmable bandwidth, tracking range, phase-slope limiting, and other advanced features
- Locking to gapped-clock input signals

Output Clocks

- Any frequency 0.5 Hz to 750 MHz
- Each OUTP/N pair can be LVDS, LVPECL, 2xCMOS, Low-V_{CM}, or programmable differential
- In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125 MHz and 25 MHz)
- VDD per output pair, CMOS voltages 1.8V to 3.3V
- Per-synth phase adjustment, 1 ps resolution
- Per-output duty cycle adjustment
- Precise output alignment circuitry and per-output phase adjustment
- Per-output enable/disable and glitchless start/stop (stop high or low)

Local Oscillator

- Operates from a single oscillator 9.72 MHz to 400 MHz

General Features

- Automatic self-configuration at power-up from internal Flash memory, 7 configurations
- Input-to-output alignment <100 ps
- Numerically controlled oscillator behavior in each DPLL and each synthesizer
- Easy-to-configure design requires no external VCXO or loop filter components
- 5 GPIO pins with many possible behaviors, each REF can be GPI, each OUT can be GPO
- SPI or I^2C processor Interface
- 1.8V and 3.3V core VDD voltages
- 48-Lead 7 mm x 7 mm VQFN Package (ZL30272)
- 64-Lead 9 mm x 9 mm VQFN Package (ZL30273, ZL30274)
- Easy-to-use evaluation/programming software

Applications

- Frequency conversion, jitter attenuation and frequency synthesis in a wide variety of equipment types

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1.0 BLOCK DIAGRAM

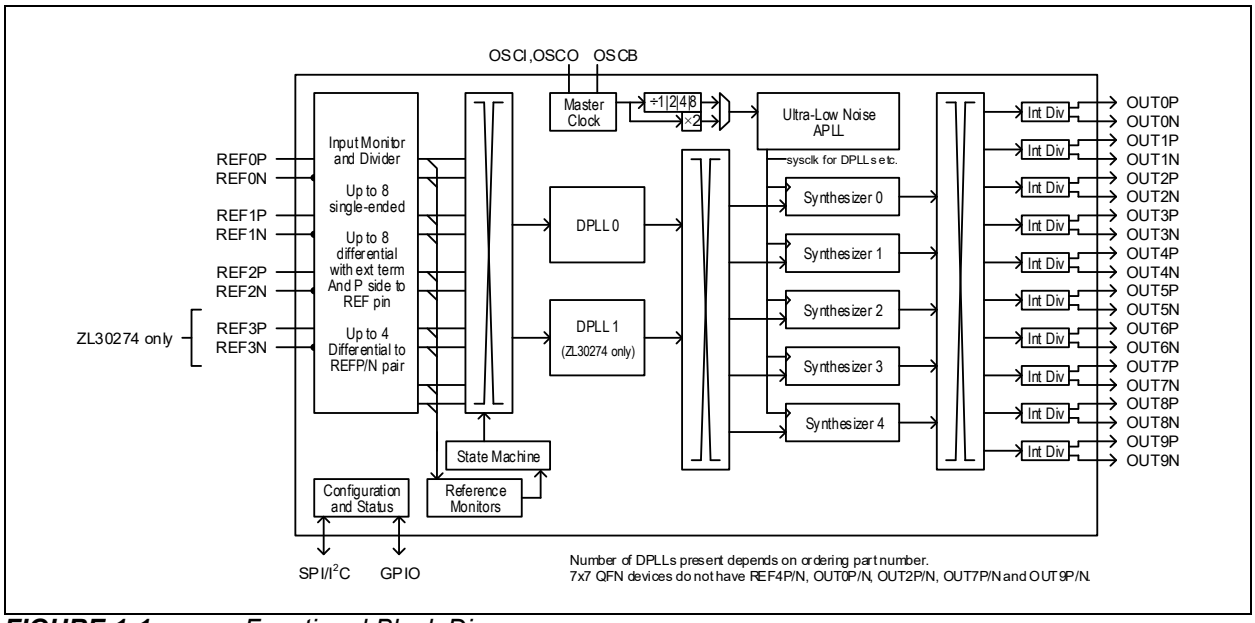


FIGURE 1-1: *Functional Block Diagram.*

2.0 DETAILED FEATURES

2.1 General

- One (ZL30272, ZL30273) or two (ZL30274) independent clock channels
- Operates from a single crystal resonator or clock oscillator
  - ≥48 MHz for lowest jitter
  - 9.72 MHz to 400 MHz total frequency range
- Configurable via SPI or I^2C interface
- Internal nonvolatile memory
  - Factory-configurable power-on configuration
  - Multiple time writeable/re-writeable
- Default settings can be overridden using SPI/I^2C

2.2 Input Block Features

- 6 (ZL30272, ZL30273) or 8 (ZL30274) input reference pins; each can accept a CMOS signal or the POS side of a differential pair; or two can be paired to accept both sides of a differential pair (see Figure 5-3)
- Any input can be a SYNC signal (0.5 Hz to 8 kHz) for Ref-Sync frequency/phase/time locking
- Input clocks can be any frequency from 0.5 Hz up to 1250 MHz for regular two-pin differential mode, 400 MHz for single-pin differential mode, or 300 MHz for CMOS
- Inputs constantly monitored by programmable frequency and single-cycle monitors
- Single-cycle monitor can quickly disqualify a reference when measured period is incorrect
- Frequency measurement and monitoring (coarse, fine, and frequency-step monitors)
- Optional input clock invalidation on GPIO or GPI assertion to react to LOS signals from PHYs
- Input phase measurement, 1 ps resolution
- Per-input phase adjustment, 1 ps resolution
- Each REF pin can be a GPI (general-purpose input)

2.3 DPLL Features

- One (ZL30272, ZL30273) or two (ZL30274) DPLLs
- State machine automatically transitions among freerun, tracking, and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 14 Hz to 403 Hz
- Programmable phase-slope limiting (PSL)
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching
- Per-DPLL phase adjustment, 1 ps resolution
- High-resolution frequency and phase measurement (4e-15 and 1 ps)
- Fast detection of input clock failure and transition to holdover mode

2.4 Synthesizer Features

- Five next-generation low-jitter, low-power, any-frequency synthesizers
- A total of five output frequency families
- Any-to-any frequency conversion with 0 ppm error
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Jitter suitable for OC-192, STM-64, and 1G, 10G, 40G, 100G, and 400G Ethernet jitter requirements

2.5 Output Clock Features

- Up to 20 single-ended outputs, up to 10 differential outputs, from any synthesizer (ZL30272: up to 12 single-ended, up to 6 differential)
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 0.5 Hz to 750 MHz (250 MHz max for CMOS)
- Output jitter 100 fs_{RMS} typical for 156.25 MHz and many other frequencies (12 kHz to 20 MHz)
- In CMOS mode, the OUTxN frequency can be an integer divisor of the OUTxP frequency (Example 1: OUT3P 125 MHz, OUT3N 25 MHz. Example 2: OUT2P 25 MHz, OUT2N 1 Hz)
- Outputs directly interface (DC-coupled) with LVDS, LVPECL, HCSL, and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs, and other components
- Can produce PCIe Gen 1 to 5 clocks
- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1 ps resolution
- Per-output phase adjustment to accommodate trace delays or compensate for system routing paths
- Per-output duty cycle/pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)
- Each OUT pin can be a GPO (general-purpose output)

2.6 Local Oscillator

- Operates from a single oscillator (jitter reference for the device). Acceptable frequencies: 9.72 MHz to 400 MHz. Best jitter: ≥48 MHz.

2.7 General Features

- Automatic self-configuration at power-up from internal Flash memory
- Input-to-output alignment <200 ps with external feedback
- Generates output SYNC signals: 1PPS (IEEE 1588), 2 kHz or 8 kHz (SONET/SDH), or other frequency
- JESD204B clocking: clock and SYSREF signal generation with skew adjustment
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency or synthesizer frequency with resolution better than 0.005 ppt

- Spread-spectrum modulation available in each synthesizer (PCIe compliant)
- Five general-purpose I/O pins each with many possible status and control options
- SPI or I^2C serial microprocessor interface

2.8 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts
- Works with or without an evaluation board

3.0 PIN DIAGRAMS

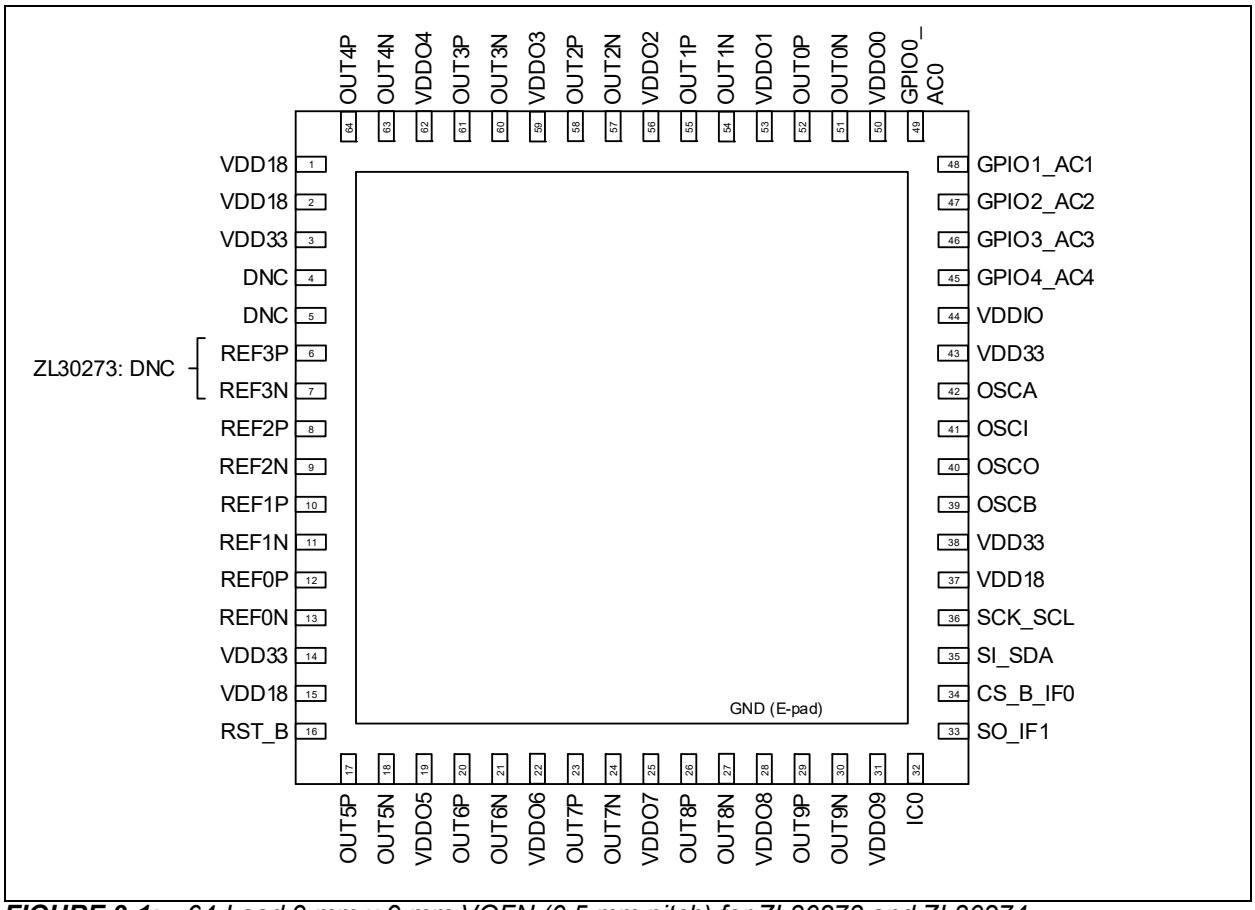


FIGURE 3-1: *64-Lead 9 mm x 9 mm VQFN (0.5 mm pitch) for ZL30273 and ZL30274.*

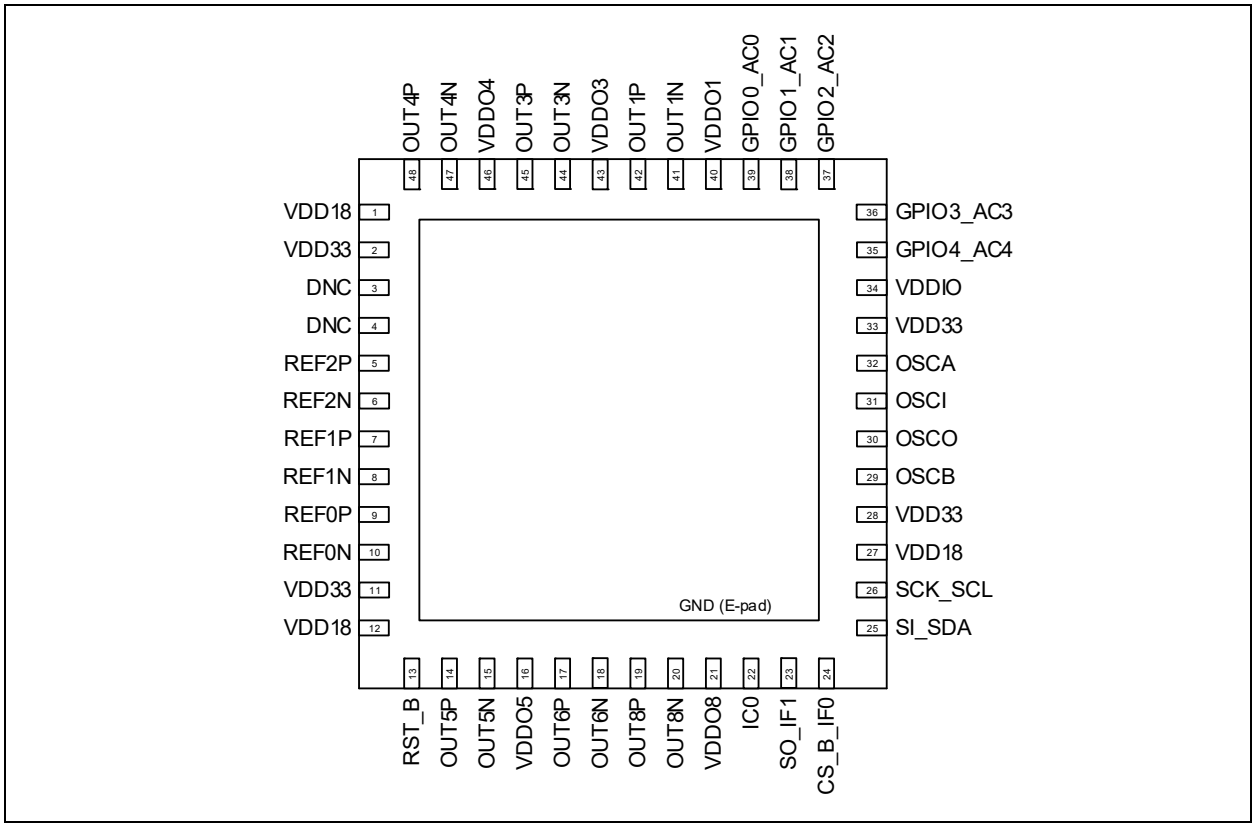


FIGURE 3-2: *48-Lead 7 mm x 7 mm VQFN (0.5 mm pitch) for ZL30272.*

4.0 PIN DESCRIPTIONS

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, I_{PU} – input with internal pull-up resistor, I_{OPD} – input/output with internal pull-down resistor, O – output, A – analog, P – power supply pin. All GPIO and SPI/I^2C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

TABLE 4-1: PIN DESCRIPTIONS

7x7 Pin Number	9x9 Pin Number	Pin Name	Type	Description
Input References				
9	12	REF0P	I	**Input References (CMOS, LVDS, LVPECL, CML, HCSL)** Each REFxP/REFxN pair can accept a differential signal or up to two single-ended signals. Single-ended signals can be CMOS or one side of a differential signal, as shown in Figure 5-3c (this is called single-pin differential mode). Recommended termination circuitry for all of these options is shown in Figure 5-3. See Table 9-5 for electrical specifications. Input frequency range for LVPECL, LVDS, HCSL, CML is from 0.5 Hz to 1250 MHz for regular two-pin differential mode and 400MHz for single-pin differential mode. Unused REF inputs should have ref_config.enable=0 and be left floating. On ZL30273 pins 6 and 7 are DNC (do not connect) instead of REF3P, REF3N.
10	13	REF0N		
7	10	REF1P		
8	11	REF1N		
5	8	REF2P		
6	9	REF2N		
3	6	REF3P		
4	7	REF3N		
Output Clocks				
—	52	OUT0P	O	**Outputs Clocks** LVDS, LVPECL, programmable differential, Low-V_{CM} differential (HCSL-like) or 1 or 2 CMOS. Programmable frequency and drive strength. Programmable common-mode voltage and signal amplitude in programmable differential mode. See Figure 5-7 for example external interface circuitry. See Table 9-7, Table 9-8, and Table 9-9 for electrical specifications for LVDS, LVPECL, and Low-V_{CM} signal format, respectively. See Table 9-10 for electrical specifications for interfacing to CMOS inputs on neighboring devices. Microchip does not recommend using an output clock from this device as a system clock for the processor that controls this device. In some scenarios output clocks are not available from the device, such as during device reset after firmware upgrade. For the 7 mm x 7 mm VQFN package only: OUT6P/N and OUT8P/N share power supply pin VDDO8 which makes crosstalk worse between these outputs when they are different frequencies. When OUT6 and OUT8 must be low jitter Microchip recommends they follow the same synthesizer and are the same frequency or the frequency of one is an integer divide of the other.
—	51	OUT0N		
42	55	OUT1P		
41	54	OUT1N		
—	58	OUT2P		
—	57	OUT2N		
45	61	OUT3P		
44	60	OUT3N		
48	64	OUT4P		
47	63	OUT4N		
14	17	OUT5P		
15	18	OUT5N		
17	20	OUT6P		
18	21	OUT6N		
—	23	OUT7P		
—	24	OUT7N		
19	26	OUT8P		
20	27	OUT8N		
—	29	OUT9P		
—	30	OUT9N		

TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

7x7 Pin Number	9x9 Pin Number	Pin Name	Type	Description
Control and Status				
13	16	RST_B	I_{PU}	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up by driving the RST_B pin low. The RST_B pin should be held low for at least 2 ms. This pin has an internal 85 kΩ pull-up to VDD33 (not VDDIO). Device registers can be accessed either 500 ms after RST_B goes high or after bit 7 in register at address 0x00 goes high. Note that the supply rail for RST_B is VDD33 not VDDIO. When the host interface is I^2C, Microchip recommends RST_B be wired to a general-purpose output pin on an FPGA, microcontroller or other software-controlled component.
39	49	GPIO0_AC0	IO_{PD}	**General Purpose I/O / Auto-Configuration** General-Purpose I/O: These are general-purpose pins with many possible uses, including: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • Interrupt Output: indicates changes of device status prompting system software to read the interrupt service registers (ISR). These pins have internal pull-down resistors (80 kΩ typical). Each pull-down can be disabled by a register field. If not used, GPIO can be left unconnected. Auto-Configuration: On the rising edge of RST_B GPIO3_AC3 and GPIO4_AC4 must be 0 for normal operation, and GPIO0_AC0 to GPIO2_AC2 behave as auto-configuration pins to specify a custom configuration stored in internal Flash. 000 = configuration 0 001 = configuration 1 010 = configuration 2 011 = configuration 3 100 = configuration 4 101 = configuration 5 110 = configuration 6 111 = factory default state (no configuration) If the specified configuration is empty in internal flash then the device powers up in factory default state. Legacy recommendation: When the host interface is I^2C, Microchip recommends GPIO3 be wired to a 1 kΩ resistor to ground and to a general-purpose output pin on an FPGA, microcontroller or other software-controlled component. Latest recommendation: Regardless of host interface type, Microchip recommends all five GPIO pins be wired to GPIO pins on an FPGA, microcontroller or other software-controlled component.
38	48	GPIO1_AC1		
37	47	GPIO2_AC2		
36	46	GPIO3_AC3		
35	45	GPIO4_AC4		

TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

7x7 Pin Number	9x9 Pin Number	Pin Name	Type	Description
Host Interface (SPI or I^2C)				
26	36	SCK_SCL	I/O	**SPI Clock/I^2C Clock** *SPI Clock:* An external SPI controller must provide the SPI clock signal on SCK. *I^2C Clock:* An external I^2C controller must provide the I^2C clock signal on the SCL pin. This pin should be externally pulled high by 1 kΩ to 5 kΩ resistor. See the I^2C bus specification for sizing guidance for this resistor, referred to as RP in that specification. This pin has an internal pull-up (typical 85 kΩ) to VDDIO.
25	35	SI_SDA	I/O	**SPI Data In/I^2C Data** *SPI Data In:* An external SPI controller sends commands, addresses and data to the device on SI. *I^2C Data:* SDA is the bidirectional data line between the device and an external I^2C controller. This pin should be externally pulled high by 1 kΩ to 5 kΩ resistor. See the I^2C bus specification for sizing guidance for this resistor, referred to as RP in that specification. This pin has an internal pull-up (typical 85 kΩ) to VDDIO.
23	33	SO_IF1	I/O	**SPI Data Out/Interface Mode 1** *SPI Data Out:* After reset this pin is SO. The device outputs data to an external SPI controller on SO during SPI read transactions. *Interface Mode:* On the rising edge of RST_B this pin behaves as IF1. In I^2C interface mode IF1 specifies bit 0 of the I^2C device address. In SPI interface mode IF1 is ignored. The interface mode is set by the CS_B_IF0 pin state on the rising edge of RST_B. See Section 7.0, "Host Interface".
24	34	CS_B_IF0	I_{PU}	**SPI Chip Select (Active Low)/Interface Mode 0** *SPI Chip Select:* After reset this pin is CS_B. An external SPI controller must assert (low) CS_B to access device registers. CS_B should not be allowed to float. *Interface Mode:* On the rising edge of RST_B this pin behaves as IF0: 0=I^2C, 1=SPI. This pin has an internal pull-up (typical 85 kΩ) to VDDIO.
System Clock				
31	41	OSCI	A-I	**Crystal Pins (Jitter Reference)** *Crystal:* An on-chip crystal driver circuit is designed to work with an external crystal connected to the OSCI and OSCO pins. See Section 5.7.2 for crystal characteristics and recommended external components. *Input Clock:* Wire OSCI to a 1 kΩ resistor to ground. Leave OSCO unconnected.
30	40	OSCO	A-O	
32	42	OSCA	P	**Crystal Oscillator Guard Pin** This pin is internally connected to crystal driver circuit ground. *Crystal:* Wire OSCA to a top-layer ring around the external crystal and a layer-2 island under the ring, the crystal and the OSCA, OSCI, OSCO, and OSCB pins. Void all other PCB layers under the layer-2 island. See Section 5.7.2 for details. *Input Clock:* Leave OSCA unconnected.
29	39	OSCB	A-I	**System Clock Input (Jitter Reference)** *Crystal:* When a crystal is connected to the OSCI and OSCO pins, wire OSCB to the ring and layer-2 island that are connected to OSCA. *Input Clock:* An external single-ended local oscillator or clock signal can be connected to the OSCB pin. This is a design alternative instead of a crystal connected to OSCI and OSCO. Only one crystal or clock signal should be wired to the OSC* pins at a time.

TABLE 4-1: PIN DESCRIPTIONS (CONTINUED)

7x7 Pin Number	9x9 Pin Number	Pin Name	Type	Description
Miscellaneous				
22	32	IC0	A-I/O	**Internal Connection.** Leave unconnected. Do not attach to any routing.
Power and Ground				
1	1	VDD18	P	**Core Power Supply.** 1.8V ±5%.
—	2			
12	15			
27	37			
2	3	VDD33	P	**Core Power Supply.** 3.3V ±5%.
11	14			
28	38			
33	43			
34	44	VDDIO	P	**Digital I/O Supply.** 1.8V±5% to VDD33. Supply pin for SPI/I^2C and GPIO[4:0] pins.
—	50	VDDO0	P	**OUT0P/N Power Supply.** 1.8V±5% to VDD33.
40	53	VDDO1	P	**OUT1P/N Power Supply.** 1.8V±5% to VDD33.
-	56	VDDO2	P	**OUT2P/N Power Supply.** 1.8V±5% to VDD33.
43	59	VDDO3	P	**OUT3P/N Power Supply.** 1.8V±5% to VDD33.
46	62	VDDO4	P	**OUT4P/N Power Supply.** 1.8V±5% to VDD33.
16	19	VDDO5	P	**OUT5P/N Power Supply.** 1.8V±5% to VDD33.
—	22	VDDO6	P	**OUT6P/N Power Supply.** 1.8V±5% to VDD33. For the 7 mm x 7 mm VQFN package only: OUT6P/N is on VDDO8 with OUT8P/N
—	25	VDDO7	P	**OUT7P/N Power Supply.** 1.8V±5% to VDD33.
21	28	VDDO8	P	**OUT8P/N Power Supply.** 1.8V±5% to VDD33.
—	31	VDDO9	P	**OUT9P/N Power Supply.** 1.8V±5% to VDD33.
—	—	NC	—	Not connected Not internally connected.
3, 4	4, 5	DNC	—	**Do Not Connect.** Do not wire anything to these pins. Leave unconnected.
E-pad	E-pad	VSS	P	**Ground.** 0 volts.

5.0 FUNCTIONAL DESCRIPTION

5.1 Input References

5.1.1 INPUT SOURCES

The device has ten inputs (single-ended or differential) as possible references for the DPLLs. See Figure 5-3 for connection options and recommended external components. Each input can be enabled or disabled with the ref_config::enable bit and optionally inverted by setting ref_config::invert=1.

The device synchronizes (locks) to any input reference which is a 1 kHz multiple, or any input reference that is an M/N x 1 kHz multiple (FEC rate) where M and N are 16 bits wide. In some cases M/N x 1 Hz, M/N x 10 Hz and M/N x 100Hz are supported.

The input reference frequency is configured in the ref_freq_base, ref_freq_mult, ref_ratio_m, and ref_ratio_n registers. The input reference frequency can be changed when the input reference is not the active source for a DPLL.

The device accepts an input reference with a maximum frequency of 1250 MHz for regular two-pin differential mode, 400 MHz for single-pin differential mode, or 300 MHz for CMOS.

If the frequency of an input reference exceeds 800 MHz, the reference must be internally divided by 2 before being fed to a DPLL. The ref_config::pre_divide field controls enable/disable of the internal divide-by-2 circuitry).

Unused input references can be disabled to reduce power consumption.

5.1.2 INPUT REFERENCE MONITORING

The input references are monitored by reference monitor indicators that are independent for each reference. The monitors indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

It is possible to mask an individual reference monitor from triggering a reference failure by setting the corresponding bits in the ref_mon_th_mask_x and ref_mon_tl_mask_x registers.

5.1.2.1 Input Loss of Signal Monitor (LOS)

LOS is an external signal, wired to one of the GPIO pins or a REF pin configured as a GPI. LOS is typically generated by a PHY device whose recovered clock is fed to one of the reference inputs. The PHY device generates a LOS signal when it cannot reliably extract the clock from the line. The user can set one of the GPIO pins as an LOS input by setting the corresponding gpio_config_x::ctrl field to 010 (control mode) and setting gpio_select_x fields to specify the appropriate bit in the ref_los_3_0 register

The GPIO inputs are read approximately every 10 ms to 25 ms.

5.1.2.2 Input Coarse Frequency Monitor (CFM)

The CFM monitors the input reference frequency for 100 ms so that it can quickly detect large changes in frequency. The CFM limit for each input reference can be specified in the ref_cfm mailbox register with a threshold from 0.1% to 50%. If the CFM limit is exceeded, then CFM failure is declared for the corresponding reference.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

5.1.2.3 Input Precise Frequency Monitor (PFM)

The PFM block measures the frequency accuracy of the reference and updates the indicator bit. To prevent PFM from being falsely triggered by jitter/wander at the reference input, PFM averages frequency for approximately 10 seconds (approximately 20 seconds for a 0.5 Hz input) and indicates failure when the measured frequency exceeds the limit specified in the ref_pfm_disqualify register. To ensure an accurate frequency measurement, the PFM measurement interval is re-started if phase or frequency irregularities are detected by SCM or CFM. The PFM provides a level of hysteresis to prevent a failure indication from toggling between valid and invalid for input references that are on the edge of the acceptance range. The PFM limit should be set as described in ref_pfm_disqualify and ref_pfm_qualify mailbox registers. The resolution of these registers is 5 ppb (0.005 ppm).

PFM uses the local crystal or XO connected to OSCI or OSCB as its reference. As a result, the actual acceptance and rejection frequencies can be offset with respect to the external oscillator's output frequency. This is accounted for in the acceptance and rejection requirements as described in Telcordia GR-1244 section 3.4.1. An example of the acceptance and rejection ranges for the Stratum 3 application (acceptance in the range of ±9.2 ppm, rejection at ±12 ppm given a ±4.6 ppm freerun frequency accuracy of a Stratum 3 reference oscillator) is shown in the figure below.

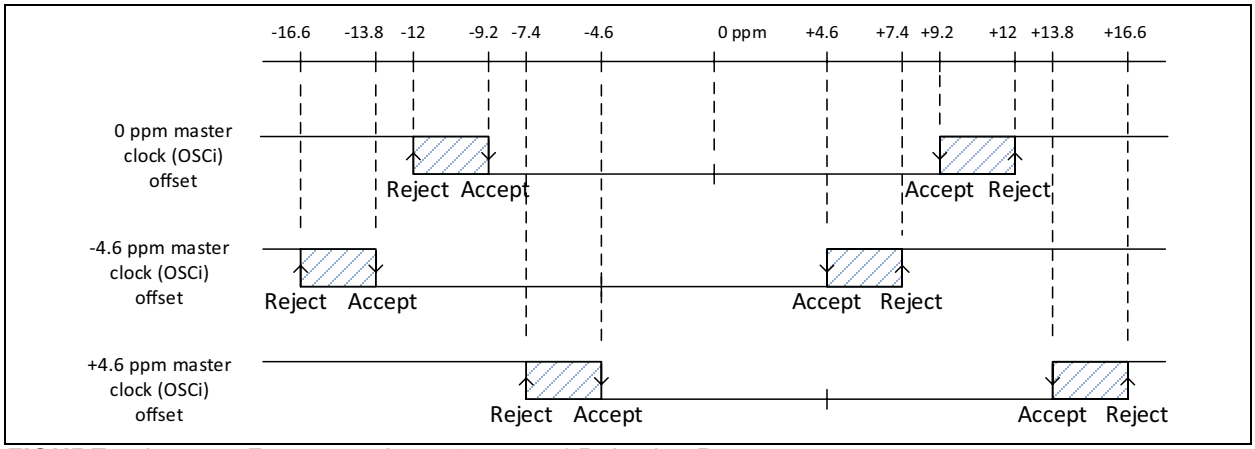


FIGURE 5-1: *Frequency Acceptance and Rejection Ranges.*

5.1.2.4 Input Single Cycle Monitor (SCM)

This detector measures the rising-edge-to-rising-edge and falling-edge-to-falling-edge periods of the input reference. If either exceeds the predefined SCM limit then an SCM failure is declared. The SCM limit for each input reference can be selected in the ref_scm mailbox register with percentage settings from 0.1% to 50%. When ref_scm::fine_en=1, a fine SCM option is enabled that allows the SCM limit to be specified in ~0.5 ns steps in the ref_scm_fine mailbox register.

For frequencies below 16 kHz, the CFM and SCM limits should be set to the same value for proper operation.

For frequencies above 400 MHz, SCM (and the GST) should not be used.

Note that SCM (percentage or fine) is not available for 0.5 Hz input references.

5.1.2.5 Input Guard Soak Timer (GST)

When selected, the guard soak timer adds extra time to qualify and disqualify a reference. The default time to wait to qualify a reference is 200 ms after the CFM and SCM limits have been satisfied. When disqualifying a reference, the time starts after a CFM or SCM failure is detected and before the reference is disqualified. The default disqualification time is 50 ms. A PFM failure does not affect this timer.

When a reference is currently qualified and a failure occurs, the timer for disqualification is started. When the timer reaches the programmed threshold the reference is disqualified. If at any time between the starting of the timer and reaching the programmed threshold the input reference returns to a good state then the disqualification timer is reset.

When a reference is currently disqualified and the reference returns to good status, the timer for qualification is started. When the timer reaches the programmed threshold the reference is qualified. If at any time between the starting of the timer and reaching the programmed threshold the input reference returns to a failure state then the qualification timer is reset.

For frequencies above 400 MHz, the GST should not be used because the single cycle monitor (SCM) is never valid.

Mailbox registers ref_gst_disqual and ref_gst_qual configure the disqualification and qualification timers.

5.1.2.6 Input Reference Monitoring Interrupt Generation

A block diagram describing how reference monitoring blocks interact and how they generate an interrupt is shown in Figure 5-2. As can be seen from the block diagram the reference monitoring interrupt generation is separate from reference monitoring DPLL control which is described in the next section. The purpose of this is to allow user full flexibility during forced reference (manual) control.

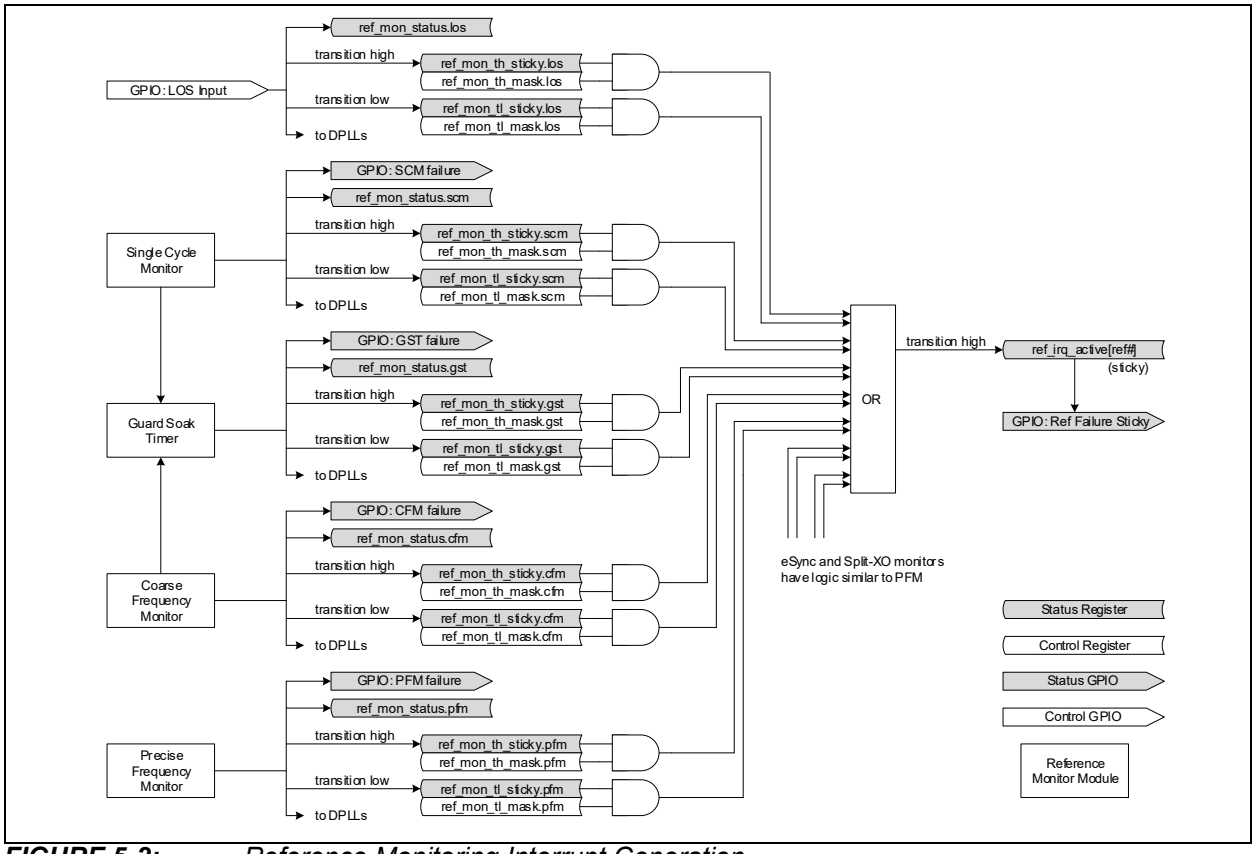


FIGURE 5-2: *Reference Monitoring Interrupt Generation.*

5.1.3 INPUT FREQUENCY MEASUREMENT

The device reports the measured frequency of each input reference in Hz in the ref_freq_x registers. The value is a running average and therefore, for a stable input reference, become more accurate over time as averaging has a filtering effect on input noise.

The frequencies of the references can be read in Hz or in fractional frequency offset (ppb, ppm) vs. their user-specified nominal frequencies.

For debug it is often useful to read the reference frequencies in Hz. If, for example, a reference is expected to be 25 MHz but a frequency read indicates the incoming clock signal is actually 1 MHz, then the problem is with the source of the clock signal and not with the device. This can be done by issuing a read command by setting ref_freq_meas_ctrl::latch to 01. The lsb of the ref_freq_x registers for this type of read is 1 Hz.

When the nominal frequency of the incoming clock signal is correct, it is often more useful to read the reference's fractional frequency offset ([actual – expected] / expected) in ppm or ppb. This can be done by issuing a read command by setting ref_freq_meas_ctrl::latch to 10 (for measurement in local XOs timebase) or to 11 (for measurement in a user-specified DPLL's timebase). The lsb of the ref_freq_x registers for this type of read is 2^{-32}.

All reference frequencies are latched at the same instant using the read frequency command.

When the ref_freq_meas_ctrl::latch value is 10, all input reference frequency measurements use a local oscillator's timebasefrom the XO wired to the OSCI pin or OSCB pin.

When the ref_freq_meas_ctrl::latch value is 11, all input reference frequency measurements use a user-specified DPLL's timebase. The DPLL is specified by dpll_meas_ref_freq_ctrl::idx. The dpll_meas_ref_freq_ctrl::en bit must be set to 1 to use this behavior. When a DPLL is locked to an input reference that is known to be high-accuracy (e.g. known to be traceable to a primary reference source), that DPLL can be chosen as the timebase for reference frequency measurements.

See also the ref_freq_meas_mask_3_0 register.

5.1.4 INPUT GAPPED CLOCKS

The device supports locking to input gapped clocks.

5.1.5 INPUT BUFFERS

The device has ten reference inputs arranged in REFxP and REFxN pairs. Each input can receive a CMOS or differential signal, or a pair can receive a differential signal. This is specified in the ref_config mailbox register. The input frequency range for a differential signal is 0.5 Hz to 1250 MHz for regular two-pin differential mode, 400 MHz for single-pin differential mode, or 300 MHz for CMOS.

Figure 5-3a shows a DC-coupled LVDS example. In this case ref_config::diff_en=1 enables just one internal differential receiver, and ref_config::ac_couple=0 disables internally-provided DC-bias of the REFxP/N pins because the LVDS transmitter sets the DC bias.

Figure 5-3b shows an AC-coupled LVPECL example. In this case ref_config::diff_en=1 enables just one internal differential receiver, and ref_config::ac_couple=1 enables internally-provided DC-bias on the receive side of the AC-coupling caps. Setting ref_config::vcm=00 gives a 1.75V DC-bias allowing the device to accept large input signal swings.

Figure 5-3c shows a generic differential example of wiring the positive side of a differential signal to a REF pin. Many differential drivers require a DC path through termination resistor(s) and therefore the AC coupling cap must be after the termination resistor(s). In this case ref_config::diff_en=0 enables both internal differential receivers, and ref_config::ac_couple=1 enables internally-provided DC-bias on the receive side of the AC-coupling caps.

Figure 5-3d shows an example of wiring two CMOS inputs to a REF pair. In this case ref_config::diff_en=0 enables both internal differential receivers, and ref_config::ac_couple=0 disables internally provided DC-bias on the REFxP and REFxN pins. The ref_config::vcm field is set for 0.95V, 1.27V, or 1.75V logic threshold voltage to accommodate 1.8V, 2.5V, or 3.3V CMOS signal swing, respectively.

The tables below provide recommendations for interfacing a variety of signal types to the device.

TABLE 5-1: INTERFACING DIFFERENTIAL SIGNALS TO A REFxP/N PAIR (DIFF_EN=1 FOR REFxP)

Signal Format	Interface Recommendation	ac_couple bit	vcm field
LVDS	DC-couple	0	01=1.27V
	AC-couple	1	01=1.27V
LVPECL	AC-couple	1	00=1.75V
CML			
HCSL			
Other differential format			

TABLE 5-2: INTERFACING DIFFERENTIAL OR CMOS SIGNALS TO ONE REFx PIN (DIFF_EN=0 FOR REFxP)

Signal Format (typ V_{CM})	Interface Recommendation	ac_couple bit	vcm field
LVDS	Externally terminate the differential signal and AC-couple signal POS side to pin	1	00=1.75V
LVPECL			
CML			
HCSL			
Other differential format			
3.3V CMOS	DC-couple	0	00=1.75V
2.5V CMOS	DC-couple	0	01=1.27V
1.8V CMOS	DC-couple	0	10=0.95V
<1.8V CMOS (>0.2V)	AC-couple	1	00=1.75V

Note 1: A REFxP/REFxN pair can accept any combination of Figure 5-3c differential and Figure 5-3d CMOS signals.

2: The complementary side of each internal differential receiver is always internally DC-biased as specified by ref_config::vcm, which sets the logic threshold voltage.

3: The ref_config::diff_en bit for REFxP controls differential vs. 2x single-ended for the REFxP/REFxN pair. The ref_config::diff_en bit for REFxN pins is ignored.

4: The ref_config::vcm field always sets the logic threshold. When ac_couple=1, vcm also sets the internally provided DC bias voltage.

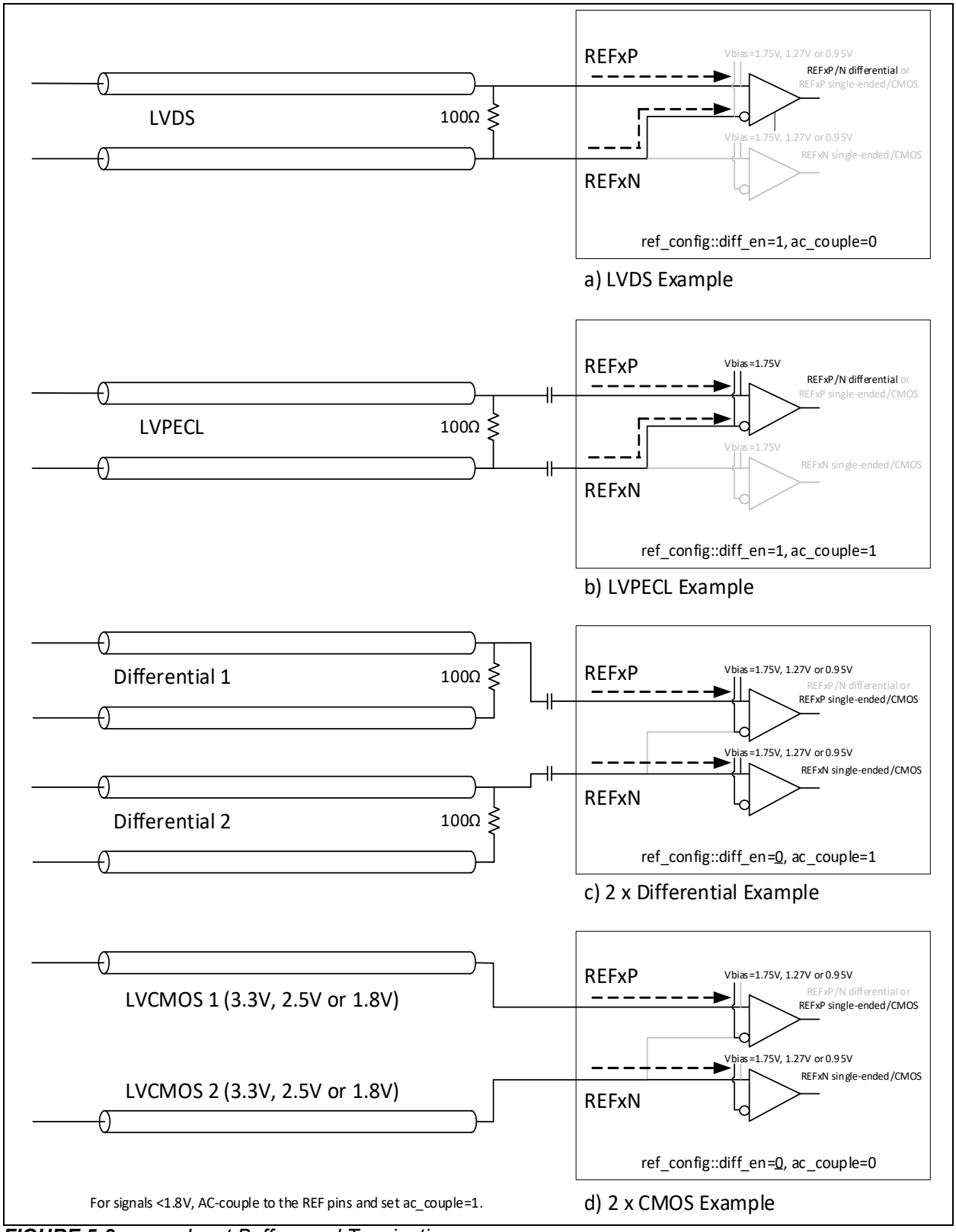


FIGURE 5-3: *Input Buffers and Termination.*

The transmission line for an LVCMOS signal should be terminated at the source with a series resistor of approximately 22Ω as shown in the figure below. Consult the data sheet for the signal driver to determine its output impedance and set the series resistor to 50Ω minus the driver output impedance.

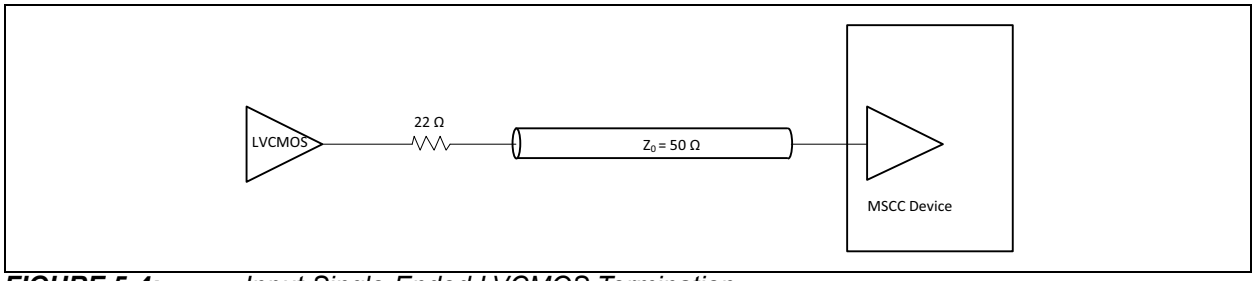


FIGURE 5-4: *Input Single-Ended LVCMOS Termination.*

5.1.6 INPUT-VS-INPUT PHASE MEASUREMENT

The phase difference between any two inputs can be measured using the input-vs-DPLL phase measurement tool described in Section 5.1.7.2 below. After the phases of all ten REFs have been measured vs. the selected DPLL, any input-vs-input phase measurement can be calculated by subtracting the measured phases of the two inputs. See Section 5.1.7.2 for more details.

5.1.7 INPUT-VS-DPLL PHASE MEASUREMENT

5.1.7.1 DPLL vs. Its Selected Reference

Two tools are available for input-to-DPLL phase offset measurement. For each DPLL that is (a) in automatic or forced reference switching mode, and (b) that has an input reference present, the phase offset between a DPLL and its reference can be read from register dpll_phase_err_data_x (where x is the DPLL number). This feature can be used not only while the DPLL is locked to the input reference but also during pull-in, but it is not available when the DPLL is freerun, holdover or NCO modes or the holdover state of automatic mode.

5.1.7.2 DPLL vs. All References

The phases of all ten REFs can be measured simultaneously vs. the DPLL specified by dpll_meas_idx. This feature is enabled by setting dpll_meas_ctrl::en, and the phases are read from the ref_phase_x registers. This behavior is available in all DPLL modes and states.

Note that this feature also supports input-vs-input phase measurement. For example, to get REF0P vs. REF0N phase measurement, read REF0P vs. DPLL phase from the ref_phase_0P register, read REF0N vs. DPLL phase from the ref_phase_0N register, and calculate REF0P_vs_REF0N = ref_phase_0P – ref_phase_0N. DPLL phase cancels out of the calculation.

The timebase for the phase measurement can be controlled by specifying the DPLL with the desired timebase. When a DPLL's reference is known to be high accuracy (such as a reference known to be traceable to a primary reference clock), then that DPLL can be chosen as the timebase.

The ref_phase_x register value is affected by the input phase adjustment specified in the ref_phase_offset_compensation mailbox register for REFx. See Section 5.1.8.

For 1 Hz vs 1 Hz phase measurements the averaging can take several minutes to converge due to the 1 Hz sample rate.

5.1.8 INPUT PHASE ADJUSTMENT

Input phase offset adjustment can be used to adjust the phase of input references with resolution of 1 ps and maximum range of ±2.1 ms. Each input reference has its own independent adjustment that can be programmed in the ref_phase_offset_compensation mailbox register.

5.1.9 INPUTS REFs AS GENERAL-PURPOSE INPUTS

Each REFxP and REFxN pin can serve as a general-purpose input (GPI). The GPI logic is always enabled alongside the input clock logic. The ref_gpi_config::ctrl mailbox register field configures the GPI logic for either input mode or control mode. In input mode, the state of the REF pin is shown in the corresponding bit of gpi_in_status_7_0. In control mode The REF pin can control a register bit specified by the page, offset and bit fields of the ref_gpi_select mailbox register.

5.2 Input-Output Special Formats

There are a variety of input and output formats beyond typical high frequency clocks, such as

- Ref-Sync (combination of high speed clock and low speed frame sync pulse)

These formats are supported on the input side and the output side of the device. The input and output formats can be different (such as ePPS on the input and 1PPS on the output). The device may reference-switch between inputs of different formats (such as between an ePPS input and a Ref-Sync pair of signals).

5.2.1 INPUT-OUTPUT REFERENCE-SYNC PAIR

5.2.1.1 Input Operation

The loop bandwidth of a PLL needs to be at least 10 times lower than the frequency of the signal the PLL is locked to. Therefore when a PLL is locked to a 1 Hz (1PPS) reference, its loop bandwidth needs to be less than 0.1 Hz which requires use of a very stable local oscillator such as a TCXO or OCXO for the device's system clock.

The device can provide significant cost savings because it can synchronize to a reference clock of any frequency (typically higher than 1 kHz) plus a sync signal (e.g. 1PPS). This is referred to as a Ref-Sync pair. In this case the loop bandwidth of the PLL is governed by the input clock frequency which is presumably much higher than 1 Hz (typically higher than 1 kHz). This allows much wider loop bandwidth and faster lock time. Hence Ref-Sync pair behavior requires only a low-cost XO for the device's system clock. The timing diagram of the Ref-Sync pair is shown in the following figure.

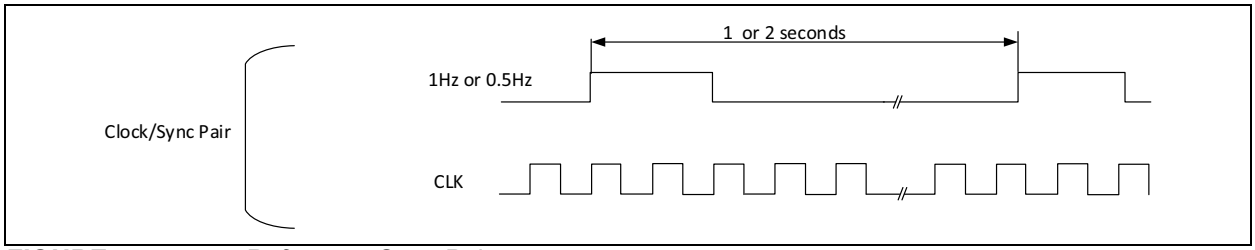


FIGURE 5-5: *Reference-Sync Pair.*

The device can synchronize to a Ref-Sync pair by enabling this feature for a particular reference input and by specifying which input has the Sync signal in the ref_sync_ctrl mailbox register. Although Figure 5-5 shows the Sync pulse aligned to the rising edge of the clock, the device can be programmed in the ref_sync_misc mailbox register to lock to a Ref-Sync pair where the Sync pulse is aligned with the falling edge of the reference clock. Duty cycle of the Sync pulse does not have to be 50%. Any duty cycle is accepted as long as the width of the pulse is more than 5 ns.

The device can terminate up to 5 Ref-Sync pairs (on 10 inputs) and each DPLL can synchronize to any of the Ref-Sync pairs. When an input is used as a Sync input, it is important to remove this reference from all automatic reference selection priority lists in the device (see Section 5.3.2). If the Sync input is not qualified, the Ref input is treated like a normal reference input. When a DPLL's selected reference is a Ref-Sync pair, it is assumed that output clock and sync phase should match input Ref-Sync phase, and the state of TIE-clear is ignored.

The timing of when a DPLL remeasures the phase of the Sync signal is configurable in the dpll_fp_first_realign and dpll_fp_realign_intvl registers. The Sync signal phase can be measured only once, two times with a programmable interval in between, repeatedly at a programmable interval, or continuously. The dpll_fp_lock_thresh register specifies an optional Sync phase-lock criteria that is applied in addition to regular Clock phase-lock criteria. System software can force a remeasure/realign with the Sync signal by asserting dpll_cmd_x::ref_sync_align.

Note that another DPLL can be configured to lock to only the Ref signal without considering the Sync signal if that other DPLL has dpll_ctrl_x::ref_sync_en=0.

5.2.1.2 Output Operation

The device can also generate a Ref-Sync pair, and an example of output frame pulse alignment is shown in Figure 5-6.

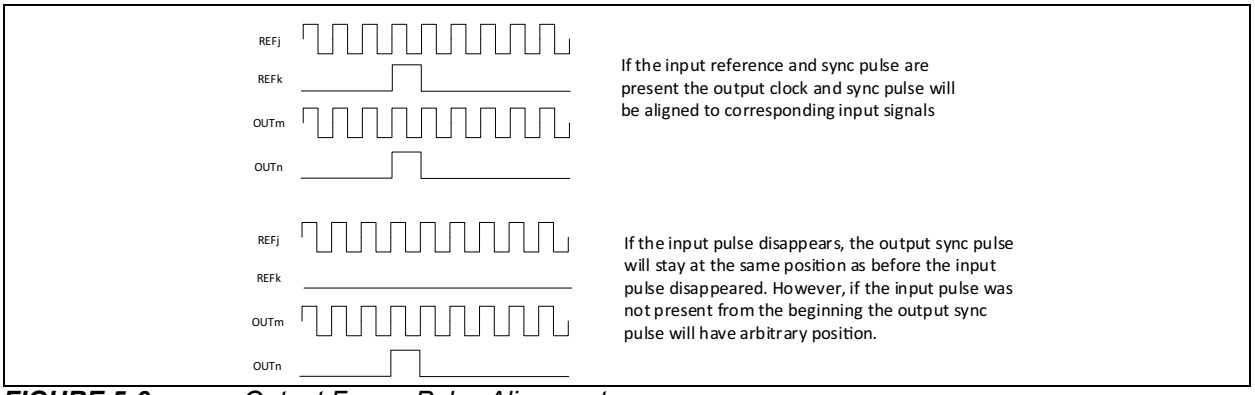


FIGURE 5-6: *Output Frame Pulse Alignment.*

In this example, the reference is on REFj and the sync pulse is on REFk where j ≠ k. The output clock is on OUTm and the output sync pulse is on OUTn where m ≠ n. Any two input references can be used for Ref-Sync pairing, but the output clock and output frame pulse must be on the same synthesizer. Although Figure 5-6 shows single-ended outputs, the clock and sync pulse can be generated on differential or mixed (one single-ended and the other differential) outputs as well.

5.3 Digital Phase Locked Loops (DPLLs)

The device supports one (ZL30273) or two (ZL30274) independent DPLL channels. DPLLs are enabled by default. Each DPLL can be enabled/disabled through the host registers.

5.3.1 DPLL INPUT MONITORING MASKS

Each DPLL has its own reference switching (dpll_ref_sw_mask) and holdover (dpll_ref_ho_mask) mask mailbox registers which are used to prevent reference monitoring circuits from triggering the DPLL to switch references or to go into the holdover state. Please note that the GST bit should not be unmasked (GST trigger enabled) without unmasking either the SCM, the CFM, or both bits. The reference switching mask is used only in the automatic control mode. In forced reference mode this register is ignored. The holdover mask register is active in both automatic and forced reference modes.

5.3.2 DPLL INPUT REFERENCE PRIORITY

For each DPLL, each input reference can be assigned a local priority value in the dpll_ref_prio_x mailbox registers. The priorities are relative to each other, with lower numbers being the higher priority. Value “1111" disables the ability to select the reference (i.e., don’t use for synchronization). If two or more inputs are given the same priority number, those inputs are ranked by input number (i.e., REF0P is higher priority than REF0N). The default reference selection priority is equal to its reference number (i.e., REF0P is highest priority).

When two or more same-priority references are the highest-priority valid inputs, DPLL reference switching among those inputs is nonrevertive. But if a higher-priority reference becomes valid the DPLL switches to the higher-priority reference (a revertive switch).

5.3.3 DPLL INPUT PULL-IN, HOLD-IN RANGE

Pull-in/hold-in range is programmable in the dpll_range mailbox register. When the input reference frequency offset exceeds the pull-in/hold-in limit a notification can be generated. Refer to the **flhit** bits in the dpll_mon_status_x status registers.

5.3.4 DPLL INPUT TOLERANCE CRITERIA

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, reference switching or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with the input reference type.

5.3.5 DPLL INPUT ADVANCE AND DELAY

The DPLL phase may be advanced or delayed. There are two resolution-and-range options available. The fine option has resolution of 1 ps and maximum change per update of ±2.1 ms. The coarse option has resolution of 1 ns and maximum change per update of ±2 seconds. This feature uses the dpll_tie_data_x, dpll_tie_ctrl and dpll_tie_ctrl_mask registers. See also the dpll_tie_wr_thresh mailbox register. This phase adjustment feature acts as if the input signal is ahead or behind its true location by the programmed amount; therefore, any changes to the phase adjustment are filtered through the DPLL bandwidth. Each advance or delay is relative to the current DPLL phase; therefore, changes can be commanded sequentially so that cumulative phase offset is unlimited. The value applied is retained for all inputs and all modes of operation of the DPLL, and is only cleared by the user.

5.3.6 DPLL PHASE SLOPE LIMITER

A sudden phase change at the input of the DPLL can occur due to a reference rearrangement upstream in the timing chain. While most modern devices (DPLL) can perform a hitless switch between references, telecom standards allow for relatively large phase changes. The response of a DPLL to such a phase transient is governed by the DPLL's loop bandwidth—the narrower the loop bandwidth the slower the phase change at the output.

Some applications may be sensitive to fast phase transients and mitigating them with DPLL loop bandwidth reduction may not be possible (the loop bandwidths are generally restricted to a specific range for compliance with a particular standard). In such cases the DPLLs offer Phase Slope Limiter (PSL) behavior, which limits the DPLL output phase change per unit time to a specified value.

The phase slope limit can be adjusted in the dpll_psi mailbox register from 1 ns/s to 65535 ns/s. These low PSL values can be very useful to slow input clock phase transients. They can also be used to limit the frequency offset (compared with the system clock) since phase slope is in units of ns/s, which is equivalent to ppb (parts per billion). Care must be taken when setting a low PSL value that the oscillator is sufficiently stable. Care must also be taken when wander transfer is important to ensure that the PSL does not impact any expected input-to-output wander transfer behavior.

When the DPLL phase changing is limited by the PSL setting a notification can be generated. See the **pslhit** bits in the dpll_mon_status_x status registers.

5.3.7 DPLL CORE MODES

The DPLL in the device support five modes: freerun, forced holdover, automatic, forced reference, and numerically controlled oscillator (NCO) specified by dpll_mode_refsel_x::mode. To lock the DPLL to a reference, automatic or forced reference mode should be used. In each of these two modes, there are three states: acquiring, locked, and holdover. The acquiring state is temporary state between the availability of a reference and the completion of the locking process. In the automatic mode, the DPLL may transition between the states depending on the availability of the references. In forced reference mode, the device goes into holdover if the reference selected by dpll_mode_refsel_x::ref is unavailable even if other references are available. The availability of a reference is determined by the reference qualification process. In the holdover mode and the holdover state, the device provides output clocks which are not locked to an external reference signal, but are based on an estimate of the frequency during the previous time in the locked state. To force the DPLL into holdover, even with good references present, the forced holdover mode is used.

In addition, the DPLL can be put into the freerun mode. This is used when synchronization to an input reference is not required or is not possible. Typically, this is used immediately following system power-up. In the freerun mode, the device provides timing and synchronization signals which are based on the device's system clock frequency offset only, and are not synchronized to the input reference signals. The freerun accuracy of the output clock is equal to the accuracy of the system clock. Therefore if a ±20 ppm freerun output clock is required, the system clock must also be ±20 ppm.

The freerun mode:

- The DPLL has to generate all its output clocks based only on the system clock.
- The DPLL does not lock or switch to a reference or go into holdover.
- The reference switch mask and the reference holdover mask are ignored.

The forced holdover mode:

- All references are ignored and the DPLL must go to holdover (at the frequency offset of the most recent selected reference).
- The reference switch mask and the reference holdover mask are ignored.

The forced reference lock mode:

- The DPLL tries to lock to the host-specified reference.

- The reference switch mask is ignored. No reference switching is performed.
- If the holdover mask is set, then the DPLL switches to holdover if the selected reference fails.
- If the holdover mask is not set, then the DPLL attempts to lock to the selected reference, even if it is failing one of the reference monitors. The input frequency tracking is limited by the pull-in/hold-in settings of the DPLL.

The automatic mode:

- Reference selection and holdover are automatically handled by the DPLL, based on the holdover and reference switch masks.
- If the reference switch mask is set, then a reference is selected based on availability and priority. If all enabled references are bad, then the DPLL enters holdover.
- If the holdover mask is set (and the reference switch mask cleared), then the DPLL switches to holdover on reference failure.
- If neither the reference switch nor the holdover masks are set, then the device continues to try to lock to a failed reference. The input frequency tracking is limited by the pull-in/hold-in settings of the DPLL.

The NCO mode:

- Similar to freerun mode, but with frequency control. The output clock is the configured frequency with a frequency offset specified by the dpll_df_offset_x register. This write-only register changes the output frequency offset of the DPLL.

5.3.8 DPLL STATUS INDICATORS

The DPLL provides lock and holdover indicators in the dpll_mon_status_x::lock and ho bits. The DPLL also provides state information in the dpll_state_refsel_status_x::state field.

5.3.9 DPLL BANDWIDTH (JITTER/WANDER TRANSFER)

Loop bandwidth is set by programming the dpll_bw_fixed mailbox register for one of five loop bandwidths.

The DPLL locks to an input reference and provides a stable low-jitter output clock when the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a DPLL fed with a 19.44 MHz reference can have loop bandwidth up to the maximum of 403 Hz. For a 1 kHz input reference, the DPLL loop bandwidth can be up to 14 Hz. For an 8 kHz reference the recommended maximum loop bandwidth is 61 Hz.

5.3.10 DPLL PROGRAMMABLE DAMPING AND PHASE GAIN

The device supports programmable damping and phase gain using the dpll_damping mailbox register. A common value is the default value of 0x5 for gain peaking < 0.1 dB.

5.3.11 DPLL LOCK TIME AND FAST LOCK METHODS

Without enabling special fast lock behaviors, DPLL lock time is dependent on the DPLL loop bandwidth. The device has a lock time of less than 2 seconds for loop bandwidths ≥10 Hz and phase slope limit set to unlimited. For lock times with other loop bandwidths and phase slope limits refer to Table 10-1.

Lock and loss-of-lock thresholds are independently configurable for hysteresis if desired. Refer to dpll_phase_good, dpll_phase_bad, dpll_duration_good and dpll_lock_delay mailbox registers for more details.

5.3.11.1 Automatic DPLL Fast Lock

Due to general PLL dynamics, the lock time is dependent on the phase slope limiter, loop bandwidth, damping factor and input frequency. For some values of these parameters the lock time may be prohibitively long for some applications, including those with 1 Hz inputs and outputs. To mitigate this issue, the device offers two different methods of fast lock: continuous and discrete. The discrete method is much faster, but the output phase moves in discrete step(s) (but only for participating outputs). The discrete method is generally recommended to be used for applications where the device locks to a Ref-Sync pair where the Sync signal is 1 Hz (1PPS) because in these situations lock time is very slow even with the continuous fast lock because output phase has to move by up to one second.

5.3.11.1.1 Continuous Fast Lock

It is recommended that the fast lock mode be enabled when phase slope limiting is used and disabled when PSL is unlimited. Fast lock is enabled in the dpll_fast_lock_ctrl mailbox register. A phase error threshold for triggering fast lock can be specified in the dpll_fast_lock_phase_err mailbox register. A frequency error threshold (DPLL frequency vs. input reference frequency) can be specified in the dpll_fast_lock_freq_err mailbox register. See also the dpll_fast_lock_ideal_time and dpll_fast_lock_phase_rate registers.

5.3.12 DPLL HITLESS REFERENCE SWITCHING

Referring to Table 10-1 the device is able to switch between input references with typical performance of 0.6 ns. Note that the device transitions through the holdover state when switching between input references. The switching between input references may be fully automated when an old input reference fails (is disqualified) and a new input reference is available (is qualified). Hitless reference switching is enabled when dpll_ctrl_x::tie_clear=0.

5.3.13 DPLL SUPERVISION & MANAGEMENT

5.3.13.1 DPLL Management Mode Comparisons

In unmanaged mode of operation, the DPLL state (locked, holdover, acquiring) and the selected reference are automatically set by the internal state machine of the device. It is based on availability of a valid reference and on the reference's selection priority.

In managed mode of operation, the DPLL state and the selected reference are manually set by the user.

The device allows for smooth transitions between managed and unmanaged modes. Hence, if the DPLL is in managed mode, for example locked to REF1P reference, and then is switched to unmanaged mode of operation, the state machine keeps the DPLL locked to REF1P and it does not force reference switching to any other reference unless REF1P is disqualified by its input monitors.

Each DPLL has its own independent state control and reference selection state machine.

5.3.13.2 DPLL Unmanaged Mode

The unmanaged mode combines the functionality of the normal state with automatic holdover and automatic reference switching. In this mode, transitioning from one state to another is controlled by the device internal state machine.

The on-chip state machine monitors the input reference status bits and makes decisions to perform reference switches or to change to the holdover state.

The reference switching state machine is based on the internal clock monitoring of each of the available input references and their priorities.

The state machine selects a reference source based on its priority value defined in a control register (dpll_ref_prio_x register) and the current availability of the reference. If all the references are available, the reference with the highest priority is selected; if this reference fails, the next highest priority valid reference is selected, and so on.

In unmanaged mode, the state machine only reacts to reference failure indicators and performs reference switching anytime one of the following conditions takes place, assuming they are not masked with their corresponding mask bits:

- LOS detected a failure and refswitch mask LOS is at logic “1”
- SCM detected a failure and refswitch mask SCM is at logic “1”
- CFM detected a failure and refswitch mask CFM is at logic “1"
- GST is triggered and refswitch mask GST is at logic “1"
- PFM detected a failure and refswitch mask PFM is at logic “1"

In unmanaged mode, the device automatically selects a valid reference input. If the current reference used for synchronization fails, the state machine switches to another valid reference. If all the available references fail, then the device enters the holdover state under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"

In unmanaged mode of operation, the state machine automatically recovers from holdover when the conditions to enter holdover are not present.

The reference selection is based on reference priority. The current active reference for each DPLL can be read from the dpll_state_refsel_status_x register.

If neither the reference switch nor the holdover masks are set, then the device continually tries to lock to a failed reference subject to the limits of the pull-in/hold-in range.

5.3.13.3 DPLL Managed (Manual) Mode

In managed mode, the device does not auto-select among the reference inputs. Instead the user specifies which reference input to use, and if that reference fails the DPLL enters the holdover state without switching to another reference.

The user (external software) monitors the device status bits. Based on the status information, the user makes a decision to force holdover or to perform a reference switch. In managed mode the active reference input is selected using the ref field of the dpll_mode_refsel_x register. If the user sets the device to lock to a failed reference, the device stays in holdover and only locks to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and holdover mask LOS is at logic “1”
- SCM detected a failure and holdover mask SCM is at logic “1”
- CFM detected a failure and holdover mask CFM is at logic “1"
- GST is triggered and holdover mask GST is at logic “1"
- PFM detected a failure and holdover mask PFM is at logic “1"

The state machine automatically recovers from holdover when the conditions to enter holdover are not present.

Time-critical transitions for entry into holdover and exit from holdover are managed by the internal state machine. A change of the reference select bits triggers an internal state transition into holdover and then an exit into Normal state and locking to the new reference.

If neither the reference switch nor the holdover masks are set, then the device continually tries to lock to a failed reference subject to the limits of the pull-in/hold-in range.

5.3.14 DPLL JITTER/WANDER GENERATION

The wander generation is dominated by the high-pass filter characteristics of the local oscillator above the programmed DPLL filter bandwidth.

The jitter generation performance is provided in Section 10.0.

5.3.15 DPLL FREQUENCY AND PHASE REPORTING

The frequency offset of the DPLL vs. the system clock oscillator can be read from the dpll_df_offset_x register by initiating a read using the fields of the dpll_df_read_x register with read_sem=1. The frequency offset of the DPLL vs. the input reference it is tracking can be read from the dpll_df_offset_x register using the fields of the dpll_df_ctrl_x register with read_sem=1 and ref_ofst=1. The resolution of both values is 2^{-48} (~0.0000035 ppb or 3.5E–15).

5.4 Input-Output Conversion

5.4.1 INPUT-TO-OUTPUT AND OUTPUT-TO-OUTPUT PHASE ALIGNMENT

5.4.1.1 Phase Alignment Control

When the output clock is locked to a jitter-free and wander-free input clock, input-to-output latency is expected to have a typical error of 0 ns. This is accomplished within the device using advanced, automatic precision input-output alignment routines at initialization. See Table 9-14 for alignment specifications.

Additionally, there are user-accessible phase adjustments that allow for input-to-output and output-to-output latency corrections to compensate for PCB load delay, as detailed in Section 5.3.5 DPLL Input Advance and Delay and Section 5.6.3 Output Phase Alignment and Phase Adjustment.

5.4.1.2 External Feedback

The PLL architecture allows for implementation of an external feedback path where one of the output clocks signals is externally wired to one of the reference inputs. External feedback automatically maintains tight alignment of output phase with reference input phase, dynamically compensating for changes in PCB trace delay and external buffer delay caused by changes in temperature.

External feedback is enabled by first wiring an OUT pin or a signal downstream of a OUT pin, such as a fanout buffer output) to a REF pin. Then the DPLL must be specified in ext_fb_sel::dpll, and the REF pin must be specified in ext_fb_sel::ref. Finally external feedback is enabled by setting ext_fb_ctrl::ext_fb=1.

Note that external feedback is only for clock phase alignment, not for sync phase alignment. The feedback signal must be a MHz clock signal or embedded Sync signal. It cannot be a Ref-Sync pair. If the feedback signal is an embedded Sync signal the REF pin must be configured as a regular clock, not as embedded Sync.

5.4.2 RATE CONVERSION FUNCTION AND FEC SUPPORT

The DPLL provides frequency up-scaling and down-scaling functions. It has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports:

Simple rate conversion (e.g. take in 19.44 MHz and create 255/238 FEC SONET/SDH clock of 666.51 MHz)

Double rate conversion (e.g. take in 19.44 MHz and create FEC 10GbE clock of 644.5313 MHz, which is 66/64 x 625 MHz, or create 690.5692 MHz which is 255/238 x 66/64 x 625 MHz)

The following is just an example of the frequencies that can be supported at the input and output independently (many more frequencies can be supported):

GbE:

- 25 MHz
- 125 MHz

XAUI (chip-to-chip interface, which is a common chassis-to-chassis interface):

- 156.25 MHz or x2 or x4 version

OC-192/STM-64:

- 155.52 MHz or x2 or x4 version
- 155.52 MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
- 155.52 MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version

10GbE:

- 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
- 155.52 MHz x 66/64 or x2 or x4 version

Long reach 10GE might require the following frequencies with simple rate conversion: (156.25 MHz x 255/237) and (156.25 MHz x 255/238).

The following frequencies with double rate conversion: (155.52 MHz x 66/64 x 255/237) or (155.52 MHz x 66/64 x 255/238) and (156.25 MHz x 66/64 x 255/238) or (156.25 MHz x 66/64 x 255/238). Also, users can use x2 or x4 version of the listed frequencies.

5.5 Output Frequency Synthesizers

5.5.1 SYNTHESIZER ENABLE AND MAPPING DPLLS TO SYNTHESIZERS

A synthesizer is enabled by setting synth_ctrl_x::en=1. Each synthesizer can be connected to any DPLL as shown in Figure 1-1. The synth_ctrl_x::dpll_sel field specifies the DPLL.

5.5.2 SYNTHESIZER NOMINAL FREQUENCY

The synthesizers can each generate any clock frequency from just above the system APLL frequency divided by 64 up to and including system APLL frequency divided by 16. For a typical case of APLL frequency being 12.0 GHz, this range is from just above 187.5 MHz up to and including 750 MHz.

The frequency for a synthesizer is programmed as B * K * M / N Hz where B, M, and N are 16-bit registers and K is a 32-bit register. The synth_freq_base, synth_freq_mult, synth_freq_m and synth_freq_n mailbox registers specify B, K, M, and N respectively.

5.5.3 SYNTHESIZER FREQUENCY OFFSET AND NCO BEHAVIOR

The frequency offset of a synthesizer can be adjusted with resolution of 2^{-48} (~0.0000035 ppb or 3.5E–15) in the synth_df_offset_manual_x register. The adjustment affects all outputs configured to follow the synthesizer. This offset is in addition to any offset applied by the DPLL. This register can be written as fast as once every 600 µs.

5.5.4 SPREAD-SPECTRUM MODULATION

For applications that require 100 MHz PCI Express clocks, the device can perform spread spectrum modulation (SSM) in any synthesizer. In SSM the frequency of the output clock is continually varied over a narrow frequency range to spread the energy of the signal and thereby reduce EMI. Spread-spectrum is enabled by setting synth_ctrl_x::spread_spectrum_en=1.

For center-spread applications, the frequency modulation is triangle-wave center-spread up to ±5% deviation from the center frequency with modulation rate configurable from 10 kHz to 100 kHz. (Values outside of these ranges are often achievable as well.)

For down-spread applications, such as PCI Express Refclk, the frequency modulation is triangle-wave down-spread of up to –10% deviation from the nominal frequency with modulation rate configurable from 10 kHz to 100 kHz. (Values outside of these ranges are often achievable as well.) See the synth_spread_spectrum_cfg, synth_spread_spectrum_rate and synth_spread_spectrum_spread registers.

5.5.5 SYNTHESIZER PHASE ADJUSTMENT

The phase of a synthesizer when enabled is set by the synth_phase_compensation mailbox register with 1 ps step size.

5.6 Output Clocks

The device has ten OUTxP/N output clock signal pairs that each can be internally connected to any synthesizer. Each output pair has individual enable, signal format, divider, pulse width, and start/stop controls. In CMOS mode, each signal pair can become two CMOS outputs, allowing the device to have up to 20 output clock signals. Also in CMOS mode, the OUTxN pin can have an additional divider that allows the OUTxN frequency to be an integer divisor of the OUTxP frequency (example: OUT3P 125 MHz and OUT3N 25 MHz). The outputs can be aligned relative to each other and the phases of output signals can be adjusted dynamically with fine resolution.

5.6.1 OUTPUT ENABLE, SIGNAL FORMAT, VOLTAGE AND INTERFACING

To use an output, the output driver must be enabled in output_mode::signal_format and the per-output divider must be enabled by setting output_ctrl_x::en. The per-output dividers include the per-output phase adjustment/alignment circuitry and start/stop logic.

Each output pair can be disabled or configured as LVDS, LVPECL, programmable differential, Low-V_{CM} (HCSL-like), or one or two CMOS outputs. When an output is disabled, it is high impedance, and the output driver is in a low-power state. In CMOS mode, the OUTxN pin can be disabled, in-phase, or inverted vs. the OUTxP pin. Also the OUTxP pin can be disabled while the OUTxN pin is enabled. The clock to the output driver can inverted by setting output_mode::polarity. The CMOS output driver can be set to any of four drive strengths in the output_driver_level::drive mailbox register field.

When the output driver is in LVDS mode. V_{OD} is forced to 400 mV. V_{CM} can be configured in output_driver_config::vcm mailbox register field, but the default value is typically used to get V_{CM}=1.2V for LVDS.

When the output driver is in programmable differential mode the output swing (V_{OD}) can be configured in the output_driver_level::vod mailbox register field to any value from 300 mV to 900 mV in 100 mV steps, and the common-mode voltage can be configured to any voltage from 1.0V to 2.1V in 0.1V steps in the output_driver_level::vcm mailbox register field. Together these fields allow the output signal to be customized to meet the requirements of the clock receiver and minimize the need for external components. By default, programmable differential mode provides 800 mV LVPECL signal swing with a 1.2V common mode voltage. This gives a signal that can be AC-coupled to receivers that are LVPECL or that require a larger signal swing than LVDS. The output driver can also be configured for LVPECL output with standard 2.0V common-mode voltage.

In both LVDS mode and programmable differential mode, the output driver requires a DC path between OUTxP and OUTxN for proper operation. This DC path is often a 100Ω termination resistor placed as close as possible to the receiver inputs to terminate the differential signal as shown in Figure 5-7 parts a) and b). If the receiver requires a common-mode voltage that cannot be matched by the output driver then the POS and NEG signals can be AC-coupled to the receiver after the 100Ω resistor as shown in Figure 5-7 part b). For the case where the receiver already has a 100Ω termination resistor and AC-coupling is required, a resistor can be placed between OUTxP and OUTxN as close as possible to the device to provide the required DC path as shown in Figure 5-7 part c). This resistor can be 100Ω for double-termination of the signal or it can be up to 200Ω, in which case the signal is single-terminated by the 100Ω resistor at the receiver and the signal amplitude at the receiver is larger than the double-termination case. The device provides an optional internal 200Ω that can be enabled by setting output_driver_config::rbias=1.

When the output driver is in Low-V_{CM} mode the output format is HCSL-like with electrical specs as shown in Table 9-9.

Each output has its own power supply pin, VDDO0 through VDDO9, to allow CMOS signal swing from 1.8V to 3.3V for glueless interfacing to neighboring components.

Note that LVPECL signal formats must have a VDDOx power supply of 2.5V or 3.3V and LVDS must have a VDDOx power supply of 1.8V, 2.5V, or 3.3V.

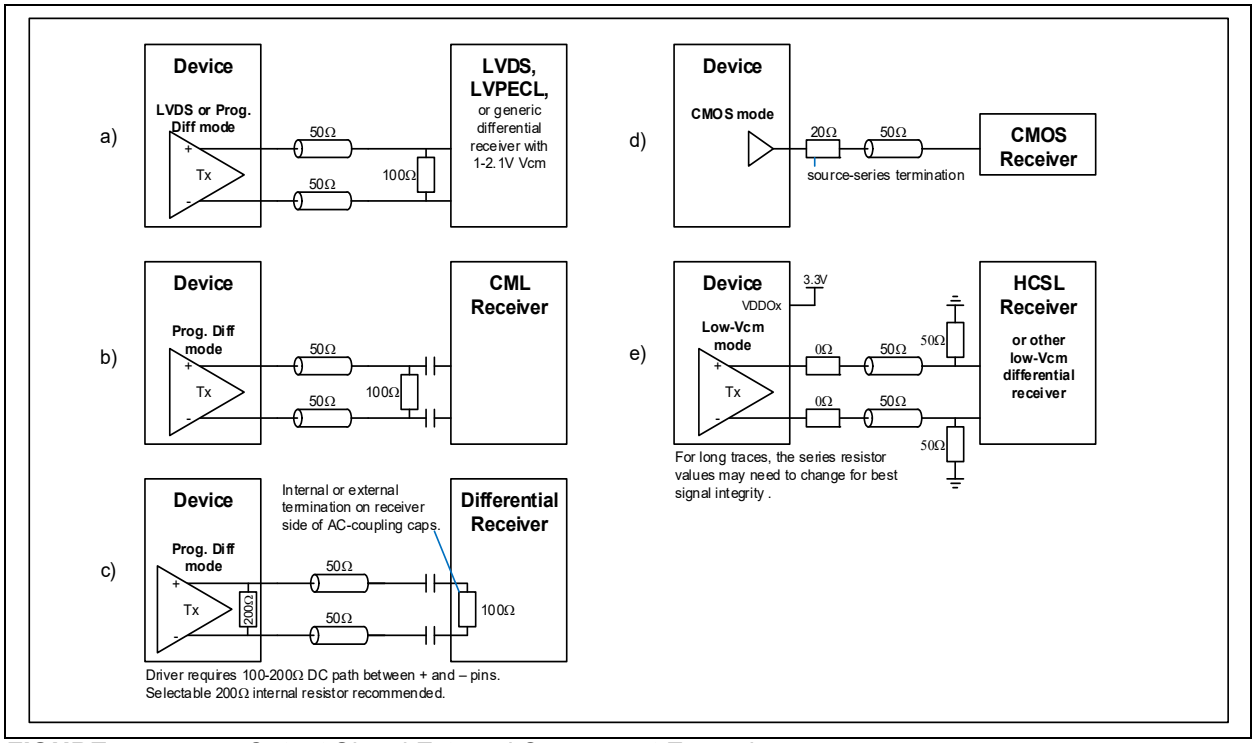


FIGURE 5-7: *Output Signal External Component Examples.*

5.6.2 OUTPUT FREQUENCY CONFIGURATION

The frequency of each output is determined by the configuration of the source synthesizer and the output divider. Each OUTxP/N pair can be connected to any synthesizer using output_ctrl_x::synth_sel. The output divider (output_div mailbox register) can produce signals with 50% duty cycle for all divider values including odd numbers. The maximum input frequency for the output divider is 750 MHz.

Because each output pair has its own independent divider, the device can output families of related frequencies that have a synthesizer divider frequency as a common multiple. For example, for Ethernet clocks, a 625 MHz clock from a synthesizer can be divided by four for one output to get 156.25 MHz, divided by five for another output to get 125 MHz, and divided by 25 for another output to get 25 MHz. Similarly, for SDH/SONET clocks, a 622.08 MHz clock can be divided by 4 to get 155.52 MHz, by 8 to get 77.76 MHz, by 16 to get 38.88 MHz or by 32 to get 19.44 MHz.

Two Different Frequencies in 2xCMOS Mode

When an output is in 2xCMOS mode it can be configured, using the 1100 and 1111 decodes of output_mode::signal_format, for N-pin divide mode. In this mode, an additional divider allows the OUTxN frequency to be an integer divide of the OUTxP frequency. Examples of where this can be useful:

- 125 MHz on OUTxP and 25 MHz on OUTxN for Ethernet applications
- 77.76 MHz on OUTxP and 19.44 MHz on OUTxN for SONET/SDH applications
- 25 MHz on OUTxP and 1 Hz (i.e. 1PPS) on OUTxN for telecom applications with IEEE1588 timing

In N-pin divide mode,the output_esync_period register specifies the additional divide value.

Note that the per-output divider must be configured to divide by 2 or more in N-pin divide mode.

5.6.3 OUTPUT PHASE ALIGNMENT AND PHASE ADJUSTMENT

The device automatically maintains alignment of enabled outputs. The default behavior is rising-edge alignment of all outputs. The phase of an output signal can be shifted by 180° by inverting the polarity (output_mode::polarity). In addition, the phase of an output signal can be shifted using the output_phase_compensation register with a step size equal to ½ of the source synthesizer clock period. For example, if the synthesizer is 625 MHz then one synthesizer period is 1.6 ns and the smallest phase adjustment is 0.8 ns.

Also, one or more low-frequency (<20 Hz) outputs can have their phase adjusted up to 1UI using the output_phase_step_ctrl, output_phase_step_data and output_phase_step_mask registers. The data register is a signed integer with units of synthesizer clock periods. The maximum phase step amplitude is limited to ±49% of a UI, i.e. ±0.49 seconds. For example, if the synthesizer is 625 MHz then one synthesizer period is 1.6 ns and the smallest phase adjustment is 1.6 ns. Phase steps are cumulative, and, therefore, the range of phase adjustment is unlimited.

In addition to the per-output controls mentioned above, the phase of all outputs derived from the same synthesizer can be controlled with 1 ps resolution. See Section 5.5.5 for details.

5.6.4 OUTPUT DUTY CYCLE/PULSE WIDTH ADJUSTMENT

The duty cycle of the output clock can be modified using the output_width mailbox register. For normal polarity outputs, the pulse is high and the signal is low the remainder of the cycle. For inverse polarity outputs, the pulse is low and the signal is high the remainder of the cycle.

When an OUTxP/N pair is configured for two different frequencies using N-pin divide mode, the OUTxN duty cycle can be modified using the output_esync_width mailbox register.

5.6.5 OUTPUT CLOCK START/STOP AND SQUELCH

5.6.5.1 Output Start/Stop

Output clocks can be stopped high or low or high-impedance. One use for this behavior is to ensure “glitchless” output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an output_ctrl_x register with bits to control this behavior. When bit **stop_high**=1 and the **stop** bit is asserted, the output clock is stopped after the next rising edge of the output clock. When **stop_high**=0 and the **stop** bit is asserted, the output clock is stopped after the next falling edge of the output clock. When the output is stopped, the output driver goes high-impedance if bit **stop_hz**=1. Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on. Low-speed output clocks can take long intervals before being stopped after the stop signal goes active. For example, a 1 Hz output could take up to 1 second to stop.

When the output polarity is inverted the output stops on the opposite polarity that is specified by the stop mode field.

The output divider must be dividing by 2 or more (output_div mailbox register ≥ 2) to use start/stop behavior because divider set to 1 bypasses the start-stop circuits.

Note that when the OUTxP/N pair is configured for two frequencies using N-pin divide mode the start-stop logic controls both OUTxP and OUTxN simultaneously. This is glitchless (no short high or low times) for the OUTxP signal, but the lower-frequency OUTxN signal can have high time or low time as short as one OUTxP cycle.

5.6.6 OUTPUT CLOCK PINS AS GENERAL-PURPOSE OUTPUTS

When an output pair is configured for a CMOS signal format, the OUTxP pin and the OUTxN pin each can be individually configured as a general-purpose output with similar behaviors to the GPIO pins (see Section 6.4). Setting output_gpo_en::out_p=1 configures the OUTxP pin as a GPO. Setting output_gpo_en::out_n=1 configures the OUTxN pin as a GPO. Note that the pin must be enabled in the output_mode::signal_format register field to be a GPO. For example if signal_format="0101 – One CMOS, OCxP Enabled, OCxN High impedance" then OCxN is disabled even when output_gpo_en::out_n=1. When an output is configured as a GPO, its behavior can be output-high, output-low, status or IRQ as specified by the output_gpo_config_out_p or output_gpo_config_out_n register. When an output is a *status* GPO it can be configured to follow an internal status bit specified by output_gpo_select_out_p or output_gpo_select_out_n.

5.7 System Clock and Local Oscillator/Crystal

The device internal system clocks are generated from a crystal wired to the OSCI and OSCO pins or from an oscillator wired to the OSCB pin. For a list of reference oscillators, refer to ZLAN-442.

5.7.1 EXTERNAL OSCILLATOR

When using a clock oscillator as the device's system clock source, connect the oscillator's output clock to the OSCB pin and set xo_config::xtal_en=0.

The jitter on output clock signals depends on the phase noise and frequency of the oscillator. For the device to operate with the lowest possible output jitter, the external oscillator should have the following characteristics:

- Phase Jitter: less than 0.1 ps_{RMS} over the 12 kHz to 5 MHz integration band
- Frequency: The higher the better, all else being equal

Several vendors offer XO products with the required jitter. Three good choices from Vectron are the 114.285 MHz VCC1-9004-114M285, the 49.152 MHz VCC1-1545-49M152, and the 48 MHz Vectron VCC1-9003-48M0000. Each of these is a standard VCC1 XO but with a max jitter specification of 0.1 ps_{RMS} over the 12 kHz to 5 MHz integration band.

5.7.2 EXTERNAL CRYSTAL

The on-chip crystal driver circuit is designed to work with a fundamental mode, AT-cut crystal resonator. See Table 5-3 for recommended crystal specifications. To enable the crystal driver, set xo_config::xtal_en=1.

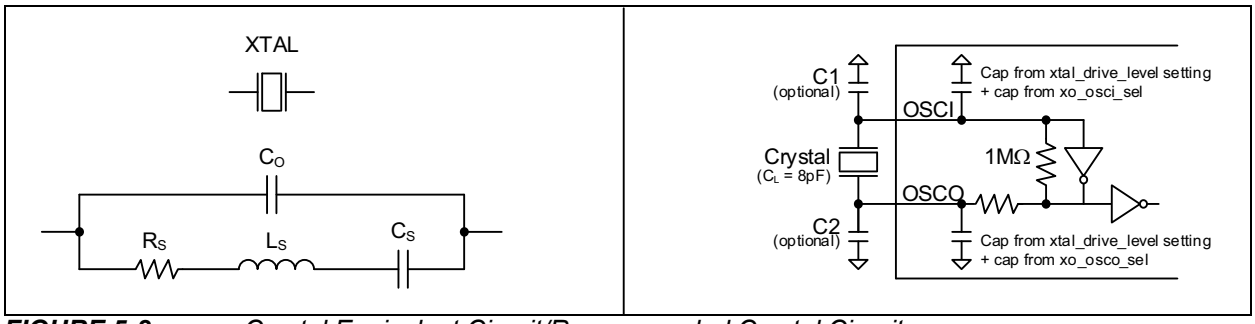


FIGURE 5-8: *Crystal Equivalent Circuit/Recommended Crystal Circuit.*

See Figure 5-8 for the crystal equivalent circuit and the recommended external component connections. The driver circuit design includes configurable internal load capacitors. For an 8 pF crystal the total capacitance on each of OSCI and OSCO should be 2 x 8 pF = 16 pF. To achieve these loads without external capacitors, first an appropriate crystal drive level should be set in xo_amp_sel::xtal_drive_level. This sets baseline internal capacitance numbers for OSCI and OSCO as described in the xtal_drive_level description. Then register field xo_osci_sel should be set to 16 pF minus the baseline internal OSCI capacitance minus the actual external OSCI board trace capacitance. Register field xo_osco_sel should be set in a similar manner for OSCO load capacitance. Crystals with nominal load capacitance other than 8 pF usually can be supported with only internal load capacitance. If the xo_osci_sel and xo_osco_sel fields do not have sufficient range for the application, capacitance can be increased by using external caps C1 and C2.

Users should also note that on-chip capacitors are not nearly as accurate as discrete capacitors (which can have 1% accuracy). If tight frequency accuracy is required for the crystal driver circuit, then set xo_osci_sel and xo_osco_sel both to 0 and choose appropriate C1 and C2 external capacitors with 1% tolerance.

The crystal and traces (and two external capacitors sites C1 and C2, if included) should be placed on the board as close as possible to the OSCI and OSCO pins to reduce crosstalk of active signals into the oscillator. No active signals should be routed under the crystal circuitry. A ground ring should surround the crystal (and optional C1 and C2) from the OSCA pin to the OSCB pin. Layer 2 below the crystal (and optional C1 and C2) should have a ground island that is connected to the layer 1 ground ring with multiple vias along the layer-1 ground ring. All other board layers should be void in the area inside the ground ring.

Note: Crystals have temperature sensitivities that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO or TCXO should be used instead.

TABLE 5-3: CRYSTAL SELECTION PARAMETERS

Parameter		Symbol	Min.	Typ.	Max.	Units
Crystal Oscillation Frequency, (Note 1)		f_{OSC}	25	—	60	MHz
Shunt Capacitance		C_O	—	2	5	pF
Load Capacitance		C_L	—	8	—	pF
Equivalent Series Resistance (ESR), (Note 2)	f_{OSC} < 40 MHz	R_S	—	—	60	Ω
	f_{OSC} > 40 MHz	R_S	—	—	50	Ω
Maximum Crystal Drive Level		—	100	100, 200, 300	—	µW
Crystal Frequency Stability vs. Power Supply		f_{FVD}	—	0.2	0.5	ppm per 10% Δ in VDD

Note 1: Higher frequencies give lower output jitter, all else being equal.

2: These ESR limits are chosen to constrain crystal drive level to less than 100 µW. If the crystal can tolerate a drive level greater than 100 µW then proportionally higher ESR is acceptable.

5.7.3 SYSTEM CLOCK FREQUENCY SELECTION

The frequency of the device's system clock on the OSCI/OSCO pins or the OSCB pin is set with the following procedure:

1. Reset the device by asserting then deasserting the RST_B pin as described in Section 5.9.
2. Set xo_config::xtal_en to 0 for clock signal on OSCB, or to 1 for crystal on OSCI/OSCO
3. Set xo_config::simple_doubler_en=1 if enabling the internal doubler
4. Set sys_apll_primary_div_int, sys_apll_primary_div_frac, and sys_apll_secondary_div so that: VCO_freq = [OSC_freq * 2^{double} * (sys_apll_primary_div_int + sys_apll_primary_div_frac / 2^{36}) * sys_apll_secondary_div] is within 1% of 12 GHz. The variable double is 1 when simple_doubler_en=1 and 0 otherwise. The GUI has prelabled options for each of these register fields to support commonly used XO frequencies such as 48 MHz, 49.152 MHz, and 114.285 MHz.
5. Set the central_freq_offset register appropriately whenever the APLL VCO frequency is not exactly 12.0 GHz. See the register description for calculations and examples. The GUI automatically calculates this value.
6. Set master_clk_cfg_ready=1.
7. Verify the setup is good by reading the master_clk_status register. Bit 3 (sys_apll_lock) should be 0 to indicate the APLL is locked. Bits 1:0 (state) should be 11 to indicate 'ready'. Also read the info register and verify bit 7 (ready) is 1.

5.7.3.1 Crystal Doubler

When operating with a crystal as the system clock source, it is usually beneficial to enable the crystal doubler (xo_config::simple_doubler_en=1). This doubles the input clock frequency to the system clock APLL, which reduces random jitter with little or no adverse effect for most frequency plans. Note that the doubler causes a spur at the OSCI frequency. If this spur falls within the output jitter band of interest then the doubler can be disabled if needed.

5.8 Power Supplies

Most of the device is powered from VDD33 (3.3V) and VDD18 (1.8V). Each OUTxP/N output pair can be independently powered with 1.5V, 1.8V, 2.5V, or 3.3V on a VDDOx supply. (The 1.5V option only applies for CMOS output signal formats. The 1.8V option only applies for CMOS and LVDS.) Digital I/O (SPI/I^2C interface pins, GPIOs) are powered from VDDIO.

5.8.1 POWER UP/DOWN SEQUENCE

There are no sequence requirements for power-up or power-down on these devices.

5.8.2 POWER SUPPLY FILTERING

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3V and 1.8V supply pins. Microchip application note ZLAN-810 provides power supply filtering recommendations.

5.8.3 POWER CALCULATOR

The GUI software for the device includes a useful power calculator that estimates power utilization for a specific configuration or application.

5.9 Reset and Configuration Pins

To ensure proper operation, the device must be reset after power-up by driving the RST_B pin low. The RST_B pin should be held low for at least 2 ms after all power supplies are within 5% of nominal voltage. Following reset, the device operates under specified default settings.

The RST_B input has Schmidt trigger properties to prevent level bouncing.

Pin SO_IF1 and CS_B_IF0 are used to configure the device on power up. These pins must be held at the desired level for at least 550 ms after RST_B goes high. Then they can used for normal functions as described in Section 7.0.

By default all outputs are disabled to allow programing of required frequencies before enabling the outputs.

6.0 CONFIGURATION AND CONTROL

The SPI/I^2C host interface allows field programmability of the device's configuration registers. As an example, the user might start the device at nominal synchronous Ethernet rate and then switch to an OTN FEC rate after the link's FEC rate is negotiated.

6.1 Pre-Configured Default Values on Power-Up

Upon power up, device registers have values as described in the Register Map section. If the device should start up with settings different from default, it can be pre-configured (pre-programmed) by Microchip. The device can be pre-configured with up to seven different custom configurations. Any of the custom configurations can be selected just after reset using the GPIO0_AC0, GPIO1_AC1, and GPIO2_AC2 pins. The values of these pins are ignored at reset if the device is not pre-configured.

6.2 Configuration Sequence

After power-up or reset the device has sequence requirements for configuration. The required sequence is as follows:

1. Poll for device ID in the id register. During initial boot the device does not respond to SPI or I^2C accesses until it is ready. System software can poll the id register to wait for the end of this interval. While not ready, the device returns 0 for SPI read accesses and NACK over the I^2C interface. When ready the device returns the device ID value.
2. Configure the system clock APLL. See Section 5.7 and its subsections, especially the procedure in Section 5.7.3.
3. Configure the rest of the device in all other registers.

Note that the device does not accept writes to mailbox registers before master_clk_status::sys_apll_lock=1 and info::ready=1.

Configurations saved by the evaluation board GUI follow this sequence. Microchip recommends creating configuration files using the GUI. System software can follow the write sequence in the configuration files after system power-up or reset.

6.3 Register Configuration

This section refers to configuration registers that are set by the user to control operation of the device.

6.3.1 INPUT REFERENCE CONFIGURATION

The following are some of the parameters can be configured for each reference input:

- Input reference frequency
- Default input reference selection
- Reference selection priority
- Automatic or manual reference switching
- Glitchless or hitless reference switching
- Reference switch based on single cycle monitor, coarse frequency monitor, precise frequency monitor, step frequency monitor, and guard soak timer

6.3.2 DPLL CONFIGURATION

The following are some of the parameters that can be configured for each DPLL:

- Input reference
- Loop bandwidth
- Phase slope limiter
- Pull-in range
- Fast-lock behaviors

6.3.3 SYNTHESIZER CONFIGURATION

The following are some of the parameters that can be configured for each Synthesizer:

- Select which DPLL drives each synthesizer
- Synthesizers can be configured to be locked to any DPLL or disabled
- Synthesizer frequency: >187.5 MHz to 750 MHz

6.3.4 OUTPUT DIVIDERS AND OUTPUT PHASE OFFSET (SKEW) CONFIGURATION

The following are some of the parameters that can be configured:

- Select which synthesizer drives each output
- Output divider enable/disable
- Divider value
- Output phase offset
- Output pulse width

6.3.5 OUTPUT DRIVERS CONFIGURATION

The following are some of the parameters that can be configured:

- Output enable/disable
- Output start/stop, (stop high, stop low, stop high-impedance)
- Output driver type (LVDS, LVPECL, programmable differential, Low-V_{CM}, CMOS)

6.4 GPIO Configuration

The device GPIO are configured using the SPI/I^2C. Each GPIO pin can be programmed independently in the gpio_config_x register to be:

General Input: In this mode, system software can read the logic level of the corresponding pin (either high or low). For example, the logic level of GPIO0 is reflected in the register gpio_in_status, bit 0.

General Output: In this mode, system software can configure a GPIO pin to drive either high or low. For example, GPIO0 would drive the value specified in register gpio_out_4_0, bit 0.

Control Inputs: In this mode, the user can control the device function via GPIOs. For example, the function controlled by GPIO0 is selected by configuring gpio_select_0. Nearly any device function that is controllable through the device registers can be controlled via GPIO. A small subset of control functions is shown below:

- Select DPLL reference
- External Loss Of Signal (LOS) indications
- Enable/disable differential and single ended outputs
- Enable/disable hitless switching
- Stop/start output clocks

Status Outputs: In this mode the device can connect a status value from any of the device status registers to the corresponding GPIO pin. For example GPIO0 mirrors a bit from the status register specified in register gpio_select_0. A subset of status messages is listed below:

- DPLL loss of lock indicators
- DPLL holdover indicators
- Reference 0 to 9 fail indicators

Interrupt Signal (IRQ): This function can configure one of the GPIOs to behave as an interrupt service request signal to software running on an external processor. In this mode, the pin behavior can be configured by the gpio_irq_config register for edge-triggered vs. level-triggered, active high vs. active low, and whether the inactive state is high-impedance or not.

The GPIO outputs are updated and the GPIO inputs are read by the device approximately every 10 ms to 25 ms.

7.0 HOST INTERFACE

A host processor controls and receives status from the device using either a SPI or I^2C interface.

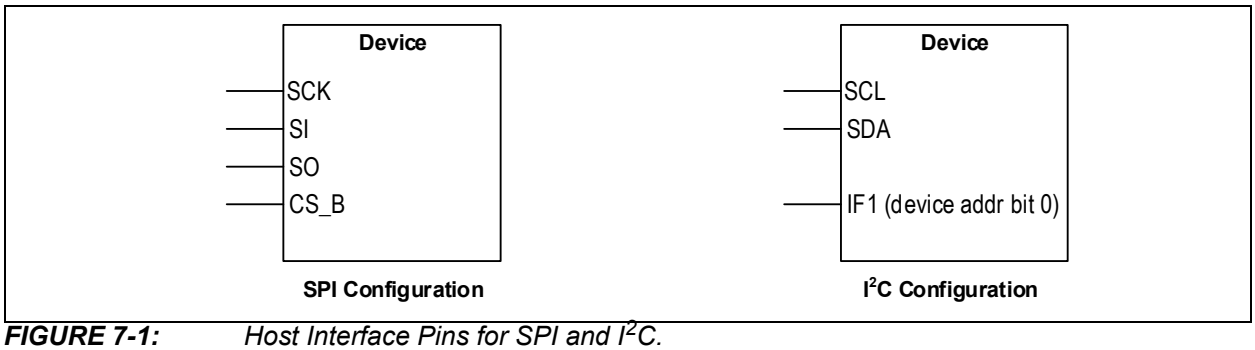


FIGURE 7-1: *Host Interface Pins for SPI and I^2C.*

The selection between I^2C and SPI interfaces is performed at start-up using the CS_B_IF0 pin. This pin must be held at the required level for 550 ms after the de-assertion of the RST_B pin, after which time it can be released and used as a the SPI chip-select signal if SPI mode is selected at reset.

TABLE 7-1: SERIAL INTERFACE SELECTION

CS_B_IF0	Serial Interface
0	I^2C
1	SPI

Both interfaces use a seven-bit address field. The device register space is divided into multiple pages of 127 registers each. Page 0 has addresses 0x000 to 0x07E, Page 1 has addresses 0x080 to 0x0FE and so on. The host selects between the pages by writing to the Page Select register (address 0x7F on each page). For example, writing a 0x03 to the page select register makes registers 0x180 to 0x1FE available through the host interface.

The device registers are divided into direct-access and indirect-access (mailbox) registers. The direct-access registers (Pages 0 to 9) are accessed simply by reading or writing specific memory locations. The mailbox access registers (Pages 10+) have shared address space. For example, Page 10 is shared among all input references. To initialize one of the input references, the user needs to specify which input reference needs to be updated (ref_mb_mask register) and then read the mailbox by setting the rd bit high in ref_mb_sem (reference mailbox semaphore). The user then changes register values in the mailbox as needed and then issues the write command by setting the wr bit high in ref_mb_sem. The device then transfers values from the mailbox to internal registers for that reference. The behavior of other mailbox register pages is similar.

7.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the device's registers.

The SPI interface operates in half-duplex processor mode. During the data-out portion of a read cycle, the **SI**_SDA pin is ignored by the device. During a write cycle, the driver on the **SO**_IF1 pin remains disabled. The SPI interface is compatible with both 4-pin and 3-pin SPI controllers. In 3-pin configuration, when externally connecting SI_SDA and **SO**_IF1, a 1 kΩ series resistor is recommended on the **SO**_IF1 pin to limit current during bus turnaround and possible contention due to programming errors. The **SO**_IF1 driver is enabled on the rising edge of **SCK**_SCL that latches the final read address bit and disabled on the rising edge of **CS_B**_IF0.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission and Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of **SCK**_SCL pin when the **CS_B**_IF0 pin is active. If the **SCK**_SCL pin is low during **CS_B**_IF0 activation, then MSb-first timing is selected. If the **SCK**_SCL pin is high during **CS_B**_IF0 activation, then LSb-first timing is assumed.

The SPI port expects 1 bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the **CS_B**_IF0 pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal **CS_B**_IF0 low after a read or a write. The register address is automatically incremented after each data byte is read or written.

Functional waveforms for the LSb-first and MSb-first modes, and burst mode are shown in Figure 7-2, Figure 7-3, and Figure 7-4. Timing characteristics are shown in Table 9-15, Figure 9-5, and Figure 9-6.

7.1.1 LEAST SIGNIFICANT BIT (LSb) FIRST TRANSMISSION MODE

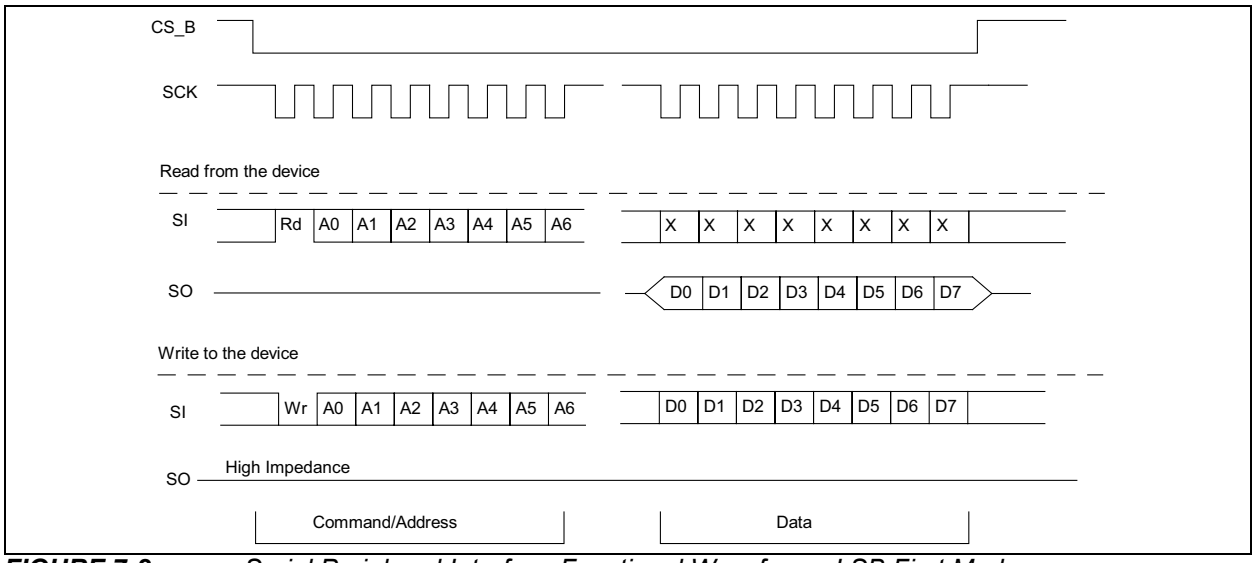


FIGURE 7-2: *Serial Peripheral Interface Functional Waveform - LSB First Mode.*

7.1.2 MOST SIGNIFICANT BIT (MSb) FIRST TRANSMISSION MODE

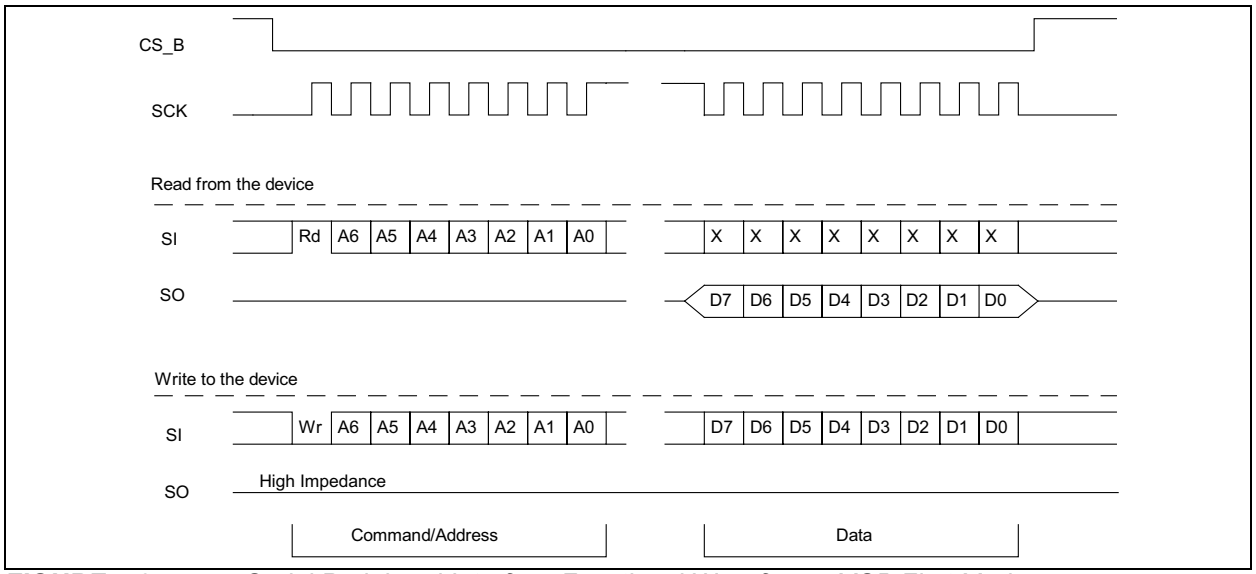


FIGURE 7-3: *Serial Peripheral Interface Functional Waveform - MSB First Mode.*

7.1.3 SPI BURST MODE OPERATION

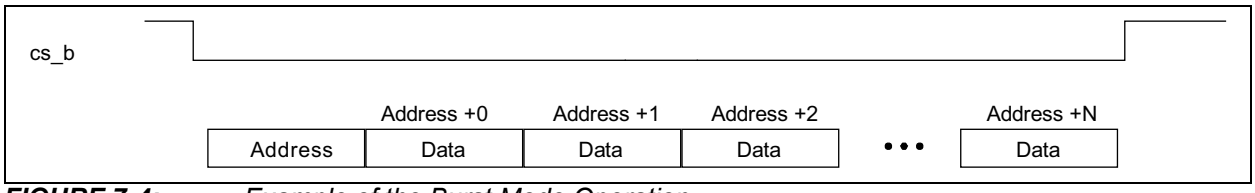


FIGURE 7-4: *Example of the Burst Mode Operation.*

7.1.4 INTERFACING TO A 1.8V, 2.5V, OR 3.3V SPI BUS

The supply voltage for the SPI interface pins is the VDDIO pin. This pin should be wired to the desired supply voltage for the SPI interface. Note that VDDIO is also the supply pin for the GPIO0 through GPIO4 pins.

7.2 I²C Interface

The I²C interface supports version 2.1 (January 2000) of the Philips I²C bus specification. The device cannot control the bus, it can only respond to an external controller. The device uses 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) modes. Burst mode is supported in both standard and fast modes.

Data is transferred MSb first and occurs in 1 byte blocks. As shown in Figure 7-5, a write command consists of a 7-bit device address, a R/W indicator bit, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

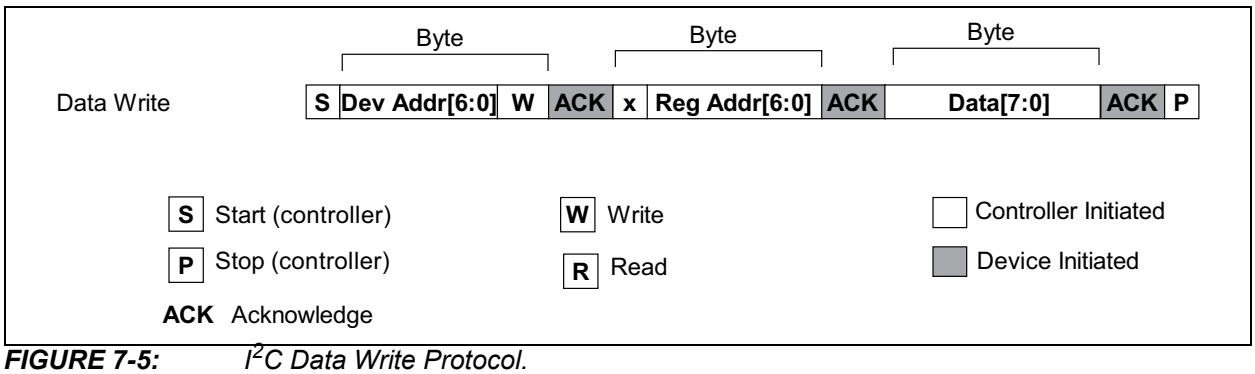


FIGURE 7-5: *I²C Data Write Protocol.*

A read is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in following figure.

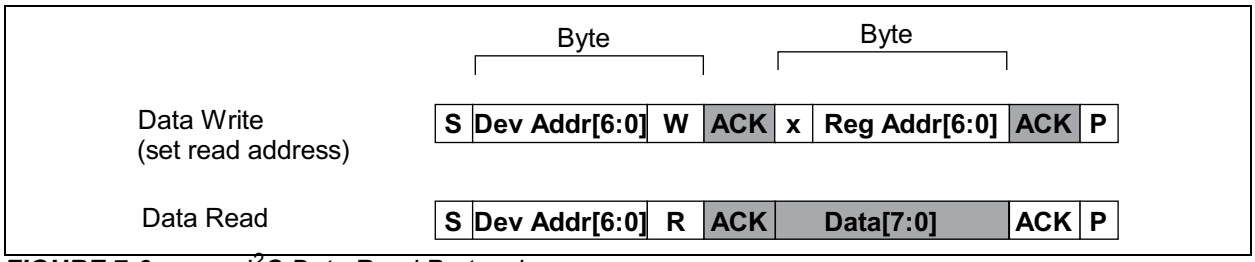


FIGURE 7-6: *I²C Data Read Protocol.*

The 7-bit device address has 6 fixed address bits plus the least-significant address set by the SO_**IF1** pin at reset. This allows multiple devices to share the same I²C bus. The address configuration is shown in following figure.

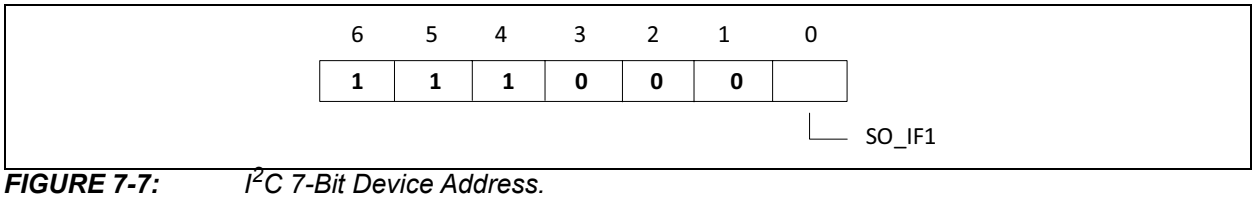


FIGURE 7-7: *I²C 7-Bit Device Address.*

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 7-8 (write) and Figure 7-6 (read). The first data byte is written/read to/from the specified address, and subsequent data bytes are written/read using an automatically incremented address. The maximum auto increment address of a burst operation is 0x7F and operations beyond this limit are ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

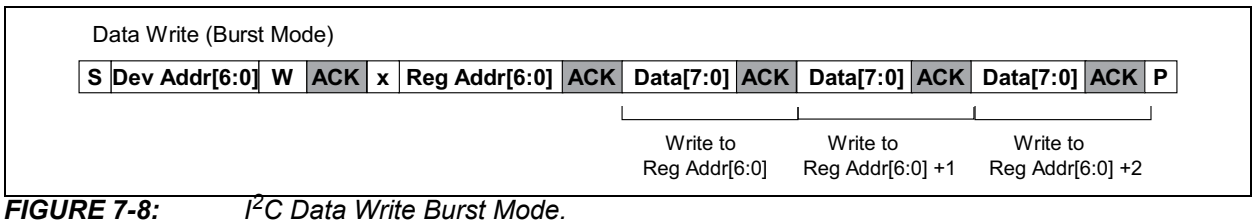


FIGURE 7-8: *I^2C Data Write Burst Mode.*

8.0 REGISTER MAP

The device is controlled by accessing registers through the serial interface (SPI or I^2C). The device can be configured to operate in unmanaged (automatic) mode, which minimizes its interaction with system software, or it can operate in a managed (manual) mode where the system software controls operation of the device.

The register map is big-endian format.

A simple way to generate configuration for the device is to use the evaluation software (GUI), which can operate connected to an evaluation board or standalone (without an evaluation board). Through the GUI, the user can quickly set all required parameters and save the configuration to a text file which can then be used by the system processor to load and configure the device.

8.1 Multi-Byte Register Values

The device register map is based on 8-bit register access. Therefore, register values that require more than 8 bits are spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 8-1. When writing a multi-byte value, the value is latched when the LSB is written.

In this example the central_freq_offset register has the value 0x046AAAAB, a 32-bit value spread over four 8-bit registers. The MSB is contained in address 0x000B and the LSB in 0x000E. When reading or writing this multi-byte value, the MSB must be accessed first, then the middle bytes, and the LSB last.

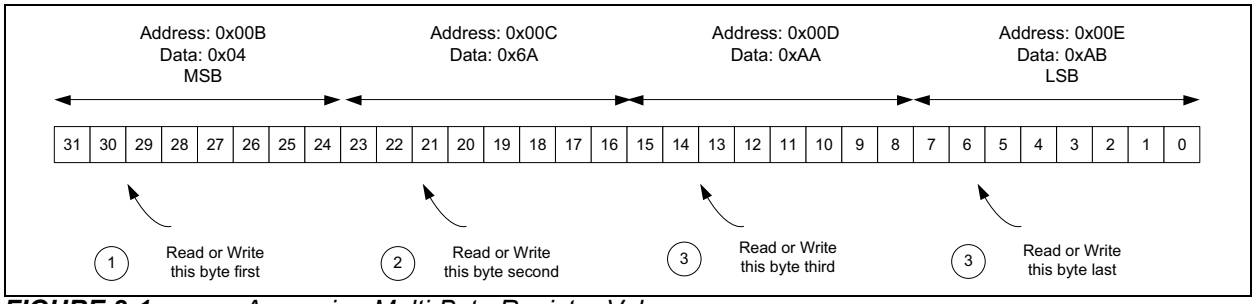


FIGURE 8-1: *Accessing Multi-Byte Register Value.*

8.1.1 TIME BETWEEN TWO WRITE ACCESSES TO THE SAME REGISTER

The user should not write to the same register faster than 25 ms. Some registers that control state machine or system clock operation require larger delays after writing in order for the state and configurations to be updated. One example is the register central_freq_offset requires much longer time, but this register should not be changed dynamically. Other examples include those related to precise input-output alignment.

The dpll_df_offset_x registers can be written with a minimum wait time of 600 microseconds between write accesses to the same register to support NCO operation.

For the page selection register (at addresses 0x07F, 0x0FF, 0x17F, etc.), there is no waiting time required between write accesses.

8.1.2 TIME AFTER CHANGE TO STATE MACHINE OR SYSTEM-CLOCK RELATED CONFIGURATION

The user should wait for appropriate time after configuration of state machine or system clock related configuration prior to updating other registers. One example is the register central_freq_offset. Other examples include those related to precise input-output alignment.

8.2 Sticky Read

Some status registers are defined as Sticky Read (StickyR, Type=S in the tables below). The procedure for accessing these registers is:

- write 0x01 to sticky_lock register at address 0x180
- clear sticky registers by writing 0x00 to them
- write 0x00 to sticky_lock at address 0x180
- wait for 25 ms
- read the status register(s)

8.3 Register Map List Summary

The following tables provides a summary of the registers available for status and configuration of the device.

Note that devices do not respond to mailbox register accesses after power-up or reset until system software configures the system clock APLL registers and sets master_clk_cfg_ready to 1 and the device responds by setting the **ready** bit in the info register.

TABLE 8-1: TOP-LEVEL REGISTER MAP

Address	Register Map Page
0x000	Register Map Page 0, General
0x080	Register Map Page 1, GPIOs
0x100	Register Map Page 2, Status
0x180	Register Map Page 3, Sticky
0x200	Register Map Page 4, Ref
0x280	Register Map Page 5, DPLL
0x300	Register Map Page 6, DPLL Data
0x480	Register Map Page 9, Synth and Output
0x500	Register Map Page 10, Ref Mailbox
0x600	Register Map Page 12, DPLL Mailbox
0x680	Register Map Page 13, Synth Mailbox
0x700	Register Map Page 14, Output Mailbox

Register Map Page 0, General

Address	Name	Default	Type
0x0000	info	0x21	R
0x0001:0x0002	id	see description	R
0x0003	revision	0x03	R
0x0005:0x0006	fw_ver	contact Microchip	R
0x0007:0x000A	custom_config_ver	0xFFFFFFFF	R/W
0x000B:0x000E	central_freq_offset	0x02769140	R/W
0x0018	reset_status	0x00	R/W
0x0019:0x001A	gpio_at_startup	0x0000	R
0x0021	xo_amp_sel	0x00	R/W
0x0022	xo_osci_sel	0x00	R/W
0x0023	xo_osco_sel	0x00	R/W
0x0025	xo_tst_ctrl	0x00	R/W
0x0026	xo_config	0x00	R/W
0x0029	sys_apll_source_config	0x00	R/W
0x002A	sys_apll_primary_div_int	0x34	R/W

Register Map Page 0, General (Continued)

Address	Name	Default	Type
0x002B:0x002F	sys_apll_primary_div_frac	0x0000000000	R/W
0x0030	sys_apll_secondary_div	0x02	R/W
0x0032	master_clk_status	0x00	R
0x0033	master_clk_cfg_ready	0x00	R/W
0x003E	i2c_device_addr	0x38	R
0x0046:0x004A	master_clk_ofst	0x0000000000	R/W
0x0050:0x006F	available for customer use	0x00	R/W
0x007E	uport	0x00	R/W
0x007F	page_sel	0x00	R/W

Register Map Page 1, GPIOs

Address	Name	Default	Type
0x0080	gpio_irq_config	0x00	R/W
0x0082	ref_mon_th_mask_0P	0x00	R/W
0x0083	ref_mon_th_mask_0N	0x00	R/W
0x0084	ref_mon_th_mask_1P	0x00	R/W
0x0085	ref_mon_th_mask_1N	0x00	R/W
0x0086	ref_mon_th_mask_2P	0x00	R/W
0x0087	ref_mon_th_mask_2N	0x00	R/W
0x0088	ref_mon_th_mask_3P	0x00	R/W
0x0089	ref_mon_th_mask_3N	0x00	R/W
0x0090	dpll_mon_th_mask_0	0x00	R/W
0x0091	dpll_mon_th_mask_1	0x00	R/W
0x00B2	ref_mon_tl_mask_0P	0x00	R/W
0x00B3	ref_mon_tl_mask_0N	0x00	R/W
0x00B4	ref_mon_tl_mask_1P	0x00	R/W
0x00B5	ref_mon_tl_mask_1N	0x00	R/W
0x00B6	ref_mon_tl_mask_2P	0x00	R/W
0x00B7	ref_mon_tl_mask_2N	0x00	R/W
0x00B8	ref_mon_tl_mask_3P	0x00	R/W
0x00B9	ref_mon_tl_mask_3N	0x00	R/W
0x00C0	dpll_mon_tl_mask_0	0x00	R/W
0x00C1	dpll_mon_tl_mask_1	0x00	R/W
0x00E0:0x00E1	gpio_select_0	0x0000	R/W
0x00E2	gpio_config_0	0x00	R/W
0x00E3:0x00E4	gpio_select_1	0x0000	R/W
0x00E5	gpio_config_1	0x00	R/W
0x00E6:0x00E7	gpio_select_2	0x0000	R/W
0x00E8	gpio_config_2	0x00	R/W
0x00E9:0x00EA	gpio_select_3	0x0000	R/W
0x00EB	gpio_config_3	0x00	R/W
0x00EC:0x00ED	gpio_select_4	0x0000	R/W
0x00EE	gpio_config_4	0x00	R/W
0x00EF	gpio_out_4_0	0x00	R/W

Register Map Page 1, GPIOs (Continued)

Address	Name	Default	Type
0x00F0	gpo_out_7_0	0x00	R/W
0x00F1	gpo_out_15_8	0x00	R/W
0x00F2	gpo_out_19_16	0x00	R/W
0x00F3	gpio_freeze_4_0	0x00	R/W
0x00F4	gpi_freeze_7_0	0x00	R/W
0x00FE	uport	0x00	R/W
0x00FF	page_sel	0x00	R/W

Register Map Page 2, Status

Address	Name	Default	Type
0x0102	ref_mon_status_0P	0x00	R
0x0103	ref_mon_status_0N	0x00	R
0x0104	ref_mon_status_1P	0x00	R
0x0105	ref_mon_status_1N	0x00	R
0x0106	ref_mon_status_2P	0x00	R
0x0107	ref_mon_status_2N	0x00	R
0x0108	ref_mon_status_3P	0x00	R
0x0109	ref_mon_status_3N	0x00	R
0x0110	dpll_mon_status_0	0x00	R
0x0111	dpll_mon_status_1	0x00	R
0x0130	dpll_state_refsel_status_0	0x00	R
0x0131	dpll_state_refsel_status_1	0x00	R
0x0140	gpio_in_status	0x00	R
0x0141	gpi_in_status_7_0	0x00	R
0x0144:0x0147	ref_freq_0P	0x00000000	R
0x0148:0x014B	ref_freq_0N	0x00000000	R
0x014C:0x014F	ref_freq_1P	0x00000000	R
0x0150:0x0153	ref_freq_1N	0x00000000	R
0x0154:0x0157	ref_freq_2P	0x00000000	R
0x0158:0x015B	ref_freq_2N	0x00000000	R
0x015C:0x015F	ref_freq_3P	0x00000000	R
0x0160:0x0163	ref_freq_3N	0x00000000	R
0x017E	uport	0x00	R/W
0x017F	page_sel	0x00	R/W

Register Map Page 3, Sticky

Address	Name	Default	Type
0x0180	sticky_lock	0x00	R/W
0x0182	ref_mon_th_sticky_0P	0x00	S
0x0183	ref_mon_th_sticky_0N	0x00	S
0x0184	ref_mon_th_sticky_1P	0x00	S
0x0185	ref_mon_th_sticky_1N	0x00	S
0x0186	ref_mon_th_sticky_2P	0x00	S

Register Map Page 3, Sticky (Continued)

Address	Name	Default	Type
0x0187	ref_mon_th_sticky_2N	0x00	S
0x0188	ref_mon_th_sticky_3P	0x00	S
0x0189	ref_mon_th_sticky_3N	0x00	S
0x018C	ref_dpll_freq_sticky_3_0	0x00	S
0x018E	dpll_meas_ref_sticky_3_0	0x00	S
0x0190	dpll_mon_th_sticky_0	0x00	S
0x0191	dpll_mon_th_sticky_1	0x00	S
0x01B2	ref_mon_tl_sticky_0P	0x00	S
0x01B3	ref_mon_tl_sticky_0N	0x00	S
0x01B4	ref_mon_tl_sticky_1P	0x00	S
0x01B5	ref_mon_tl_sticky_1N	0x00	S
0x01B6	ref_mon_tl_sticky_2P	0x00	S
0x01B7	ref_mon_tl_sticky_2N	0x00	S
0x01B8	ref_mon_tl_sticky_3P	0x00	S
0x01B9	ref_mon_tl_sticky_3N	0x00	S
0x01C0	dpll_mon_tl_sticky_0	0x00	S
0x01C1	dpll_mon_tl_sticky_1	0x00	S
0x01E0	dpll_fastlock_phase_sticky	0x00	S
0x01E1	dpll_fastlock_freq_sticky	0x00	S
0x01E4	dpll_tie_wr_sticky	0x00	S
0x01E8	ref_irq_active_3_0	0x00	S
0x01EB	dpll_irq_active	0x00	S
0x01EC	synth_irq_active	0x00	S
0x01ED	output_irq_active_7_0	0x00	S
0x01EE	output_irq_active_9_8	0x00	S
0x01EF	dpll_ns_rollover_irq_active	0x00	S
0x01FE	uport	0x00	R/W
0x01FF	page_sel	0x00	R/W

Register Map Page 4, Ref

Address	Name	Default	Type
0x0200	ref_los_3_0	0x00	R/W
0x020F	ref_phase_err_read_rqst	0x00	R/W
0x021C	ref_freq_meas_ctrl	0x00	R/W
0x021D	ref_freq_meas_mask_3_0	0x00	R/W
0x021F	dpll_meas_ref_freq_ctrl	0x00	R/W
0x0220:0x0225	ref_phase_0P	0x000000000000	R
0x0226:0x022B	ref_phase_0N	0x000000000000	R
0x022C:0x0231	ref_phase_1P	0x000000000000	R
0x0232:0x0237	ref_phase_1N	0x000000000000	R
0x0238:0x023D	ref_phase_2P	0x000000000000	R
0x023E:0x0243	ref_phase_2N	0x000000000000	R
0x0244:0x0249	ref_phase_3P	0x000000000000	R
0x024A:0x024F	ref_phase_3N	0x000000000000	R

Register Map Page 4, Ref (Continued)

Address	Name	Default	Type
0x025C:0x0261	dpll_phase_0	0x000000000000	R
0x0262:0x0267	dpll_phase_1	0x000000000000	R
0x027E	uport	0x00	R/W
0x027F	page_sel	0x00	R/W

Register Map Page 5, DPLL

Address	Name	Default	Type
0x0283	dpll_enable	0x05	R/W
0x0284	dpll_mode_refsel_0	0x00	R/W
0x0285	dpll_ctrl_0	0x6C	R/W
0x0286	dpll_cmd_0	0x00	R/W
0x0288	dpll_mode_refsel_1	0x00	R/W
0x0289	dpll_ctrl_1	0x0C	R/W
0x028A	dpll_cmd_1	0x00	R/W
0x02A4	ext_fb_ctrl	0x00	R/W
0x02A5	ext_fb_sel	0x00	R/W
0x02A6	dpll_df_read_all_mask	0x00	R/W
0x02A7	dpll_df_read_all	0x00	R/W
0x02A8	dpll_df_read_0	0x00	R/W
0x02A9	dpll_df_read_1	0x00	R/W
0x02B0	dpll_tie_ctrl	0x00	R/W
0x02B1	dpll_tie_ctrl_mask	0x00	R/W
0x02D0	dpll_meas_ctrl	0x00	R/W
0x02D1	dpll_meas_idx	0x00	R/W
0x02D2	dpll_meas_ref_edge_3_0	0x00	R/W
0x02D4	dpll_phase_err_read_mask	0x00	R/W
0x02D5:0x02DA	dpll_phase_err_data_0	0x000000000000	R
0x02DB:0x02E0	dpll_phase_err_data_1	0x000000000000	R
0x02FE	uport	0x00	R/W
0x02FF	page_sel	0x00	R/W

Register Map Page 6, DPLL Data

Address	Name	Default	Type
0x0300:0x0305	dpll_df_offset_0	0x000000000000	R/W
0x030C:0x0311	dpll_tie_data_0	0x000000000000	R/W
0x0320:0x0325	dpll_df_offset_1	0x000000000000	R/W
0x032C:0x0331	dpll_tie_data_1	0x000000000000	R/W
0x037E	uport	0x00	R/W
0x037F	page_sel	0x00	R/W

Register Map Page 9, Synth and Output

Address	Name	Default	Type
0x0480	synth_ctrl_0	0x00	R/W
0x0481	synth_ctrl_1	0x00	R/W
0x0482	synth_ctrl_2	0x00	R/W
0x0483	synth_ctrl_3	0x00	R/W
0x0484	synth_ctrl_4	0x00	R/W
0x0485:0x0489	synth_df_offset_manual_0	0x0000000000	R/W
0x048A:0x048E	synth_df_offset_manual_1	0x0000000000	R/W
0x048F:0x0493	synth_df_offset_manual_2	0x0000000000	R/W
0x0494:0x0498	synth_df_offset_manual_3	0x0000000000	R/W
0x0499:0x049D	synth_df_offset_manual_4	0x0000000000	R/W
0x04A8	output_ctrl_0	0x01	R/W
0x04A9	output_ctrl_1	0x01	R/W
0x04AA	output_ctrl_2	0x01	R/W
0x04AB	output_ctrl_3	0x01	R/W
0x04AC	output_ctrl_4	0x01	R/W
0x04AD	output_ctrl_5	0x01	R/W
0x04AE	output_ctrl_6	0x01	R/W
0x04AF	output_ctrl_7	0x01	R/W
0x04B0	output_ctrl_8	0x01	R/W
0x04B1	output_ctrl_9	0x01	R/W
0x04B8	output_phase_step_ctrl	0x00	R/W
0x04B9	output_phase_step_number	0x01	R/W
0x04BA:0x04BB	output_phase_step_mask	0x0000	R/W
0x04BC:0x04BF	output_phase_step_data	0x00000000	R/W
0x04FE	uport	0x00	R/W
0x04FF	page_sel	0x00	R/W

Register Map Page 10, Ref Mailbox

Address	Name	Default	Type
0x0502:0x0503	ref_mb_mask	0x0001	R/W
0x0504	ref_mb_sem	0x00	R/W
0x0505:0x0506	ref_freq_base	0x61A8	R/W
0x0507:0x0508	ref_freq_mult	0x03E8	R/W
0x0509:0x050A	ref_ratio_m	0x0001	R/W
0x050B:0x050C	ref_ratio_n	0x0001	R/W
0x050D	ref_config	0x01	R/W
0x050F	ref_scm	0x05	R/W
0x0510:0x0513	ref_scm_fine	0x00000000	R/W
0x0514	ref_cfm	0x05	R/W
0x0516:0x0517	ref_gst_disqual	0x0005	R/W
0x0518:0x0519	ref_gst_qual	0x0014	R/W
0x051A	ref_meas_freq_period	0x01	R/W
0x051B	ref_pfm_ctrl	0x00	R/W
0x051C:0x051D	ref_pfm_disqualify	0xB3B0	R/W
0x051E:0x051F	ref_pfm_qualify	0x9C40	R/W
0x0520:0x0521	ref_pfm_period	0x0000	R/W
0x0522	ref_pfm_filter_limit	0x28	R/W
0x0528:0x052B	ref_phase_offset_compensation	0x00000000	R/W
0x052E	ref_sync_ctrl	0x00	R/W
0x052F	ref_sync_misc	0x00	R/W
0x0534:0x0535	ref_gpi_select	0x0000	R/W
0x0536	ref_gpi_config	0x00	R/W
0x057E	uport	0x00	R/W
0x057F	page_sel	0x00	R/W

Register Map Page 12, DPLL Mailbox

Address	Name	Default	Type
0x0602:0x0603	dpll_mb_mask	0x0001	R/W
0x0604	dpll_mb_sem	0x00	R/W
0x0605	dpll_config	0x01	R/W
0x0609	dpll_fast_lock_ctrl	0x01	R/W
0x060A:0x060B	dpll_fast_lock_ideal_time	0x0000	R/W
0x060C:0x060D	dpll_fast_lock_phase_rate	0x07D0	R/W
0x060E:0x060F	dpll_fast_lock_fcl	0x0000	R/W
0x0610:0x0611	dpll_fast_lock_phase_err	0x0100	R/W
0x0612	dpll_fast_lock_freq_err	0x04	R/W
0x0620	dpll_bw_fixed	0x00	R/W
0x0622:0x0623	dpll_psi	0x0000	R/W
0x0626	dpll_damping	0x00	R/W
0x0627	dpll_duration_good	0x09	R/W
0x0628:0x062B	dpll_phase_good	0x02255100	R/W
0x062C:0x062F	dpll_phase_bad	0x02255100	R/W

Register Map Page 12, DPLL Mailbox (Continued)

Address	Name	Default	Type
0x0645:0x0646	dpll_range	0x0BB8	R/W
0x0648:0x064C	dpll_df_offset_manual	0x0000000000	R/W
0x064D:0x064E	dpll_tie_wr_thresh	0x0002	R/W
0x064F	dpll_lock_delay	0x00	R/W
0x0650	dpll_ref_sw_mask	0x08	R/W
0x0652	dpll_ref_prio_0	0x10	R/W
0x0653	dpll_ref_prio_1	0x32	R/W
0x0654	dpll_ref_prio_2	0x54	R/W
0x0655	dpll_ref_prio_3	0x76	R/W
0x0660	dpll_ref_ho_mask	0x17	R/W
0x0668	dpll_fp_first_realign	0x7F	R/W
0x0669	dpll_fp_realign_intvl	0x00	R/W
0x066A:0x066B	dpll_fp_lock_thresh	0x0000	R/W
0x066C	dpll_fp_sync_mask	0xFF	R/W
0x067E	uport	0x00	R/W
0x067F	page_sel	0x00	R/W

Register Map Page 13, Synth Mailbox

Address	Name	Default	Type
0x0682:0x0683	synth_mb_mask	0x0001	R/W
0x0684	synth_mb_sem	0x00	R/W
0x0686:0x0687	synth_freq_base	0x0001	R/W
0x0688:0x068B	synth_freq_mult	0x12A05F20	R/W
0x068C:0x068D	synth_freq_m	0x0001	R/W
0x068E:0x068F	synth_freq_n	0x0001	R/W
0x0690:0x0691	synth_phase_compensation	0x0000	R/W
0x0692	synth_align_compensation	0x00	R/W
0x0694	synth_spread_spectrum_cfg	0x00	R/W
0x0695:0x0696	synth_spread_spectrum_rate	0x0000	R/W
0x0697	synth_spread_spectrum_spread	0x00	R/W
0x06FE	uport	0x00	R/W
0x06FF	page_sel	0x00	R/W

Register Map Page 14, Output Mailbox

Address	Name	Default	Type
0x0702:0x0703	output_mb_mask	0x0001	R/W
0x0704	output_mb_sem	0x00	R/W
0x0705	output_mode	0x00	R/W
0x0706	output_driver_level	0x52	R/W
0x0707:0x0708	output_driver_config	0x0000	R/W
0x070C:0x070F	output_div	0x00000002	R/W
0x0710:0x0713	output_width	0x00000002	R/W
0x0714:0x0717	output_esync_period	0x00000002	R/W

Register Map Page 14, Output Mailbox (Continued)

Address	Name	Default	Type
0x0718:0x071B	output_esync_width	0x00000002	R/W
0x0720:0x0723	output_phase_compensation	0x00000000	R/W
0x0724	output_gpo_en	0x00	R/W
0x0725:0x0726	output_gpo_select_out_p	0x0000	R/W
0x0727	output_gpo_config_out_p	0x01	R/W
0x0728:0x0729	output_gpo_select_out_n	0x0000	R/W
0x072A	output_gpo_config_out_n	0x01	R/W
0x077E	uport	0x00	R/W
0x077F	page_sel	0x00	R/W

REGISTER LIST PAGE 0, GENERAL

Address:	0x0000	
Name:	info	
Default:	0x21	
Type:	R	
Bit Field	**Function Name**	**Description**
7	ready	The device sets this status bit after the APLL (and crystal driver if in use) have been successfully configured and the APLL is locked. This bit indicates that the device is fully ready and mailbox registers can be read and written.
6:0	reserved	—

Address:	0x0001:0x0002	
Name:	id	
Default:	see below	
Type:	R	
Bit Field	**Function Name**	**Description**
15:0	—	Chip identification number. ZL30272 = 0x8CC8 ZL30273 = 0x0CC9 ZL30274 = 0x0CCA

Address:	0x0003	
Name:	revision	
Default:	0x03	
Type:	R	
Bit Field	**Function Name**	**Description**
15:0	—	Chip revision number. 0x02 = Revision B 0x03 = Revision C

Address:	0x0005:0x0006	
Name:	fw_ver	
Default:	contact Microchip	
Type:	R	
Bit Field	**Function Name**	**Description**
15	fw_dirty	Firmware dirty indicator. This bit is set when the firmware is built from source code that has not been checked-in to the firmware repository. This bit should never be set in released firmware.
15:0	—	Firmware revision number. This field indicates the firmware revision of the source code used to build this image.

Address:	0x0007:0x000A	
Name:	custom_config_ver	
Default:	0xFFFFFFFF	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	This register is intended (but not limited) to be used as configuration version number. Up to 7 custom register configurations can be programmed into the device.

Address:	0x000B:0x000E	
Name:	central_freq_offset	
Default:	0x02769140	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	2's complement binary value of these bits represent central frequency offset for the device. This value indicates the fractional frequency offset of the actual VCO frequency vs. 12.0 GHz. Expressed in steps of ±2^–32 of nominal setting. The actual VCO frequency (f_vco) is the product of the XO frequency, the primary divider specified in sys_apll_primary_div_int (0x002A) and sys_apll_primary_div_frac (0x002B to 0x002F), and the secondary divider specified in sys_apll_secondary_div (0x0030). The nominal VCO frequency (f_nom) is always 12.0 GHz. The value to be programmed in this register should satisfy the following relationships: 1 + X * 2^(–32) = f_nom / f_vco, if f_vco < f_nom X * 2^(–32) = f_nom / f_vco, if f_vco > f_nom. Equivalently, if X is treated as a signed number, the following equation always holds: 1 + X * 2^(–32) = f_nom / f_vco. When the VCO frequency is lower than the 12.0 GHz nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1: if VCO frequency offset is –0.1% (f_vco = 11.988 GHz); X = (12.0/11.988 – 1)*2^32 = 4299267 = 0x00419A03 Example 2: if XO is 49.152 MHz, the primary divider is 244 and the secondary divider is 1 (f_vco = 11.993088 GHz); X = (12.0/11.993088 – 1)*2^32 = 2475327 = 0x0025C53F Example 3: if VCO inaccuracy is +0.1% (f_vco = 12.012 GHz); X = (12/12.012)*2^32 = 4290676619 = 0xFFBE878B Note: central_freq_offset should not be programmed to exceed ±1% because the APLL VCO range is 12 GHz±1%.

Address:	0x0018	
Name:	reset_status	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	reset	This field can be used to detect when a reset has occurred. During reset, this bit is cleared. The host controller can write a one to this bit, and then periodically read the register to check for a reset.

Address:	0x0019:0x001A	
Name:	gpio_at_startup	
Default:	0x0000	
Type:	R	
Bit Field	**Function Name**	**Description**
15:5	reserved	—
4	gpio4	The value of GPIO4 latched at device reset.
3	gpio3	The value of GPIO3 latched at device reset.
2	gpio2	The value of GPIO2 latched at device reset.
1	gpio1	The value of GPIO1 latched at device reset.
0	gpio0	The value of GPIO0 latched at device reset.

Address:	0x0021	
Name:	xo_amp_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	dis_hyst	Disables the normal hysteresis circuits of the OSCB pin receiver
3	en_fdbk	Disables hysteresis and connects a 250 kΩ resistor to 1.25V to the OSCB pin for DC-bias. This allows AC-coupling a clock signal. Enabling this bit is not recommended for rail-to-rail CMOS signals ≥1.8V. This feature and external AC-coupling are only for signal amplitudes <1.8V.
2:0	xtal_drive_level	Controls the XTAL driver strength on OSCO pin and selects the external XO on the OSB pin. 000 - disables the XTAL driver and selects the signal on the OSCB pin. 001 – drive 1 010 – drive 2 011 – drive 3 100 – driver 4--recommended 101 – drive 5 110 – drive 6 111 – drive 7

Address:	0x0022	
Name:	xo_osci_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Affects the capacitive loading of the OSCI pin. Used to select the total XTAL loading (which affects the oscillation frequency). Resolution is 0.25 pF and range is 0 pF to 11.75 pF.

Address:	0x0023	
Name:	xo_osco_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Affects the capacitive loading of the OSCO pin. Used to select the total XTAL loading (which affects the oscillation frequency), Resolution is 0.25 pF and range is 0 pF to 11.75 pF.

Address:	0x0025	
Name:	xo_tst_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	—	The bits in this register control the crystal driver circuit series resistance for OSCO. Each bit controls a resistor, and the resistors are arranged in parallel. All-ones enables 72 kΩ. 0 = Enable 562.6Ω resistor
6	—	0 = Enable 1.125 kΩ resistor
5	—	0 = Enable 2.25 kΩ resistor
4	—	0 = Enable 4.5 kΩ resistor
3	—	0 = Enable 9 kΩ resistor
2	—	0 = Enable 18 kΩ resistor
1	—	0 = Enable 36 kΩ resistor
0	—	0 = Enable 72 kΩ resistor

Address:	0x0026	
Name:	xo_config	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:6	reserved	—
5	xtal_en	0 = Disable crystal oscillator. The XO clock comes from an external XO connected to the OSCB pin. 1 = Enable crystal oscillator. (Must also set xtal_drive_level > 1 at in xo_amp_sel register (0x0021).
4:2	reserved	—
1	simple_doubler_en	Enable the simple crystal doubler. Only appropriate when using a crystal as system clock source. Not for use with an XO. 0 = Disable 1 = Enable
0	passclk	When this bit is set, the XO clock is passed directly to the APLL, bypassing inversion, division selection and the simple doubler. The simple doubler should be disabled in this case.

Address:	0x0029	
Name:	sys_apll_source_config	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6	pfd_gain_boost	When the doubler is disabled, setting this bit minimizes output jitter in most cases. 0 = Disable 1 = Enable
5:4	div	Divide the source clock for the APLL 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8
3	invert	APLL source invert 0 = Not inverted 1 = Inverted
2:0	reserved	—

Address:	0x002A	
Name:	sys_apll_primary_div_int	
Default:	0x34	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	System APLL primary divider (integer part). Range is 16 to 67. If any other value is written to this register, the default value 0x34 (52) is used. The value must be ≥20 if sys_apll_primary_div_frac (0x002B-0x002F) register is non-zero.

Address:	0x002B:0x002F	
Name:	sys_apll_primary_div_frac	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	System APLL primary divider (fractional part). Only 36 bits are used. The 4 most significant bits are ignored.

Address:	0x0030	
Name:	sys_apll_secondary_div	
Default:	0x02	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:6	reserved	—
5:0	div	System APLL secondary divider. Range is 1 to 63. If any other value is written to this register, the divider value is set to 1.

Address:	0x0032	
Name:	master_clk_status	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:4	reserved	—
3	sys_apll_lock	0 = APLL is locked. 1 = APLL lost lock.
2	cfg_invalid	Invalid host system clock info 0 = Valid 1 = Invalid
1:0	state	System clock state: 00 = Not started 01 = Waiting for host config information 10 = In progress 11 = Ready

Address:	0x0033	
Name:	master_clk_cfg_ready	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	ready	0 = System clock configuration is not ready 1 = System clock configuration is ready Whenever changing system clock configuration, set this bit to 0 first, then apply the changes and finally set the bit to 1. The device only latches system clock configuration into hardware on the first 0-to-1 transition of this bit after reset.

Address:	0x003E	
Name:	i2c_device_addr	
Default:	0x38	
Type:	R	
Bit Field	**Function Name**	**Description**
7:0	—	Indicate I^2C device address upper six bits (bit[6:1]) if uPort is configured to I^2C.

Address:	0x0046:0x004A	
Name:	master_clk_ofst	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	System clock offset compensation. This register is intended to be used to compensate for known oscillator aging. The compensation value will affect the following reference monitors: SCM, CFM, and PFM. It also affects reference frequency measurements; see register 0x205 (ref_freq_cmd) for further details. This register does not affect any DPLL operations. This register is a signed value with LSB=2^–48. This register can be programmed with the known change in oscillator frequency. E.g., if the oscillator frequency changes by –5.4 ppb (slows down): master_clk_ofst = –5.4 * 10^–9 * 2^48 master_clk_ofst = 0xFFFFE8CEA4

Address:	0x007E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x007F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 1, GPIOs

Address:	0x0080	
Name:	gpio_irq_config	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—

2	high_z	This register should be written before enabling IRQ mode in gpio_config_x. 0 = The device actively drives the GPIO IRQ pin low when the interrupt is inactive. 1 = The device puts the GPIO IRQ pin in high-z mode when the interrupt is inactive.
1	active_high	0 = The GPIO IRQ pin is high when the interrupt is inactive (active-low mode). 1 = The GPIO IRQ pin is high when the interrupt is active (active-high mode).
0	level_trig	0 = The GPIO IRQ pin is in edge-triggered mode. When an interrupt occurs, the device generates a short pulse on the GPIO IRQ pin then return it to the inactive state immediately. Once the interrupt has been acknowledged, new interrupts can be generated. 1 = The GPIO IRQ pin is in level-triggered mode. The GPIO IRQ pin stays low or high (depending on the active_high bit) until the interrupt has been acknowledged. New interrupts cannot be generated until the host has acknowledged the current one by clearing the sticky bits in registers: 0x1E8 (ref_irq_active_3_0) 0x1EB (dpll_irq_active) 0x1EC (synth_irq_active) 0x1ED (output_irq_active_7_0) 0x1EE (output_irq_active_9_8) For both modes, interrupts are generated whenever the status changes (0-to-1 or 1-to-0).

ref_mon_th_mask_x

Address:	0x0082	
Name:	ref_mon_th_mask_0P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	0 = REF0P PFM status transitions 0->1 are masked. 1 = REF0P PFM status transitions 0->1 are unmasked. See pfm status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.
3	gst	0 = REF0P GST status transitions 0->1 are masked. 1 = REF0P GST status transitions 0->1 are unmasked. See gst status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.
2	cfm	0 = REF0P CFM status transitions 0->1 are masked. 1 = REF0P CFM status transitions 0->1 are unmasked. See cfm status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.

1	scm	0 = REF0P SCM status transitions 0->1 are masked. 1 = REF0P SCM status transitions 0->1 are unmasked. See scm status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.
0	los	0 = REF0P LOS status transitions 0->1 are masked. 1 = REF0P LOS status transitions 0->1 are unmasked. See los status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.

Address:	0x0083	
Name:	ref_mon_th_mask_0N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x082, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at address 0x082, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at address 0x082, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at address 0x082, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at address 0x082, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x0084	
Name:	ref_mon_th_mask_1P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x082, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at address 0x082, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at address 0x082, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at address 0x082, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at address 0x082, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x0085	
Name:	ref_mon_th_mask_1N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x082, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at address 0x082, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at address 0x082, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at address 0x082, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at address 0x082, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x0086	
Name:	ref_mon_th_mask_2P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x082, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at address 0x082, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at address 0x082, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at address 0x082, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at address 0x082, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x0087	
Name:	ref_mon_th_mask_2N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x082, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at address 0x082, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at address 0x082, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at address 0x082, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at address 0x082, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x0088	
Name:	ref_mon_th_mask_3P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x082, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at address 0x082, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at address 0x082, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at address 0x082, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at address 0x082, bit 0 (ref_mon_th_mask_0P::los).

Address:	0x0089	
Name:	ref_mon_th_mask_3N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x082, bit 4 (ref_mon_th_mask_0P::pfm).
3	gst	See description for register at address 0x082, bit 3 (ref_mon_th_mask_0P::gst).
2	cfm	See description for register at address 0x082, bit 2 (ref_mon_th_mask_0P::cfm).
1	scm	See description for register at address 0x082, bit 1 (ref_mon_th_mask_0P::scm).
0	los	See description for register at address 0x082, bit 0 (ref_mon_th_mask_0P::los).

dpll_mon_th_mask_x

Address:	0x0090	
Name:	dpll_mon_th_mask_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	pslhit	The letters "_th_" in this and other mask register names indicate "transition high", i.e. the 0->1 transition of a status bit. 0 = DPLL0 phase slope limit status transitions 0->1 are masked. 1 = DPLL0 phase slope limit status transitions 0->1 are unmasked. See pslhit status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.
6	reserved	—
5	flhit	0 = DPLL0 pull-in/hold-in range limit status transitions 0->1 are masked. 1 = DPLL0 pull-in/hold-in range limit status transitions 0->1 are unmasked. See flhit status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.
4:3	reserved	—
2	ho_ready	0 = DPLL0 holdover ready status transitions 0->1 are masked. 1 = DPLL0 holdover ready status transitions 0->1 are unmasked. See ho_ready status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.
1	ho	0 = DPLL0 holdover status transitions 0->1 are masked. 1 = DPLL0 holdover status transitions 0->1 are unmasked. See ho status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.
0	lock	0 = DPLL0 lock status transitions 0->1 are masked. 1 = DPLL0 lock status transitions 0->1 are unmasked. See lock status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.

Address:	0x0091	
Name:	dpll_mon_th_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	pslhit	See description for register at address 0x090, bit 7 (dpll_mon_th_mask_0::pslhit).
6	reserved	—
5	flhit	See description for register at address 0x090, bit 5 (dpll_mon_th_mask_0::flhit).
4:3	reserved	—

2	ho_ready	See description for register at address 0x090, bit 2 (dpll_mon_th_mask_0::ho_ready).
1	ho	See description for register at address 0x090, bit 1 (dpll_mon_th_mask_0::ho).
0	lock	See description for register at address 0x090, bit 0 (dpll_mon_th_mask_0::lock).

ref_mon_tl_mask_x

Address:	0x00B2	
Name:	ref_mon_tl_mask_0P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	0 = REF0P PFM status transitions 1->0 are masked. 1 = REF0P PFM status transitions 1->0 are unmasked. A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.
3	gst	0 = REF0P GST status transitions 1->0 are masked. 1 = REF0P GST status transitions 1->0 are unmasked. See gst status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.
2	cfm	0 = REF0P CFM status transitions 1->0 are masked. 1 = REF0P CFM status transitions 1->0 are unmasked. See cfm status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.
1	scm	0 = REF0P SCM status transitions 1->0 are masked. 1 = REF0P SCM status transitions 1->0 are unmasked. See scm status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.
0	los	0 = REF0P LOS status transitions 1->0 are masked. 1 = REF0P LOS status transitions 1->0 are unmasked. See los status bit in 0x102 (ref_mon_status_0P). A GPIO interrupt is generated and register 0x1E8 bit 0 (ref_irq_active_3_0::irq_0P) is set to 1.

Address:	0x00B3	
Name:	ref_mon_tl_mask_0N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x0B2, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at address 0x0B2, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at address 0x0B2, bit 2 (ref_mon_tl_mask_0P::cfm).

1	scm	See description for register at address 0x0B2, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at address 0x0B2, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B4	
Name:	ref_mon_tl_mask_1P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x0B2, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at address 0x0B2, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at address 0x0B2, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at address 0x0B2, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at address 0x0B2, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B5	
Name:	ref_mon_tl_mask_1N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x0B2, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at address 0x0B2, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at address 0x0B2, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at address 0x0B2, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at address 0x0B2, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B6	
Name:	ref_mon_tl_mask_2P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x0B2, bit 4 (ref_mon_tl_mask_0P::pfm).

3	gst	See description for register at address 0x0B2, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at address 0x0B2, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at address 0x0B2, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at address 0x0B2, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B7	
Name:	ref_mon_tl_mask_2N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x0B2, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at address 0x0B2, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at address 0x0B2, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at address 0x0B2, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at address 0x0B2, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B8	
Name:	ref_mon_tl_mask_3P	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x0B2, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at address 0x0B2, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at address 0x0B2, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at address 0x0B2, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at address 0x0B2, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00B9	
Name:	ref_mon_tl_mask_3N	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x0B2, bit 4 (ref_mon_tl_mask_0P::pfm).
3	gst	See description for register at address 0x0B2, bit 3 (ref_mon_tl_mask_0P::gst).
2	cfm	See description for register at address 0x0B2, bit 2 (ref_mon_tl_mask_0P::cfm).
1	scm	See description for register at address 0x0B2, bit 1 (ref_mon_tl_mask_0P::scm).
0	los	See description for register at address 0x0B2, bit 0 (ref_mon_tl_mask_0P::los).

Address:	0x00C0	
Name:	dpll_mon_tl_mask_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	pslhit	The letters "_tl_" in this and other mask register names indicate "transition low", i.e. the 1->0 transition of a status bit. 0 = DPLL0 phase slope limit status transitions 1->0 are masked. 1 = DPLL0 phase slope limit status transitions 1->0 are unmasked. See pslhit status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.
6	reserved	—
5	flhit	0 = DPLL0 pull-in/hold-in range limit status transitions 1->0 are masked. 1 = DPLL0 pull-in/hold-in range limit status transitions 1->0 are unmasked. See flhit status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.
4:3	reserved	—
2	ho_ready	0 = DPLL0 holdover ready status transitions 1->0 are masked. 1 = DPLL0 holdover ready status transitions 1->0 are unmasked. See ho_ready status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.
1	ho	0 = DPLL0 holdover status transitions 1->0 are masked. 1 = DPLL0 holdover status transitions 1->0 are unmasked. See ho status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.

0	lock	0 = DPLL0 lock status transitions 1->0 are masked. 1 = DPLL0 lock status transitions 1->0 are unmasked. See lock status bit in 0x110 (dpll_mon_status_0). A GPIO interrupt is generated and register 0x1EB bit 0 (dpll_irq_active::irq_0) is set to 1.

Address:	0x00C1	
Name:	dpll_mon_tl_mask_1	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	pslhit	See description for register at address 0x0C0, bit 7 (dpll_mon_tl_mask_0::pslhit).
6	reserved	—
5	flhit	See description for register at address 0x0C0, bit 5 (dpll_mon_tl_mask_0::flhit).
4:3	reserved	—
2	ho_ready	See description for register at address 0x0C0, bit 2 (dpll_mon_tl_mask_0::ho_ready).
1	ho	See description for register at address 0x0C0, bit 1 (dpll_mon_tl_mask_0::ho).
0	lock	See description for register at address 0x0C0, bit 0 (dpll_mon_tl_mask_0::lock).

Address:	0x00E0:0x00E1	
Name:	gpio_select_0	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	bit	Note: The fields in this register are only useful when GPIO0 is configured as a Status or Control. This field works with the page and offset field to select a single bit in the host register map. This field selects the bit position of the selected register byte.
11:8	page	This field works with the bit and offset fields to select a single bit in the host register map. This field selects the page.
7	reserved	—
6:0	offset	When GPIO0 is configured as a Status or Control, then this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page.

gpio_config_x

Address:	0x00E2	
Name:	gpio_config_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	This field determines the mode of operation for GPIO0. Register 0x0E0-0x0E1 (gpio_select_0) should be set before writing this register, if the mode being set requires additional configuration. However, the new gpio_select value must refer to an register that is also valid for the old mode because GPIO0 would still be in the old mode before this register is written. Therefore, it is much safer to first set GPIO0 to input or output mode, then change gpio_select_0, and then set GPIO0 to the new mode. 000 = Input The logic value sensed on GPIO0 is reflected in register 0x140, bit 0 (gpio_in_status::gpio0). 001 = Output GPIO0 actively drives the value specified in register 0x0EF, bit 0 (gpio_out::gpio0). 010 = Control Certain device functions can be actively controlled via GPIO0. The device function to be controlled is selected by configuring register gpio_select_0. Whenever a change is detected on GPIO0 or the selected host register bit, then the device ORs together the GPIO and register bit values before applying the corresponding configuration. In this mode, the selected host register bit must satisfy the following requirements: 1) It must be R/W type; 2) It cannot be one of the GPIO control registers (including gpio_irq_config, gpio_select_x, gpio_config_x, gpio_freeze_4_0, gpi_freeze_7_0 and gpi_freeze_9_8); 3) It cannot be one of the mailbox registers. Note: An input reference can be forced into failure (LOS) through GPIO0 using the Control decode (010 above). In this case, gpio_select_0 should be configured for controlling the appropriate bit in ref_los_3_0 (0x200) or ref_los_4 (0x201). 011 = Status The device status can be actively supervised via GPIO0. The device mirrors the host register bit specified in register gpio_select_0, onto GPIO0. Typically, the selected host register bit is a status bit (either R or S type) in this mode. 100 = IRQ No matter how many GPIOs are configured to IRQ mode, only the GPIO that was most recently configured generates interrupts. If the latest GPIO is then configured to other modes, the next latest GPIO becomes active and generate interrupts. GPIO interrupt is disabled only if all the GPIOs are set to non-IRQ modes.

Address:	0x00E3:0x00E4	
Name:	gpio_select_1	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	bit	See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page).
7	reserved	—
6:0	offset	See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset).

Address:	0x00E5	
Name:	gpio_config_1	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl).

Address:	0x00E6:0x00E7	
Name:	gpio_select_2	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	bit	See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page).
7	reserved	—
6:0	offset	See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset).

Address:	0x00E8	
Name:	gpio_config_2	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl).

Address:	0x00E9:0x00EA	
Name:	gpio_select_3	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	bit	See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page).
7	reserved	—
6:0	offset	See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset).

Address:	0x00EB	
Name:	gpio_config_3	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl).

Address:	0x00EC:0x00ED	
Name:	gpio_select_4	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	bit	See description for register at address 0x0E0, bits 14:12 (gpio_select_0::bit).
11:8	page	See description for register at address 0x0E0, bits 11:8 (gpio_select_0::page).
7	reserved	—
6:0	offset	See description for register at address 0x0E1, bits 6:0 (gpio_select_0::offset).

Address:	0x00EE	
Name:	gpio_config_4	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	See description for register at address 0x0E2, bits 2:0 (gpio_config_0::ctrl).

Address:	0x00EF	
Name:	gpio_out_4_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	gpio4	Sets the output value on pin GPIO4. See gpio0 description.
3	gpio3	Sets the output value on pin GPIO3. See gpio0 description.
2	gpio2	Sets the output value on pin GPIO2. See gpio0 description.
1	gpio1	Sets the output value on pin GPIO1. See gpio0 description.
0	gpio0	Sets the output value on pin GPIO0. When the ctrl field of gpio_config_0 is set to 001 = Output then this gpio0 bit specifies the GPIO0 output logic value.

Address:	0x00F0	
Name:	gpo_out_7_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	gpo7	Sets the output value on pin OUT3N. See gpo0 description.
6	gpo6	Sets the output value on pin OUT3P. See gpo0 description.
5	gpo5	Sets the output value on pin OUT2N. See gpo0 description.
4	gpo4	Sets the output value on pin OUT2P. See gpo0 description.
3	gpo3	Sets the output value on pin OUT1N. See gpo0 description.
2	gpo2	Sets the output value on pin OUT1P. See gpo0 description.
1	gpo1	Sets the output value on pin OUT0N. See gpo0 description.
0	gpo0	Sets the output value on pin OUT0P. When the OUT0P pin is configured as a general-purpose output (GPO) and the ctrl field in the corresponding output_gpo_config_out_p or output_gpo_config_out_n mailbox register is set to 001 = Output then this bit specifies the OUT0P output logic value.

Address:	0x00F1	
Name:	gpo_out_15_8	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	gpo15	Sets the output value on pin OUT7N. See gpo0 description.
6	gpo14	Sets the output value on pin OUT7P. See gpo0 description.
5	gpo13	Sets the output value on pin OUT6N. See gpo0 description.
4	gpo12	Sets the output value on pin OUT6P. See gpo0 description.
3	gpo11	Sets the output value on pin OUT5N. See gpo0 description.
2	gpo10	Sets the output value on pin OUT5P. See gpo0 description.
1	gpo9	Sets the output value on pin OUT4N. See gpo0 description.
0	gpo8	Sets the output value on pin OUT4P. See gpo0 description.

Address:	0x00F2	
Name:	gpo_out_19_16	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	reserved	—
3	gpo19	Sets the output value on pin OUT9N. See gpo0 description.
2	gpo18	Sets the output value on pin OUT9P. See gpo0 description.
1	gpo17	Sets the output value on pin OUT8N. See gpo0 description.
0	gpo16	Sets the output value on pin OUT8P. See gpo0 description.

Address:	0x00F3	
Name:	gpio_freeze_4_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	gpio4	See description for gpio0.
3	gpio3	See description for gpio0.
2	gpio2	See description for gpio0.
1	gpio1	See description for gpio0.
0	gpio0	Freeze the value in register 0x140 bit 0 (gpio_in_status_4_0::gpio0) if GPIO0 is configured as input or control mode.

Address:	0x00F4	
Name:	gpi_freeze_7_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	gpi7	REF3N freeze. See description for gpi0.
6	gpi6	REF3P freeze. See description for gpi0.
5	gpi5	REF2N freeze. See description for gpi0.
4	gpi4	REF2P freeze. See description for gpi0.
3	gpi3	REF1N freeze. See description for gpi0.
2	gpi2	REF1P freeze. See description for gpi0.
1	gpi1	REF0N freeze. See description for gpi0.
0	gpi0	REF0P freeze. Freeze the value in register 0x141, bit 0 (gpi_in_status_7_0::gpi0) if REF0P is configured as input or control mode.

Address:	0x00FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x00FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 2, STATUS

Address:	0x0102	
Name:	ref_mon_status_0P	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	0 = No PFM failure on REF0P. 1 = PFM failure on REF0P detected.
3	gst	0 = No GST failure on REF0P. 1 = GST failure on REF0P detected.
2	cfm	0 = No CFM failure on REF0P. 1 = CFM failure on REF0P detected.
1	scm	0 = No SCM failure on REF0P. 1 = SCM failure on REF0P detected. For REF0P frequencies below 8 kHz this bit should be ignored and instead the SCM sticky bits in 0x182 (ref_mon_th_sticky_0P) and 0x1B2 (ref_mon_tl_sticky_0P) should be used to check for changes in SCM status.
0	los	0 = No LOS failure on REF0P. 1 = LOS failure on REF0P detected.

Address:	0x0103	
Name:	ref_mon_status_0N	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x102, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x102, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x102, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x102, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x102, bit 0 (ref_mon_status_0P::los).

Address:	0x0104	
Name:	ref_mon_status_1P	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x102, bit 4 (ref_mon_status_0P::pfm).

3	gst	See description for register at address 0x102, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x102, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x102, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x102, bit 0 (ref_mon_status_0P::los).

Address:	0x0105	
Name:	ref_mon_status_1N	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x102, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x102, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x102, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x102, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x102, bit 0 (ref_mon_status_0P::los).

Address:	0x0106	
Name:	ref_mon_status_2P	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x102, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x102, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x102, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x102, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x102, bit 0 (ref_mon_status_0P::los).

Address:	0x0107	
Name:	ref_mon_status_2N	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x102, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x102, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x102, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x102, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x102, bit 0 (ref_mon_status_0P::los).

Address:	0x0108	
Name:	ref_mon_status_3P	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x102, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x102, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x102, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x102, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x102, bit 0 (ref_mon_status_0P::los).

Address:	0x0109	
Name:	ref_mon_status_3N	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x102, bit 4 (ref_mon_status_0P::pfm).
3	gst	See description for register at address 0x102, bit 3 (ref_mon_status_0P::gst).
2	cfm	See description for register at address 0x102, bit 2 (ref_mon_status_0P::cfm).
1	scm	See description for register at address 0x102, bit 1 (ref_mon_status_0P::scm).
0	los	See description for register at address 0x102, bit 0 (ref_mon_status_0P::los).

dpll_mon_status_x

Address:	0x0110	
Name:	dpll_mon_status_0	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7	pslhit	0 = DPLL0 is below the configured phase slope limit. 1 = DPLL0 has hit the configured phase slope limit.
6	reserved	—
5	flhit	0 = DPLL0 is within the configured pull-in/hold-in range limit. 1 = DPLL0 has hit the specified pull-in/hold-in range limit.
4:3	reserved	—
2	ho_ready	0 = DPLL0 holdover storage delay requirements not met 1 = DPLL0 holdover value has the programmed storage delay applied This bit becomes set in locked state and remains unchanged on transitions to holdover state, forced holdover mode, and NCO mode. This bit is cleared when the DPLL is forced to freerun, upon DPLL change of REF, and upon DPLL exit from holdover. See mailbox register at address 0x663 (dpll_ho_delay) for details on holdover storage delay.
1	ho	0 = DPLL0 is not in holdover. 1 = DPLL0 is in holdover.
0	lock	0 = DPLL0 is not locked. 1 = DPLL0 is locked.

Address:	0x0111	
Name:	dpll_mon_status_1	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7	pslhit	See description for register at address 0x110, bit 7 (dpll_mon_status_0::pslhit).
5	flhit	See description for register at address 0x110, bit 5 (dpll_mon_status_0::flhit).
4:3	reserved	—
2	ho_ready	See description for register at address 0x110, bit 2 (dpll_mon_status_0::ho_ready).
1	ho	See description for register at address 0x110, bit 1 (dpll_mon_status_0::ho).
0	lock	See description for register at address 0x110, bit 0 (dpll_mon_status_0::lock).

dpll_state_refsel_status_x

Address:	0x0130	
Name:	dpll_state_refsel_status_0	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	state	Current state of the DPLL 0 = FREERUN (or mode) 1 = HOLDOVER 2 = FAST_LOCK 3 = ACQUIRING 4 = LOCK
3:0	refsel	Indicates the reference selected by DPLL0. 0=REF0P, 1=REF0N, etc.

Address:	0x0131	
Name:	dpll_state_refsel_status_1	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	state	See description for register at address 0x130, bits 6:4 (dpll_state_refsel_status_0::state).
3:0	refsel	See description for register at address 0x130, bits 3:0 (dpll_state_refsel_status_0::refsel).

Address:	0x0140	
Name:	gpio_in_status	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	gpio4	See description for gpio0.
3	gpio3	See description for gpio0.
2	gpio2	See description for gpio0.
1	gpio1	See description for gpio0.
0	gpio0	Logic value seen on pin GPIO0 if it is configured as input or control mode in the ctrl field of register gpio_config_0.

Address:	0x0141	
Name:	gpi_in_status_7_0	
Default:	0x00	
Type:	R	
Bit Field	**Function Name**	**Description**
7	gpi7	REF3N status. See description for gpi0.
6	gpi6	REF3P status. See description for gpi0.
5	gpi5	REF2N status. See description for gpi0.
4	gpi4	REF2P status. See description for gpi0.
3	gpi3	REF1N status. See description for gpi0.
2	gpi2	REF1P status. See description for gpi0.
1	gpi1	REF0N status. See description for gpi0.
0	gpi0	REF0P status. Logic value seen on pin REF0P if it is configured as input or control mode in the ctrl field of mailbox register ref_gpi_config.

ref_freq_x

Address:	0x0144:0x0147	
Name:	ref_freq_0P	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See register 0x21C bits 1:0 (ref_freq_meas_ctrl::latch) for details on how this register is data-filled. For a reference frequency read, LSB=1 Hz (unsigned). For a reference offset read, LSB=2^–32 (signed). Note that the estimated error for these measurements is dependent on input frequency: error[FFO] = ref_freq * 1.5 * (central_freq_offset + 2^32) / (2^56 * 800e6) where central_freq_offset is the value in registers 0x00B-0x00E. The estimated error in integer Hz is: error[Hz] = error[FFO] * ref_freq The measured frequency offset is with respect to the XO wired to the OSCB pin or the crystal wired to the OSCI and OSCO pins.

Address:	0x0148:0x014B	
Name:	ref_freq_0N	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See description for ref_freq_0P register (0x0144:0x0147)

Address:	0x014C:0x014F	
Name:	ref_freq_1P	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See description for ref_freq_0P register (0x0144:0x0147)

Address:	0x0150:0x0153	
Name:	ref_freq_1N	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See description for ref_freq_0P register (0x0144:0x0147)

Address:	0x0154:0x0157	
Name:	ref_freq_2P	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See description for ref_freq_0P register (0x0144:0x0147)

Address:	0x0158:0x015B	
Name:	ref_freq_2N	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See description for ref_freq_0P register (0x0144:0x0147)

Address:	0x015C:0x015F	
Name:	ref_freq_3P	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See description for ref_freq_0P register (0x0144:0x0147)

Address:	0x0160:0x0163	
Name:	ref_freq_3N	
Default:	0x00000000	
Type:	R	
Bit Field	**Function Name**	**Description**
31:0	—	See description for ref_freq_0P register (0x0144:0x0147)

Address:	0x017E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be host read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x017F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 3, STICKY

Address:	0x0180	
Name:	sticky_lock	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	This register needs to be set to a non-zero value prior to clearing sticky bits, to avoid race condition that can happen when the internal processor updates the register while the host clears the bit. Having non-zero value in this register prevents the internal processor from updating the sticky bit registers. For proper sticky bit monitoring, the following procedure is recommended: 1) Write non-zero value into this register 2) Clear sticky bits in other registers 3) Write 0 into this register 4) Read sticky bits status registers

Address:	0x0182	
Name:	ref_mon_th_sticky_0P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	0 = REF0P PFM failure status has not transitioned 0->1. 1 = REF0P PFM failure status transitioned 0->1, not yet acknowledged.
3	gst	0 = REF0P GST failure status has not transitioned 0->1. 1 = REF0P GST failure status transitioned 0->1, not yet acknowledged.
2	cfm	0 = REF0P CFM failure status has not transitioned 0->1. 1 = REF0P CFM failure status transitioned 0->1, not yet acknowledged.
1	scm	0 = REF0P SCM failure status has not transitioned 0->1. 1 = REF0P SCM failure status transitioned 0->1, not yet acknowledged.
0	los	0 = REF0P LOS failure status has not transitioned 0->1. 1 = REF0P LOS failure status transitioned 0->1, not yet acknowledged.

Address:	0x0183	
Name:	ref_mon_th_sticky_0N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x182, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at address 0x182, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at address 0x182, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at address 0x182, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at address 0x182, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x0184	
Name:	ref_mon_th_sticky_1P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x182, bit 4 (ref_mon_th_sticky_0P::pfm).

3	gst	See description for register at address 0x182, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at address 0x182, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at address 0x182, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at address 0x182, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x0185	
Name:	ref_mon_th_sticky_1N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x182, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at address 0x182, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at address 0x182, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at address 0x182, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at address 0x182, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x0186	
Name:	ref_mon_th_sticky_2P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x182, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at address 0x182, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at address 0x182, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at address 0x182, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at address 0x182, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x0187	
Name:	ref_mon_th_sticky_2N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x182, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at address 0x182, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at address 0x182, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at address 0x182, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at address 0x182, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x0188	
Name:	ref_mon_th_sticky_3P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x182, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at address 0x182, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at address 0x182, bit 2 (ref_mon_th_sticky_0P::cfm).
1	scm	See description for register at address 0x182, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at address 0x182, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x0189	
Name:	ref_mon_th_sticky_3N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x182, bit 4 (ref_mon_th_sticky_0P::pfm).
3	gst	See description for register at address 0x182, bit 3 (ref_mon_th_sticky_0P::gst).
2	cfm	See description for register at address 0x182, bit 2 (ref_mon_th_sticky_0P::cfm).

1	scm	See description for register at address 0x182, bit 1 (ref_mon_th_sticky_0P::scm).
0	los	See description for register at address 0x182, bit 0 (ref_mon_th_sticky_0P::los).

Address:	0x018C	
Name:	ref_dpll_freq_sticky_3_0	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	ref_3N	See description for ref_0P.
6	ref_3P	See description for ref_0P.
5	ref_2N	See description for ref_0P.
4	ref_2P	See description for ref_0P.
3	ref_1N	See description for ref_0P.
2	ref_1P	See description for ref_0P.
1	ref_0N	See description for ref_0P.
0	ref_0P	0 = No REF0P-to-DPLL frequency offset measurement calculated since this bit was last cleared. 1 = REF0P-to-DPLL frequency offset measurement is ready. Latch measurements by setting register 0x21C bits 1:0 (ref_freq_meas_ctrl::latch) to value 11.

Address:	0x018E	
Name:	dpll_meas_ref_sticky_3_0	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	ref_3N	See description for ref_0P.
6	ref_3P	See description for ref_0P.
5	ref_2N	See description for ref_0P.
4	ref_2P	See description for ref_0P.
3	ref_1N	See description for ref_0P.
2	ref_1P	See description for ref_0P.
1	ref_0N	See description for ref_0P.
0	ref_0P	0 = No DPLL-to-REF0P phase measurement calculated since this bit was last cleared. 1 = DPLL-to-REF0P phase measurement is ready. Latch by setting register 0x20F bit 0 (ref_phase_err_read_rqst::rd).

dpll_mon_th_sticky_x

Address:	0x0190	
Name:	dpll_mon_th_sticky_0	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	pslhit	The letters "_th_" in this and other sticky register names indicate "transition high", i.e. the 0->1 transition of a status bit. 0 = DPLL0 phase slope limit failure status has not transitioned 0->1. 1 = DPLL0 phase slope limit failure status transitioned 0->1, not yet acknowledged.
6	reserved	—
5	flhit	0 = DPLL0 pull-in/hold-in range limit failure status has not transitioned 0->1. 1 = DPLL0 pull-in/hold-in range limit failure status transitioned 0->1, not yet acknowledged.
4:3	reserved	—
2	ho_ready	0 = DPLL0 holdover ready status has not transitioned 0->1. 1 = DPLL0 holdover ready status transitioned 0->1, not yet acknowledged.
1	ho	0 = DPLL0 holdover status has not transitioned 0->1. 1 = DPLL0 holdover status transitioned 0->1, not yet acknowledged.
0	lock	0 = DPLL0 lock status has not transitioned 0->1. 1 = DPLL0 lock status transitioned 0->1, not yet acknowledged.

Address:	0x0191	
Name:	dpll_mon_th_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	pslhit	See description for register at address 0x190, bit 7 (dpll_mon_th_sticky_0::pslhit).
6	reserved	—
5	flhit	See description for register at address 0x190, bit 5 (dpll_mon_th_sticky_0::flhit).
4:3	reserved	—
2	ho_ready	See description for register at address 0x190, bit 2 (dpll_mon_th_sticky_0::ho_ready).
1	ho	See description for register at address 0x190, bit 1 (dpll_mon_th_sticky_0::ho).
0	lock	See description for register at address 0x190, bit 0 (dpll_mon_th_sticky_0::lock).

Address:	0x01B2	
Name:	ref_mon_tl_sticky_0P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	0 = REF0P PFM failure status has not transitioned 1->0. 1 = REF0P PFM failure status transitioned 1->0, not yet acknowledged.
3	gst	0 = REF0P GST failure status has not transitioned 1->0. 1 = REF0P GST failure status transitioned 1->0, not yet acknowledged.
2	cfm	0 = REF0P CFM failure status has not transitioned 1->0. 1 = REF0P CFM failure status transitioned 1->0, not yet acknowledged.
1	scm	0 = REF0P SCM failure status has not transitioned 1->0. 1 = REF0P SCM failure status transitioned 1->0, not yet acknowledged.
0	los	0 = REF0P LOS failure status has not transitioned 1->0. 1 = REF0P LOS failure status transitioned 1->0, not yet acknowledged.

Address:	0x01B3	
Name:	ref_mon_tl_sticky_0N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x1B2, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at address 0x1B2, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at address 0x1B2, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at address 0x1B2, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at address 0x1B2, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B4	
Name:	ref_mon_tl_sticky_1P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x1B2, bit 4 (ref_mon_tl_sticky_0P::pfm).

3	gst	See description for register at address 0x1B2, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at address 0x1B2, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at address 0x1B2, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at address 0x1B2, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B5	
Name:	ref_mon_tl_sticky_1N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x1B2, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at address 0x1B2, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at address 0x1B2, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at address 0x1B2, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at address 0x1B2, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B6	
Name:	ref_mon_tl_sticky_2P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x1B2, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at address 0x1B2, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at address 0x1B2, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at address 0x1B2, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at address 0x1B2, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B7	
Name:	ref_mon_tl_sticky_2N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x1B2, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at address 0x1B2, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at address 0x1B2, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at address 0x1B2, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at address 0x1B2, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B8	
Name:	ref_mon_tl_sticky_3P	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x1B2, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at address 0x1B2, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at address 0x1B2, bit 2 (ref_mon_tl_sticky_0P::cfm).
1	scm	See description for register at address 0x1B2, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at address 0x1B2, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01B9	
Name:	ref_mon_tl_sticky_3N	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	See description for register at address 0x1B2, bit 4 (ref_mon_tl_sticky_0P::pfm).
3	gst	See description for register at address 0x1B2, bit 3 (ref_mon_tl_sticky_0P::gst).
2	cfm	See description for register at address 0x1B2, bit 2 (ref_mon_tl_sticky_0P::cfm).

1	scm	See description for register at address 0x1B2, bit 1 (ref_mon_tl_sticky_0P::scm).
0	los	See description for register at address 0x1B2, bit 0 (ref_mon_tl_sticky_0P::los).

Address:	0x01C0	
Name:	dpll_mon_tl_sticky_0	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	pslhit	The letters "_tl_" in this and other sticky register names indicate "transition low", i.e. the 1->0 transition of a status bit. 0 = DPLL0 phase slope limit failure status has not transitioned 1->0. 1 = DPLL0 phase slope limit failure status transitioned 1->0, not yet acknowledged.
6	reserved	—
5	flhit	0 = DPLL0 pull-in/hold-in range limit failure status has not transitioned 1->0. 1 = DPLL0 pull-in/hold-in range limit failure status transitioned 1->0, not yet acknowledged.
4:3	reserved	—
2	ho_ready	0 = DPLL0 holdover ready status has not transitioned 1->0. 1 = DPLL0 holdover ready status transitioned 1->0, not yet acknowledged.
1	ho	0 = DPLL0 holdover status has not transitioned 1->0. 1 = DPLL0 holdover status transitioned 1->0, not yet acknowledged.
0	lock	0 = DPLL0 lock status has not transitioned 1->0. 1 = DPLL0 lock status transitioned 1->0, not yet acknowledged.

Address:	0x01C1	
Name:	dpll_mon_tl_sticky_1	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	pslhit	See description for register at address 0x1C0, bit 7 (dpll_mon_tl_sticky_0::pslhit).
6	reserved	—
5	flhit	See description for register at address 0x1C0, bit 5 (dpll_mon_tl_sticky_0::flhit).
4:3	reserved	—
2	ho_ready	See description for register at address 0x1C0, bit 2 (dpll_mon_tl_sticky_0::ho_ready).
1	ho	See description for register at address 0x1C0, bit 1 (dpll_mon_tl_sticky_0::ho).

0	lock	See description for register at address 0x1C0, bit 0 (dpll_mon_tl_sticky_0::lock).

Address:	0x01E0	
Name:	dpll_fastlock_phase_sticky	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	dpll_1	See description for dpll_0.
0	dpll_0	0 = DPLL0 has no unacknowledged fast lock phase error status. 1 = DPLL0 fast lock phase error threshold exceeded, not yet acknowledged.

Address:	0x01E1	
Name:	dpll_fastlock_freq_sticky	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	dpll_1	See description for dpll_0.
0	dpll_0	0 = DPLL0 has no unacknowledged fast lock frequency error status. 1 = DPLL0 fast lock frequency error threshold exceeded, not yet acknowledged.

Address:	0x01E4	
Name:	dpll_tie_wr_sticky	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	dpll_1	See description for dpll_0.
0	dpll_0	0 = DPLL0 has no unacknowledged TIE write status. 1 = DPLL0 TIE write completed, not yet acknowledged.

Address:	0x01E8	
Name:	ref_irq_active_3_0	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	irq_3N	See description for irq_0P.
6	irq_3P	See description for irq_0P.
5	irq_2N	See description for irq_0P.

4	irq_2P	See description for irq_0P.
3	irq_1N	See description for irq_0P.
2	irq_1P	See description for irq_0P.
1	irq_0N	See description for irq_0P.
0	irq_0P	0 = REF0P has no unacknowledged interrupts. 1 = REF0P interrupt has occurred, not yet acknowledged.

Address:	0x01EB	
Name:	dpll_irq_active	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	irq_1	See description for irq_0.
0	irq_0	0 = DPLL0 has no unacknowledged interrupts. 1 = DPLL0 interrupt has occurred, not yet acknowledged.

Address:	0x01EC	
Name:	synth_irq_active	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	irq_4	See description for irq_0.
3	irq_3	See description for irq_0.
2	irq_2	See description for irq_0.
1	irq_1	See description for irq_0.
0	irq_0	0 = synth0 has no unacknowledged interrupts. 1 = synth0 interrupt has occurred, not yet acknowledged.

Address:	0x01ED	
Name:	output_irq_active_7_0	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7	irq_7	See description for irq_0.
6	irq_6	See description for irq_0.
5	irq_5	See description for irq_0.
4	irq_4	See description for irq_0.
3	irq_3	See description for irq_0.
2	irq_2	See description for irq_0.
1	irq_1	See description for irq_0.
0	irq_0	0 = output0 has no unacknowledged interrupts. 1 = output0 interrupt has occurred, not yet acknowledged.

Address:	0x01EE	
Name:	output_irq_active_9_8	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	irq_9	See description for register at address 0x1ED, bit 0 (output_irq_active_7_0::irq_0).
0	irq_8	See description for register at address 0x1ED, bit 0 (output_irq_active_7_0::irq_0).

Address:	0x01EF	
Name:	dpll_ns_rollover_irq_active	
Default:	0x00	
Type:	S	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	irq_ns_rollover	0 = There are no unacknowledged ToD ns rollover interrupts 1 = ToD ns rollover interrupt(s) occurred, not yet acknowledged

Address:	0x01FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x01FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 4, REF

Address:	0x0200	
Name:	ref_los_3_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	los_3N	See description for los_0P.
6	los_3P	See description for los_0P.
5	los_2N	See description for los_0P.
4	los_2P	See description for los_0P.
3	los_1N	See description for los_0P.
2	los_1P	See description for los_0P.
1	los_0N	See description for los_0P.
0	los_0P	REF0P external Loss Of Signal (LOS) - indicator to DPLLs that REF0P has failed. Internally in the DPLLs this signal is used for reference monitor indicator, reference switching or holdover entry and for interrupt generation.

Address:	0x020F	
Name:	ref_phase_err_read_rqst	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	rd	The host sets this bit to 1 to request a read of the current phase error measurements. The device sets this bit to 0 when the data has been successfully latched into the registers: 0x220-0x25B (ref_phase), 0x25C-0x279 (dpll_phase) and 0x2D5-0x2F2 (dpll_phase_err_data).

Address:	0x021C	
Name:	ref_freq_meas_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1:0	latch	00 = Previous reference frequency latch operation complete. 01 = Request a reference frequency latch operation. The measured frequency (in integer Hz) for all references is written to registers 0x144-0x16B. 10 = Request a reference frequency offset latch operation. The measured offset (in units of 2^–32, signed) for all references is written to registers 0x144-0x16B. 11 = Request a reference to DPLL frequency offset latch operation. The reference DPLL is set in register 0x21F. The measured offset (in units of 2^–32, signed) for all references is written to registers 0x144-0x16B. Note: The host should wait for this bitfield to read 00, then write a non-zero value to it to ensure the data is coherent. Note: The appropriate bit in ref_freq_meas_mask_3_0 and ref_freq_meas_mask_4 (0x21D and 0x21E) must be set to 1 to enable frequency measurement for each reference.

Address:	0x021D	
Name:	ref_freq_meas_mask_3_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	ref_3N	See description for ref_0P.
6	ref_3P	See description for ref_0P.
5	ref_2N	See description for ref_0P.
4	ref_2P	See description for ref_0P.

3	ref_1N	See description for ref_0P.
2	ref_1P	See description for ref_0P.
1	ref_0N	See description for ref_0P.
0	ref_0P	0 = Do not measure frequency of REF0P 1 = Measure frequency of REF0P

Address:	0x021F	
Name:	dpll_meas_ref_freq_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	idx	Sets the DPLL index that all REF-to-DPLL frequency offset measurements are performed against. 000 = DPLL0 001 = DPLL1 Other values reserved
3:1	reserved	—
0	enable	0 = REF-to-DPLL frequency measurement block disabled. 1 = REF-to-DPLL frequency measurement block enabled.

ref_phase_x

Address:	0x0220:0x0225	
Name:	ref_phase_0P	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	DPLL-to-REF0P phase measurement. Signed 48-bit, LSB=0.01 ps. The value is modded to [–0.5 periods, +0.5 periods) of the configured REF0P frequency. A positive value means the selected DPLL (specified by dpll_meas_idx::idx at 0x2D1) is earlier in time with respect to REF0P (more to the left on a scope). To populate this register, the DPLL measurement block must be enabled with register 0x2D0 bit 0 (dpll_meas_ctrl::en), and a read requested with register 0x20F bit 0 (ref_phase_err_read_rqst::rd). Note that if the DPLL in this measurement is locked to a REF with a higher frequency than REF0P then the to get the desired phase offset, system software should calculate the phase as the remainder of ref_phase_0P divided by the period of the REF to which the DPLL is locked. In other words, phase = remainder(ref_phase_0P, DPLL_REF_period)

Address:	0x0226:0x022B	
Name:	ref_phase_0N	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x220-0x225 (ref_phase_0P).

Address:	0x022C:0x0231	
Name:	ref_phase_1P	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x220-0x225 (ref_phase_0P).

Address:	0x0232:0x0237	
Name:	ref_phase_1N	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x220-0x225 (ref_phase_0P).

Address:	0x0238:0x023D	
Name:	ref_phase_2P	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x220-0x225 (ref_phase_0P).

Address:	0x023E:0x0243	
Name:	ref_phase_2N	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x220-0x225 (ref_phase_0P).

Address:	0x0244:0x0249	
Name:	ref_phase_3P	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x220-0x225 (ref_phase_0P).

Address:	0x024A:0x024F	
Name:	ref_phase_3N	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x220-0x225 (ref_phase_0P).

Address:	0x025C:0x0261	
Name:	dpll_phase_0	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	DPLL-to-DPLL0 phase measurement. Signed 48-bit, LSB=0.01 ps. The value is modded to [–1 second, +1 second). A positive value means the selected DPLL (specified by dpll_meas_idx::idx at 0x2D1) is earlier in time with respect to DPLL0 (more to the left on a scope). To populate this register, the DPLL measurement block must be enabled with register 0x2D0 bit 0 (dpll_meas_ctrl::en), and a read requested with register 0x20F bit 0 (ref_phase_err_read_rqst::rd). Note that in general absolute DPLL-to-DPLL phase numbers are arbitrary since each DPLL locks to an arbitrary phase of the REF and because of internal DPLL architecture details. But changes in these phase numbers are valid. The absolute phase numbers are valid in the one special case where the two DPLLs are locked to the same 1 Hz REF.

Address:	0x0262:0x0267	
Name:	dpll_phase_1	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x025C (dpll_phase_0)

Address:	0x027E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x027F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 5, DPLL

Address:	0x0283	
Name:	dpll_enable	
Default:	0x05	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	num	0 = All DPLLs disabled. n = DPLL0 to DPLL(n-1) enabled. If n is greater than the highest numbered DPLL, all DPLLs are enabled.

dpll_mode_refsel_x

Address:	0x0284	
Name:	dpll_mode_refsel_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	ref	Specifies which reference the DPLL0 is forced to select, when the mode bitfield is set to '010' (forced reference lock mode). When this forced reference fails, DPLL0 goes to holdover mode. An invalid reference number selects REF0P. When DPLL0 is not in forced reference lock mode, this bitfield is ignored. 0000 = REF0P 0001 = REF0N 0010 = REF1P 0011 = REF1N 0100 = REF2P 0101 = REF2N 0110 = REF3P 0111 = REF3N 1000-1111 = Invalid
3	reserved	—
2:0	mode	000 = Freerun mode 001 = Forced holodover mode 010 = Forced reference lock mode 011 = Automatic mode 100 = NCO mode 101-111 = Invalid (automatic mode)

dpll_ctrl_x

Address:	0x0285	
Name:	dpll_ctrl_0	
Default:	0x6C	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	nco_auto_read	0 = DPLL0 automatic NCO read is disabled. 1 = DPLL0 automatic NCO read is enabled. When switching to forced holdover or NCO modes, an NCO read operation is automatically performed, and the device writes DPLL0's frequency offset to register 0x300:0x305 (dpll_df_offset_0).
6	tie_wr_trigger_ref_sync_meas	0 = A TIE-write does not affect sync pulse measurement. 1 = A TIE-write causes a sync pulse measurement to occur as soon as possible. This setting has no effect if DPLL0 is locking to a clock-only input reference. This bit and tie_wr_wait_until_ref_sync_meas should always be set to the same value.

5	tie_wr_wait_until_ref_sync_meas	0 = All TIE-writes are applied as soon as possible. TIE-clear is evaluated as soon as possible. 1 = When DPLL0 is configured to lock to a ref-sync pair , TIE-write and TIE-clear operations are delayed until the sync pulse offset has been measured. When locking to a clock-only input, TIE-write and TIE-clear operations are applied as soon as possible. This bit and tie_wr_trigger_ref_sync_meas should always be set to the same value.
4	ref_sync_align_wait_until_lock	0 = DPLL0 measures the sync pulse offset as soon as possible. 1 = DPLL0 only measures the sync pulse offset when the programmed lock criteria is met (see registers 0x627-0x62B).
3	ref_sync_en	0 = DPLL0 ignores the sync input of a ref-sync pair). 1 = DPLL0 phase-locks to the sync component of a ref-sync pair. Note that if ref_sync_en is changed from 1 to 0 while the DPLL is tracking an input, the DPLL's phase target continues to be determined by the last observed sync phase to avoid a sudden phase change. To give the DPLL a phase target determined only by the ref signal, set ref_sync_en=0 then change DPLL mode to holdover and then back to desired mode.
2	tod_step_reset	0: DPLL0 ToD step reset is disabled. 1: DPLL0 ToD step reset is enabled. When switching out of NCO mode with tie_clear enabled, a negated version of the internal "ToD step accumulator" is applied to the DPLL using the TIE-write mechanism. See register 0x4B8 bit 3 (output_phase_step_ctrl::tod_step) for details on the internal "ToD step accumulator".
1	tie_wr_clear_after_switch	This bit enables the TIE-write clear on reference switch mode of operation. DPLL0's tie_clear bit (bit 0 of this register) must also be set to 1, or DPLL0 must be configured to lock to a ref-sync pair for this feature to be enabled. When this bit is set, the DPLL clears the accumulated TIE from all previous TIE-write operations whenever the DPLL performs a reference switch, whenever the DPLL mode is changed from NCO to either Automatic or Forced Reference, and whenever the DPLL exits the holdover state.
0	tie_clear	0 = DPLL0 does not align its output to the reset position. This represents "hitless" reference switching mode. 1 = DPLL0 aligns its outputs to the reset position (specified by appropriate phase shift selection). This bit should be set when initial output to input alignment is desired even after numerous reference rearrangements.

dpll_cmd_x

Address:	0x0286	
Name:	dpll_cmd_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	ref_sync_align	0 = DPLL0 Ref-Sync alignment computation complete. 1 = Request a new Ref-Sync alignment computation for DPLL0. The device clears the bit once the computation is complete. Note that it might still take some time for the alignment to occur, after the computation is complete.

Address:	0x0288	
Name:	dpll_mode_refsel_1	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	ref	See description for register at address 0x284, bits 7:4 (dpll_mode_refsel_0::ref).
3	reserved	—
2:0	mode	See description for register at address 0x284, bits 2:0 (dpll_mode_refsel_0::mode).

Address:	0x0289	
Name:	dpll_ctrl_1	
Default:	0x0C	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	nco_auto_read	See description for register at address 0x285, bits 7 (dpll_ctrl_0::nco_auto_read).
6	tie_wr_trigger_ref_sync_meas	See description for register at address 0x285, bits 6 (dpll_ctrl_0::tie_wr_trigger_ref_sync_meas).
5	tie_wr_wait_until_ref_sync_meas	See description for register at address 0x285, bits 5 (dpll_ctrl_0::tie_wr_wait_until_ref_sync_meas).
4	ref_sync_align_wait_until_lock	See description for register at address 0x285, bits 4 (dpll_ctrl_0::ref_sync_align_wait_until_lock).
3	ref_sync_en	See description for register at address 0x285, bits 3 (dpll_ctrl_0::ref_sync_en).
2	tod_step_reset	See description for register at address 0x285, bits 2 (dpll_ctrl_0::tod_step_reset).
1	tie_wr_clear_after_switch	See description for register at address 0x285, bits 1 (dpll_ctrl_0::tie_wr_clear_after_switch).
0	tie_clear	See description for register at address 0x285, bits 0 (dpll_ctrl_0::tie_clear).

Address:	0x028A	
Name:	dpll_cmd_1	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	ref_sync_align	See description for register at address 0x286, bits 0 (dpll_cmd_0::ref_sync_align).

Address:	0x02A4	
Name:	ext_fb_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	en	0 = External feedback is disabled 1 = External feedback is enabled Before modifying this bit, all synths driven by the DPLL specified in register 0x2A5, bits 2:0 (ext_fb_sel::dpll) should be disabled. After modifying this bit, the synths can then be re-enabled. External feedback configuration is normally used to tightly phase-align one or more output signals of the device or one or more output signals of a fanout buffer downstream of the device with the DPLL's input reference. Normally the external feedback DPLL has dpll_ctrl_x::tie_clear=1. Other DPLLs can be phase-compensated along with the external feedback DPLL. See 0x605 bit 5 (dpll_config::ext_fb_en) for details.

Address:	0x02A5	
Name:	ext_fb_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	ref	Sets the reference to use as the external feedback source. An invalid reference number disables external feedback. 0=REF0P, 1=REF0N, etc..
3:2	reserved	—

1:0	dpll	Sets the DPLL to use for external feedback. External feedback phase represents the difference in phase between this DPLL's selected active reference and selected feedback source. An invalid DPLL number disables external feedback. Note 1: If external feedback is enabled for a specific DPLL (see mailbox register 0x605 bit 5, dpll_config::ext_fb_en), that DPLL's output phase is compensated for by the external feedback phase, regardless which DPLL is used for the external feedback phase calculation. Note 2: In order to have proper behavior with external feedback, it is required that main reference and the external feedback source are frequency locked (they are not required to have the same nominal frequency).

Address:	0x02A6	
Name:	dpll_df_read_all_mask	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	mask_dpll_1	See the mask_dpll_0 description.
0	mask_dpll_0	0 = DPLL 0 is not read when dpll_df_read_all command is requested (0x2A7) 1 = DPLL 0 is read when dpll_df_read_all command is requested (0x2A7)

Address:	0x02A7	
Name:	dpll_df_read_all	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	rd	0 = Previous DPLL frequency command complete. 1 = Request a DPLL frequency latch operation. For all DPLLs selected in dpll_df_read_all_mask (0x2A6), df offsets are latched at the same instant and written to registers 0x300-305, 0x320-0x325, etc. (dpll_df_offset_x). The frequency value reported is the option selected in registers 0x2A8, 0x2A9, etc. (dpll_df_ctrl_x::cmd). Note: The host should wait for this bit to read 0, then write 1 to it to ensure the data is coherent.

dpll_df_read_x

Address:	0x02A8	
Name:	dpll_df_read_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	read_sem	Set to 1 to perform a manual df offset read. When the operation has completed, the result is written to registers 0x300-0x305 (dpll_df_offset_0), then the device sets this bit to 0. The host always writes a 1 value, while the device writes 0. To avoid race conditions, the host should check this bit for a 0 value, before writing to it.
3	ref_ofst	0 = DPLL0 df offset read will be based on cmd bitfield. 1 = DPLL0 df offset read will be the frequency offset of DPLL0 with respect to its input reference (NOT the system clock). The cmd bitfield will be ignored for manual reads, but used for automatic NCO reads.
2:0	dpll	Sets the type of delta frequency read operation for manual reads (by setting read_sem to 1) and automatic NCO reads (when dpll_ctrl_0::nco_auto_read is 1). All of the options listed below are the frequency offset of DPLL0 with respect to the system clock. Normal operation: x00 = Read the accumulated I-part (iMemory) x01 = Read the output of the holdover filter (filtered iMemory) x10 = Read the sum of the P and I-parts (delta frequency) x11 = Read P-part only Holdover: 0xx = Read the output of the holdover filter (returns I-part when holdover filter is bypassed) 100 = Read the accumulated I-part, latched before entering holdover 101 = Read the output of the holdover filter (returns 0 when holdover filter is bypassed) 110 = Read the sum of the P and I-parts, latched before entering holdover 111 = Read P-part only, latched before entering holdover NCO (all reads represent values latched before entering NCO): x00 = Read the accumulated I-part x01 = Read the output of the holdover filter. If NCO holdover updates are enabled (see mailbox register 0x662, bit 4), this is the current output of the holdover filter. 010 = Depends on previous state... Normal: Read the sum of the P and I-parts Holdover: Read the output of the holdover filter 110 = Read the sum of the P and I-parts x11 = Read P-part only

Address:	0x02A9	
Name:	dpll_df_read_1	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	read_sem	See description for register at address 0x2A8, bit 4 (dpll_df_read_0::read_sem).
3	reserved	—
2:0	dpll	See description for register at address 0x2A8, bits 2:0 (dpll_df_read_0::cmd).

Address:	0x02B0	
Name:	dpll_tie_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—

2:0	op	This field selects a time interval error (TIE) related operation to perform. When the operation request has been latched by the device, this bitfield reads 000. To prevent race conditions, the host only writes non-zero values to this register, while the device only writes zero. The host controller should read this register prior to writing, and should only write to this bitfield when it contains value 000. When a TIE operation is requested, the operation is applied to only the DPLLs unmasked by the dpll_tie_ctrl_mask register (0x02B1). All operations provided by this register are only valid when the unmasked registers DPLLs are in forced reference or automatic or mode (see register 0x0284) with a valid, qualified reference. If an operation is requested on DPLLs in another mode of operation (e.g., NCO mode), then the operation is delayed until DPLL0 is configured to forced reference or automatic mode with a qualified reference. Available operations are: 000 = Previous operation complete / new operation can be requested 001 = Request a Snap MTIE operation 010 = Request to read instantaneous TIE (TIE data is within [–1, 1] second, where T is the period for the reference signal). 011 = Request to read instantaneous TIE (TIE data is within [–T/2, T/2], where T is the period for the reference signal). 100 = Request to write TIE 101 = Request to read historical TIE writes 110 = Request to clear historical TIE writes Snap MTIE: This operation allows the user to perform an instantaneous I/O alignment. This alignment zeros out hitless reference switch TIE and Write TIE offsets, but excludes output-divider phase steps and fine phase shifts. The instantaneous alignment is completed when this bitfield reads 000. This feature should not be used together with step time. Read TIE-read: Reads the TIE between the input reference and output, not including output-divider phase steps and synthesizer phase shifts. The results are returned in the dpll_tie_data_x registers in Pages 6 and 7. The results are valid when this bitfield reads 000. The return values "wrap around" such that the range is either –1s to 1s, or [–T/2, T/2] where T is the period of the reference for the corresponding DPLL. This operation is atomic for different DPLLs: the TIE data read through a single command is latched at the same time for all the unmasked DPLLs. Write TIE-write: Write the TIE between the input reference and output. The desired TIE values are written to the dpll_tie_data_x registers (0x30E, 0x32E0x30C, 0x32C, etc.) and if the correct corresponding mask is set in dpll_tie_ctrl_mask (0x02B1) prior to writing this bitfield. The allowed range is –1s to 1s. Another write TIE request can be made only after this bitfield reads 000. Register 0x1E4 (dpll_tie_wr_sticky) can be used to determine when the requested TIE has been fully applied to the output. Write TIE operations are cumulative; subsequent write TIEs are added to the previous TIE. Clear TIE: Clear all historical TIE writes. All the historical TIE writes are reversed by applying a negative TIE write. The initial TIE that existed before all the write TIE writes operations would not be cleared.

Address:	0x02B1	
Name:	dpll_tie_ctrl_mask	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	dpll1	See description for dpll0.
0	dpll0	TIE control operation mask bit for DPLL0. If this bit is set, any TIE control operation requested by the host through the dpll_tie_ctrl register (0x02B0) is applied to DPLL0. If this bit is cleared, all TIE control operations are ignored for DPLL0.

Address:	0x02D0	
Name:	dpll_meas_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	avg_factor	Sets the averaging factor for all calculations made by the DPLL measurement block. This block uses an exponential moving average, calculated using the following equation: curr_avg = prev_avg * ((2^N – 1) / 2^N) + new_measurement * (1 / 2^N) If avg_factor > 0, then N = (avg_factor – 1) If avg_factor == 0, then N = 15 Setting this bitfield to 0x1 (N=0) disables averaging. For DPLL-to-REF, new measurements are taken at approximately 40 Hz, or at the frequency of the input REF (whichever is lower). For DPLL-to-DPLL, new measurements are taken at approximately 40 Hz.
3:1	reserved	—
0	en	0 = DPLL measurement block disabled. 1 = DPLL measurement block enabled.

Address:	0x02D1	
Name:	dpll_meas_idx	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	idx	Specifies the DPLL that all DPLL-to-REF and DPLL-to-DPLL measurements are performed against. 000 = DPLL0 001 = DPLL1 010-111 = Invalid

Address:	0x02D2	
Name:	dpll_meas_ref_edge_3_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	ref_3N	See description for ref_0P.
6	ref_3P	See description for ref_0P.
5	ref_2N	See description for ref_0P.
4	ref_2P	See description for ref_0P.
3	ref_1N	See description for ref_0P.
2	ref_1P	See description for ref_0P.
1	ref_0N	See description for ref_0P.
0	ref_0P	0 = Use rising edge for DPLL-to-REF0P measurements. 1 = Use falling edge for DPLL-to-REF0P measurements.

Address:	0x02D4	
Name:	dpll_phase_err_read_mask	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	dpll_1	See description for dpll_0
0	dpll_0	0 = Do not measure DPLL0 phase error vs. its reference 1 = Measure DPLL0 phase error vs. its reference; see 0x02D5-0x02DA (dpll_phase_err_data_0).

dpll_phase_err_data_x

Address:	0x02D5:0x02DA	
Name:	dpll_phase_err_data_0	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	This register stores the readback phase error data when the host issues a phase error read request through the register ref_phase_err_read_rqst (0x020F). The unit is 0.01 ps. The range is ±0.5 cycles of the input reference. To populate this register, the DPLL measurement block must be enabled with register 0x2D0 bit 0 (dpll_meas_ctrl::en), 0x2D4 bit 0 (dpll_phase_err_read_mask::dpll_0) should be set to 1, and a read requested with register 0x20F bit 0 (ref_phase_err_read_rqst::rd). A positive value means the phase of DPLL0 is earlier in time (more to the left on a scope) than its input reference. A negative value means the phase of DPLL0 later in time (more to the right on a scope) than its input reference.

Address:	0x02DB:0x02E0	
Name:	dpll_phase_err_data_1	
Default:	0x000000000000	
Type:	R	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at addresses 0x2D5-0x2DA (dpll_phase_err_data_0).

Address:	0x02FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x02FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 6, DPLL DATA

dpll_df_offset_x

Address:	0x0300:0x0305	
Name:	dpll_df_offset_0	
Default:	0x000000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
47:0	—	When DPLL0 is programmed into NCO mode (dpll_-mode_refsel_0 register), this register contains a 2's complement binary value of delta frequency offset. This register controls delta frequency of synthesizers that are associated with DPLL0. Delta frequency is expressed in steps of ±2^–48 of nominal setting. The value to write in NCO mode is: df_offset = (–X) * 2^48 where X is the desired offset from nominal. E.g., for a –1 ppm offset, X=–1e–6, df_offset=0x000010C6F7A0 After performing an NCO read, the output frequency can be calculated as per formula: f_offset = f_nom * (–df_offset) / 2^48 where, df_offset is 2's complement number read from this register, f_nom is the nominal output frequency and f_offset is the desired frequency offset to the output. Note 1: The delta frequency offset should not exceed ±1% of the nominal value. Note 2: This register can be written as fast as once per 600 µs, but no faster. Note 3: This register should not be written while a read operation is pending. Note 4: The read value of this register during NCO mode is the value latched just prior to entering NCO mode.

dpll_tie_data_x

Address:	0x030C:0x0311	
Name:	dpll_tie_data_0	
Default:	0x000000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
47:0	—	This register contains the argument or results of a DPLL0 time interval error (TIE) control operation. The value is a 48-bit signed 2's complement with LSB=0.01 ps. See registers 0x2B0 (dpll_tie_ctrl_0) and 0x2B1 (dpll_tie_ctrl_mask) for details on TIE control operations. This register should only be read or written when register 0x2B0 bits 2:0 (dpll_tie_ctrl_0::op) == 000. For TIE-read, a positive value means the phase of DPLL0 is earlier in time (more to the left on a scope) than its input reference. A negative value means the phase of DPLL0 is later in time (more to the right on a scope) than its input reference. For TIE-write, a positive value moves the phase of DPLL0 earlier in time (more to the left on a scope) with respect to its input reference. A negative value moves the phase of DPLL0 later in time (more to the right on a scope) with respect to its input reference.

Address:	0x0320:0x0325	
Name:	dpll_df_offset_1	
Default:	0x000000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x300-0x305 (dpll_df_offset_0).

Address:	0x032C:0x0331	
Name:	dpll_tie_data_1	
Default:	0x000000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
47:0	—	See description for register at address 0x30C-0x311 (dpll_tie_data_0).

Address:	0x037E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.

6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x037F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 9, SYNTH AND OUTPUT

synth_ctrl_x

Address:	0x0480	
Name:	synth_ctrl_0	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	dpll_sel	Select the DPLL to drive this synthesizer. 0 = DPLL0 1 = DPLL1
3:2	reserved	—
1	spread_spectrum_en	Enable or disable spread spectrum for this synthesizer 0 = Disable
0	en	Enable or disable the synthesizer: 0 = Disable 1 = Enable

Address:	0x0481	
Name:	synth_ctrl_1	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	dpll_sel	See description for register at address 0x480, bits 6:4 (synth_ctrl_0::dpll_sel).
3:2	reserved	—
1	spread_spectrum_en	See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en).
0	en	See description for register at address 0x480, bit 0 (synth_ctrl_0::en).

Address:	0x0482	
Name:	synth_ctrl_2	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	dpll_sel	See description for register at address 0x480, bits 6:4 (synth_ctrl_0::dpll_sel).
3:2	reserved	—
1	spread_spectrum_en	See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en).
0	en	See description for register at address 0x480, bit 0 (synth_ctrl_0::en).

Address:	0x0483	
Name:	synth_ctrl_3	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	dpll_sel	See description for register at address 0x480, bits 6:4 (synth_ctrl_0::dpll_sel).
3:2	reserved	—
1	spread_spectrum_en	See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en).
0	en	See description for register at address 0x480, bit 0 (synth_ctrl_0::en).

Address:	0x0484	
Name:	synth_ctrl_4	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	dpll_sel	See description for register at address 0x480, bits 6:4 (synth_ctrl_0::dpll_sel).
3:2	reserved	—
1	spread_spectrum_en	See description for register at address 0x480, bit 1 (synth_ctrl_0::spread_spectrum_en).
0	en	See description for register at address 0x480, bit 0 (synth_ctrl_0::en).

synth_df_offset_manual_x

Address:	0x0485:0x0489	
Name:	synth_df_offset_manual_0	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
39:0	—	Manual delta frequency offset adjustment for Synth0. This offset is applied in addition to any offset applied by the DPLL. This register contains a 2's complement binary value in steps of 2^–48. The frequency offset should be calculated as per formula: f_offset = –(X/2^48)*f_nom where, X is 2's complement number specified in this register, f_nom is the nominal frequency set by Bs, Ks, Ms, Ns for the synthesizer and f_offset is the desired frequency for the output. Note 1: This register can be written as fast as once per 600 µs, but no faster. Note 2: The offset frequency is based on the system clock. If the system clock experiences frequency drift, the offset frequency is affected.

Address:	0x048A:0x048E	
Name:	synth_df_offset_manual_1	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
39:0	—	See description for register at address 0x485-0x489 (synth_df_offset_manual_0).

Address:	0x048F:0x0493	
Name:	synth_df_offset_manual_2	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
39:0	—	See description for register at address 0x485-0x489 (synth_df_offset_manual_0).

Address:	0x0494:0x0498	
Name:	synth_df_offset_manual_3	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
39:0	—	See description for register at address 0x485-0x489 (synth_df_offset_manual_0).

Address:	0x0499:0x049D	
Name:	synth_df_offset_manual_4	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
39:0	—	See description for register at address 0x485-0x489 (synth_df_offset_manual_0).

output_ctrl_x

Address:	0x04A8	
Name:	output_ctrl_0	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	This field selects the synthesizer that drives this output. 0=Synth0, 1=Synth2, etc.
3	stop_hz	This is a configuration bit that does not trigger action. 0 = After the output stops, it stays low or high as set by the stop_high field (bit 2). 1 = After the output stops, the output driver is disabled and the output goes high-impedance This bit does not affect the N-divided clock under the N-divider mode. The N-divided clock could stop at either high or low.
2	stop_high	This is a configuration bit that does not trigger action. 0 = Stop low. When the output clock is stopped by the stop field (bit 1), the output stops after a falling edge. 1 = Stop high. When the output clock is stopped by the stop field (bit 1), the output stops after a rising edge. This bit does not affect the N-divided clock under the N-divider mode. The N-divided clock could stop at either high or low.
1	stop	0 = Restart the output clock cleanly. Wait until the proper edge and start the output clock signal. 1 = Stop the output clock cleanly. Wait until the proper edge and stop the output clock signal at 1 or 0 based on the stop_high bit.
0	en	Enable or disable the output module. 0 = Disable. 1 = Enable.

Address:	0x04A9	
Name:	output_ctrl_1	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04AA	
Name:	output_ctrl_2	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04AB	
Name:	output_ctrl_3	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).

1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04AC	
Name:	output_ctrl_4	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04AD	
Name:	output_ctrl_5	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04AE	
Name:	output_ctrl_6	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).

3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04AF	
Name:	output_ctrl_7	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04B0	
Name:	output_ctrl_8	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04B1	
Name:	output_ctrl_9	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	synth_sel	See description for register at address 0x4A8, bits 6:4 (output_ctrl_0::synth_sel).
3	stop_hz	See description for register at address 0x4A8, bit 3 (output_ctrl_0::stop_hz).
2	stop_high	See description for register at address 0x4A8, bit 2 (output_ctrl_0::stop_high).
1	stop	See description for register at address 0x4A8, bit 1 (output_ctrl_0::stop).
0	en	See description for register at address 0x4A8, bit 0 (output_ctrl_0::en).

Address:	0x04B8	
Name:	output_phase_step_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:4	dpll	Selects the DPLL that is the target of the requested ToD step operation (i.e., phase step operation with tod_step=1). This bitfield should be set to 000 when tod_step=0. This bitfield should be set during the same write that changes the op bitfield to a non-zero value. If this value is invalid, no phase step operation will execute.
3	tod_step	This bit changes the behavior of phase step read and write commands. It is expected that the host will only set this bit to 1 when the DPLL is in NCO mode. 0 = No change to the phase step read and write commands. 1 = If a phase step write is requested, the output clock(s) will be stepped as normal, the ToD counter will be stepped by the amount programmed in output_phase_step_data, and this value is added to an internal "ToD step accumulator". If a phase step read is requested, output_phase_step_data will be filled with the value of the internal "ToD step accumulator" to ±0.5 sec. Value will be expressed in ns.
2	reserved	—

1:0	op	This field selects the phase step operation to perform. The device clears this field to 00 after it has completed the operation. To prevent race conditions, the host only writes non-zero values to this field, while the device only writes zero. The host controller should read this field prior to writing, and only write tog this field when it contains the value 00. Available operations are: 00 = Previous operation complete; new operation can be requested 01 = Request a phase step reset 10 = Request a phase step read 11 = Request a phase step write Phase step reset: Clears all previously applied phase steps. Phase step read: Read the current phase step offset for the specified output. The output divider to read is selected with registers 0x4BA-0x4BB (output_phase_step_mask), and only one bit should be set. The result is returned in registers 0x4BC-0x4BF (output_phase_step_data). The results are valid when this bitfield reads 00. The results are in the interval [–period/2, period/2], where period refers to the period of the output signal. Phase step write: Apply a phase step offset to the specified output(s) for the number of times specified in 0x4B9 (output_phase_-step_number). The output dividers to write are selected with registers 0x4BA-0x4BB (output_phase_step_mask), and multiple bits can be set. The desired phase step offset value must be written to registers 0x4BC-0x4BF (output_phase_step_data) prior to writing this field. Phase step writes are cumulative; subsequent phase steps are added to the previous accumulated phase step offset.

Address:	0x04B9	
Name:	output_phase_step_number	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	The number of phase steps to run. See "Phase step write" in 0x4B8 (output_phase_step_ctrl::op).

Address:	0x04BA:0x04BB	
Name:	output_phase_step_mask	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:10	reserved	—
9	output_9	See description for output_0.
8	output_8	See description for output_0.
7	output_7	See description for output_0.
6	output_6	See description for output_0.
5	output_5	See description for output_0.
4	output_4	See description for output_0.
3	output_3	See description for output_0.
2	output_2	See description for output_0.
1	output_1	See description for output_0.
0	output_0	Phase step operation enable mask for OUT0.

Address:	0x04BC:0x04BF	
Name:	output_phase_step_data	
Default:	0x00000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	Phase step in units of synthesizer clock cycles. When a phase step read is requested with tod_step=1 this register is expressed in ns. This register contains the argument or results of a phase step operation. See register 0x4B8 (output_phase_step_ctrl) for details. This register should not be read or written while a phase step operation is in progress. This register must only be read or written when register 0x4B8, bits 1:0 (output_phase_step_ctrl::op) is zero. The phase step contained in this register is a 32-bit 2's-complement signed integer. A positive value moves the output phase earlier in time (more to the left on a scope). A negative value moves the output phase later in time (more to the right on a scope). Note: when output_mode::signal_format is one of the CMOS N-pin divided modes, negative phase step writes are not supported. If a negative phase step is desired, add one OUTxN period to a negative value to get the equivalent positive value and do a phase step write of the positive value.

Address:	0x04FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x04FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 10, REF MB

Address:	0x0502:0x0503	
Name:	ref_mb_mask	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:10	reserved	—
9:0	mask	For a write operation (see ref_mb_sem::wr bit), this field determines which input reference's configuration is modified. Multiple bits can be set to affect multiple references in a single operation. For a read operation (see ref_mb_sem::rd bit), this field determines which input reference configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 for REF0P, bit 1 REF0N, etc.

Address:	0x0504	
Name:	ref_mb_sem	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	rd	When this bit is written to a one by the host controller, the device performs a read of the masked reference (see ref_mb_mask register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding input reference configuration.
0	wr	When this bit is written to a one by the host controller (and the read bit is zero), the device performs a write of the masked references (see ref_mb_mask register). All of the configuration options on this page are applied to each of the references indicated by the ref_mb_mask mask. The write is complete when this register reads back a zero.

Address:	0x0505:0x0506	
Name:	ref_freq_base	
Default:	0x61A8	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the input reference base frequency (Br), in Hz. The final expected input reference is given by: f_hz = Br * Kr * Mr / Nr Valid values for this registers must satisfy the rule 500 MHz divided by value is an integer. Some example frequency configurations are show below: Reference Frequency — ref_freq_base(Br) — ref_freq_mult(Kr) 8 kHz — 1 kHz (0x03E8) — 8 (0x0008) 19.44 MHz — 20 kHz(0x4E20) — 972 (0x03CC) 155.52 MHz — 20 kHz(0x4E20) — 7776 (0x1E60)

Address:	0x0507:0x0508	
Name:	ref_freq_mult	
Default:	0x03E8	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the input reference frequency multiple (Kr).

Address:	0x0509:0x050A	
Name:	ref_ratio_m	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the FEC ratio numerator (Mr).

Address:	0x050B:0x050C	
Name:	ref_ratio_n	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the FEC ratio denominator (Nr).

Address:	0x050D	
Name:	ref_config	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:6	vcm	This field in a REFxP mailbox register applies to both REFxP and REFxN. This field in a REFxN mailbox register is ignored. These bits specify the logic threshold V_{THRESH} for the receivers. When the ref_config::ac_couple bit is set to indicate an AC-coupled application, these bits also specify the internal DC bias voltage V_{BIAS}. These settings apply in both differential mode (ref_config::diff_en=1) and single-ended (diff_en=0) configurations. 00 = Set V_{THRESH} and optionally V_{BIAS} to 1.75V 01 = Set V_{THRESH} and optionally V_{BIAS} to 1.27V 10 or 11 = Set V_{THRESH} and optionally V_{BIAS} to 0.95V If the input signal is singled-ended CMOS, set the V_{CM} value to 1.75V/1.27V/0.95V for 3.3V/2.5V/1.8V CMOS, respectively. If the input is one side of a differential signal or a differential pair, if the signal's common-mode voltage matches one of the three settings above then the signal can be DC-coupled to the pin. Otherwise it should be AC-coupled. If the input is AC-coupled, the 1.75V V_{CM} setting is recommended. Note: Input swing cannot be higher than 3.3V. See Section 5.1.5 for detailed recommendations.
5	ac_couple	This field in a REFxP mailbox register applies to both REFxP and REFxN. This field in a REFxN mailbox register is ignored. 0 = The input signal is DC-coupled. Internal DC bias circuit is disabled. 1 = The input signal is AC-coupled. Internal DC bias circuit sets V_{BIAS} as specified by the ref_config::vcm field.
4	pre_divide	This field in a REFxP mailbox register applies to the REFxP/N differential pair or to REFxP singled-ended. This field in a REFxN mailbox register is ignored. There is no pre_divide control for REFxN pins. When this bit is set, the associated reference input clock is divided by 2 prior to being processed by the DPLLs. All register programming that requires information about this reference's frequency should be done with half of the actual input frequency. When cleared, the associated reference input is not divided prior to being processed by the DPLLs. This bit must be set when REF frequency is greater than 800 MHz.

3	invert	When this bit is set, the associated reference signal is internally inverted. In differential mode (ref_config::diff_en=1) the invert field in the REFxP mailbox register controls the behavior and the invert field in the REFxN mailbox register is ignored.
2	diff_en	This field in a REFxP mailbox register applies to both REFxP and REFxN. This field in a REFxN mailbox register is ignored. When this bit is set, the device expects a differential signal on the associated reference pins (REFxP and REFxN). When cleared, the device expects a single-ended signal on each of the associated REFxP and REFxN pins.
1	reserved	—
0	enable	When this bit is set, the phase acquisition module of the associated reference is enabled. When cleared, the associated phase acquisition module is disabled (powered down). In differential mode (ref_config::diff_en=1) the enable field in the REFxP mailbox register controls the behavior and the enable field in the REFxN mailbox register ignored.

Address:	0x050F	
Name:	ref_scm	
Default:	0x05	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	fine_en	0 = Regular SCM, SCM limits set by the limit field below. 1 = Fine SCM, SCM limits are set by the register at addresses 0x510-0x513 (ref_scm_fine). This feature can be enabled when the application requires a very small phase jump (<0.1% of input clock period) to be detected on a low frequency clock.
3	reserved	—
2:0	limit	Sets the regular Single Cycle Monitor (SCM) limit selection. When the reference fails the specified criteria, the scm bit in the associated ref_mon_status_x register is set. Selection: 000 = ±0.1% (percentage of input period) 001 = ±0.5% 010 = ±1% 011 = ±2% 100 = ±5% 101 = ±10% 110 = ±20% 111 = ±50% For example, ±10% SCM limit means input clock duty cycle (high time as percentage of clock period) must be in the range 40% to 60%. Note that measurement granularity is 0.5 ns. This imposes limitation to SCM limits that can be programmed depending on the input clock frequency: ±0.1% = can be programmed for frequencies below 2 MHz ±0.5% = below 10 MHz ±1% = below 20 MHz ±2% = below 40 MHz ±5% = below 100 MHz ±10% = below 200 MHz ±20% = below 400 MHz ±50% = below 1 GHz SCM indicator should not be used (should be masked) for reference frequencies above 1 GHz.

Address:	0x0510:0x0513	
Name:	ref_scm_fine	
Default:	0x00000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	Fine SCM limit configuration. The units of this register depend on the real system clock frequency, and can be calculated using the register at addresses 0x00B-0x00E (central_freq_offset). LSB = 0.5 ns * (2^32 + central_freq_offset) / 2^32 This field must be set to less than half of the reference signal period. Note: For 1 Hz and kHz input references, this field must be set larger than the input reference period multiplied by the worst-case frequency offset of the local oscillator connected to the OSCI pin or OSCB pin. For example, if the local oscillator frequency offset spec is ±50 ppm, that offset would lead to a 50 ppm measurement error of the input reference's period, which is 1s * 50 ppm = 50 µs. In this case ref_fine_scm must be set larger than 50 µs (50,000 ns) to avoid falsely invalidating the input reference due to frequency offset of the XO.

Address:	0x0514	
Name:	ref_cfm	
Default:	0x05	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	limit	Sets the Coarse Frequency Monitor (CFM) limit selection. When the reference fails the specified criteria, the cfm bit in the associated ref_mon_status_x register is set. Selection: 000 = ±0.1% (input frequency units) 001 = ±0.5% 010 = ±1% 011 = ±2% 100 = ±5% 101 = ±10% 110 = ±20% 111 = ±50%

Address:	0x0516:0x0517	
Name:	ref_gst_disqual	
Default:	0x0005	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the time to disqualify the reference after detecting either a CFM or SCM failure. If the Guard Soak Timer (GST) disqualify time expires and the source of the failure is still present, the gst bit in the associated ref_mon_status_s register is set. LSB = 10 ms

Address:	0x0518:0x0519	
Name:	ref_gst_qual	
Default:	0x0005	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the time to qualify the reference after both the CFM and SCM indicators are low. If the GST qualify timer expires without detecting a CFM or SCM failure, the gst bit in the associated ref_mon_status_n register is cleared. LSB = 10 ms

Address:	0x051A	
Name:	ref_meas_freq_period	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Sets the fixed-window time for REF-to-DPLL frequency measurement for this REF. LSB = 1 second. A value of 0 specifies averaging with the minimum fixed window time possible, but no minimum time is guaranteed.

Address:	0x051B	
Name:	ref_pfm_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	resolution	Sets the resolution and range of ref_pfm_disqualify (0x51C:0x51D) and ref_pfm_qualify (0x51E:0x51F). 0 = Resolution is 0.005 ppm, range is (±) 0.005 ppm to 327.675 ppm. 1 = Resolution is 0.05 ppm, range is (±) 0.05 ppm to 3276.75 ppm. PFM should not be configured greater than the maximum pull-in range for DPLLs (±2100 ppm). For reference frequency > 20 MHz precision may worse than one lsb. Precision is 1/((4 GHz/Freq)*2^24).

Address:	0x051C:0x051D	
Name:	ref_pfm_disqualify	
Default:	0xB3B0	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the Precise Frequency Monitor (PFM) disqualify frequency offset, where LSB is either 0.005 ppm or 0.05 ppm as specified by ref_pfm_ctrl::resolution. If a reference exceeds this offset, the pfm bit in the associated ref_mon_status_x register is set The default value is 230 ppm. Microchip recommends a –0.2 ppm guard band on the PFM disqualify threshold. It is recommended that this disqualify threshold be set smaller than the dpll tracking range set by the dpll_range mailbox register for each DPLL that may use the reference. This offset is with respect to the crystal or XO wired to the OSCI or OSCB pin.

Address:	0x051E:0x051F	
Name:	ref_pfm_qualify	
Default:	0x9C40	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the PFM qualify frequency offset, where LSB is either 0.005 ppm or 0.05 ppm as specified by ref_pfm_ctrl::resolution. If a reference is below this offset, the pfm bit in the associated ref_mon_status_x register is cleared The default value is 200 ppm. Microchip recommends a +0.2 ppm guard band on the PFM qualify threshold. Note that when the reference offset is between the qualify and disqualify limits (the two limits provide hysteresis), the state of the pfm bit in the ref_mon_status_x register is not changed. This offset is with respect to the crystal or XO wired to the OSCI or OSCB pin.

Address:	0x0520:0x0521	
Name:	ref_pfm_period	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	This is the observation time of the precise frequency monitor. Range 1 sec. to 2048 sec. with 1 sec. resolution. The default value of 0 represents 10 seconds. After a reference signal is applied to the device the PFM takes this duration to qualify the input.

Address:	0x0522	
Name:	ref_pfm_filter_limit	
Default:	0x28	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	The PFM filter limit represents a threshold. When the threshold is a non-zero value, and the difference between the PFM average filter output and 10 second PFM average is larger than this threshold, the PFM average filter is replaced by 10 second PFM average output. The purpose of this is to speed up the filter reaction. The default value corresponds to a 4 ppm filter limit. A value of 0 disables the filter limit check. Any other value is in units (or resolution) of 100 ppb. Thus the allowed range is 100 ppb to 25.5 ppm. It is recommended that PFM filter average time be larger than 10 sec. This threshold should be set to 0 (disabled) when the average time is smaller than 10 sec.

Address:	0x0528:0x052B	
Name:	ref_phase_offset_compensation	
Default:	0x00000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	Phase offset compensation for references. The value is specified as a 32-bit signed two's complement, in units of ps. A positive value moves the phase of any DPLL that locks to this reference earlier in time (more to the left on a scope). A negative value moves the phase of any DPLL that locks to this reference later in time (more to the right on a scope). Note: When a DPLL with hitless switching enabled (dpll_ctrl_x::tie_clear=0) switches to a REF, the ref_phase_offset_compensation value has no effect on DPLL phase. This is because in hitless switching the DPLL phase should not change regardless of the phase of the new REF. AFTER the DPLL has switched to the REF, any CHANGE in ref_phase_offset_compensation affects DPLL phase. Note: Microchip plans to change the size of this register from 4 bytes to 6 (0x0528:0x52D). Resolution will still be 1 ps, but range will expand from approximately ±2 ms to ±2 sec. When the device has register 0x004C bit 0 set to 1, the device has this size and range for this register.

Address:	0x052E	
Name:	ref_sync_ctrl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	pair	This bitfield is only used when the ref_sync_ctrl::mode bit-field is set to 0x1 (physical Ref-Sync pair mode enabled). This field indicates which input reference should be treated as the frame sync for the associated reference. An invalid value disables Ref-Sync pairing mode (i.e., the behavior of this reference is the same as though the mode bitfield is programmed to 0x0). 0=REF0P, 1=REF0N, etc. For example, if this bitfield is programmed to 0x5 for the REF0P mailbox, when a DPLL locks to REF0P, its output frame pulses is phase aligned with the frame pulse on REF2N.
3	reserved	—
2:0	mode	This field enables a frame sync input for the reference, and selects the source of the frame information: 0x0 = Ref-Sync pairing mode is disabled. 0x1 = Physical Ref-Sync pair mode is enabled. The frame sync clock phase information is derived from the reference clock indicated by the pair field, above. Other values reserved

Address:	0x052F	
Name:	ref_sync_misc	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	edge_sel	Sets the expected edge alignment of an input sync relative to its associated input reference (e.g., if REF0P uses REF2N as its sync, this bit must be configured in the REF2N mailbox). 0 = Sync is aligned to the rising edge of the associated input reference 1 = Sync is aligned to the falling edge of the associated input reference

Address:	0x0534:0x0535	
Name:	ref_gpi_select	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	bit	This field works with the page and offset field to select a single bit in the host register map. Specifically, this field selects the bit position of the selected register byte.
11:8	page	This field works with the bit and offset fields to select a single bit in the host register map. Specifically, this field selects the page.
7	reserved	—
6:0	offset	When GPI is configured to the control mode, this field works with the bit and page fields to select a single bit in the host register map. This field selects the offset within the page. If this GPI is already in Control mode, the new page and offset fields must refer to an appropriate register. Pointing to a status register, mailbox register or undefined register may cause the device to enter unknown states.

Address:	0x0536	
Name:	ref_gpi_config	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	This field determines the mode of operation for the GPI logic of this REF pin. If the GPI logic is to be set to the control mode, register 0x534-0x535 (gpi_select) should be set in the previous or in the same mailbox write. Otherwise, the GPI logic may affect device status by unintentionally controlling another host register bit. 000 = Input The logic value sensed on the REF pin is reflected in register 0x141-0x142 (gpi_in_status_3_0 and gpi_in_status_4). 010 = Control Certain device functions can be actively controlled via a REF's GPI logic. The device function to be controlled is selected by configuring register ref_gpi_select. Whenever a change is detected on the REF pin or the selected host register bit, the device ORs together the REF and register bit states before applying the corresponding configuration. In this mode, the selected host register bit must be a R/W type. Other values = Reserved (default to input mode) Note: the reference must be set to single-ended mode for GPI functionality. Note: An input reference can be forced into failure (LOS) through the GPI using the Control decode (010 above). In this case, ref_gpi_select should be configured for controlling the appropriate bit in ref_los_3_0 (0x200) or ref_los_4 (0x201).

Address:	0x057E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x057F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 12, DPLL MB

Address:	0x0602:0x0603	
Name:	dpll_mb_mask	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:8	reserved	—
7:0	mask	For a write operation (see dpll_mb_sem::wr bit), this field determines which DPLL's configuration is modified. Multiple bits can be set to affect multiple DPLLs in a single operation. For a read operation (see dpll_mb_sem::rd bit), this field determines which DPLL configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 for DPLL0, bit 1 for DPLL1, etc.

Address:	0x0604	
Name:	dpll_mb_sem	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	rd	When this bit is written to a one by the host controller, the device performs a read of the masked DPLL mailbox (see dpll_mb_mask register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding DPLL configuration.
0	wr	When this bit is written to a one by the host controller (and the rd bit is zero), the device performs a write of the masked DPLL mailbox(es) (see dpll_mb_mask register). All of the configuration options on this page are applied to each of the DPLLs indicated by the mask. The write is complete when this register reads back a zero.

Address:	0x0605	
Name:	dpll_config	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:6	ref_edge	Sets the DPLL selected reference edge sensitivity. 00 = Positive (rising) edge 01 = Negative (falling) edge 10 = Low pulse 11 = High pulse The low and high pulse options select the middle between edges.

5	ext_fb_en	0 = External feedback compensation disabled 1 = External feedback compensation enabled Before modifying this bit, all synths driven by this DPLL should be disabled. After modifying this bit, the synths can then be re-enabled. In external feedback (enabled when 0x2A4 bit 0 is set to 1) the DPLL specified in 0x2A5 bits 2:0 is the external feedback DPLL. See 0x2A4 description for additional details. The external feedback DPLL has a phase compensation applied that is equal to the difference in phase between the feedback input REF and the DPLL's uncompensated phase. When this dpll_config::ext_fb_en mailbox register bit is set to 1 for DPLLx, DPLLx also gets this phase compensation. If DPLLx is locked to the same REF as the external feedback DPLL then outputs from DPLLx are aligned with outputs from the external feedback DPLL (subject to synthesizer and output phase adjustment register settings). This bit has no effect for the external feedback DPLL.
4:0	reserved	—

Address:	0x0609	
Name:	dpll_fast_lock_ctrl	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:6	reserved	—
5:4	fcl_en	Frequency change limiting enable. 00 = FCL is disabled. 10 = FCL is enabled. x1 = FCL is disabled.
3	reserved	—
2	nco_en	Controls whether fast lock is forcibly disabled during transitions out of NCO mode. 0 = Fast lock is disabled during transitions out of NCO mode 1 = Fast lock is allowed during transitions out of NCO mode
1	force_en	This is the control to force-enable the fast lock state. Note that the master_en control (bit 0 of this register) still has to be enabled for this control to work. This control, when enabled, causes the DPLL to ignore the outputs of the frequency and phase error monitors.
0	master_en	0 = Fast lock state disabled 1 = Fast lock state enabled

Address:	0x060A:0x060B	
Name:	dpll_fast_lock_ideal_time	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Ideal time for fast lock in units of 0.01 sec. If the input wander is much lower than standard levels, this register can be reprogrammed to speed up the fast lock process. If this value is set to zero, the device uses a default value of 0.6 seconds. Note that this is the target time for fast lock which is usually the first step to lock to a reference.

Address:	0x060C:0x060D	
Name:	dpll_fast_lock_phase_rate	
Default:	0x07D0	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Fast lock phase rate-of-change limit and frequency offset limit. LSB = 1 µs/s = 1 ppm. This register controls the maximum phase rate-of-change and the maximum frequency offset this DPLL can apply while in the fast lock mode. The value should not exceed the default value (2000 µs/s = 2000 ppm) unless recommended by Microchip. Note: Microchip plans to change the resolution of this register from 1 µs/s = 1 ppm to 1 ns/s = 1 ppb and change the default value from 0x07D0 (which means 2000 µs/s = 2000 ppm) to 0x0000 (which indicates 2000 µs/s = 2000 ppm). When the device has register 0x004C bit 0 set to 1, the device has this new resolution and default value for this register.

Address:	0x060E:0x060F	
Name:	dpll_fast_lock_fcl	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Fast lock frequency change limit. When fast lock frequency change limiting is enabled by 0x609 bits 5:4 (dpll_fast_lock_ctrl::fcl_en), this field specifies the maximum rate-of-change of frequency offset during fast lock. LSB = 1 ppb/s. The default value of 0x0000 specifies 2000 ppb/s = 2 ppm/s.

Address:	0x0610:0x0611	
Name:	dpll_fast_lock_phase_err	
Default:	0x0100	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	This is the phase error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 250 ns, with a value of zero being reserved for disabling the phase error threshold check.

Address:	0x0612	
Name:	dpll_fast_lock_freq_err	
Default:	0x04	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	This is the frequency error threshold for triggering a transition to fast-lock. The threshold is specified in steps of 1ppm, programmable from 1 ppm to 255 ppm. If the threshold is programmed to zero, the fast-lock frequency error check is disabled.

Address:	0x0620	
Name:	dpll_bw_fixed	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	bw	Sets the DPLL loop filter corner frequency. 000 = 14 Hz 001 = 29 Hz 010 = 61 Hz 011 = 141 Hz 100 = 403 Hz 101-111 = Reserved

Address:	0x0622:0x0623	
Name:	dpll_psi	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the phase slope limit, in units of ns/s. The range is 1 ns/s to 65535 ns/s. A value of 0 sets the PSL to "unlimited". For very low frequency inputs such as 1 Hz, the DPLL should select a small PSL value such as 885 ns/s. If fast-lock is disabled then PSL must be set larger than twice the worst-case input frequency offset. If fast-lock is enabled then when a fast-lock phase or frequency threshold is exceeded then PSL is disabled during fast-lock.

Address:	0x0626	
Name:	dpll_damping	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4:0	factor	Sets the DPLL damping factor. 0 = 5 1 = 1 2 = 2 3 = 2.998801 4 = 4.003204 5 = 5 (default, peaking <0.1 dB) 6 = 6.019293 7 = 7.0014 8 = 8.006408 9 = 8.980265 10 = 10 11 = 10.91089 12 = 12.12678 13 = 12.90994 14 = 13.8675 15 = 15.07557 16 = 15.81139 17 = 16.66667 18 = 17.67767 19 = 18.89822 20 = 20.41241 21 = 22.36068 22 = 25 23 = 28.86751 24 = 35.35534 25-31 = 50

Address:	0x0627	
Name:	dpll_duration_good	
Default:	0x09	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	DPLL phase magnitude must be less than dpll_phase_-good for the duration specified by this field for the DPLL to declare lock. The desired duration and the dpll_duration_-good value are related as follows: duration[sec] = dpll_duration_good + 1 The default value (0x09) is 10 sec.

Address:	0x0628:0x062B	
Name:	dpll_phase_good	
Default:	0x02255100	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	Sets the phase for lock declaration, LSB=1ps. The default value (0x02255100) is 36 µs. The DPLL's phase offset must be less than this value for the duration programmed in register 0x627 (dpll_duration_good).

Address:	0x062C:0x062F	
Name:	dpll_phase_bad	
Default:	0x02255100	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	Sets the phase for loss-of-lock, LSB = 1 ps. The default value (0x02255100) is 36 µs. Any time the DPLL's phase offset is greater than this value, the DPLL lock indicator goes low. Programming this register to 0x00000000 internally sets the value using registers 0x628 (dpll_phase_-good).

Address:	0x0645:0x0646	
Name:	dpll_range	
Default:	0x0BB8	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Sets the pull-in/hold-in range, in steps of 0.1 ppm. (from 0.1 ppm to 2100 ppm, in 0.1 ppm steps). Default value corresponds to 300 ppm.

Address:	0x0648:0x064C	
Name:	dpll_df_offset_manual	
Default:	0x0000000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Manual delta frequency offset adjustment for DPLL loop. If the DPLL is in free run, holdover or NCO mode, this additional frequency offset will be applied to the DPLL output. If the DPLL is lock state, this offset may cause the DPLL to lose lock. This signed value is specified in steps of 2^–48. The frequency offset should be calculated as per formula: f_offset = –(X/2^48)*f_nom where, X is 2's complement number specified in this register, f_nom is the nominal output frequency and f_offset is the desired frequency offset to the output.

Address:	0x064D:0x064E	
Name:	dpll_tie_wr_thresh	
Default:	0x0002	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	This register specifies the threshold for declaring a TIE Write operation has completed. When the output has moved within the threshold of the expected alignment position, then the dpll_tie_wr_sticky register indicates that the TIE Write operation has completed. When this register is programmed to the default of 0x0000, the sticky bits in dpll_tie_wr_sticky are never set. Otherwise, a non-zero value specifies the threshold in 1 ns steps (1 ns to 65.535 µs range).

Address:	0x064F	
Name:	dpll_lock_delay	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Sets the lock declaration delay time. The actual delay time is the square of the value written to this register, giving a range of 0 to 255^2, in seconds. A value of 0 disables the lock delay timer.

Address:	0x0650	
Name:	dpll_ref_sw_mask	
Default:	0x08	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	This bit acts as an enable mask for the PFM failure reference switch. When this bit is set, a PFM failure of the selected reference causes the associated DPLL to perform a reference switch. When the bit is cleared, a PFM failure is ignored by the reference switch algorithm (a switch to holdover may still be possible, see the dpll_ref_ho_mask::pfm bitfield for details). Note that the DPLL also does not switch to a reference which has a PFM failure while either the PFM reference switch or holdover mask bits are set.
3	gst	This bit acts as an enable mask for the GST failure reference switch. See pfm bit description.
2	cfm	This bit acts as an enable mask for the CFM failure reference switch. See pfm bit description.
1	scm	This bit acts as an enable mask for the SCM failure reference switch. See pfm bit description.
0	los	This bit acts as an enable mask for the LOS failure reference switch. See pfm bit description.

dpll_ref_prio_x

Address:	0x0652	
Name:	dpll_ref_prio_0	
Default:	0x10	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	ref_0N	When the DPLL is in automatic mode of operation (see dpll_mode_refsel_x::mode bitfield), these bits set the priority of each reference for the DPLL. 0000 is highest priority and 1110 is lowest priority. Setting these bits to 1111 disables the reference (the DPLL never locks to it). When two references are programmed to have different priority numbers, the DPLL performs revertive switching between them: the DPLL always switches to the highest priority reference (lowest priority number) whenever that reference is qualified. When two references are programmed to have the same priority number, the DPLL performs non-revertive switching between them: the DPLL does not switch to the reference with the same priority when that reference qualifies. Combinations of same and different priority numbers can be used, such that DPLL performs revertive switching between different priority references, but non-revertive switching among references with the same priority. Example: if REF0P has priority 0 (highest), REF0N, REF1P and REF1N have priority 1. Whenever REF0P is qualified, the DPLL switches to it. If REF0P is disqualified, the DPLL does not change the currently selected reference (e.g., REF1N) even if another reference with the same priority is qualified (e.g., REF0N or REF1P). Priority of REF0N.
3:0	ref_0P	Priority of REF0P.

Address:	0x0653	
Name:	dpll_ref_prio_1	
Default:	0x32	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	ref_1N	Priority of REF1N.
3:0	ref_1P	Priority of REF1P.

Address:	0x0654	
Name:	dpll_ref_prio_2	
Default:	0x54	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	ref_2N	Priority of REF2N.
3:0	ref_2P	Priority of REF2P.

Address:	0x0655	
Name:	dpll_ref_prio_3	
Default:	0x76	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	ref_3N	Priority of REF3N.
3:0	ref_3P	Priority of REF3P.

Address:	0x0660	
Name:	dpll_ref_ho_mask	
Default:	0x17	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	When set to high, this bit allows PFM failures from the selected reference to cause this DPLL to go to holdover. When low, PFM failure is masked and this DPLL does not go to holdover due to the PFM failure. A switch to holdover is only attempted after all reference switching options have been exhausted, regardless of the state of the dpll_ref_ho_mask bits.
3	gst	This bit acts as an enable mask for the GST holdover switch. See pfm bit description.
2	cfm	This bit acts as an enable mask for the CFM holdover switch. See pfm bit description.
1	scm	This bit acts as an enable mask for the SCM holdover switch. See pfm bit description.
0	los	This bit acts as an enable mask for the LOS holdover switch. See pfm bit description.

Address:	0x0668	
Name:	dpll_fp_first_realign	
Default:	0x7F	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	reserved	—
6:0	time	When the DPLL is configured to lock to a Ref-Sync pair (frame pulse), it performs phase measurements of the frame pulse and aligns its phase based on this measurement. This parameter sets the time between the first and second frame pulse phase measurements. LSB = 1 second. Values 0 and 1 are invalid. See register 0x52E, bits 3:0 (ref_sync_ctrl::mode) for additional details about reference configuration. See register 0x669, bits 6:0 (dpll_fp_realign_intvl::time) for details about periodic phase measurements.

Address:	0x0669	
Name:	dpll_fp_realign_intvl	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	continuous	0 = Continuous Ref-Sync measurement disabled. The time bitfield in this register is used. 1 = Continuous Ref-Sync measurement enabled. The DPLL measures the Ref-Sync offset and realign as fast as possible. The time bitfield in this register is ignored.
6:0	time	When the DPLL is configured to lock to a Ref-Sync pair (frame pulse), it performs phase measurements of the frame pulse and aligns its phase based on this measurement. This parameter sets the time between the periodic phase measurements, which occur after the second measurement. LSB = 1 second. If this bitfield is programmed to zero, periodic realignment is disabled. See register 0x52E, bits 3:0 (ref_sync_ctrl::mode) for additional details about reference configuration. See register 0x668, bits 6:0 (dpll_fp_first_realign::time) for details about first and second phase measurements.

Address:	0x066A:0x066B	
Name:	dpll_fp_lock_thresh	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	When the DPLL is configured to lock to a Ref-Sync pair or eSync (frame pulse), it performs phase measurements of the frame pulse and aligns its phase based on this measurement. This parameter sets the phase threshold to declare lock and is logcially ANDed with all other lock criteria. LSB = 1 ns. A value of 0x00 disables this feature. When the active input is clock-only, this parameter is ignored. See register 0x52E, bits 3:0 (ref_sync_ctrl::mode) for additional details about reference configuration.

Address:	0x066C	
Name:	dpll_fp_sync_mask	
Default:	0xFF	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:5	reserved	—
4	pfm	When set to high, PFM failures from the selected sync input prevent this DPLL from performing Ref-Sync measurement and alignment. When low, this DPLL performs ref-sync alignment regardless of whether the sync input PFM passes or fails.
3	gst	This bit acts as an enable mask to allow GST failures to prevent Ref-Sync alignment. See pfm bit description.
2	cfm	This bit acts as an enable mask to allow CFM failures to prevent Ref-Sync alignment. See pfm bit description.
1	scm	This bit acts as an enable mask to allow SCM failures to prevent Ref-Sync alignment. See pfm bit description.
0	los	This bit acts as an enable mask to allow LOS failures to prevent Ref-Sync alignment. See pfm bit description.

Address:	0x067E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	pfm	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x067F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^{2}C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 13, SYNTH MAILBOX

Address:	0x0682:0x0683	
Name:	synth_mb_mask	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:5	reserved	—
4:0	mask	For a write operation (see synth_mb_sem::wr bit), this field determines which synth's configuration is modified. Multiple bits can be set to affect multiple synths in a single operation. For a read operation (see synth_mb_sem::rd bit), this field determines which synth configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 for Synth0, bit 1 for Synth1, etc.

Address:	0x0684	
Name:	synth_mb_sem	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—

1	rd	When this bit is written to a one by the host controller, the device performs a read of the masked synth mailbox (see synth_mb_mask register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding synth configuration.
0	wr	When this bit is written to a one by the host controller (and the read bit is zero), the device performs a write of the masked synth mailbox(es) (see synth_mb_mask register). All of the configuration options on this page are applied to each of the synth indicated by synth_mb_mask. The write is complete when this register reads back a zero.

Address:	0x0686:0x0687	
Name:	synth_freq_base	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the synthesizer base frequency (Bs), in Hz. The final frequency is given by: fsynth = Bs x Ks x Ms / Ns Valid values for this registers must satisfy the rule 500 MHz divided by value is an integer. The synthesizer clock frequency has to satisfy the following range: 187.5 MHz ≤ fsynth ≤ 750 MHz. If the central frequency offset (central_freq_offset register) is non-zero, the range is affected accordingly. In addition, some margin is needed to accommodate any frequency variations, such as when the DPLL driving this synthesizer is in lock, holdover or NCO mode. Typically this register can be left at its default value of 1 Hz and the synthesizer frequency can be fully specified by the synth_freq_mult, synth_freq_m and synth_freq_n registers.

Address:	0x0688:0x068B	
Name:	synth_freq_mult	
Default:	0x12A05F20	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	Sets the synthesizer frequency multiplier (Ks). See synth_freq_base description for more information.

Address:	0x068C:0x068D	
Name:	synth_freq_m	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the synthesizer frequency numerator (Ms). See synth_freq_base description for more information.

Address:	0x068E:0x068F	
Name:	synth_freq_n	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Sets the synthesizer frequency numerator (Ns). See synth_freq_base description for more information.

Address:	0x0690:0x0691	
Name:	synth_phase_compensation	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Specifies the amount of initial phase shift that is applied to this synthesizer when the synthesizer is turned on. This number is a 16-bit signed integer with LSB of 1 ps. After the first time a non-zero value is written to this register, the actual synthesizer phase has an offset, in ps, of 389000/vco*(12-vco)/vco where vco is the actual VCO frequency in GHz. For example 303ps for 12114.21MHz.This offset is consistent and can be compensated by adding the offset to the desired phase and writing the result to the register. Note that this offset is not present when the device is first configured from flash after power-up or reset.or when the device is configured by loading a config file using the GUI after power-up or reset. In those cases it will only be present if a new value is written to this register.

Address:	0x0692	
Name:	synth_align_compensation	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—

2:0	align_comp_select	The propagation delay from synthesizer to output is slightly different depending on signal format and whether the output divider is used (div>1) or bypassed (div=1). For applications that need I/O delay to be as close as possible to zero, the user must decide, on a per-synthesizer basis, which output type (listed in the decodes below) is compensated as close as possible to zero. Since often not all synthesizers are needed for the frequency plan, one application tactic is to use an otherwise-unused synthesizer for outputs of a second type. Example: Outputs from DPLL0 are both differential and single-ended, and the system design really needs both types to have I/O delay as close to zero as possible. The application can connect both SynthA and SynthB to DPLL0, connect differential outputs to SynthA, set SynthA 0x692 to 0=differential, connect CMOS outputs to SynthB, and set SynthB 0x692 to 1=CMOS. Then both sets of outputs are compensated. Internal delay settings are shown in parentheses below. 000 = Differential outputs from the output divider (1788 ps) 001 = CMOS outputs from the divider (2858 ps) 010 = Differential outputs, divider bypassed (div=1) (1747 ps) 011 = CMOS outputs, divider bypassed (div=1) (2872 ps) 100 = CMOS outputs, N-pin divide mode (2970 ps) 101 = No compensation (0 ps) 110, 111 = Reserved

Address:	0x0694	
Name:	synth_spread_spectrum_cfg	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:1	reserved	—
0	mode	Spread spectrum mode: 0 - Center mode 1 - Down mode In both modes, the synthesizer frequency starts at the nominal frequency configured for the synthesizer. In the center mode, the frequency linearly sweeps down half of the peak-to-peak spread, then up the whole peak-to-peak spread then back to the nominal frequency. In the down mode, the frequency linearly sweeps down the whole peak-to-peak spread then back to the nominal frequency. The peak-to-peak spread is specified by the synth_spread_spectrum_spread register (0x0697). The period of this frequency modulation is specified by the synth_spread_spectrum_rate register (0x0695 to 0x0696).

Address:	0x0695:0x0696	
Name:	synth_spread_spectrum_rate	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:0	—	Spread spectrum modulate rate in 250 Hz units. The valid range is 25 kHz to 55 kHz (100 to 220 decimal for the register value).

Address:	0x0697	
Name:	synth_spread_spectrum_spread	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Peak-to-peak spread of synthesizer frequency, in 0.025% units.The valid range is 0.025% to 5% (1 to 200 decimal for the register value).

Address:	0x06FE	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x06FF	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

REGISTER LIST PAGE 14, OUTPUT MAILBOX

Address:	0x0702:0x0703	
Name:	output_mb_mask	
Default:	0x0001	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15:10	reserved	—
9:0	mask	For a write operation (see output_mb_sem::wr bit), this field determines which output's configuration is modified. Multiple bits can be set to affect multiple outputs in a single operation. For a read operation (see output_mb_sem::rd bit), this field determines which output configuration to read back from the device. One (and only one) bit should be set for a read operation. Bit 0 for OUT0, bit 1 for OUT1, etc.

Address:	0x0704	
Name:	output_mb_sem	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—

1	rd	When this bit is written to a one by the host controller, the device performs a read of the masked output mailbox (see output_mb_mask register). Only one mask bit should be set in this case. When this register reads back 0x00, then the read has completed, and the host can read back any or all of the registers on this page to determine the corresponding output configuration.
0	wr	When this bit is written to a one by the host controller (and the read bit is zero), the device performs a write of the masked output mailbox(es) (see output_mb_mask register). All of the configuration options on this page are applied to each of the outputs indicated by the mask. The write is complete when this register reads back a zero.

Address:	0x0705	
Name:	output_mode	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	signal_format	0000 = Disabled (High Impedance, Low Power Mode) 0001 = LVDS mode (V_{OD} internally set to 400 mV, output_driver_level::vod ignored, V_{CM} set by output_driver_config::vcm which defaults to 1.2V) 0010 = Differential mode (V_{OD} set by output_driver_level::vod, V_{CM} set by output_driver_config::vcm) 0011 = Low-V_{CM} mode (approx. 0.375V V_{CM}, approx. 0.75V V_{OD}) Must set output_driver_level::vod to 0x9, 0xA, 0xB, or 0xC (0xC recommended), output_driver_config::vcm to 0xF, and output_driver_config::regv to 0xD. 0100 = Two CMOS, OCxN in phase with OCxP 0101 = One CMOS, OCxP Enabled, OCxN High impedance 0110 = One CMOS, OCxP High impedance, OCxN Enabled 0111 = Two CMOS, OCxN inverted vs. OCxP 10xx = Reserved 1100 = Two CMOS, N-pin divide mode, OCxN in phase with OCxP 1101 = Reserved 1110 = Reserved 1111 = Two CMOS, N-pin divide mode, OCxN inverted vs. OCxP CMOS signal amplitude for OUTx is set by VDDx supply voltage (1.5V, 1.8V, 2.5V, or 3.3V).
3	polarity	1 = Inverted 0 = Normal Not applicable to N-pin divide modes.
2:0	clock_type	000 = Normal clock Other values reserved

Address:	0x0706	
Name:	output_driver_level	
Default:	0x52	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:4	vod	This field specifies the differential output voltage (V_{OD}) for the differential output driver. In the device this field actually controls driver output current: 0000 = 3 mA, 0001 = 4 mA, etc. When the specified current is driven into the required external 100Ω termination resistor, the voltage across the termination resistor is the desired V_{OD}. V_{OD} is equivalent to the single-ended voltage swing of the OUT0P pin or the OUT0N pin. This field is ignored for CMOS signal formats. Programmable differential signal format, DC-coupled, internal 200Ω bias resistor disabled, 100Ω termination at receiver: 0000 = 330 mV 0001 = 440 mV 0010 = 550 mV 0011 = 660 mV 0100 = 770 mV (recommended for LVPECL) 0101 = 880 mV (default) 0110 = 990 mV 0111-1111 = Do not use Programmable differential signal format, AC-coupled, internal 200Ω bias resistor enabled, 100Ω termination at receiver: 000x = Do not use 0010 = 367 mV 0011 = 440 mV 0100 = 513 mV 0101 = 587 mV (default) 0110 = 660 mV 0111 = 733 mV 1000 = 807 mV 1001 = 880 mV 1010-1111 = Do not use When output_mode::signal_format=0001 (LVDS), V_{OD} is internally set to 440 mV and this field is ignored. When output_mode::signal_format=0011 (Low-V_{CM}), set this vod field to 0x9, 0xA, 0xB, or 0xC (0xC recommended). The bias resistor is enabled/disabled by output_driver_config::rbias (0x0707:0x0708).

3:2	vddo	This field specifies the power supply voltage externally applied to the VDDOx pin (where x is the OUTx number, 0 to 9). The device does not do anything with this value, but the GUI and system software can use this field to indicate the VDDOx voltage and then compare it to the internal regulator voltage (output_driver config::regv). In general, GUI and system software must ensure regulator voltage ≤ VDDOx voltage – 0.5V. For the special case of LVDS signal format with VDDOx = 1.8V, the 0.5V term can be reduced to 0.3V. VDDOx of 1.5V is only valid for CMOS signal formats. VDDOx of 1.8V is only valid for LVDS and CMOS signal formats 00 = 3.3V 01 = 2.5V 10 = 1.8V 11 = 1.5V
1:0	drive	Output driver CMOS level. 00 = 1x 01 = 2x 10 = 3x 11 = 4x The 3x and 4x settings are recommended for lowest-jitter applications. This field is ignored for non-CMOS signal formats. Typical output impedances of the CMOS driver are listed below.The trace impedance and parasitics must be taken into account when choose an external source series resistor value VDDO = 3.3V, Drive = 4x: 18Ω VDDO = 3.3V, Drive = 3x: 23Ω VDDO = 3.3V, Drive = 2x: 33Ω VDDO = 3.3V, Drive = 1x: 65Ω VDDO = 2.5V, Drive = 4x: 20Ω VDDO = 2.5V, Drive = 3x: 27Ω VDDO = 2.5V, Drive = 2x: 39Ω VDDO = 2.5V, Drive = 1x: 80Ω VDDO = 1.8V, Drive = 4x: 28Ω VDDO = 1.8V, Drive = 3x: 37Ω VDDO = 1.8V, Drive = 2x: 55Ω VDDO = 1.8V, Drive = 1x: not recommended VDDO = 1.5V, Drive = 4x: 29Ω VDDO = 1.5V, Drive = 3x|2x|1x: not recommended

Address:	0x0707:0x0708	
Name:	output_driver_config	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	vreg1p1_vsel	Output pad 1.1V regulator voltage select. Leave this field at its default value unless recommended by Microchip. 000 = 1.10V (default) 001 = 0.95V 010 = 1.00V 011 = 1.05V 100 = 0.90V 101 = 1.15V 110 = 1.20V 111 = 1.25V
11:8	rbias	This field enables/disables an internal bias resistor between OUTxP and OUTxN. When the output driver is in LVDS or programmable differential mode and the device is AC-coupled to the receiver, the output driver requires a DC path between OUTxP and OUTxN. This resistor can provide that DC path. This field should be set to 0 for CMOS and Low-V_{CM} signal formats. 0000 = None 0001 = approx. 200Ω 0002 to 1111 = None
7:4	regv	Output driver regulator voltage. This value must be > V_{CM} + 0.5V_{OD} + 0.5V except for the case of LVDS with VDDOx = 1.8V for which this field should be set to 0. This field should be set to 0 for CMOS signal formats. 0000 = Center voltage close to 2.2V (default) 1000 = 2.28V 1001 = 2.37V 1010 = 2.45V 1011 = 2.56V 1100 = 2.67V 1101 = 2.79V (Use this value when signal format = Low-V_{CM})
3:0	vcm	Output driver common mode voltage 0000 = 1.2V (default) - recommended for LVDS and AC-coupled 0100 = 1.0V 0101 = 1.1V 0110 = 1.3V 0111 = 1.4V 1000 = 1.5V 1001 = 1.6V 1010 = 1.8V 1011 = 1.9V 1100 = 2.0V - typical for DC-coupled LVPECL 1101 = 2.1V 1110 = 2.2V 1111 = Use this decode only if signal format = Low-V_{CM} This field is ignored for CMOS signal formats.

Address:	0x070C:0x070F	
Name:	output_div	
Default:	0x00000002	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	The divider of the output clock. Expressed as the number of synthesizer clock cycles. The value 0 is undefined. The value 1 bypasses the output divider and pulse width logic and passes the synthesizer frequency directly to the output driver.

Address:	0x0710:0x0713	
Name:	output_width	
Default:	0x00000002	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	The pulse width of the output clock. Expressed as the number of 1/2 synthesizer clock cycles. Valid range has a minimum of 2 (half cycles, i.e. 1 cycle) and a maximum of output_div * 2 – 1 (half cycles). This field is ignored when output_div (0x70C-0x70F) is less than 2.

Address:	0x0714:0x0717	
Name:	output_esync_period	
Default:	0x00000002	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	For N-pin divide modes, the period of the N-pin clock. Expressed as the number of output divider clock cycles. The values 0 and 1 are undefined. This field is ignored when output_div (0x70C-0x70F) is less than 2.

Address:	0x0718:0x071B	
Name:	output_esync_width	
Default:	0x00000002	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	For N-pin divide modes, the pulse width of the N-pin divided clock. Expressed as the number of 1/2 output clock cycles (instead of synthesizer clock cycles). This field is ignored when output_div (0x70C-0x70F) is less than 2.

Address:	0x0720:0x0723	
Name:	output_phase_compensation	
Default:	0x00000000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
31:0	—	Output phase shift, expressed in ½ synth clock cycles. Two-complement signed integer. A positive value moves the phase of the output later in time (more to the right on a scope). A negative value moves the phase earlier in time (more to the left on a scope). Note: non-zero values are not supported when output_-mode::signal_format is one of the CMOS N-pin divided modes or when output_mode::clock_type is one of the embedded sync options. To make an output pair with this configuration later than other outputs, consider moving the other outputs earlier instead. Another option is to put the output pair on its own synthesizer and use synthesizer phase adjustment (synth_phase_compensation register).

Address:	0x0724	
Name:	output_gpo_en	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:2	reserved	—
1	out_n	0 = The output is driven by the divided clock. 1 = The output is driven according to Register 0x72A (output_gpo_config_out_n).
0	out_p	0 = The output is driven by the divided clock. 1 = The output is driven by according to Register 0x727 (output_gpo_config_out_p).

Address:	0x0725:0x0726	
Name:	output_gpo_select_out_p	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—
14:12	bit	This field works with the page and offset fields to select a single bit in the host register map. Specifically, this field selects the bit position in the selected register byte.
11:8	page	This field works with the bit and offset fields to select a single bit in the host register map. Specifically, this field selects the page.
7	reserved	—

6:0	offset	When this GPO is configured to the status mode, this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page.

Address:	0x0727	
Name:	output_gpo_config_out_p	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	This field determines the mode of operation for this GPO. If the GPO is to be set to status mode, Register 0x725-0x726 (gpo_select) should be set in the previous or in the same mailbox write. 001 = Output GPOx actively drives the value specified in register gpo_out (0xF0-0xF2), where x = output index * 2. 011 = Status The device status can be actively supervised via GPOx. The device mirrors the host register bit, specified in register output_gpo_select_out_p, onto GPOx. Typically, the selected host register bit is a status bit (either R or S type) in this mode. 100 = IRQ GPOx is an interrupt request (IRQ) output, as configured in Register 0x080 (gpio_irq_config). No matter how many GPIOs and GPOs are configured to IRQ mode, only the GPIO or GPO most recently configured generates interrupts. If the latest GPIO or GPO is then configured to other modes, the next latest GPIO or GPO becomes active and generate interrupts. GPIO interrupt is disabled only if all the GPIOs and GPOs are set to non-IRQ modes. Other values = Reserved Note: To use the above modes, the output must be set to CMOS (Register 0x705, bit 7:4, output_mode: signal_format) with GPO enabled (Register 0x724, bit 0, output_gpo_en:out_p).

Address:	0x0728:0x0729	
Name:	output_gpo_select_out_n	
Default:	0x0000	
Type:	R/W	
Bit Field	**Function Name**	**Description**
15	reserved	—

14:12	bit	This field works with the page and offset fields to select a single bit in the host register map. Specifically, this field selects the bit position in the selected register byte.
11:8	page	This field works with the bit and offset fields to select a single bit in the host register map. Specifically, this field selects the page.
7	reserved	—
6:0	offset	When this GPO is configured to the status mode, this field works with the bit and page fields to select a single bit in the host register map. Specifically, this field selects the offset within the page.

Address:	0x072A	
Name:	output_gpo_config_out_n	
Default:	0x01	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:3	reserved	—
2:0	ctrl	This field determines the mode of operation for this GPO. If the GPO is to be set to status mode, Register 0x728-0x729 (output_gpo_select_out_n) should be set in the previous or in the same mailbox write. 001 = Output GPOx actively drives the value specified in register gpo_out (0xF0-0xF2), where x = output index * 2 + 1. 011 = Status The device status can be actively supervised via GPOx. The device mirrors the host register bit, specified in register output_gpo_select_out_n, onto GPOx. Typically, the selected host register bit is a status bit (either R or S type) in this mode. 100 = IRQ GPOx is an interrupt request (IRQ) output, as configured in Register 0x080 (gpio_irq_config). No matter how many GPIOs and GPOs are configured to IRQ mode, only the GPIO or GPO most recently configured generates interrupts. If the latest GPIO or GPO is then configured to other modes, the next latest GPIO or GPO becomes active and generate interrupts. GPIO interrupt is disabled only if all the GPIOs and GPOs are set to non-IRQ modes. Other values = Reserved Note: To use the above modes, the output must be set to CMOS (Register 0x705, bit 7:4, output_mode: signal_format) with GPO enabled (Register 0x724, bit 1, output_gpo_en:out_n).

Address:	0x077E	
Name:	uport	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7	lockout	When set, this field causes all other uport registers to be read-only. When zero, all registers are open for writing.
6:1	reserved	—
0	status	This field indicates if microport attempted access was been successful. The register content is 0x00 if the access was successful.

Address:	0x077F	
Name:	page_sel	
Default:	0x00	
Type:	R/W	
Bit Field	**Function Name**	**Description**
7:0	—	Unsigned binary value of these bits represents selected page for SPI/I^2C access: 0x00 = page 0 (first 128 bytes) 0x01 = page 1 (second 128 bytes) 0x02 = page 2 (third 128 bytes) 0x03 = page 3 (fourth 128 bytes) 0x04 = page 4 (fifth 128 bytes) 0x05 = page 5 (sixth 128 bytes) 0x06 = page 6 (seventh 128 bytes) 0x07 = page 7 (eighth 128 bytes) 0x08 = page 8 (ninth 128 bytes) 0x09 = page 9 (tenth 128 bytes) 0x0A = page 10 (eleventh 128 bytes) 0x0B = page 11 (twelfth 128 bytes) 0x0C = page 12 (thirteenth 128 bytes) 0x0D = page 13 (fourteenth 128 bytes) 0x0E = page 14 (fifteenth 128 bytes) 0x0F = page 15 (sixteenth 128 bytes) 0x10-0xFF = reserved

9.0 ELECTRICAL CHARACTERISTICS

TABLE 9-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, nominal 1.8V	VDD18	–0.3	+1.98	V
Supply Voltage, nominal 3.3V	VDD33	–0.3	+3.6	V
Supply voltage, nominal 1.8V, 2.5V, or 3.3V	VDDIO	–0.3	+3.6	V
Supply voltage, nominal 1.5V, 1.8V, 2.5V, or 3.3V	VDDOx	–0.3	+3.6	V
Voltage on any pin	VPIN	–0.3	+3.6	V
Storage Temperature Range	T_{ST}	–55	+125	°C

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
*Voltages are with respect to ground (VSS) unless otherwise stated.

Note 1: The typical values listed in the tables of Section 10 are at nominal voltage and room temperature and are not production tested.

2: Specifications to –40°C and +85°C are guaranteed by design or characterization and not production tested.

TABLE 9-2: RECOMMENDED DC OPERATING CONDITIONS

Min. and max. values in all electrical tables below are over these operating conditions.					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**
Supply Voltage 3.3V	VDD33	3.135	3.3	3.465	V
Supply Voltage 1.8V	VDD18	1.71	1.8	1.89	V
Output Supply Voltage	VDDOx	1.425	1.5	1.575	V
		1.71	1.8	1.89	
		2.375	2.5	2.625	
		3.135	3.3	3.465	
Digital I/O Supply Voltage	VDDIO	1.71	1.8	1.89	V
		2.375	2.5	2.625	
		3.135	3.3	3.465	
Operating Temperature	T_A	–40	—	+85	°C

TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS

Characteristics		Symbol	Min.	Typ. (Note 1)	Max.	Units	Notes
Total power, two CMOS REF inputs, Synth1 and six LVDS outputs enabled		P_{DISS}	—	0.8	—	W	—
Total current, 3.3V supply (VDD33+VDDOx pins)		I_{DD33}	—	160	322	mA	Note 2
Total current, 1.8V supply (VDD18 pins)		I_{DD18}	—	207	519	mA	Note 2
Supply current change from enabling or disabling:							
the crystal driver circuit	VDD33	ΔI_{DD33_XO}	—	3	—	mA	—
	VDD18	ΔI_{DD18_XO}	—	7	—	mA	—
the crystal doubler	VDD33	ΔI_{DD33_DBL}	—	0	—	mA	—
	VDD18	ΔI_{DD18_DBL}	—	2	—	mA	—
a single-ended REFxP or N input pin	VDD33	ΔI_{DD33_REFC}	—	3.5	—	mA	Measured at 180 MHz
	VDD18	ΔI_{DD18_REFC}	—	3	—	mA	

TABLE 9-3: ELECTRICAL CHARACTERISTICS: SUPPLY CURRENTS (CONTINUED)

Characteristics		Symbol	Min.	Typ. (Note 1)	Max.	Units	Notes
a differential REFxP/N input pair	VDD33	ΔI_{DD33_REFD}	—	4	—	mA	Measured at 700 MHz
	VDD18	ΔI_{DD18_REFD}	—	5	—	mA	
a synthesizer	VDD33	ΔI_{DD33_SYN}	—	0.5	—	mA	—
	VDD18	ΔI_{DD18_SYN}	—	27	—	mA	Note 7
an OUTxP/N output pair, LVDS	VDDOx	ΔI_{DDOL}	—	12	—	mA	156.25 MHz, Note 5
			—	18	—	mA	700 MHz, Note 6
an OUTxP/N output pair, LVPECL	VDDOx	ΔI_{DDOL}	—	14	—	mA	156.25 MHz, Note 5
			—	21	—	mA	700 MHz, Note 6
an OUTxP/N output pair, Low-Vcm	VDDOx	ΔI_{DDOL}	—	25	—	mA	156.25 MHz, Note 8
an OUTxP/N output pair, CMOS	VDDOx	ΔI_{DDOC}	—	3	—	mA	25 MHz, Note 3
an OUTxP/N output pair, CMOS	VDDOx	ΔI_{DDOC}	—	29	—	mA	250 MHz, Note 4

Note 1: Typical values measured at nominal supply voltages and 25°C ambient temperature.

2: Max I_{DD} measurements made with all blocks enabled, 49.152 MHz crystal doubled as system clock, 156.25 MHz signals on all REF inputs, all synthesizers enabled, all output dividers dividing by 4, all outputs enabled as LVPECL outputs (with output_driver_level::vod=0x5) driving 156.25 MHz signals, all VDDO at 3.3V, and 200Ω differential bias resistors enabled for all output pairs. Typical I_{DD} measurements made with same setup as max. I_{DD} but only four REF inputs enabled, two synthesizers enabled, six outputs enabled with LVDS signal format, and 200Ω differential bias resistors disabled.

3: VDDOx=3.3V, 1x drive strength, f_O=25 MHz, 18 pF load per pin. Specifies the current for the OUTxP/N pair. Divide by 2 for per-pin current.

4: VDDOx=3.3V, 1x drive strength, f_O=250 MHz, 18 pF load per pin. Specifies the current for the OUTxP/N pair. Divide by 2 for per-pin current.

5: Tested at 156.25 MHz. With internal 200Ω bias resistor disabled or enabled (driver is constant current).

6: Tested at 700 MHz. With internal 200Ω bias resistor disabled or enabled (driver is constant current).

7: Tested with all synthesizers at 312.5 MHz.

8: Tested with 50Ω to ground load on each of OUTxP and OUTxN. Internal 200Ω bias resistor must be disabled for Low-V_{CM} mode.

TABLE 9-4: ELECTRICAL CHARACTERISTICS: OSCB SYSTEM CLOCK INPUT

This table covers the case when there is no external crystal connected and an external oscillator or clock signal is connected to OSCB.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Single-ended input high voltage, OSCB	V_{IH}	1.3	—	—	V	—
Single-ended input low voltage, OSCB	V_{IL}	—	—	0.75	V	—
Input frequency, OSCB	f_{IN}	9.72	—	200	MHz	Note 2
Input frequency, OSCB	f_{IN}	200+	—	400	MHz	Note 3
Input leakage current	I_{IL}	–10	—	10	µA	—
Input duty cycle	—	40	—	60	%	Note 1

Note 1: 1.1V threshold.

2: OSCB frequencies below 48 MHz cause higher output jitter all else being equal.

3: Must have sys_apll_source_config::div set to divide by 2 or more for OSCB frequencies > 200 MHz.

TABLE 9-5: ELECTRICAL CHARACTERISTICS: REFERENCE INPUTS, REFxP/N

Characteristics		Symbol	Min.	Typ.	Max.	Units	Notes
Single-ended input reference voltage and internally provided DC bias		V_{REF-SE}		0.95		V	Configurable by register field Note 2
				1.27		V	
				1.75		V	
Single-ended input high voltage, DC-coupled	V_{REF-SE}=0.95V	V_{IH-SE}	1.06	—	—	V	
	V_{REF-SE}=1.27V		1.39	—	—	V	
	V_{REF-SE}=1.75V		1.89	—	—	V	
Single-ended input low voltage, DC-coupled	V_{REF-SE}=0.95V	V_{IL-SE}	—	—	0.86	V	
	V_{REF-SE}=1.27V		—	—	1.155	V	
	V_{REF-SE}=1.75V		—	—	1.592	V	
Single-ended input high voltage, AC-coupled		$V_{IH-SE-AC}$	V_{REF-SE} + 0.1	—	—	V	Note 3, See Figure 9-1
Single-ended input low voltage, AC-coupled		$V_{IL-SE-AC}$	—	—	V_{REF-SE} – 0.1	V	
Single-ended input leakage current		I_{IL-SE}	–10	—	10	µA	V_I = V_{DD} or 0.8V, Note 4
Differential input common mode voltage		V_{CMI}	0.8	—	2.3	V	Note 1
Differential input voltage difference		V_{ID}	0.1	—	2.0	V	See Figure 9-1
Differential input leakage current		I_{IL}	–10	—	10	µA	V_I = V_{DD33} or 0, Note 4
Input hysteresis		—	—	30	—	mV	

Note 1: Each REFxP and REFxN pin has an internal 78.6 kΩ pull-up resistor to 2.5V and an internal pull-down resistor to VSS to bias the pin. For V_{CMI} = 1.27V the pull-down resistor is 73.7 kΩ. For V_{CMI} = 1.75V the pull-down resistor is 158 kΩ. These resistors can easily be overdriven by external circuitry to set a different common mode voltage anywhere in the V_{CMI} range as needed for the application. LVDS signals with 1.2V common mode voltage can be DC-coupled (ref_config::ac_couple=0). Other differential signals should be AC-coupled (ref_config::ac_couple=1) with ref_config::vcm=00 for 1.75V internal DC bias or 01 for 1.27V internal DC bias.)

2: Each REF pin has an internal 78.6 kΩ pull-up resistor to 2.5V and an internal pull-down resistor to VSS to bias the pin. For V_{REF-SE} = 0.95V the pull-down resistor is 44.2 kΩ. For V_{REF-SE} = 1.27V the pull-down resistor is 73.7 kΩ. For V_{REF-SE} = 1.75V the pull-down resistor is 158 kΩ. Set ref_config::ac_couple=0 for the DC-coupled case. ref_config::vcm controls internal DC bias and V_{REF-SE}.

3: Set ref_config::ac_couple=1 for the AC-coupled case. Set ref_config::vcm=00 for 1.75V internal DC bias and V_{REF-SE}. Set ref_config::vcm=01 for 1.27V internal DC bias and V_{REF-SE}

4: These specs apply when ref_config::ac_couple=0 and therefore internal bias is disabled. When internal bias is enabled, see Note 2 for the internal bias resistor sizes.

5: See Figure 5-3 for internal details of the REF receiver circuitry.

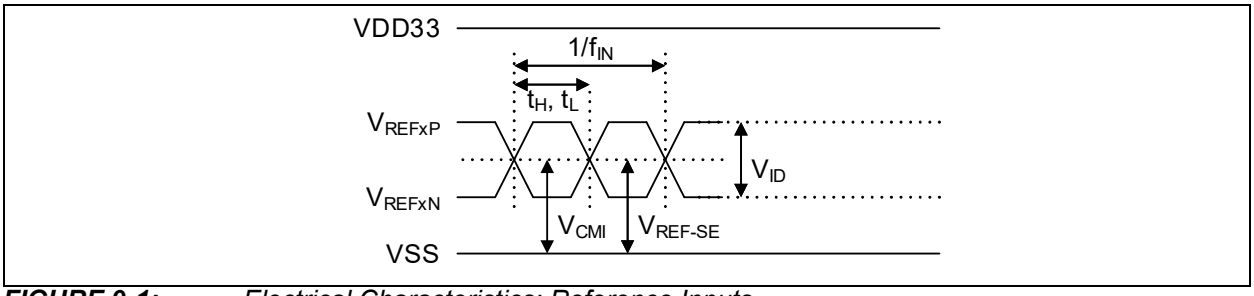


FIGURE 9-1: *Electrical Characteristics: Reference Inputs.*

TABLE 9-6: ELECTRICAL CHARACTERISTICS: OTHER INPUTS AND I/O (BIDIRECTIONAL)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, SCK_SCL and SI_SDA in I^2C Mode	V_{IH}	0.7 x V_{DDIO}	—	—	V	—
Input low voltage, SCK_SCL and SI_SDA in I^2C Mode	V_{IL}	—	—	0.3 x V_{DDIO}	V	—
Input high voltage, RST_B	V_{IH}	2.0	—	3.6	V	—
Input low voltage, RST_B	V_{IL}	–0.3	—	0.8	V	—
Input high voltage, all other digital inputs, SCK_SCL and SI_SDA (in SPI mode), SO_IF1, CS_B_IF0, all GPIOx_ACx	V_{IH}	2.0	—	3.6	V	V_{DDIO} = 3.3V±5%
		1.7	—	3.6	V	V_{DDIO} = 2.5V±5%
		1.3	—	3.6	V	V_{DDIO} = 1.8V±5%
Input low voltage, all other digital inputs, SCK_SCL and SI_SDA (in SPI mode), SO_IF1, CS_B_IF0, all GPIOx_ACx	V_{IL}	–0.3	—	0.8	V	V_{DDIO} = 3.3V±5%
		–0.3	—	0.7	V	V_{DDIO} = 2.5V±5%
		–0.3	—	0.55	V	V_{DDIO} = 1.8V±5%
Input leakage current, RST_B	I_{IL}	–100	—	10	µA	V_I = 0 – V_{DD33}, Note 1
Input leakage current, CS_B_IF0	I_{IL}	–100	—	10	µA	V_I = 0 – V_{DDIO}, Note 1
Input leakage current, SCK_SCL, SI_SDA, SO_IF1	I_{IL}	–10	—	10	µA	V_I = 0 – V_{DDIO}, Note 1
Input leakage current, all GPIOx_ACx	I_{IL}	–10	—	100	µA	V_I = 0 – V_{DDIO}, Note 1
Input capacitance	C_{IN}	—	3	10	pF	—
Input hysteresis, SCK_SCL and SI_SDA in I^2C Mode	—	0.05 x V_{DDIO}	—	—	mV	—
Input hysteresis, all other digital inputs: RST_B, SCK_SCL and SI_SDA (in SPI mode), SO_IF1, CS_B_IF0, all GPIOx-_ACx	—	—	50	—	mV	—
Output leakage (when high impedance)	I_{LO}	–10	—	10	µA	V_I = 0 – V_{DDIO}, Note 1
GPIOx_ACx, CSB_IF0 and SO_IF1 to RST_B setup time	t_{SU}	50	—	—	ns	—
GPIOx_ACx, CSB_IF0 and SO_IF1 to RST_B hold time	t_{HD}	—	—	0	ns	—

Note 1: Positive leakage is current flowing into the device.

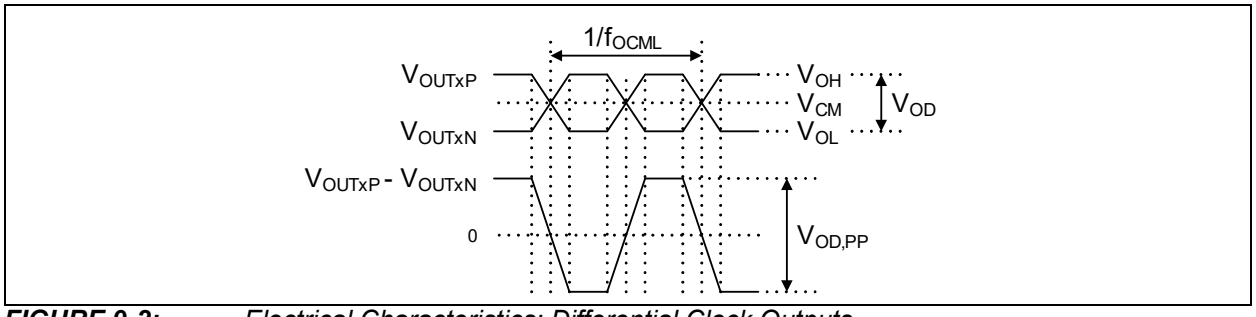


FIGURE 9-2: *Electrical Characteristics: Differential Clock Outputs.*

TABLE 9-7: ELECTRICAL CHARACTERISTICS: OUTP/N LVDS CLOCK OUTPUTS

VDDOx = 1.8V±5% or 2.5V±5% or 3.3V±5% for LVDS operation.							
Characteristics		**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Output frequency		f_{OCD}	—	—	750	MHz	—
Output common-mode voltage	VDDO=2.5V or 3.3V	V_{CM}	1.1	1.2	1.3	V	Note 1, Note 2, Note 3 See Figure 9-2
	VDDO=1.8V		0.7	0.9	1.1	V	
Output differential voltage		V_{OD}	320	430	537	mV	Note 1, Note 2, Note 3, See Figure 9-2
Output differential swing, peak-to-peak		$V_{OD,PP}$	640	860	1074	mV_{PP}	Note 1, Note 2 See Figure 9-2
Output rise/fall time		t_R, t_F	—	175	—	ps	20% to 80%
Output duty cycle		—	45	50	55	%	—

Note 1: Measured with 100Ω between OUTxP and OUTxN. Application notes: Output must have 100Ω to 200Ω DC path between OUTxP and OUTxN for proper operation. See Figure 5-7 for recommended external components. When the output signal is AC-coupled an internal 200Ω bias resistor can be switched into the circuit using output_driver_config::rbias to meet this requirement. When this 200Ω resistor is in parallel with 100Ω differential termination at the receiver, the actual V_{OD} amplitude is 2/3 of the number shown above. If larger amplitude is needed, the output should be configured for programmable differential mode where V_{OD} is configurable and V_{CM}=1.2V.

2: With output_mode::signal_format=1 (LVDS) and output_driver_config::vcm=0x0. Differential output common-mode voltageis programmable. See Section 5.6.1.

3: Must have output_driver_config::regv=0 for LVDS with VDDOx=1.8V. Power supply noise rejection may not be as good for LVDS with VDDOx=1.8V compared with VDDOx=2.5V or 3.3V

TABLE 9-8: ELECTRICAL CHARACTERISTICS: OUTP/N LVPECL CLOCK OUTPUTS

VDDOx = 2.5V±5% or 3.3V±5% for LVPECL operation.						
Characteristics	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Output frequency	f_{OCD}	—	—	750	MHz	—
Output common-mode voltage, VDDOx=3.3V	V_{CM}	1.80	1.90	2.05	V	Note 1, Note 2, Figure 9-2
Output common-Mode voltage, VDDOx=2.5V	V_{CM}	1.1	1.2	1.3	V	Note 1, Note 2, Figure 9-2
Output differential voltage	V_{OD}	600	780	1000	mV	Note 1, Note 2, Figure 9-2
Output differential swing, peak-to-peak	V_{OD}	1200	1560	2000	mV_{PP}	Note 1, Note 2, Figure 9-2
Output rise/fall time	t_R, t_F	—	185	—	ps	20% - 80%
Output duty cycle	—	45	50	55	%	—

Note 1: Measured with 100Ω between OUTxP and OUTxN. Application notes: Output must have 100Ω to 200Ω DC path between OUTxP and OUTxN for proper operation. See Figure 5-7 for recommended external components. When the output signal is AC-coupled an internal 200Ω bias resistor can be switched into the circuit using output_driver_config::rbias to meet this requirement. When this 200Ω resistor is in parallel with 100Ω differential termination at the receiver, the actual V_{OD} amplitude is 2/3 of the number shown above. If larger amplitude is needed, the output should be configured for programmable differential mode where V_{OD} is configurable.

2: With output_mode::signal_format=2 (programmable differential) and output_driver_level::vod=0x4. With output_driver_config::vcm=0x0 for 2.5V and 0xC for 3.3V. Differential output common-mode voltage and differential voltage (i.e. signal amplitude) are programmable. See Section 5.6.1

TABLE 9-9: ELECTRICAL CHARACTERISTICS: OUTP/N LOW-VCM CLOCK OUTPUTS

VDDOx = 3.3V±5% for Low-V_{CM} operation.						
Characteristics	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Output frequency	f_{OCD}	—	—	160	MHz	—
Output common-mode voltage	V_{CM}		V_{OD} / 2		V	Note 1, Figure 9-2
Output differential voltage	V_{OD}	600	810	1000	mV	Note 1, Figure 9-2
Output rise/fall time	t_R, t_F	—	310	—	ps	20% to 80%
Output duty cycle	—	45	50	55	%	Note 2

Note 1: Each of OUTxP and OUTxN with 50Ω termination resistor to ground. With output_mode::signal_format=0x3, output_driver_level::vod=0xC, output_driver_config::vcm=0xF and output_driver_config::regv=0xD.

2: Duty cycle measured differentially.

TABLE 9-10: ELECTRICAL CHARACTERISTICS: OUTP/N CMOS CLOCK OUTPUTS

Characteristics	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Output frequency	f_{OCMOS}	—	—	250	MHz	Note 1
Output high voltage	V_{OH}	VDDOx – 0.4	—	—	V	Note 2
Output low voltage	V_{OL}	—	—	0.4	V	Note 2
Output rise/fall time, VDDOx=1.8V, 4x drive strength	t_R, t_F	—	0.4	—	ns	2 pF load, Note 3
Output rise/fall time, VDDOx=1.8V, 4x drive strength		—	1.2	—	ns	15 pF load, Note 3
Output rise/fall time, VDDOx=3.3V, 1x drive strength		—	0.7	—	ns	2 pF load, Note 3
Output rise/fall time, VDDOx=3.3V, 1x drive strength		—	2.2	—	ns	15 pF load, Note 3
Output duty cycle	—	45	50	55	%	—
Output current when output disabled	I_{OH}	—	660	—	µA	—

Note 1: For VDDOx=1.5V, maximum CMOS output frequency is 160 MHz for a 10 pF load and 125 MHz for a 15 pF load.

2: For VDDOx=3.3V and 1x drive strength, I_O=3.5 mA. For VDDOx=1.8V and 4x drive strength, I_O=7 mA.

3: Measured 20% to 80%.

TABLE 9-11: ELECTRICAL CHARACTERISTICS: OTHER OUTPUTS AND I/O (BIDIRECTIONAL)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Bidirectional output high voltage for SO_IF1 and GPIO[4:0]_AC[4:0] pins	$V_{OH-BIDI}$	2.4	—	—	V	V_{DDIO} = 3.3V±5% I_{OH} = 18 mA
		1.7	—	—	V	V_{DDIO} = 2.5V±5% I_{OH} = 13 mA
		1.35	—	—	V	V_{DDIO} = 1.8V±5% I_{OH} = 4 mA
Bidirectional output low voltage for SO_IF1 and GPIO[4:0]_AC[4:0] pins	$V_{OL-BIDI}$	—	—	0.4	V	V_{DDIO} = 3.3V±5% I_{OL} = 12 mA
		—	—	0.7	V	V_{DDIO} = 2.5V±5% I_{OL} = 14 mA
		—	—	0.45	V	V_{DDIO} = 1.8V±5% I_{OL} = 6 mA
Bidirectional output low voltage for SI_SDA (I^2C mode) V_{DDIO} = 3.3V or V_{DDIO} = 2.5V	V_{OL1}	—	—	0.4	V	I_{OL} = 3 mA
Bidirectional output low voltage for SI_SDA (I^2C mode) V_{DDIO} = 1.8V	V_{OL2}	—	—	0.2 x V_{DDIO}	V	I_{OL} = 2 mA
Bidirectional output low current for SI_SDA (I^2C mode)	I_{OL}	3	—	—	mA	V_{OL} = 0.4V
		5.1	—	—	mA	V_{OL} = 0.6V

TABLE 9-12: ELECTRICAL CHARACTERISTICS: REF INPUT TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
CMOS input reference frequency for REFxP or REFxN	$1/t_{TREFP}$	—	—	300	MHz	—
Single-pin differential input reference frequency for REFxP or REFxN	$1/t_{TREFP}$	—	—	400	MHz	—
Differential input reference frequency for REFxP/N	$1/t_{TREFP}$	—	—	1250	MHz	—
CMOS or single-pin differential input reference pulse width low or high for REFxP or REFxN	t_{TREFW}	1.25	—	—	ns	—
Differential input reference pulse width low or high for REF[4:0]P/N	t_{TREFW}	0.4	—	—	ns	—

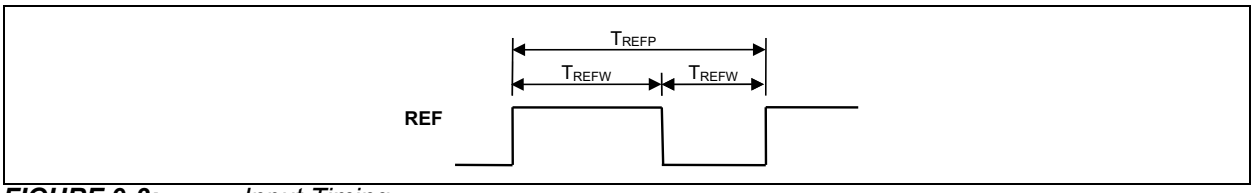


FIGURE 9-3: *Input Timing.*

TABLE 9-13: ELECTRICAL CHARACTERISTICS: Ref-Sync PAIR INPUT TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Sync lead time	$t_{SYNC-LD}$	0	—	$t_{REFP}/2 - t_{UNCERT}$	ns	See Figure 9-4
Sync lag time	$t_{SYNC-LG}$	0	—	$t_{REFP}/2 - t_{UNCERT}$	ns	
Sync alignment uncertainty	t_{UNCERT}	0		1	ns	

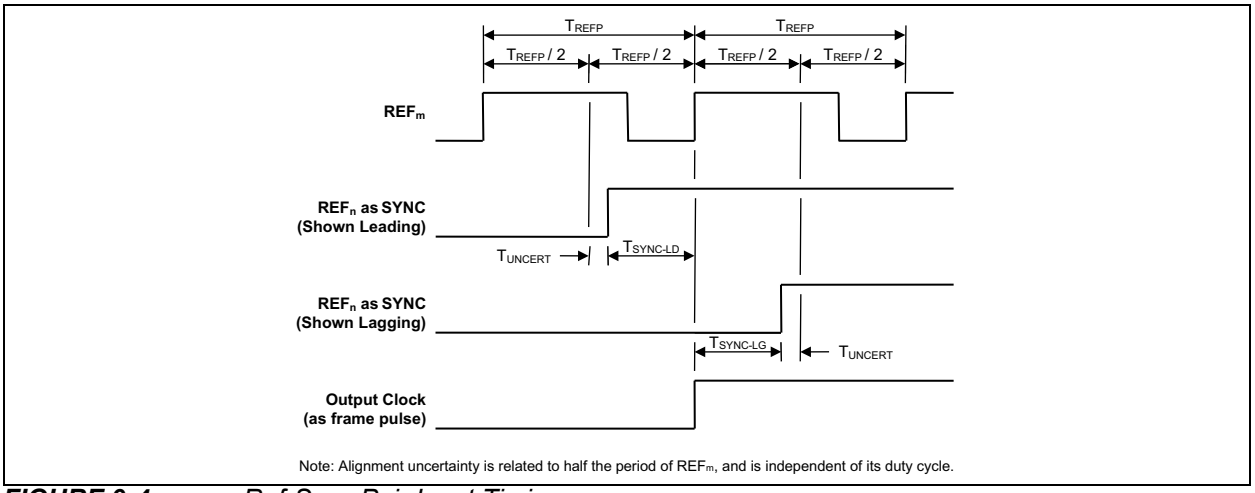


FIGURE 9-4: *Ref-Sync Pair Input Timing.*

TABLE 9-14: ELECTRICAL CHARACTERISTICS: INPUT-TO-OUTPUT AND OUTPUT-TO-OUTPUT TIMING

Characteristics		Symbol	Min.	Typ.	Max.	Units	Notes
Initial Delay and Skew							Note 1, 4
Input reference to CMOS output delay		t_{D-IO-C}	–510	0	430	ps	Note 1, 4, 6
Input reference to CMOS output delay, ext FB		$t_{D-IO-C-EFB}$	–250	0	240	ps	Note 1, 4, 6, 8
Input reference to diff output delay		t_{D-IO-D}	–360	0	350	ps	Note 1, 4, 7
Input reference to diff output delay, ext FB		$t_{D-IO-D-EFB}$	–75	0	110	ps	Note 1, 4, 7, 8
Synthx OUTa to Synthx OUTb skew	Differential	t_{OO-S}	—	40	100	ps	Note 1, 3, 4, 7
	CMOS		—	50	170	ps	Note 1, 3, 4, 6
Synthx OUTa to Synthy OUTb skew	Differential	t_{OO-S-S}	—	50	105	ps	Note 1, 3, 4, 7
	CMOS		—	50	180	ps	Note 1, 3, 4, 6
Delay and Skew Variation							Note 1, 5
Input reference to CMOS output delay variation		$t_{DV-IO-C}$	—	300	365	ps	Note 1, 5, 6
Input reference to CMOS output delay, variation ext FB		$t_{DV-IO-C-EFB}$	—	110	160	ps	Note 1, 5, 6
Input reference to diff output delay variation		$t_{DV-IO-D}$	—	145	200	ps	Note 1, 5, 7
Input reference to diff output delay, variation ext FB		$t_{DV-IO-D-EFB}$	—	30	60	ps	Note 1, 5, 7
SynthX OUTa to SynthX OUTb skew variation	Differential	t_{OOV-S}	—	8	30	ps	Note 1, 3, 5, 7
	CMOS		—	13	60	ps	Note 1, 3, 5, 6
	Diff-CMOS		—	30	110	ps	Note 1, 5, 6, 7
SynthX OUTa to SynthY OUTb skew variation	Differential	$t_{OOV-S-S}$	—	8	35	ps	Note 1, 3, 5, 7
	CMOS		—	13	60	ps	Note 1, 3, 5, 6

Note 1: All specs in this table tested with SynthX following DPLLX for X = 0 to 4, 25 MHz I/O frequencies. Input signal format and feedback signal format are always the same as output signal format in all tests. When an input is CMOS signal format it is 3.3V with rise time equivalent to OUTxP/N CMOS mode with 3x drive strength. When an input is differential format it is equivalent to OUTxP/N programmable differential mode with 1.2V V_{CM} and 800 mV V_{OD}.

2: Only applies for outputs that have the same load/termination.

3: Only applies for outputs that have the same signal format, VDDO voltage, drive strength, and loading/termination. For 2xCMOS outputs, only measured for OUTxP.

4: Initial delay and skew numbers indicate the timing relationships among the signals just after the device has been configured. Measurement is done at the same temperature and voltage used for configuration.

5: Delay and skew variation numbers indicate how the timing relationships among the signals change as the already-configured device is exposed to all combinations of min., typ., and max. V_{DD} (all supplies varied at the same time) and min., room, and max. temperature without resetting or reconfiguring the device. The values shown are zero-to-peak numbers, i.e. half the peak-to-peak value of max. measurement minus min. measurement. Max. is largest zero-to-peak number over devices. Typ. is average zero-to-peak number over devices.

6: Tested with output configured as 2xCMOS with 3x drive strength and VDDOx = 3.3V.

7: Tested with output configured as programmable differential format with 1.2V V_{CM} and 800 mV V_{OD}.

8: Initial input-to-output delay numbers for external feedback configuration are dependent on the propagation delay of the external feedback path. The number shown above are with the external feedback path propagation delay measured in advance and calibrated out using the per-REF phase adjustment capability provided in the ref_phase_offset_compensation mailbox register.

TABLE 9-15: ELECTRICAL CHARACTERISTICS: SPI INTERFACE TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
SCLK frequency	f_{SCLK}	—	—	12.5	MHz	See Figure 9-5 & Figure 9-6
SCLK period	t_{cyc}	80	—	—	ns	
SCLK high time	t_{clkh}	40	—	—	ns	
SCLK low time	t_{clkl}	40	—	—	ns	
SI setup time to SCLK rising edge	t_{rxs}	8	—	—	ns	
SI hold time from SCLK rising edge	t_{rxh}	8	—	—	ns	
SO data valid time from SCLK falling edge	t_{xd}	—	—	25	ns	
CS_B rise to output high impedance	t_{ohz}	—	—	60	ns	
CS_B setup to SCLK falling edge (LSB first)	t_{cssi}	16	—	—	ns	See Figure 9-5
CS_B hold from SCLK rising edge (LSB first)	t_{cshi}	8	—	—	ns	
CS_B setup to SCLK rising edge (MSB first)	t_{cssm}	16	—	—	ns	See Figure 9-6
CS_B hold from SCLK falling edge (MSB first)	t_{cshm}	8	—	—	ns	

Note 1: Values are over Recommended Operating Conditions.

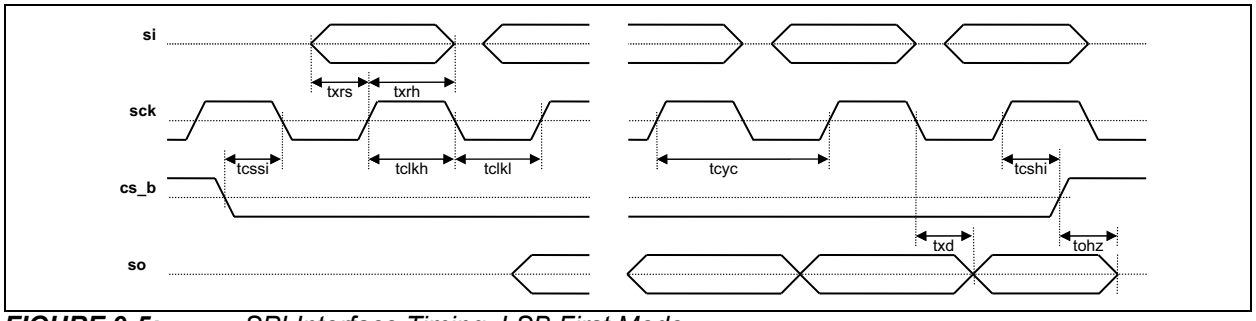


FIGURE 9-5: *SPI Interface Timing, LSB First Mode.*

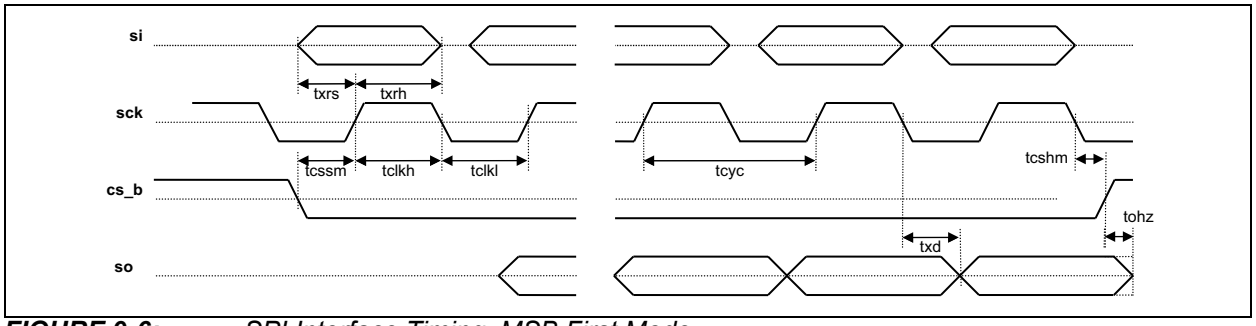


FIGURE 9-6: *SPI Interface Timing, MSB First Mode.*

TABLE 9-16: ELECTRICAL CHARACTERISTICS: I²C INTERFACE TIMING

VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%						
Characteristics	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
SCL clock frequency	f_{SCL}	—	—	400	kHz	Note 1
Hold time, START condition	$t_{HD;STA}$	0.6	—	—	µs	—
Low time, SCL	t_{LOW}	1.3	—	—	µs	—
High time, SCL	t_{HIGH}	0.6	—	—	µs	—
Setup time, START condition	$t_{SU;STA}$	0.6	—	—	µs	—
Data hold time	$t_{HD;DAT}$	0	—	—	µs	Note 2
Data valid time	$t_{VD;DAT}$	—	—	0.9	µs	—
Data valid acknowledge time	$t_{VD;ACK}$	—	—	0.9	µs	—
Data setup time	$t_{SU;DAT}$	100	—	—	ns	—
Rise time, SCL and SDA	t_r	—	—	300	ns	—
Fall time, SCL and SDA input	t_f	20 x (V_{DDIO}/5.5)	—	300	ns	—
Fall time, SDA output	t_{of}	20 x (V_{DDIO}/5.5)	—	250	ns	—
Setup time, STOP condition	$t_{SU;STO}$	0.6	—	—	µs	—
Bus free time between STOP/START	t_{BUF}	1.3	—	—	µs	—
Spike suppression, SCL and SDA inputs	t_{SP}	0	—	50	ns	—
Pin capacitance, SCL and SDA	C_p	—	—	10	pF	—
Bus capacitance, SCL and SDA	C_b	—	—	400	pF	—

Note 1: Characteristics in this table apply to Fast-mode with f_{SCL} ≤ 400 kHz. The device may be used in a Standard-mode system with f_{SCL} ≤ 100 kHz and t_r ≤ 1000 ns. The device does not stretch SCL. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 9-6).

2: The device internally provides an output hold time of at least 300 ns for SDA (with respect to the V_{IHmin} of the SCL) to bridge the undefined region (V_{IHmin} to V_{ILmax}) of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.

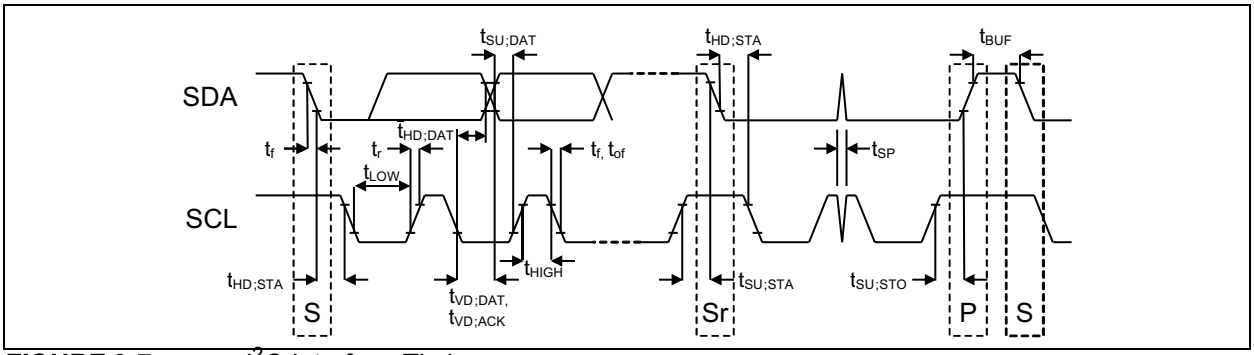


FIGURE 9-7: *I²C Interface Timing.*

10.0 PERFORMANCE CHARACTERISTICS

TABLE 10-1: DPLL PERFORMANCE CHARACTERISTICS

Characteristics	Min.	Typ.	Max.	Units	Notes
Pull-in/Hold-in Range	0.1	12	2100	ppm	Programmable
Lock Time (Bandwidth > 10 Hz)	—	1.6	2	sec	Unlimited phase slope limit 10 µs/1 sec. lock selection ±200 ppm pull-in/hold range
Reference Switching MTIE	—	0.6	—	ns	Bandwidth = 14 Hz jitter-free input (1 ps_{RMS})
Entry into Holdover MTIE	—	0.6	—	ns	
Exit from Holdover MTIE	—	0.6	—	ns	
Holdover Accuracy (Bandwidth > 10 Hz)	—	2	10	ppb	—
Damping Factor	1	5	50	—	Programmable
Phase gain in the pass band	—	0.08	0.1	dB	Damping factor set to 5

TABLE 10-2: OUTPUT CLOCK JITTER GENERATION – OUTXP/N DIFFERENTIAL

Characteristics	Test Conditions	Min.	Typ.	Max.	Units
Phase Jitter, 156.25 MHz (114.285 MHz XO)	10 kHz to 1 MHz, Note 1, Note 2	—	75	120	fs_{RMS}
	12 kHz to 20 MHz, Note 1, Note 2	—	102	145	fs_{RMS}
Phase Jitter, 156.25 MHz (49.152 MHz crystal doubled)	10 kHz to 1 MHz, Note 1, Note 4	—	68	—	fs_{RMS}
	12 kHz to 20 MHz, Note 1, Note 4	—	101	—	fs_{RMS}
Phase Jitter, 156.25 MHz (49.152 MHz crystal not doubled)	10 kHz to 1 MHz, Note 1, Note 4	—	89	—	fs_{RMS}
	12 kHz to 20 MHz, Note 1, Note 4	—	119	—	fs_{RMS}
Phase Jitter, 156.25 MHz (49.152 MHz XO)	10 kHz to 1 MHz, Note 1, Note 3	—	99	—	fs_{RMS}
	12 kHz to 20 MHz, Note 1, Note 3	—	128	—	fs_{RMS}
Period Jitter, 100 MHz	Note 1, Note 2, Note 5	—	10	—	ps_{PP}
Phase Jitter, 312.5 MHz (114.285 MHz XO)	12 kHz to 20 MHz, Note 1, Note 2	—	87	—	fs_{RMS}
Phase Jitter, 625 MHz (114.285 MHz XO)	12 kHz to 20 MHz, Note 1, Note 6	—	82	—	fs_{RMS}
Cycle-to-Cycle Jitter, 100 MHz	Note 1, Note 2, Note 5	—	10	—	ps

Note 1: Tested with VDDOx = 3.3V and programmable differential mode with V_{OD} = 800 mV and V_{CM} = 1.2V.

2: With Vectron VCC1-9004-114M285 XO connected to OSCB pin and +2 ppm frequency offset for the output signal w.r.t. the XO. APLL dividers set for 53x2=106 and xo_config::passclk=1, synth frequency 312.5 MHz.

3: With Vectron VCC1-1545-49M152 XO connected to OSCB pin and +2 ppm frequency offset for the output signal w.r.t. the XO. APLL dividers set for 27x9=243 and xo_config::passclk=1, synth frequency 312.5 MHz.

4: With Vectron VXM7-1361-49M1520000 crystal connected to OSCI/OSCO pins and +2 ppm frequency offset for the output signal w.r.t. the crystal. For crystal doubled case, APLL dividers set for 41x3=123. For the not-doubled case, xo_config::passclk=1, synth frequency 312.5 MHz.

5: N=10000. Measured using Tektronix MSO71604C, Mixed Signal Oscilloscope with DPOJET software.

6: With Vectron VCC1-9004-114M285 XO connected to OSCB pin and +2 ppm frequency offset for the output signal w.r.t. the XO. APLL dividers set for 53x2=106 and xo_config::passclk=1, synth frequency 625 MHz.

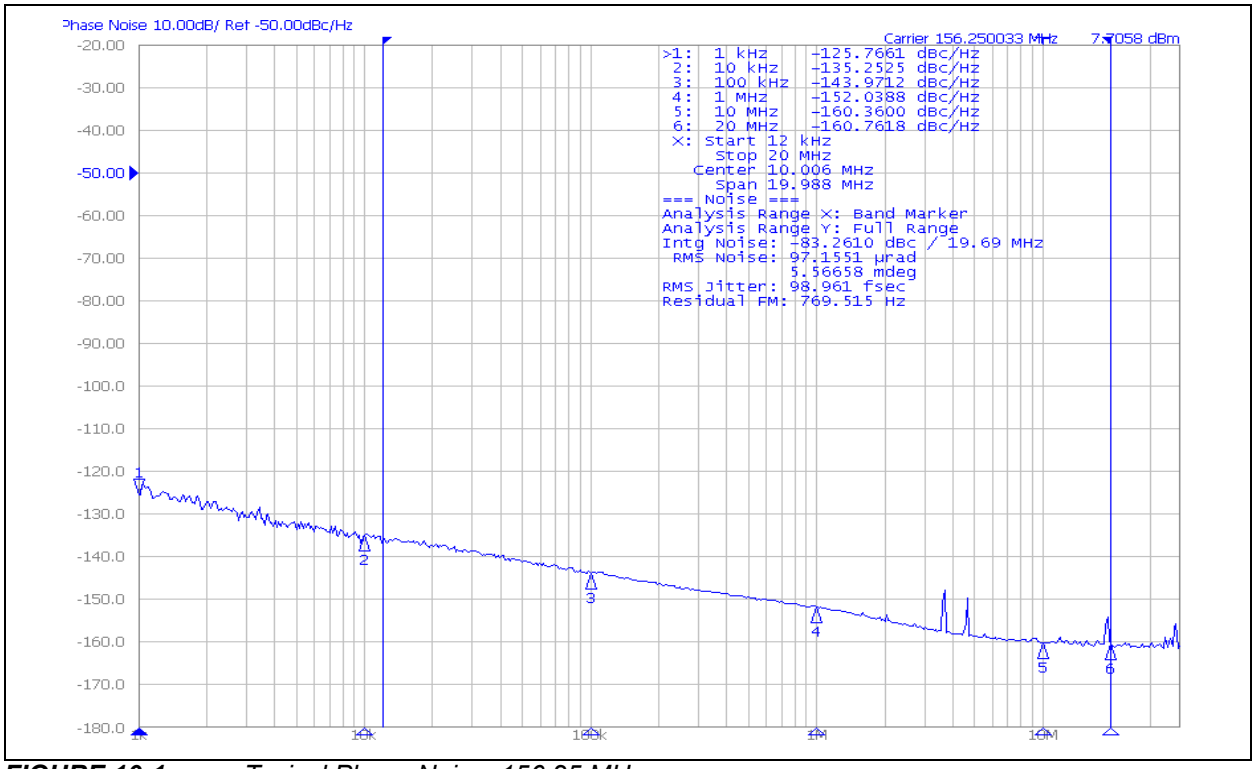


FIGURE 10-1: *Typical Phase Noise, 156.25 MHz.*

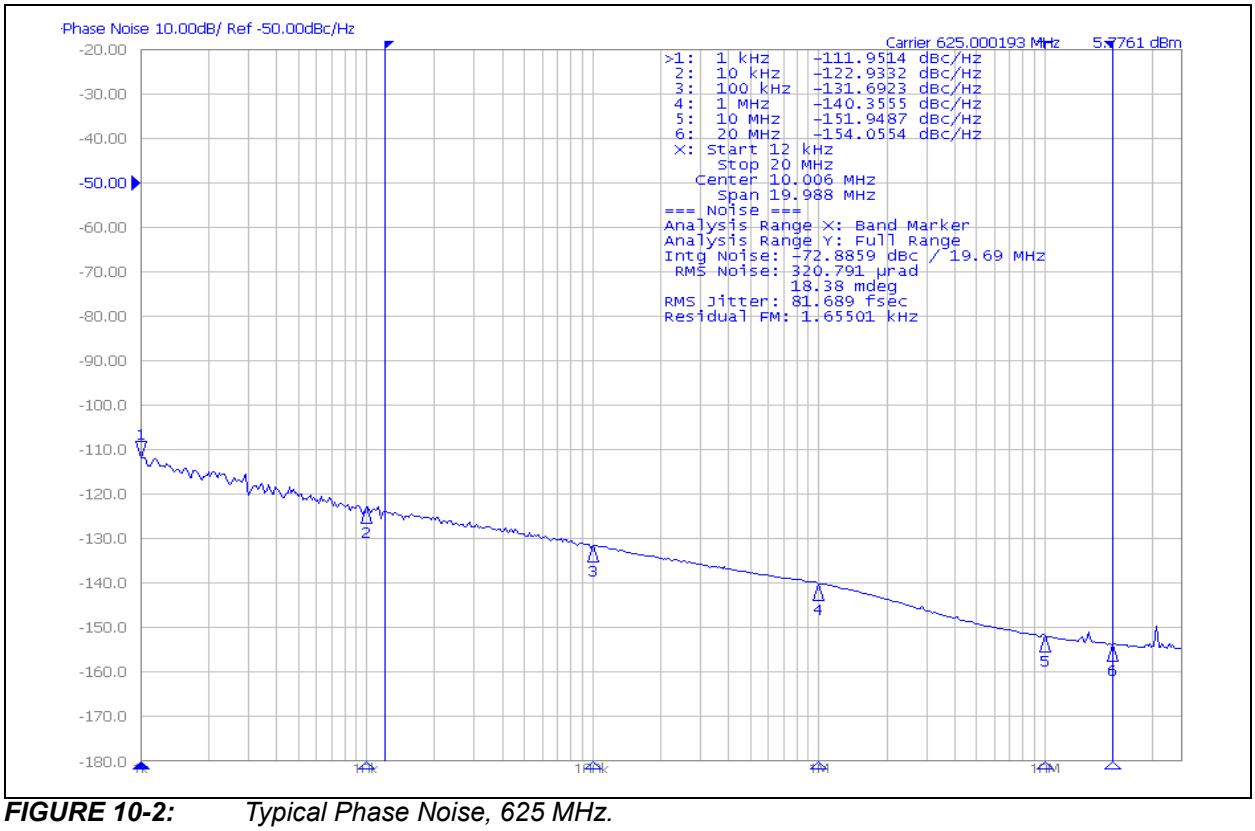


FIGURE 10-2: *Typical Phase Noise, 625 MHz.*

11.0 PACKAGE AND THERMAL INFORMATION

The device is fully functional at junction temperatures from T_{JMIN} to T_{JMAX}, but long-term exposure to junction temperatures above 110°C may eventually affect device performance.

TABLE 11-1: 9X9 VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A	—	+85	°C
Minimum Junction Temperature	T_{JMIN}	—	–40	°C
Maximum Junction Temperature	T_{JMAX}	—	+125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	still air	16.8	°C/W
		1 m/s airflow	13.6	
		2.5 m/s airflow	11.8	
Junction to Board Thermal Resistance	θ_{JB}	—	4.5	°C/W
Junction to Case Thermal Resistance	θ_{JC}	—	8.3	°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	—	1.1	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	—	0.1	°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 8-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

TABLE 11-2: 7X7 VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A	—	+85	°C
Minimum Junction Temperature	T_{JMIN}	—	–40	°C
Maximum Junction Temperature	T_{JMAX}	—	+125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	still air	16.8	°C/W
		1 m/s airflow	13.5	
		2.5 m/s airflow	11.7	
Junction to Board Thermal Resistance	θ_{JB}	—	5.5	°C/W
Junction to Case Thermal Resistance	θ_{JC}	—	9.3	°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	—	1.1	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	—	0.1	°C/W

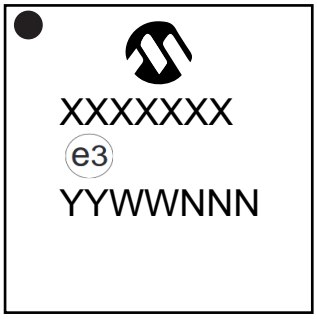
Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 8-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

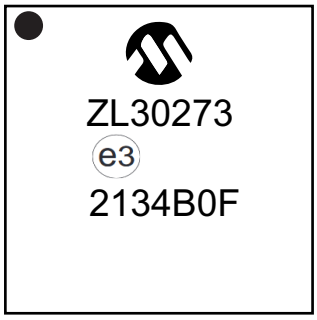
12.0 PACKAGE OUTLINE

12.1 Package Marking Information

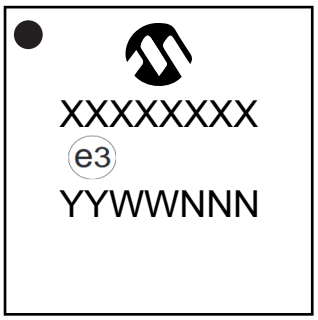
64-Lead VQFN



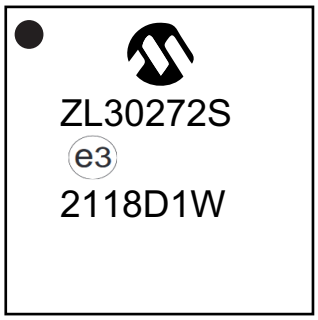
Example



48-Lead VQFN



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

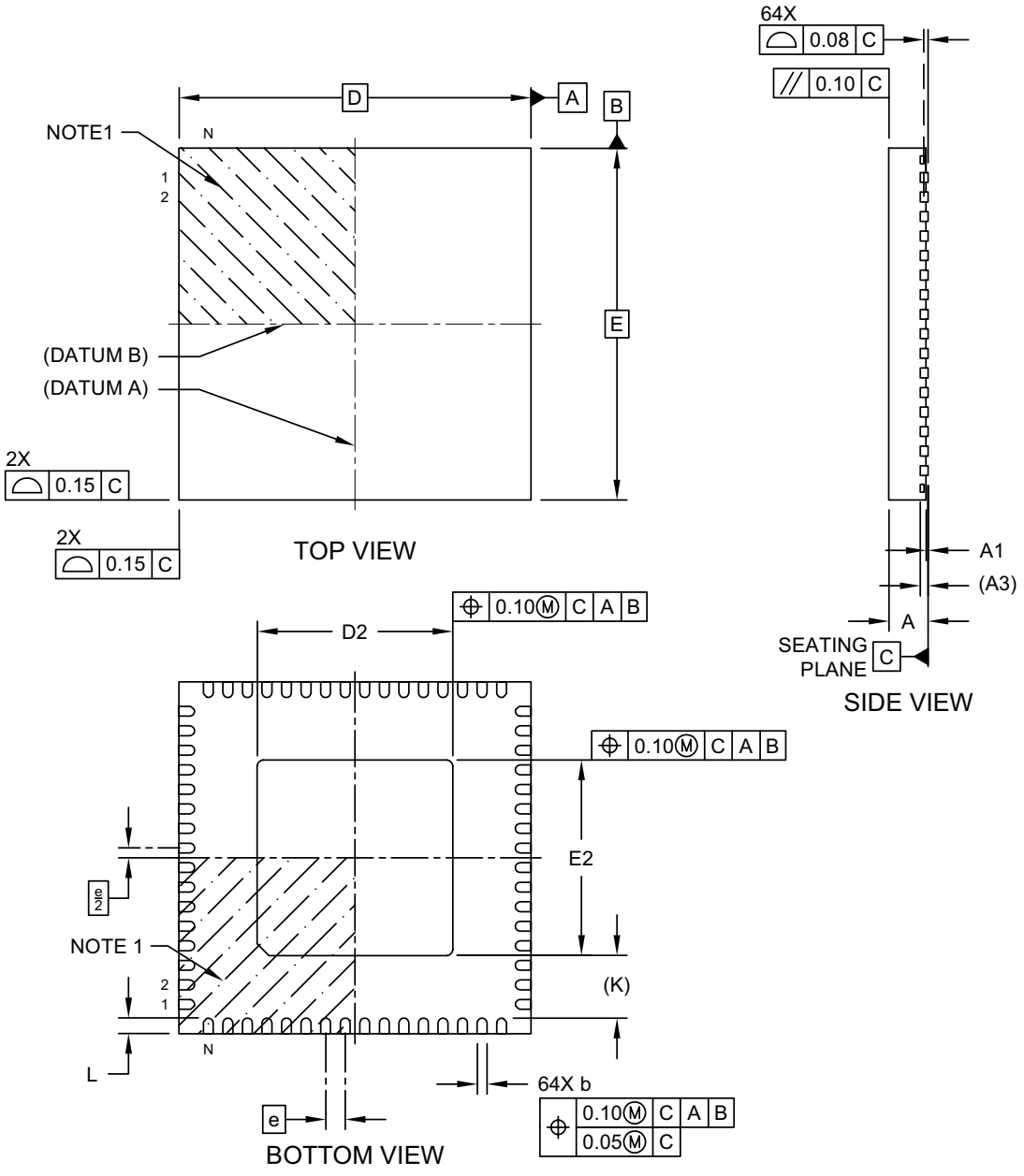
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

64-Lead 9 mm x 9 mm VQFN Package Outline and Recommended Land Pattern

64-Lead Very Thin Plastic Quad Flat, No Lead Package (MGC) - 9x9x1 mm Body [VQFN] With 5.0 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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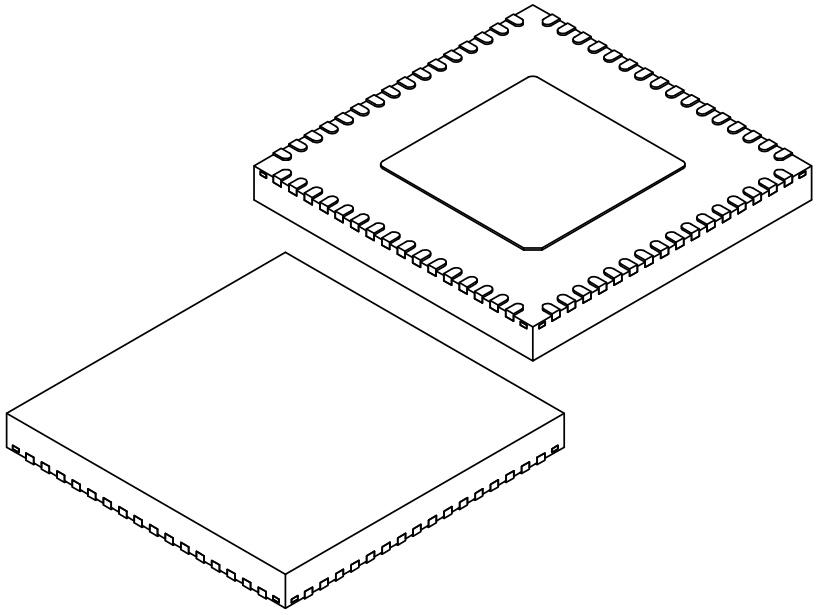
64-Lead Very Thin Plastic Quad Flat, No Lead Package (MGC) - 9x9x1 mm Body [VQFN] With 5.0 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	4.90	5.00	5.10
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	4.90	5.00	5.10
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		1.61 REF	

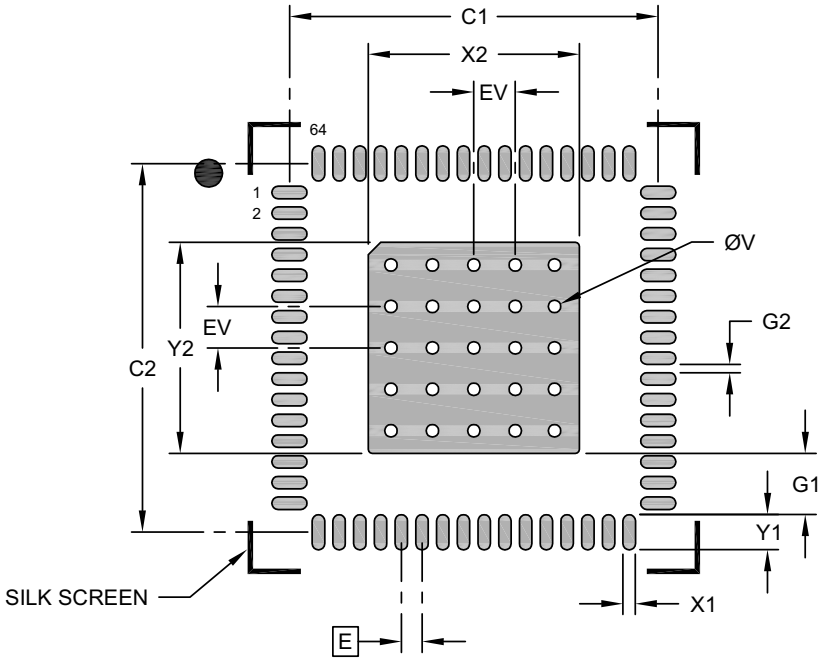
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25413 Rev B Sheet 2 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (MGC) - 9x9x1 mm Body [VQFN] With 5.0 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			5.10
Optional Center Pad Length	Y2			5.10
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.85
Contact Pad to Center Pad (X64)	G1	1.48		
Contact Pad to Contact Pad (X60)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

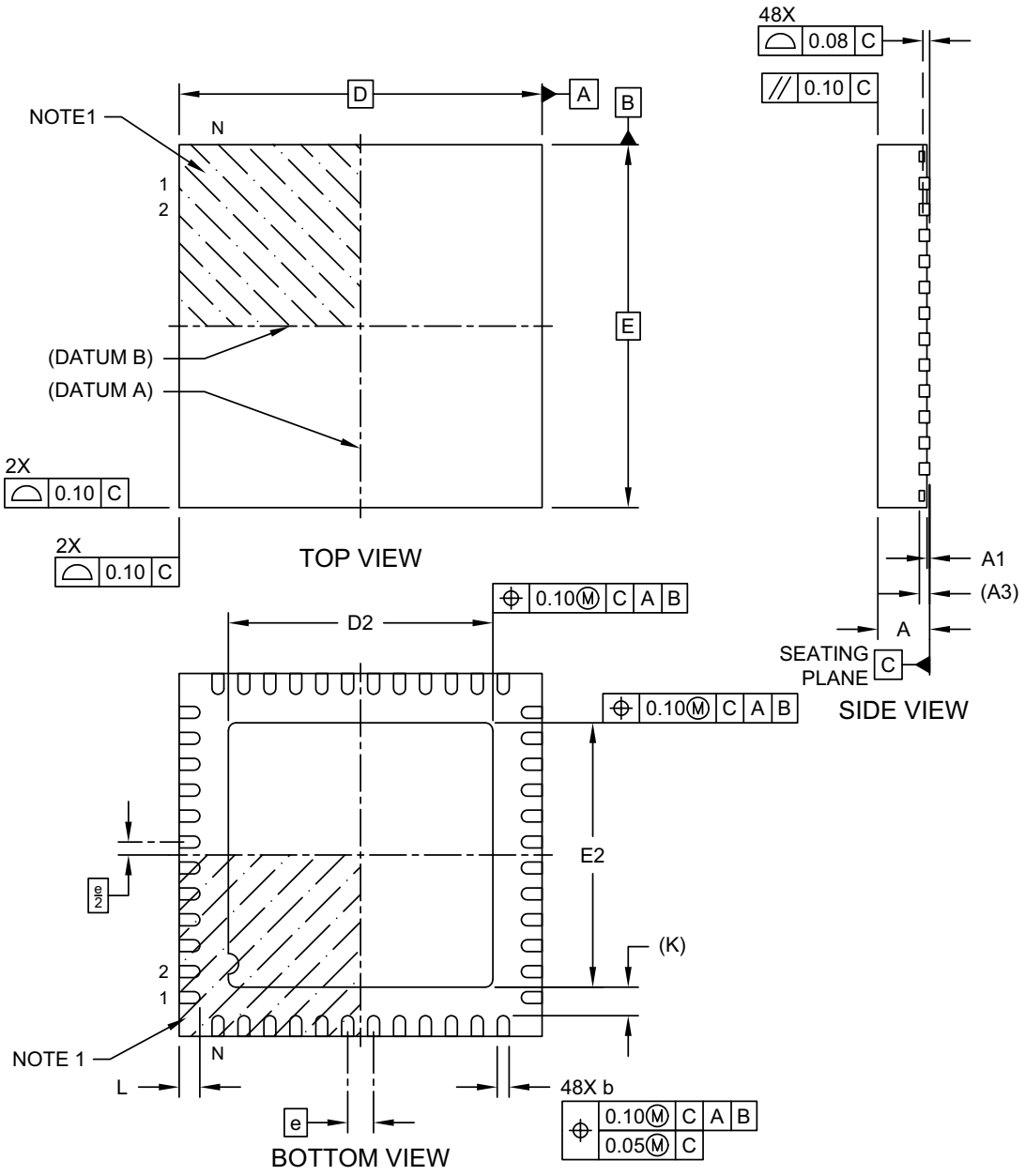
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27413 Rev B

48-Lead 7 mm x 7 mm VQFN Package Outline and Recommended Land Pattern

48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad; Microsemi Legacy Package

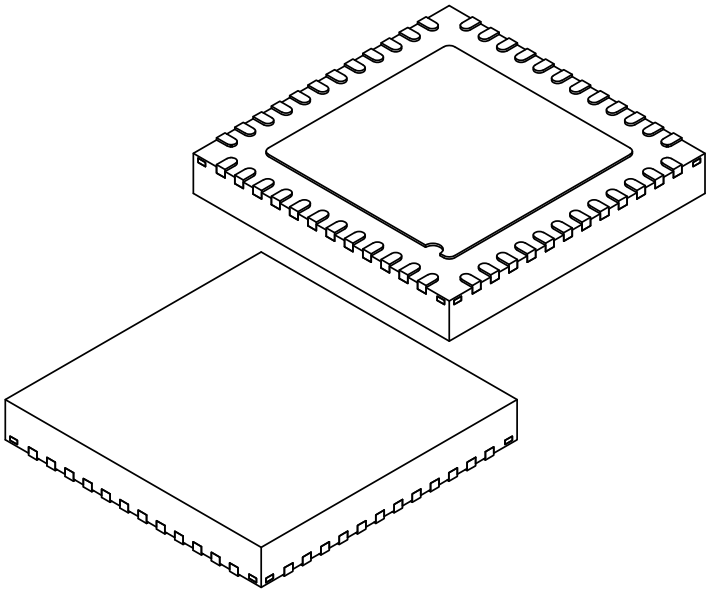
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25407 Rev B Sheet 1 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	5.00	5.10	5.20
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	5.00	5.10	5.20
Terminal Width	b	0.16	0.23	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.55 REF	

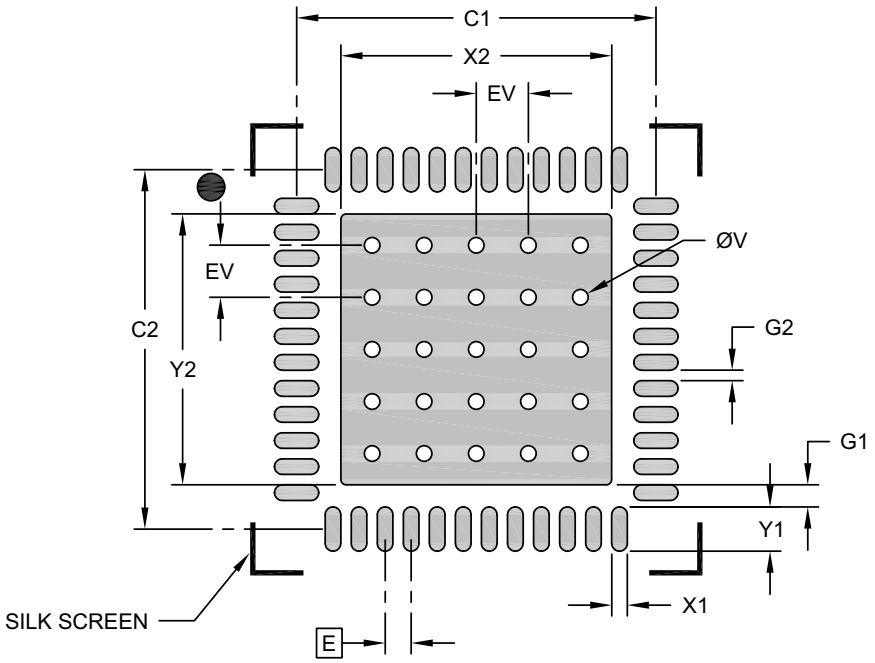
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25407 Rev B Sheet 2 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (MAC) - 7x7x1 mm Body [VQFN] With 5.1 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			5.20
Optional Center Pad Length	Y2			5.20
Contact Pad Spacing	C1		6.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.43		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27407 Rev B

13.0 ACRONYMS AND ABBREVIATIONS

APLL	analog phase locked loop
CML	current mode logic
GbE	gigabit Ethernet
HCSL	high-speed current steering logic
I/O	input/output
LOS	loss of signal
LVDS	low-voltage differential signal
LVPECL	low-voltage positive emitter-coupled logic
PFD	phase/frequency detector
pk-pk	peak-to-peak
PLL	phase locked loop
ppb	parts per billion
ppm	parts per million
PRC	primary reference clock
PRS	primary reference source
RMS	root-mean-square
RO	read-only
R/W	read/write
SS or SSM	spread spectrum modulation
TCXO	temperature-compensated crystal oscillator
UI	unit interval
UI_{PP} or UI_{P-P}	unit interval, peak-to-peak
XO	crystal oscillator

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006568A (07-14-21)	—	Converted Microsemi data sheet ZL30273 - ZL30274 to Microchip DS20006568A. Minor text changes throughout.
DS20006568B (11-02-21)	Section 5.4.1.2	Edited last paragraph to clarify that an embedded Sync signal can be used for external feedback if the REF pin is configured as a regular clock signal.
	ref_config	Edited vcm and ac_couple field descriptions to say they are ignored in REFxN mailbox registers.
	dpll_fast_lock_phase_rate	Renamed from dpll_fast_lock_fol
	dpll_fast_lock_phase_err	Deleted second paragraph because it was not correct.
	synth_align_compensation	renamed from “align_compensation”
	output_driver_level	In the drive field description added typical CMOS output impedance numbers. Also corrected default value from 0x02 to 0x52 for “all other OUTs”
	Table 9-6	Split “Input leakage current, RST_B, CS_B_IF0” spec into two, one for RST_B, one for CS_B_IF0. In the RST_B notes column, changed 0-V_{DDIO} to 0-V_{DD33}.
	Table 9-7	Deleted “and differential voltage (i.e. signal amplitude)” from note 2 because this is not programmable in LVDS mode. Also added cross ref to note 3 from VCM specs.
DS20006568C (02-28-22)	—	Documented ZL30272
	Figure 3-2	Added pin diagram for 48-lead 7 mm x 7 mm package.
	Table 4-1	Add pin numbers for 7 mm x 7 mm package.
	Table 11-2	Added 7 mm x 7 mm package thermal specs.
	Section 12.0	Added package outline and recommended land pattern for 48-lead 7 mm x 7 mm VQFN package.
	Product Identification System	Added S=48-Lead 7 mm x 7 mm package and updated the examples.
DS20006568D (05-10-22)	xo_amp_sel	Corrected the xtal_drive_level description to what it should be. Previously it was accidentally the same text as the xo_osci_sel description.
	Table 4-1	In the GPIO description added new recommendation.
	Figure 5-7	Added a footnote to part e).
	Section 5.5.4, synth_spread_spectrum_cfg, synth_spread_spectrum_rate, synth_spread_spectrum_spread	Documented these registers.
	output_phase_step_ctrl	Minor edits to the tod_step field description.
	output_phase_step_data	Minor edits to indicate two different units depending on context.
	Section 2.2, Section 4.0, Section 5.1.1, Section 5.1.5	Edits to clarify max input frequency for single-pin differential mode.

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006568D (05-10-22)	dpll_mon_status_0	Added a sentence to the ho_ready description about transitions where it remains unchanged.
	dpll_ctrl_x	Documented tod_step_reset at bit 2.
	Section 5.3.13	Added cross references to ref priority registers and forced reference control field.
	Figure 5-2	Updated this figure.
	Figure 9-2	Corrected VOC to VOUT in several places.
	ref_freq_base	Corrected hex values to match decimal values.
	Section 5.6.1	Correct last paragraph about voltages allowed for LVDS and LVPECL.
	Table 9-14	In note 1, corrected 2x to 3x.
DS20006568E (11-04-22)	output_ctrl_0	In the stop_high bit description, clarified the 0 decode is stop low and the 1 decode is stop high. Also corrected rising edge to falling edge in the 0 decode.
	Table 4-1	Added content in OUT and VDDO6 rows to say that in 7x7 package devices OUT6 is powered from VDDO8 along with OUT8. Added recommendation to the output clock pin description.
	output_phase_step_data	Added note.
	output_phase_compensation	Added note.
	synth_phase_compensation	Added note.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X	X	X
Part Number	Feature Series	Chip Carrier Type	Package	Media Type	Finish	Size

Device:	ZL30272: 1-Channel Jitter Attenuator with up to 12 Outputs ZL30273: 1-Channel Jitter Attenuator with up to 20 Outputs ZL30274: 2-Channel Jitter Attenuator with up to 20 Outputs
Feature Series:	<not present> = Original series
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = VQFN
Media Type:	G = 260/Tray
Finish:	1 = Pb-Free, Matte Tin (Sn) Finish
Size:	<blank> = 64-Lead 9 mm x 9 mm S = 48-Lead 7 mm x 7 mm

Examples:

a) ZL30273LDG1:

1-Channel Jitter Attenuator with up to 20 Outputs, Leadless Chip Carrier, VQFN, 260/Tray, Pb-Free Matte Tin (Sn) Finish, 64-Lead 9 mm x 9 mm

b) ZL30274LDG1:

2-Channel Jitter Attenuator with up to 20 Outputs, Leadless Chip Carrier, VQFN, 260/Tray, Pb-Free Matte Tin (Sn) Finish, 64-Lead 9 mm x 9 mm

c) ZL30272LDG1S:

1-Channel Jitter Attenuator with up to 12 Outputs, Leadless Chip Carrier, VQFN, 260/Tray, Pb-Free Matte Tin (Sn) Finish, 48-Lead 7 mm x 7 mm

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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China - Hong Kong SAR
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