ZL30281

Three-Output PCIe Clock Generator

Features

- 25 MHz Crystal or CMOS Input
- Generates PCIe 1, 2, 3, 4, 5, 6 Jitter-Compliant Clocks with CML Outputs
- Four Default Configurations Selected by Hardware Pins at Reset:
  - Config0: 100 MHz on Output OC1 (CML)
  - Config1: 100 MHz on OC1, OC2 (CML)
  - Config2: 100 MHz on OC1 (CML), OC2 (HSTL)
  - Config3: 100 MHz on OC1, OC2 (CML) and 25 MHz LVCMOS on OC3
- Per-Output Controls (Using SPI or I^2C Interface)
  - Per-Output Enable/Disable and Glitchless Start/Stop (Stop High or Low)
  - Precise Output Alignment Circuitry and Per-Output Phase Adjustment
- SPI or I^2C Processor Interface
- Tiny 5 mm x 5 mm VQFN Package

Applications

- PCIe Gen1 to Gen6 Clock Generation for PCIe Storage Systems, Riser Cards, JBOF, etc.

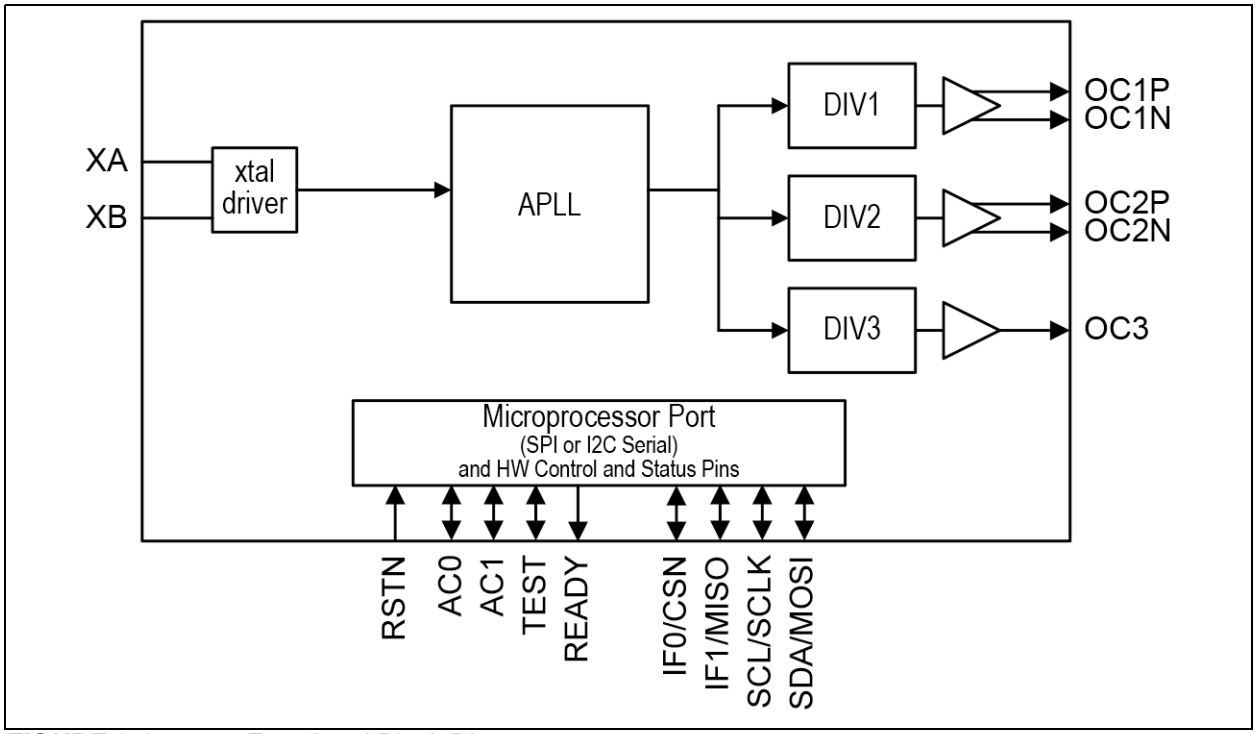

FIGURE 0-1: *Functional Block Diagram.*

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1.0 PIN DIAGRAM

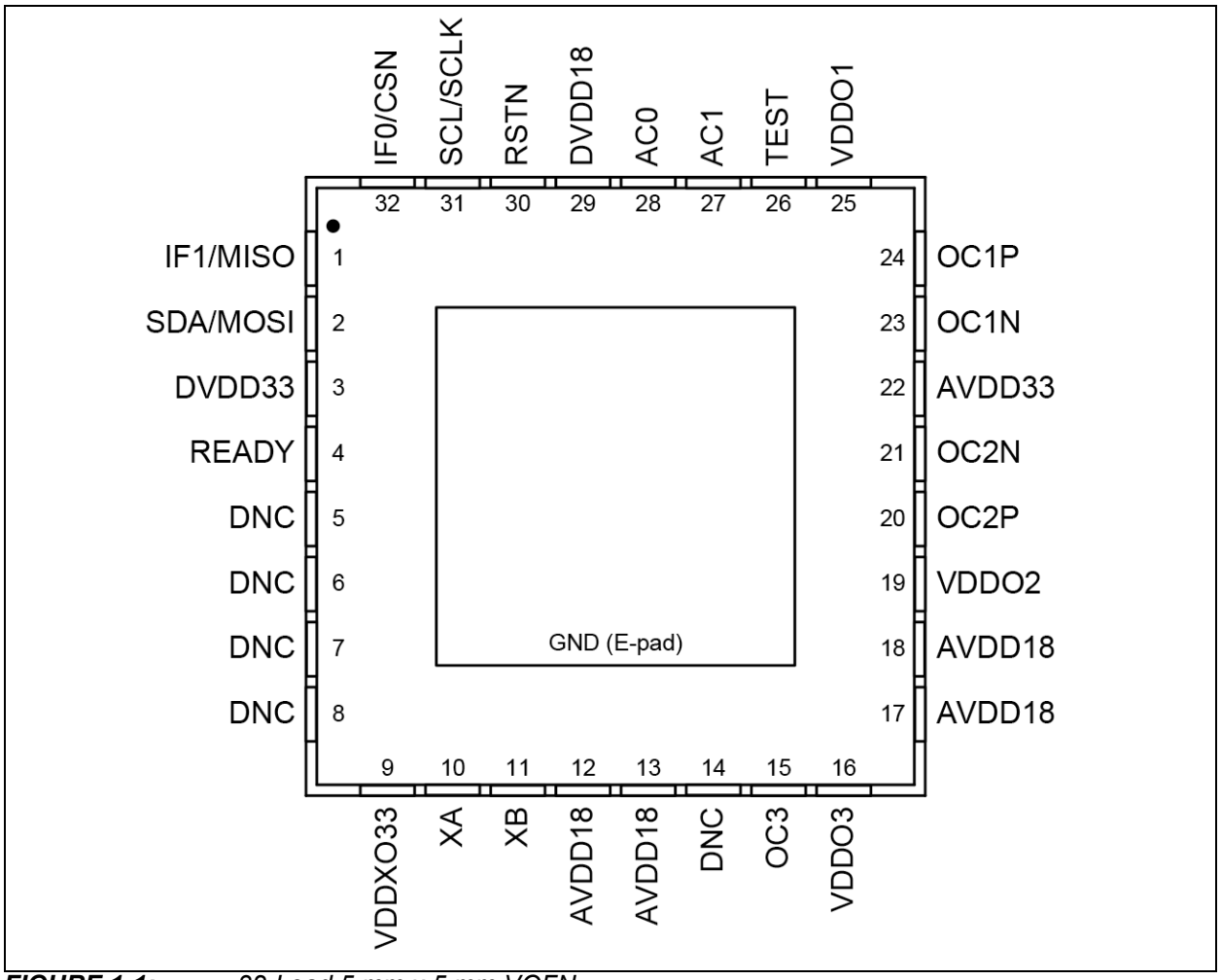


FIGURE 1-1: *32-Lead 5 mm x 5 mm VQFN.*

2.0 PIN DESCRIPTIONS

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, I_{PU} – input with 50 kΩ internal pull-up resistor, O – output, A – analog, P – power supply pin. All SPI/I^2C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

TABLE 2-1: PIN DESCRIPTIONS

Pin Number	Pin Name	I/O	Description
10	XA	A/I	**Crystal or Input Clock Pins** *Crystal:* MCR1.XAB=01. An on-chip crystal driver circuit is designed to work with an external crystal connected to the XA and XB pins. See Section 3.2.2 for crystal characteristics and recommended external components. *Input Clock:* MCR1.XAB=10. An external local oscillator or clock signal can be connected to the XA pin. The XB pin must be left unconnected.
11	XB		
24	OC1P	O	**Output Clock Pins** CML, HSTL or CMOS. Programmable frequency and drive strength. See Table 5-6 and Figure 5-2 for electrical specifications and recommended external circuitry for interfacing to LVDS, LVPECL or CML input pins on neighboring devices. See Table 5-7 for electrical specifications for interfacing to CMOS and HSTL inputs on neighboring devices. See Figure 5-3 for recommended external circuitry for interfacing to HCSL inputs on neighboring devices.
23	OC1N		
20	OC2P		
21	OC2N		
15	OC3		
30	RSTN	I_{PU}	**Reset (Active Low)** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. See Section 3.5.
28	AC0	I	Auto-Configure [1:0] On the rising edge of RSTN these pins specify the device configuration. See Section 3.1.
27	AC1		
26	TEST	I	**Factory Test** On the rising edge of RSTN the pin behaves as TEST. Factory test mode is enabled when TEST is high. For normal operation TEST must be low on the rising edge of RSTN.
4	READY	O	**PLL Lock** This pin indicates the state of the device after reset. 0=not ready, 1=ready.
32	IF0/CSN	I/O	**Interface Mode 0/SPI Chip Select (Active Low)** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF0 and, together with IF1, specifies the interface mode for the device. See Section 3.1. *SPI Chip Select:* After reset this pin is CSN. An external SPI server must assert (low) CSN to access device registers.
31	SCL/SCLK	I/O	**I^2C Clock/SPI Clock** *I^2C Clock:* When the device is configured as an I^2C client, an external I^2C server must provide the I^2C clock signal on the SCL pin. *SPI Clock:* An external SPI server must provide the SPI clock signal on SCLK.
1	IF1/MISO	I/O	**Interface Mode 1/SPI Server-In-Client-Out** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF1 and, together with IF0, specifies the interface mode for the device. See Section 3.1. *SPI MISO:* After reset this pin is MISO. The device outputs data to an external SPI server on MISO during SPI read transactions.

TABLE 2-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	I/O	Description
2	SDA/MOSI	I/O	**I²C Data/SPI Server-Out-Client-In** *I²C Data:* When the device is configured as an I²C client, SDA is the bidirectional data line between the device and an external I²C server. *SPI MOSI:* An external SPI server sends commands, addresses and data to the device on MOSI.
12	AVDD18	P	**Analog Power Supply.** 1.8V ±5%.
13			
17			
18			
22	AVDD33	P	**Analog Power Supply.** 3.3V ±5%.
29	DVDD18	P	**Digital Power Supply.** 1.8V ±5%.
3	DVDD33	P	**Digital Power Supply.** 3.3V ±5%.
25	VDDO1	P	**Output OC1 Power Supply.** 1.5V to 3.3V ±5%.
19	VDDO2	P	**Output OC2 Power Supply.** 1.5V to 3.3V ±5%.
16	VDDO3	P	**Output OC3 Power Supply.** 1.5V to 3.3V ±5%.
9	VDDXO33	P	**Analog Power Supply for Crystal Driver Circuitry.** 3.3V ±5%.
5	DNC	—	**Do Not Connect.** Leave these pins floating.
6			
7			
8			
14			
ePAD	VSS	P	**Ground.** 0 volts.

3.0 FUNCTIONAL DESCRIPTION

3.1 Pin-Controlled Automatic Configuration at Reset

The device configuration is determined at reset (i.e. on the rising edge of RSTN) by the signal levels on five device pins: TEST, AC1, AC0, IF1/MISO, and IF0/CSN. For each of these pins, the first name (TEST, AC1, AC0, IF1, IF0) indicates their function when they are sampled by the rising edge of the RSTN pin. The second name refers to their function after reset. The values of these pins are latched into the CFGSR register when RSTN goes high. To ensure the device properly samples the reset values of these pins, the following guidelines should be followed:

1. Any pullup or pull-down resistors used to set the value of these pins at reset should be 1 kΩ.
2. RSTN must be asserted at least as long as specified in Section 3.5.

The hardware configuration pins are grouped into three sets:

1. TEST - Manufacturing test mode
2. IF[1:0] – Microprocessor interface mode and I^2C address
3. AC[1:0] – Auto-configuration

The TEST pin selects manufacturing test modes when TEST=1. Therefore, TEST should be pulled low.

The IF[1:0] pins specify the processor interface mode and the I^2C client address. The AC[1:0] pins specify which of four device configurations to execute after reset.

IF1	IF0	Processor Interface
0	0	I^2C, client address 11011 00
0	1	I^2C, client address 11011 01
1	0	I^2C, client address 11011 10
1	1	SPI client

AC1	AC0	Auto-Configuration
0	0	Config0: 100 MHz on OC1 (CML signal format)
0	1	Config1: 100 MHz on OC1 and OC2 (CML)
1	0	Config2: 100 MHz on OC1 (CML) and OC2 (HSTL format)
1	1	Config3: 100 MHz on OC1 and OC2 (CML) and 25 MHz LVCMOS on OC3

All four configurations set up the part to use a 25 MHz crystal on XA and XB as the input reference.

3.2 Local Oscillator or Crystal

Section 3.2.1 describes how to connect an external oscillator and the required characteristics of the oscillator. Section 3.2.2 describes how to connect an external crystal to the on-chip crystal driver circuit and the required characteristics of the crystal.

3.2.1 EXTERNAL OSCILLATOR

A 25 MHz signal from an external oscillator can be connected to the XA pin (XB must be left unconnected). To minimize jitter, the signal must be properly terminated and must have very short trace length. A poorly terminated single-ended signal can greatly increase output jitter, and long single-ended trace lengths are more susceptible to noise. When MCR1.XAB=10, XA is enabled as a single-ended input.

The jitter on output clock signals depends on the phase noise and frequency of the external oscillator.

3.2.2 EXTERNAL CRYSTAL AND ON-CHIP DRIVER CIRCUIT

The on-chip crystal driver circuit is designed to work with a 25 MHz fundamental mode, AT-cut crystal resonator. See Table 3-1 for recommended crystal specifications. To enable the crystal driver, set MCR1.XAB=01.

See Figure 3-1 for the crystal equivalent circuit and the recommended external capacitor connections. To achieve a crystal load (C_L) of 10 pF, an external 16 pF (C1) is placed in parallel with the 4 pF internal capacitance of the XA pin, and an external 16 pF (C2) is placed in parallel with the 4 pF internal capacitance of the XB pin. The crystal then sees

a load of 20 pF in series with 20 pF, which is 10 pF total load. Note that the 16 pF capacitance include all capacitance on those nodes. If, for example, PCB trace capacitance between crystal pin and IC pin is 2 pF, then 14 pF capacitors should be used to make 16 pF total.

The crystal, traces, and two external capacitors should be placed on the board as close as possible to the XA and XB pins to reduce crosstalk of active signals into the oscillator. Also no active signals should be routed under the crystal circuitry.

Note: Crystals have temperature sensitivities that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO should be used instead.

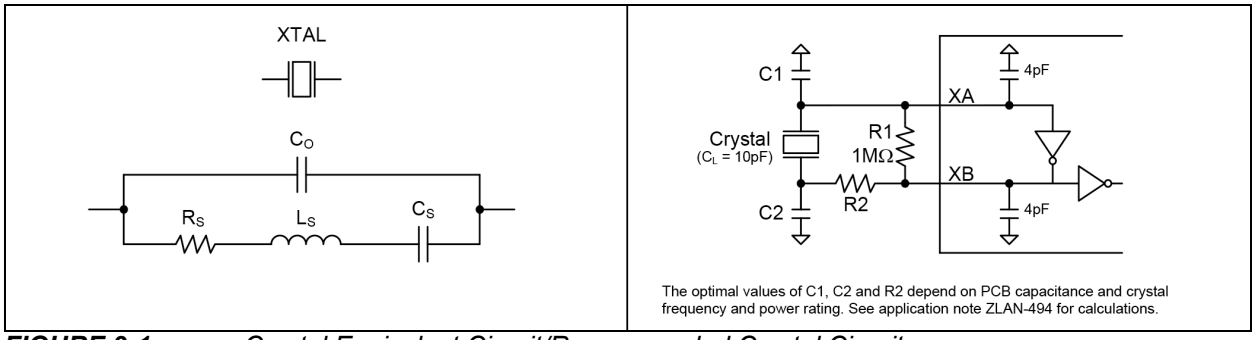


FIGURE 3-1: *Crystal Equivalent Circuit/Recommended Crystal Circuit*

TABLE 3-1: CRYSTAL SELECTION PARAMETERS

Parameter		Sym.	Min.	Typ.	Max.	Units
Crystal Oscillation Frequency		f_{OSC}		25		MHz
Shunt Capacitance		C_O	—	2	5	pF
Load Capacitance		C_L	—	10	—	F
Equivalent Series Resistance (ESR)	f_{OSC} < 40 MHz	R_S	—	—	60	Ω
	f_{OSC} > 40 MHz		—	—	50	Ω
Maximum Crystal Drive Level		—	100	—	—	µW
Crystal Frequency Stability vs. Power Supply		f_{FVD}	—	0.2	0.5	ppm per 10% Δ in V_{DD}

Note 1: Higher frequencies give lower output jitter, all else being equal.

2: These ESR limits are chosen to constrain crystal drive level to less than 100 µW. If the crystal can tolerate a drive level greater than 100 µW then proportionally higher ESR is acceptable.

3.3 Output Clock Configuration

The device has three output clock signal pairs. Each output has individual enable, start/stop and alignment controls. The outputs can be aligned relative to each other, and the phases of output signals can be adjusted dynamically with high resolution and infinite range.

3.3.1 OUTPUT SIGNAL FORMAT, VOLTAGE, AND INTERFACING

The signal format of each output is determined by the configuration number specified by the AC[1:0] pins at device reset (see the AC[1:0] table in Section 3.1). The clock to the output driver can inverted by setting OCxCR2.POL=1. The CMOS/HSTL output driver can be set to any of four drive strengths using OCxCR2.DRIVE.

Each output has its own power supply pin to allow CMOS or HSTL signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components. If OC2 is HSTL format (Config2) then a 1.8V VDDO2 voltage can be used to as shown in Figure 5-3 to get a signal compatible with HCSL receivers. Note that CML outputs must have a power supply voltage of 3.3V.

The CML outputs can be easily interfaced to LVDS, LVPECL, CML, HCSL, HSTL and other differential inputs on neighboring ICs using a few external passive components. See Figure 5-2 for examples.

3.3.2 OUTPUT PHASE ADJUSTMENT AND PHASE ALIGNMENT

The device has flexible, high-resolution tools for managing the phases of the output clocks relative to one another. The key register fields for this are found in the PACR1 global configuration register and the per-output OCxPH register. Resolution is one period of the 600 MHz APLL clock, i.e. 1.667 ns.

3.3.2.1 Phase Adjustment

A phase adjustment is a phase change for an output relative to that output's most recent phase. To cause the device to perform phase adjustment of an output clock, set PACR1.MODE=1, set OCxCR1.PHEN=1 to enable the output for phase adjustment, and write the phase adjustment amount to the output's OCxPH register. Then an arm/trigger methodology is used to cause the phase adjustment to happen.

The arm step tells the device that it is enabled to perform the phase adjustment when it sees the trigger stimulus. The arm signal is a 0-to-1 transition of the PACR1.ARM bit. The trigger signal a 0-to-1 transition of the PACR1.TRIG bit. Any combination of outputs can be phase adjusted by the same trigger, and each output can be adjusted by a different amount. Only outputs with OCxCR1.PHEN=1 and OCxPH.PHADJ≠0 have their phases adjusted.

There are a few constraints on the range of possible phase adjustments. The largest negative phase adjustment is 2 APLL periods, which is 2*1.667 ns=3.333 ns. The largest positive phase adjustment is 6 APLL periods, which is 24*1.667 ns=40 ns.

An armed phase adjustment can be canceled before the trigger occurs by setting the PACR1.RST bit.

The PASR register has real-time status bits indicating whether a phase adjustment is armed and waiting for a trigger (ARMED bit) or in progress (BUSY bit). It also has a latched status bit (ADJL bit) to indicate the adjustment has completed.

Example: +1.0 APLL period phase adjustment for output OC1:

OC1CR1.PHEN=1	(Enable phase adjust on OC1)
OC1PH.PHADJ=00000010	(Specify +1.0 APLL period phase adjustment, i.e. 1.667ns)
PACR1.MODE=1	(Phase adjustment mode)
PACR1.RST=1	(reset phase adjust/align state machine)
PACR1.ARM=1	(arm for phase adjust)
PACR1.TRIG=1	(trigger the phase adjust: add +1.0 UI to output phase)
Repeat the next two writes as needed:	
PACR1.ARM=1.TRIG=0	(arm again; clearing the TRIG bit is required)
PACR1.TRIG=1	(trigger again: add +1.0 APLL period to output phase again)

3.3.2.2 Phase Alignment, Output-to-Output

A phase alignment is a special case of phase adjustment where the dividers for all participating outputs are reset just before the phase adjustment occurs.

To avoid glitches (i.e. "runt pulses") on the output clock it is possible to manually stop the output(s), before triggering the phase alignment, and then restart the output(s) after the alignment (See Section 3.3.3).

When aligning outputs, it is important to note that, by default, the phase of outputs configured as HSTL format is opposite that of CML outputs. For example, consider the case where OC1 is 100 MHz CML format and OC2 is 100 MHz HSTL format. When OC1 and OC2 are aligned then OC2N is high when OC1P is high. The polarity bit OCxCR2.POL can be used to change this as needed

Contact Microchip Timing Applications Support for help with alignment scenarios that don't meet the rules listed above.

Example: OC1-to-OC2 alignment (+3.5 APLL cycle offset):

OC1CR1.PHEN=1	(Enable phase adjust on OC1)
OC2CR1.PHEN=1	(Enable phase adjust on OC2)
OC1PH.PHADJ=00000000	(0.0UI)
OC2PH.PHADJ=00000111	(+3.5UI)
PACR1.MODE=0	(Phase alignment mode)
PACR1.RST=1	(reset phase adjust/align state machine)

PACR1.ARM=1 (arm for phase alignment)

PACR1.TRIG=1 (trigger the phase alignment)

3.3.3 OUTPUT CLOCK START, STOP, AND HIGH-IMPEDANCE

Output clocks can be stopped high or low. One use for this behavior is to ensure “glitchless” output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an OCxSTOP register with fields to control this behavior. The OCxSTOP.MODE field specifies whether the output clock signal stops high, stops low, or does not stop. The OCxSTOP.SRC field specifies the source of the stop signal. Options include the OCxSTOP.STOP bit and the arming of a phase adjustment (which is indicate by PASR.ARMED).

When the stop mode is Stop High (OCxSTOP.MODE=01) and the stop signal is asserted, the output clock is stopped after the next rising edge of the output clock. When the stop mode is Stop Low (OCxSTOP.MODE=10) and the stop signal is asserted, the output clock is stopped after the next falling edge of the output clock. Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on.

When OCxCR2.POL=1 the output stops on the opposite polarity that is specified by the OCxSTOP.MODE field.

When OCxCR2.STOPDIS=1 the output driver is disabled (high impedance) while the output clock is stopped.

Each output has a status register (OCxSR) with several stop/start status bits. The STOPD bit is a real-time status bit indicating stopped or not stopped. The STOPL bit is a latched status bit that is set when the output clock has stopped. The STARTL bit is a latched status bit that is set when the output clock has started.

3.4 Microprocessor Interface

The device can communicate over a SPI interface or an I^2C interface.

In SPI mode the device can only be configured as a SPI client to a processor server. The device is always a client on the I^2C bus.

Section 3.1 describes reset pin settings required to configure the device for these interfaces.

3.4.1 SPI CLIENT

The device can present a SPI client port on the CSN, SCLK, MOSI, and MISO pins. SPI is a widely used server/client bus protocol that allows a server and one or more clients to communicate over a serial bus. SPI servers are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the server, which also generates the SCLK signal. The device receives serial data on the MOSI (Server Out Client In) pin and transmits serial data on the MISO (Server In Client Out) pin. MISO is high impedance except when the device is transmitting data to the bus server.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MOSI on the rising edge of SCLK and updates data on MISO on the falling edge of SCLK. SCLK does not have to toggle between accesses, i.e., when CSN is high.

Device Selection. Each SPI device has its own chip-select line. To select the device, the bus server drives its CSN pin low.

Command and Address. After driving CSN low, the bus server transmits an 8-bit command followed by a 16-bit register address. The available commands are shown below.

TABLE 3-2: SPI COMMANDS

Command	Hex	Bit Order, Left to Right
Write	0x02	0000 0010
Read	0x03	0000 0011

Read Transactions. After driving CSN low, the bus server transmits the read command followed by the 16-bit address. The device then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the bus server continues to demand data, the device continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the bus server drives CSN high. See Figure 3-2.

Write Transactions. After driving CSN low, the bus server transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device receives the first data byte on MOSI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the server continues to transmit, the device continues to write the data received and increment its address counter. The write transaction is completed when the bus server drives CSN high. See Figure 3-3.

Early Termination of Bus Transactions. The bus server can terminate SPI bus transactions at any time by pulling CSN high. In response to early terminations, the device resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, the data byte is not written.

Design Option: Wiring MOSI and MISO Together. Because communication between the bus server and the device is half-duplex, the MOSI and MISO pins can be wired together externally to reduce wire count. To support this option, the bus server must not drive the MOSI/MISO line when the device is transmitting.

AC Timing. See Table 5-10 and Table 5-4 for AC timing specifications for the SPI interface.

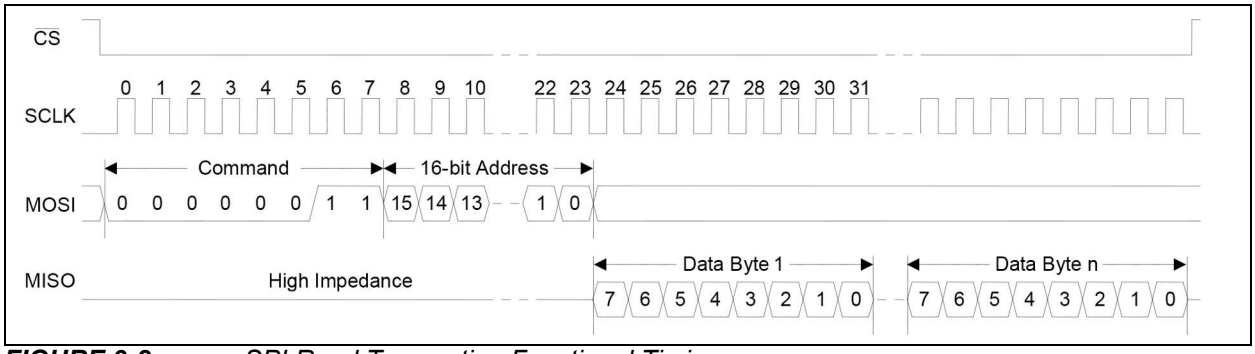


FIGURE 3-2: *SPI Read Transaction Functional Timing.*

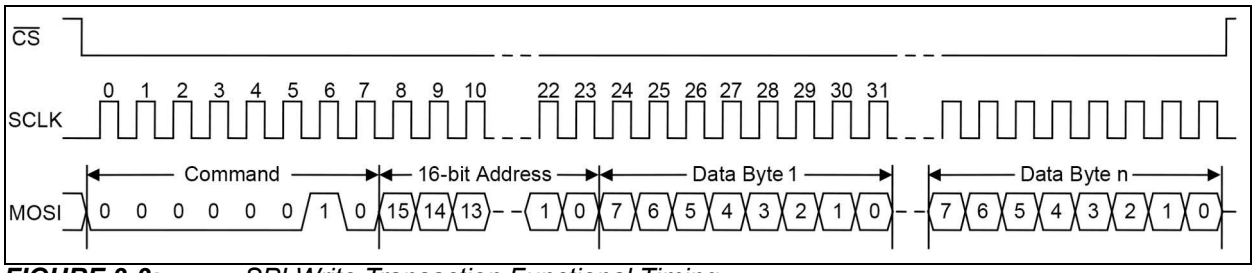


FIGURE 3-3: *SPI Write Transaction Functional Timing.*

3.4.2 I²C CLIENT

The device can present a fast-mode (400 kbit/s) I²C client port on the SCL and SDA pins. I²C is a widely used server/client bus protocol that allows one or more servers and one or more clients to communicate over a two-wire serial bus. I²C servers are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the server, which also generates the SCL signal. The device is compliant with version 2.1 of the I²C specification.

The I²C interface on the device is a protocol translator from external I²C transactions to internal SPI transactions. This explains the slightly increased protocol complexity described in the paragraphs that follow.

Read Transactions. The bus server first does an I²C write to the device. In this transaction three bytes are written: the SPI Read command (see Table 3-2), the upper byte of the register address, and the lower byte of the register address. The bus server then does an I²C read. During each acknowledge (A) bit the device fetches data from the read address and then increments the read address. The device then transmits the data to the bus server during the next 8 SCL cycles. The bus server terminates the read with a not-acknowledge (NA) followed by a STOP condition (P). See Figure 3-4. Note: If the I²C write is separated in time from the I²C read by other I²C transactions then the device only outputs the data value from the first address and repeats that same data value after each acknowledge (A) generated by the bus server.

Write Transactions. The bus server does an I²C write to the device. The first three bytes of this transaction are the SPI Write command (see Table 3-2), the upper byte of the register address, and the lower byte of the register address. Subsequent bytes are data bytes to be written. After each data byte is received, the device writes the byte to the write address and then increments the write address. The bus server terminates the write with a STOP condition (P). See Figure 3-5.

I²C Features Not Supported by the Device. The I²C specification has several optional features that are not supported by the device. These are: 3.4 Mbit/s high-speed mode (Hs-mode), 10-bit device addressing, general call address, software reset, and device ID. The device does not hold SCL low to force the server to wait.

I²C Client Address. The device's 7-bit client address can be pin-configured for any of three values. These values are show in the table in Section 3.1.

Bit Order. The I²C specification requires device address, register address, and all data bytes to be transmitted most significant bit first on the SDA signal.

Note: as required by the I²C specification, when power is removed from the device, the SDA and SCL pins are left floating so they don't obstruct the bus lines.

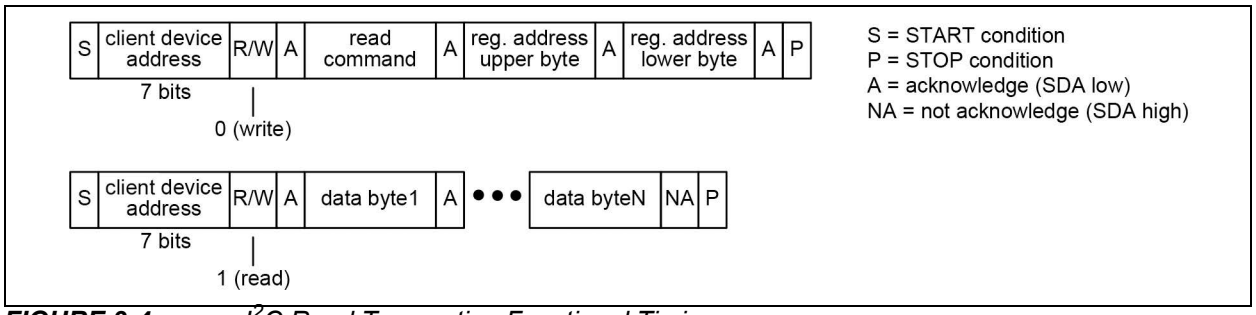


FIGURE 3-4: *I²C Read Transaction Functional Timing.*

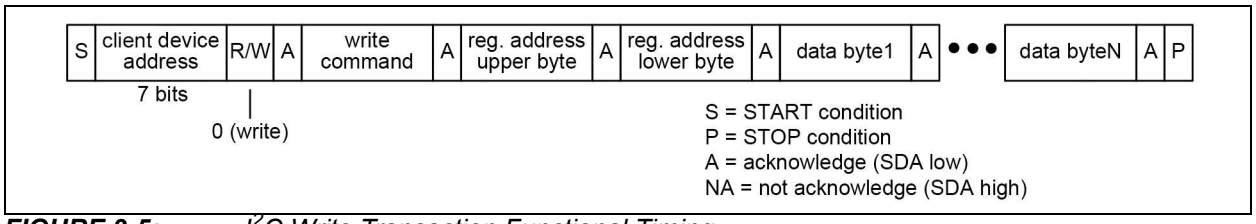


FIGURE 3-5: *I²C Write Transaction Functional Timing.*

Note: In Figure 3-4 and Figure 3-5, a STOP condition (P) immediately followed by a START condition (S) can be replaced by a repeated START condition (Sr) as described in the I²C specification.

3.5 Reset Logic

The device has two reset controls: the RSTN pin and the RST bit in MCR1. The RSTN pin asynchronously resets the entire device. When the RSTN pin is low all internal registers are reset to their default values. **The RSTN pin must have one rising edge after power-up.** At initial power-up reset should be asserted for at least 1 µs. During operation, the RSTN assertion time can be as short as 1 µs with one important exception:

> Consider the IF1/MISO pin: If (1) the pin could be an output driving high when RSTN is asserted, and (2) an external pull-down resistor is used to set the at-reset value of the pin, then RSTN should be asserted for 100 milliseconds.

The MCR1.RST bit resets the entire device (except for the microprocessor interface and the RST bit itself), but when the RST bit is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead these fields are reset to the default values that were latched when the RSTN pin was last active.

Important: System software must wait at least 100 µs after RSTN is deasserted and wait for GLOBISR.READY=1 before configuring the device.

3.6 Power Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a <3.3V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the <3.3V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop of the <3.3V supply. The second method is to ramp up the 3.3V supply first and then ramp up the <3.3V supply. In some applications VDDOx power supply pins can be at other voltages, such as 2.5V or 1.5V. In these applications, the general solution is to ramp up the supplies in order from highest nominal to lowest nominal voltage.

NOTES:

4.0 REGISTER DESCRIPTIONS

The device has an overall address range from 000h to 1FFh. Table 4-1 shows the register map. In each register, bit 7 is the MSb and bit 0 is the LSb. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 4-1.

4.1 Register Types

4.1.1 STATUS BITS

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. Status bits marked "—" are reserved and must be ignored.

4.1.2 CONFIGURATION FIELDS

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

4.2 Register Map

TABLE 4-1: REGISTER MAP

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Configuration Registers									
09	MCR1	RST	—	—	—	—	—	XAB[0:1]	
1B	PACR1	RST	TRIG	ARM	—	—	—		MODE
Status Registers									
30	ID1	IDU[7:0]							
31	ID2	IDL[3:0]				REV[3:0]			
40	CFGSR	TEST	XOFAIL	—	—	IF[1:0]		AC[1:0]	
43	GLOBISR	READY	—	—	—	—	—	—	—
48	APLLSR	—	—	ALK2L	ALK2	—	—	ALKL	ALK
4D	PASR	—	—	—	—	—	ADJL	BUSY	ARMED
53	OC1SR	—	—	—	—	STARTL	—	STOPL	STOPD
54	OC2SR	—	—	—	—	STARTL	—	STOPL	STOPD
55	OC3SR	—	—	—	—	STARTL	—	STOPL	STOPD
Output Clock Configuration Registers									
	OC1 Registers								
200	OC1CR1	PHEN	—	—	—	—	—	—	—
201	OC1CR2	—	POL	DRIVE[1:0]		STOPDIS	—	—	—
207	OC1PH	PHADJ[7:0]							
208	OC1STOP	STOP	—	SRC[3:0]				MODE[1:0]	
	OC2 Registers								
210	OC2CR1	PHEN	—	—	—	—	—	—	—
211	OC2CR2	—	POL	DRIVE[1:0]		STOPDIS	—	—	—
217	OC2PH	PHADJ[7:0]							
218	OC2STOP	STOP	—	SRC[3:0]				MODE[1:0]	

TABLE 4-1: REGISTER MAP (CONTINUED)

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OC3 Registers								
220	OC3CR1	PHEN	—	—	—	—	—	—	—
221	OC3CR2	—	POL	DRIVE[1:0]		STOPDIS	—	—	—
227	OC3PH	PHADJ[7:0]							
228	OC3STOP	STOP	—	SRC[3:0]				MODE[1:0]	

4.3 Register Definitions

4.3.1 GLOBAL CONFIGURATION REGISTERS

Register Name: MCR1
Register Description: Server Configuration Register 1
Register Address: 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	RST	—	—	—	—	—	XAB[1:0]	
Default:	0	0	0	0	0	0	0	1

Bit 7: Device Reset (RST). When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is high, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RSTN pin was last active. See Section 3.5.

0 = Normal operation

1 = Reset

Note: For proper sequencing of internal logic, write MCR1 to clear the MCSEL1, MCSEL, and ROSCD bits first (without changing the value of the RST bit) then perform a second write to set the RST bit.

(Note: on rev A devices (ID2.REV=0) do not set this bit to 1.)

Bits 1 to 0: XA/XB Pin Mode (XAB[1:0]). This field specifies the behavior of the XA and XB pins. See Section 3.2.

00 = Crystal driver and input disabled / powered down

01 = Crystal driver and input enabled on XA/XB

10 = XA enabled as single-ended input for external oscillator signal; XB must be left floating

11 = {unused value}

Register Name: PACR1
Register Description: Phase Adjust Configuration Register 1
Register Address: 1Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	RST	TRIG	ARM	—	—	—	—	MODE
Default:	0	0	0	0	0	0	0	0

Bit 7: Phase Adjustment Reset Bit (RST). This bit is used to reset the phase adjustment state machine. This is used to abort the phase adjustment after arming but before the trigger occurs. Resetting puts the state machine back to waiting for an arm signal. This bit is self-clearing. See Section 3.3.2.

1 = Reset a phase adjustment event in progress, self clearing

Bit 6: Phase Adjustment Trigger Bit (TRIG). This bit is used to trigger the phase adjustment event after the phase adjustment has been armed. This bit is self-clearing and must be written again to cause another trigger. The ARM bit must be set first then the TRIG bit can be set in a subsequent register write to initiate a trigger event. See Section 3.3.2.

1 = Trigger a phase adjustment, self clearing

Bit 5: Phase Adjustment Arm Bit (ARM). Setting this bit to 1 while PASR.ARMED=0 arms the phase adjustment. Writing a 0 to this bit has no effect. Changing the value of this bit from 0 to 1 while PASR.ARMED=1 has no effect. See Section 3.3.2.

1 = Arm the phase adjustment, self clearing

Bit 0: Phase Adjust/Alignment Mode (MODE). This field sets the mode of the phase change. In output phase alignment mode, the device aligns all participating outputs and then adjusts the phase of each participating output as specified in the OCxPH register. In output phase adjustment mode the device does align the outputs and therefore causes each participating output to have the phase adjustment specified in the OCxPH register relative to that output's previous phase. See Section 3.3.2.

0 = Phase alignment mode

1 = Phase adjustment mode

4.3.2 STATUS REGISTERS

Register Name: ID1
Register Description: Device Identification Register, MSB
Register Address: 30h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	IDU[7:0]							
Default:	0	0	0	1	1	0	0	1

Bits 7 to 0: Device ID Upper (IDU[7:0]). This field is the upper eight bits of the device ID.

Register Name: ID2
Register Description: Device Identification Register, LSB and Revision
Register Address: 31h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	IDL[3:0]				REV[3:0]			
Default:	0	0	0	1	0	0	0	1

Bits 7 to 4: Device ID Lower (IDL[3:0]). This field is the lower four bits of the device ID.

Bits 3 to 0: Device Revision (REV[3:0]). These bits are the device hardware revision starting at 0.

Register Name: CFGSR
Register Description: Configuration Status Register
Register Address: 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	TEST	XOFAIL	—	—	IF[1:0]		AC[1:0]	
Default:	see below	0	0	0	see below	see below	see below	see below

Bit 7: Test Mode (TEST). This read-only bit is the latched state of the TEST pin when the RSTN pin transitions high. For proper operation it should be 0. See Section 3.1.

Bit 6: XO Fail (XOFAIL). This read-only bit is set when the external oscillator signal on the XA pin fails or when the crystal connected to the XA/XB pins fails to oscillate.

Bits 3 to 2: Interface Mode (IF[1:0]). These read-only bits are the latched state of the IF1/MISO and IF0/CSN pins when the RSTN pin transitions high. See Section 3.1.

Bits 1 to 0: Auto-Configuration (AC[1:0]). These read-only bits are the latched state of the AC1 and AC0 pins when the RSTN pin transitions high. See Section 3.1.

Register Name: GLOBISR
Register Description: Global Functions Status Register
Register Address: 43h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	READY	—	—	—	—	—	—	—
Default:	see below	0	0	0	0	0	0	0

Bit 7: Device Ready (READY). This bit indicates the status of the device after reset. It is cleared when the device is reset and set when the device is ready for operation.

Register Name: APLLSR
Register Description: APLL Status Register
Register Address: 48h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	ALK2L	ALK2	—	—	ALKL	ALK
Default:	0	0	0	0	0	0	0	0

Bit 5: APLL Lock 2 Latched Status (ALK2L). This latched status bit is set to 1 when the ALK2 status bit changes state (set or cleared). ALK2L is cleared when written with a 1.

Bit 4: APLL Lock Status 2 (ALK2). This real-time status bit provides one type of APLL lock status. System software should consider the APLL locked when ALK (bit 0) is set to 1 AND ALK2=1.

Bit 1: APLL Lock Latched Status (ALKL). This latched status bit is set to 1 when the ALK status bit changes state (set or cleared). ALKL is cleared when written with a 1.

Bit 0: APLL Lock Status (ALK). This real-time status bit indicates one type of APLL lock status. System software should consider the APLL locked when ALK=1 AND ALK2 (bit 4) is set to 1.

0 = Not locked

1 = Locked

Register Name: PASR
Register Description: Phase Adjust Status Register
Register Address: 4Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	—	ADJL	BUSY	ARMED
Default:	1	0	0	0	0	1	0	0

Bit 2: Phase Adjustment Finished (ADJL). This latched status bit is set when the output phase adjustment is completed for all participating outputs. Writing a 1 to this bit clears it. See Section 3.3.2.

0 = Output phase adjustment has not completed

1 = Output phase adjustment has completed

Bit 1: Phase Adjustment Busy (BUSY). This bit is a real time status that indicates that the output phase adjustment has been triggered and is in progress on the participating outputs. See Section 3.3.2.

0 = Output phase adjustment is not in progress

1 = Output phase adjustment is in progress

Bit 0: Phase Adjustment Armed (ARMED). This bit is a real time status that indicates that the output phase adjustment is armed and waiting for a trigger. It is cleared when the trigger event occurs. See Section 3.3.2.

0 = Output phase adjustment is not armed

1 = Output phase adjustment is armed

OC1SR
OC2SR
OC3SR

Register Name: OCxSR
Register Description: Output Clock x Status Register
Register Address: OC1: 53h, OC2: 54h, OC3: 55h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	—	—	—	STARTL	—	STOPL	STOPD
Default:	0	0	0	0	0	0	see note	see note

Bit 3: (STARTL). This latched status bit is set when the output clock signal has been started after being stopped. Writing a 1 to this bit clears it. See Section 3.3.3.

0 = Output clock signal has not resumed from being stopped

1 = Output clock signal has resumed from being stopped

Bit 1: (STOPL). This latched status bit is set when the output clock signal has been stopped. Writing a 1 to this bit clears it. See Section 3.3.3.

0 = Output clock signal has not stopped

1 = Output clock signal has stopped

Bit 0: (STOPD). This real-time status bit is high when the output clock signal is stopped and low when the output clock is not stopped. See Section 3.3.3.

0 = Output clock signal is not stopped

1 = Output clock signal is stopped

Note: STOPL and STOPD are controlled by logic that does not have a clock at reset. Therefore their reset values are indeterminate. They will become 0 when the output clock path is configured and one of the high-speed clocks from the APLL is connected to the logic.

4.3.3 OUTPUT CLOCK CONFIGURATION REGISTERS

OC1CR1
OC3CR1

Register Name: OCxCR1
Register Description: Output Clock x Configuration Register 1
Register Address: OC1: 200h, OC2: 210h, OC3: 220h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	PHEN	—	—	—	—	—	—	—
Default:	see below	0	0	0	0	1	0	1

Bit 7: Phase Adjust Enable (PHEN). This bit enables this output to participate in phase adjustment/alignment. See Section 3.3.2.

0 = Phase adjustment/alignment disabled for this output

1 = Phase adjustment/alignment enabled for this output

PHEN default value:

—	OC1	OC2	OC3
Config0	1	0	0
Config1	1	1	0
Config2	1	1	0
Config3	1	1	1

OC1CR2
OC3CR2

Register Name: OCxCR2
Register Description: Output Clock x Configuration Register 2
Register Address: OC1: 201h, OC2: 211h, OC3: 221h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	—	POL	DRIVE[1:0]		STOPDIS	—	—	—
Default:	0	see below	see below		0	varies over config and output #		

Bit 6: Clock Path Polarity (POL). The clock path to the output is inverted when this bit set. The default value for this bit is 1 for OC2 in config2; otherwise the default value is 0. See Section 3.3.1.

Bits 5 to 4: CMOS/HSTL Output Drive Strength (DRIVE[1:0]). The CMOS/HSTL output drivers have four equal sections that can be enabled or disabled to achieve four different drive strengths from 1x to 4x. When the output power supply VDDOx is 3.3V or 2.5V, the user should start with 1x and only increase drive strength if the output is highly loaded and signal transition time is unacceptable. When VDDOx is 1.8V or 1.5V the user should start with 4x and only decrease drive strength if the output signal has unacceptable overshoot. See Section 3.3.1. This field only applies in Config2 for OC2 (HSTL) and in Config3 for OC3 (CMOS). Otherwise it is ignored. The default value is 01 for OC2 in Config2; otherwise it is 00.

00 = 1x

01 = 2x

10 = 3x

11 = 4x

Bit 3: Stop Disable (STOPDIS). This bit causes the output to become disabled (high impedance) while the output clock is stopped. See Section 3.3.3.

0 = Do not disable the output while stopped

1 = Disable the output while stopped

OC1PH
OC3PH

Register Name: OCxPH
Register Description: Output Clock x Phase Adjust Register
Register Address: OC1: 207h, OC2: 217h, OC3: 227h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	PHADJ[7:0]							
Default:	see below							

Bits 7 to 0: Phase Adjust Value (PHADJ[7:0]). When OCxCR1.PHEN=1, this field specifies the phase adjustment of the output clock during a phase adjustment event. When OCxCR1.PHEN=0, this field is ignored. The specified phase adjustment occurs once during a phase adjustment event. The format of the field is 2's-complement with the LSB being one half of an APLL output clock period. See Section 3.3.2.

00000000 = 0.0 UI
00000001 = +0.5 UI
00000010 = +1.0 UI
00000011 = +1.5 UI
…
01111110 = +63.0 UI
01111111 = +63.5 UI
10000000 = -64.0 UI
10000001 = -63.5 UI
…
11111101 = -1.5 UI
11111110 = -1.0 UI
11111111 = -0.5 UI

Default value:

—	OC1	OC2	OC3
Config0	0	0	0
Config1	0	0	0
Config2	2	0	0
Config3	2	2	0

OC1STOP
OC3STOP

Register Name: OCxSTOP
Register Description: Output Clock x Start Stop Register
Register Address: OC1: 208h, OC2: 218h, OC3: 228h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name:	STOP	—	SRC[3:0]				MODE[1:0]	
Default:	0	0	0	0	0	0	0	0

Bit 7: Output Clock Stop (STOP). When SRC=0000, this bit is used to stop the output clock high or low. The output stays stopped while this bit is high. See Section 3.3.3.

0 = Do not stop the output clock

1 = Stop the output clock

Bits 5 to 2: Output Clock Stop Source (SRC[3:0]). This field specifies the source of the stop signal. See Section 3.3.3.

0000 = STOP bit

0001 = The arming of a phase adjustment (signal stopped when PASR.ARMED is asserted; signal started when PASR.ADJL is asserted)

0010 to 1111 = {unused values}

Bits 1 to 0: Output Clock Stop Mode (MODE[1:0]). This field selects the mode of the start-stop function. See Section 3.3.3.

00 = Never stop

01 = Stop High: stop after rising edge of output clock, start after falling edge of output clock

10 = Stop Low: stop after falling edge of output clock, start after rising edge of output clock

11 = {unused value}

The following table shows which pin(s) stop high or low as specified above for each output signal format:

Signal Format	Pin that Stops as Specified
CML	OCxP
HSTL	OCxN
Two CMOS, OCxP in phase with OCxN	OCxP and OCxN
One CMOS, OCxN enabled	OCxN
One CMOS, OCxP enabled	OCxP
Two CMOS, OCxP inverted vs. OCxN	OCxN

Note 1: The highest priority condition for an output is when it is stopped and OCxCR2.STOPDIS=1. When this condition occurs both OCxP and OCxN become high-impedance regardless of the state of the control bits mentioned below.

2: When the above situation does not apply, OCxCR2.POL=1 changes Stop High to Stop Low and vice versa.

5.0 ELECTRICAL CHARACTERISTICS

Note: The typical values listed in the tables of Section 5 are not production tested. Specifications to –40°C and +85°C are ensured by design or characterization and not production tested.

TABLE 5-1: ABSOLUTE MAXIMUM RATINGS

Note 1, Note 2

Parameter	Symbol	Min.	Max.	Units
Supply voltage, nominal 1.8V	VDD18	–0.3	1.98	V
Supply voltage, nominal 3.3V	VDD33	–0.3	3.63	V
Supply voltage, VDDOx (x=1,2,3)	VDDOx	–0.3	3.63	V
Voltage on XA, any OCxP/N pin	VANAPIN	–0.3	3.63	V
Voltage on any digital I/O pin	VDIGPIN	–0.3	5.5	V
Storage Temperature Range	T_{ST}	–55	+125	°C

Note 1: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

2: Voltages are with respect to ground (VSS) unless otherwise stated.

TABLE 5-2: RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage, nominal 1.8V	VDD18	1.71	1.8	1.89	V
Supply voltage, nominal 3.3V	VDD33	3.135	3.3	3.465	V
Supply voltage, VDDOx (x=1,2,3)	VDDOx	1.425	1.5	1.575	V
		1.71	1.8	1.89	
		2.375	2.5	2.625	
		3.135	3.3	3.465	
Operating temperature	T_A	–40	—	+85	°C

TABLE 5-3: SUPPLY CURRENTS

Parameter	Symbol	Min.	Typ. [1]	Max.	Units
Total current, all 1.8V supply pins, Config 0	I_{DD18}	—	93	—	mA
Total current, all 3.3V supply pins, Config 0	I_{DD33}	—	115	—	mA
Total current, all 1.8V supply pins, Config 1	I_{DD18}	—	131	—	mA
Total current, all 3.3V supply pins, Config 1	I_{DD33}	—	132	—	mA
Total current, all 1.8V supply pins, Config 2	I_{DD18}	—	123	—	mA
Total current, all 3.3V supply pins, Config 2	I_{DD33}	—	131	—	mA
Total current, all 1.8V supply pins, Config 3	I_{DD18}	—	161	—	mA
Total current, all 3.3V supply pins, Config 3	I_{DD33}	—	167	—	mA

Note 1: Typical values measured at 1.80V and 3.30V supply voltages and +25°C ambient temperature.

TABLE 5-4: NON-CLOCK CMOS PINS ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input high voltage, SCL and SDA	V_{IH}	0.7 x VDD33	—	—	V	—
Input low voltage, SCL and SDA	V_{IL}	—	—	0.3 x VDD33	V	—
Input high voltage, all other digital inputs	V_{IH}	2.0	—	—	V	—
Input low voltage, all other digital inputs	V_{IL}	—	—	0.8	V	—
Input leakage current, RSTN pin	I_{ILPU}	–85	—	10	µA	Note 1
Input leakage current, all digital inputs	I_{IL}	–10	—	10	µA	Note 1
Input capacitance	C_{IN}	—	3	10	pF	—
Input capacitance, SCL/SCLK, SDA/MOSI	C_{IN}	—	3	11	pF	—
Input hysteresis, SCL and SDA in I2C Bus Mode	—	0.05 x VDD33	—	—	mV	—
Output leakage (when high impedance)	I_{LO}	–10	—	10	µA	Note 1
Output high voltage	V_{OH}	2.4	—	—	V	I_O = –3.0 mA
Output low voltage	V_{OL}	—	—	0.4	V	I_O = 3.0 mA

Note 1: $0V < V_{IN} <$ VDD33 for all other digital inputs.

2: V_{OH} does not apply for SCL and SDA in I^2C interface mode because they are open-drain.

TABLE 5-5: XA CLOCK INPUT ELECTRICAL CHARACTERISTICS

This table covers the case when there is no external crystal connected and an external oscillator or clock signal is connected to the XA pin.

Parameter	Symbol	Min.	Typ.	Max.	Units
Input high voltage, XA	V_{IH}	1.2	—	—	V
Input low voltage, XA	V_{IL}	—	—	0.8	V
Input frequency on XA pin	f_{IN}	25			MHz
Input leakage current	I_{IL}	–10	—	10	µA
Input duty cycle	—	40	—	60	%

TABLE 5-6: CML CLOCK OUTPUTS ELECTRICAL CHARACTERISTICS

VDDOx = 3.3V±5% for CML operation.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCML}	100			MHz	—
Output high voltage, single-ended, OCxP or OCxN	$V_{OH,S}$	—	VDDOx – 0.2	—	V	AC-coupled to 50Ω termination
Output low voltage, single-ended, OCxP or OCxN	$V_{OL,S}$	—	VDDOx – 0.6	—	V	
Output common mode voltage	$V_{CM,S}$	—	VDDOx – 0.4	—	V	
Output differential voltage	$\|V_{OD,S}\|$	320	400	500	mV	
Output differential voltage, peak-to-peak	$\|V_{OD,S,PP}\|$	640	800	1000	mV_{PP}	
Difference in Magnitude of Differential Voltage for Complementary States	V_{DOS}	—	—	50	mV	—

TABLE 5-6: CML CLOCK OUTPUTS ELECTRICAL CHARACTERISTICS (CONTINUED)

VDDOx = 3.3V±5% for CML operation.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Output Rise/Fall Time	t_R, t_F	—	150	—	ps	20% to 80%
Output Duty Cycle	—	45	50	55	%	—
Output Impedance	R_{OUT}	—	50	—	Ω	Single-ended to VDDOx
Mismatch in a pair	ΔR_{OUT}	—	—	10	%	—

Note 1: The differential CML outputs can easily be interfaced to LVDS, LVPECL, CML and other differential inputs on neighboring ICs using a few external passive components. See Figure 5-2 for details.

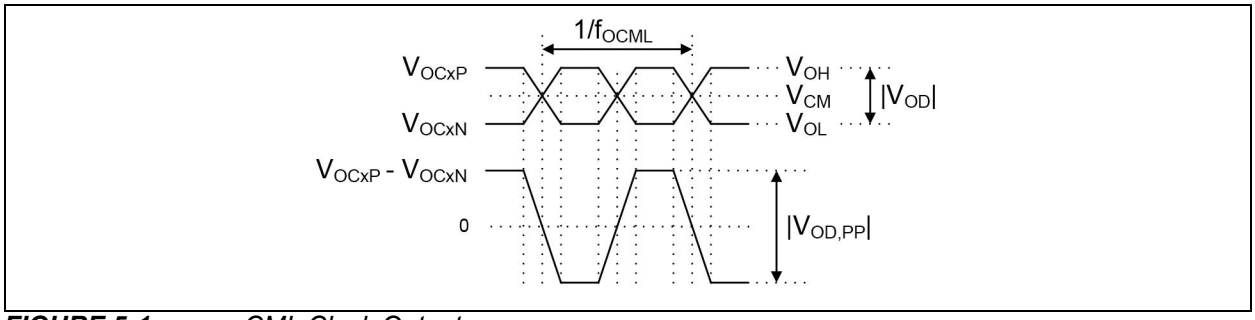


FIGURE 5-1: *CML Clock Outputs.*

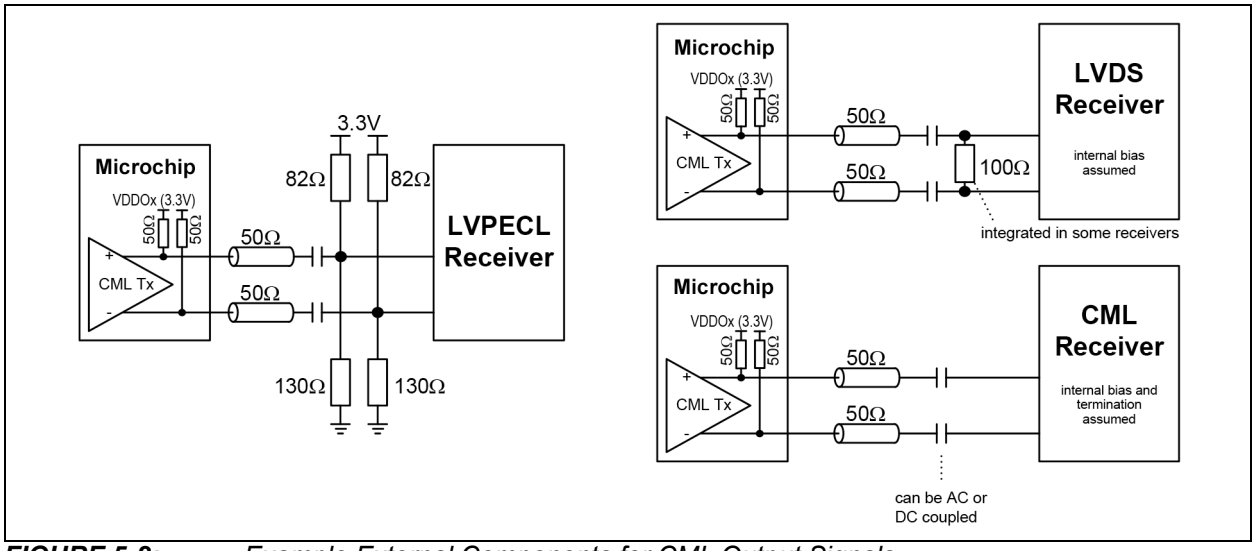


FIGURE 5-2: *Example External Components for CML Output Signals.*

TABLE 5-7: CMOS AND HSTL (CLASS I) CLOCK OUTPUTS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output frequency	f_{OCMOS}		25		MHz	—
Output high voltage	V_{OH}	VDDOx –0.4	—	VDDOx	V	Note 2, Note 3
Output low voltage	V_{OL}	0	—	0.4	V	Note 2, Note 3
Output rise/fall time, VCCOx=1.8V, OCxCR2.DRIVE=4x	t_R, t_F	—	0.4	—	ns	2 pF load
Output rise/fall time, VCCOx=1.8V, OCxCR2.DRIVE=4x		—	1.2	—		15 pF load
Output rise/fall time, VCCOx=3.3V, OCxCR2.DRIVE=1x		—	0.7	—		2 pF load
Output rise/fall time, VCCOx=3.3V, OCxCR2.DRIVE=1x		—	2.2	—		15 pF load
Output duty cycle	—	45	50	55	%	Note 4
Output duty cycle	—	42	50	58	%	Note 5, Note 6
Output duty cycle, OCxNEG single-ended	—	—	50	—	%	Note 5
Output duty cycle, OCxPOS single-ended	—	—	46	—	%	Note 5
Output current when output disabled	—	—	10	—	µA	—

Note 1: Measured with a series resistor of 33Ω and a 5 pF load capacitance unless otherwise specified.

2: For HSTL Class I, V_{OH} and V_{OL} apply for both unterminated loads and for symmetrically terminated loads, i.e. 50Ω to VDDOx/2.

3: For VDDOx = 3.3V and OCxCR2.DRIVE = 1x, I_O = 4 mA. For VDDOx = 1.5V and OCxCR2.DRIVE = 4x, I_O = 8 mA.

4: VDDOx ≥ 1.8V.

5: VDDOx < 1.8V.

6: Measured differentially.

5.1 Interfacing to HCSL Components

In Config2, output OC2 is HSTL mode. HSTL mode with VDDO2 = 1.8V can provide an HCSL-compatible signal (V_{OH} typically 0.75V) to a neighboring component when configured as shown in Figure 5-3 below. The resistor R_S should be 20Ω.

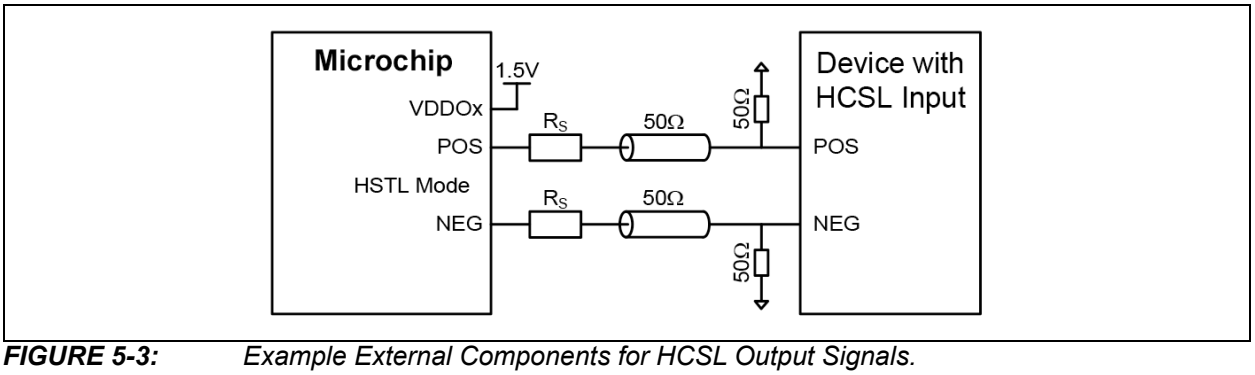


FIGURE 5-3: *Example External Components for HCSL Output Signals.*

TABLE 5-8: TYPICAL INPUT-TO-OUTPUT CLOCK DELAY

Mode	Delay, Input Clock Edge to Output Clock Edge
All Modes	Non-deterministic but constant as long as the APLL remains locked and output clock phases are not adjusted as described in Section 3.3.2.1.

TABLE 5-9: TYPICAL OUTPUT-TO-OUTPUT CLOCK DELAY

Mode	Delay, Input Clock Edge to Output Clock Edge
All Modes	<100 ps Requires phase adjustment and phase alignment capability described in Section 3.3.2.

TABLE 5-10: SPI CLIENT INTERFACE TIMING

Parameter (Note 1 through Note 3)	Symbol	Min.	Typ.	Max.	Units
SCLK frequency	f_{BUS}	—	—	10	MHz
SCLK cycle time	t_{CYC}	100	—	—	ns
CSN setup to first SCLK edge	t_{SUC}	50	—	—	ns
CSN hold time after last SCLK edge	t_{HDC}	50	—	—	ns
CSN high time	t_{CSH}	50	—	—	ns
SCLK high time	t_{CLKH}	40	—	—	ns
SCLK low time	t_{CLKL}	40	—	—	ns
MOSI data setup time	t_{SUI}	10	—	—	ns
MOSI data hold time	t_{HDI}	10	—	—	ns
MISO enable time from SCLK edge	t_{EN}	0	—	—	ns
MISO disable time from CSN high	t_{DIS}	—	—	80	ns
MISO data valid time	t_{DV}	—	—	40	ns
MISO data hold time from SCLK edge	t_{HDO}	0	—	—	ns
CSN, MOSI input rise time, fall time	t_R, t_F	—	—	10	ns

Note 1: All timing is specified with 100 pF load on all SPI pins.

2: All parameters in this table are ensured by design or characterization.

3: See the timing diagram in Figure 5-4.

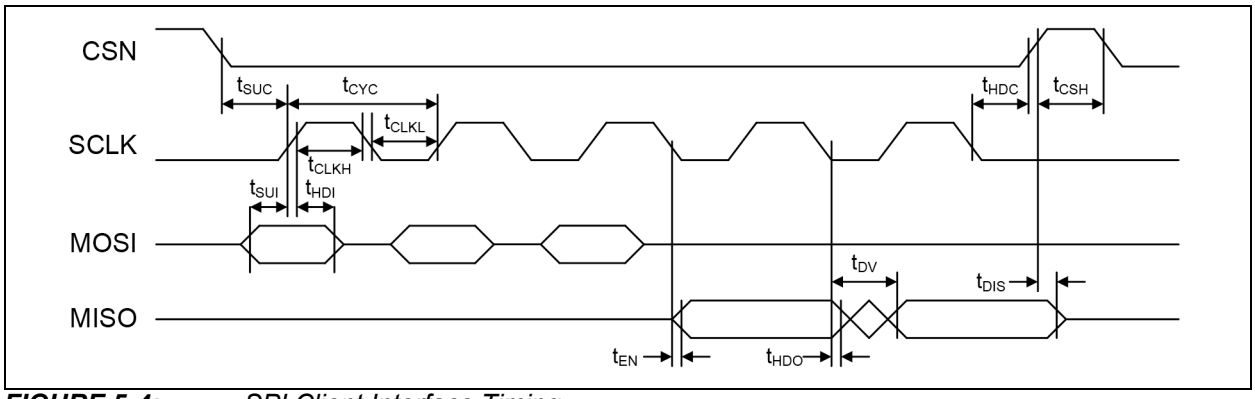


FIGURE 5-4: *SPI Client Interface Timing.*

TABLE 5-11: I²C CLIENT INTERFACE TIMING

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
SCL clock frequency	f_{SCL}	—	—	400	kHz	—
Hold time, START condition	$t_{HD:STA}$	0.6	—	—	µs	—
Low time, SCL	t_{LOW}	1.3	—	—	µs	—
High time, SCL	t_{HIGH}	0.6	—	—	µs	—
Setup time, START condition	$t_{SU:STA}$	0.6	—	—	µs	—
Data hold time	$t_{HD:DAT}$	0	—	0.9	µs	Note 2, Note 3
Data setup time	$t_{SU:DAT}$	100	—	—	ns	—
Rise time	t_R	—	—	—	ns	Note 4
Fall time	t_F	20 + 0.1C_b	—	300	ns	C_b is cap. of one bus line
Setup time, STOP condition	$t_{SU:STO}$	0.6	—	—	µs	—
Bus free time between STOP/START	t_{BUF}	1.3	—	—	µs	—
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	—	50	ns	—

Note 1: The timing parameters in this table are specifically for 400 kbps Fast Mode. Fast Mode devices are downward-compatible with 100 kbps Standard Mode I²C bus timing. All parameters in this table are ensured by design or characterization. All values referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels (see Table 5-4).

2: The device internally provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.

3: The I²C specification indicates that the maximum $t_{HD:DAT}$ spec only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. The device does not stretch the low period of the SCL signal.

4: Determined by choice of pull-up resistor.

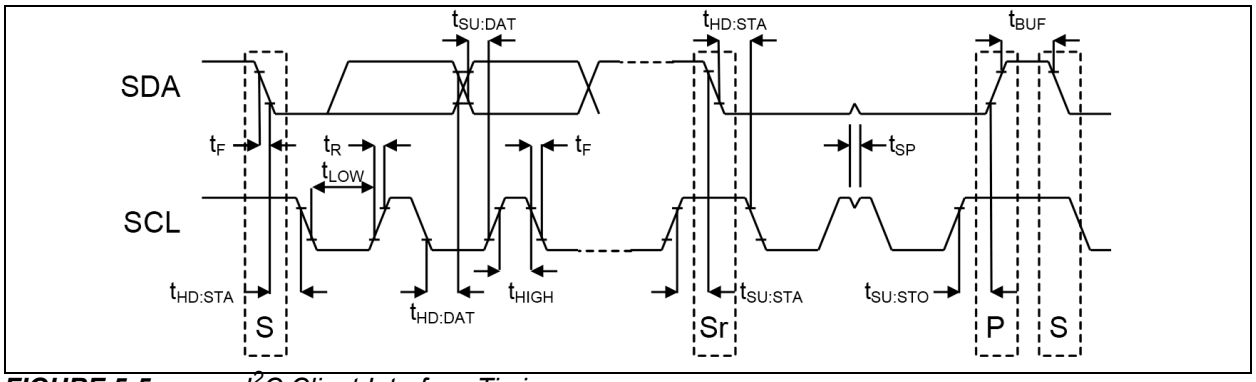


FIGURE 5-5: *I²C Client Interface Timing.*

TABLE 5-12: 5 MM X 5 MM VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Conditions	Value
Maximum Ambient Temperature	T_A	—	85°C
Maximum Junction Temperature	$T_{J(MAX)}$	—	125°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	Still-air	29.6°C/W
		1m/s airflow	23.3°C/W
		2.5m/s airflow	20.6°C/W
Junction to Board Thermal Resistance	θ_{JB}	—	9.8°C/W
Junction to Case Thermal Resistance	θ_{JC}	—	17.5°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	Still-air	3.4°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still-air	0.2°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power.

2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

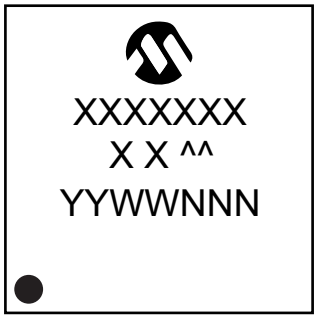
3: For all numbers in the table, the exposed pad is connected to the ground plane with a 5x5 array of thermal vias; via diameter 0.33 mm; via pitch 0.76 mm.

NOTES:

6.0 PACKAGE OUTLINE

6.1 Package Marking Information

32-Lead VQFN*



Example

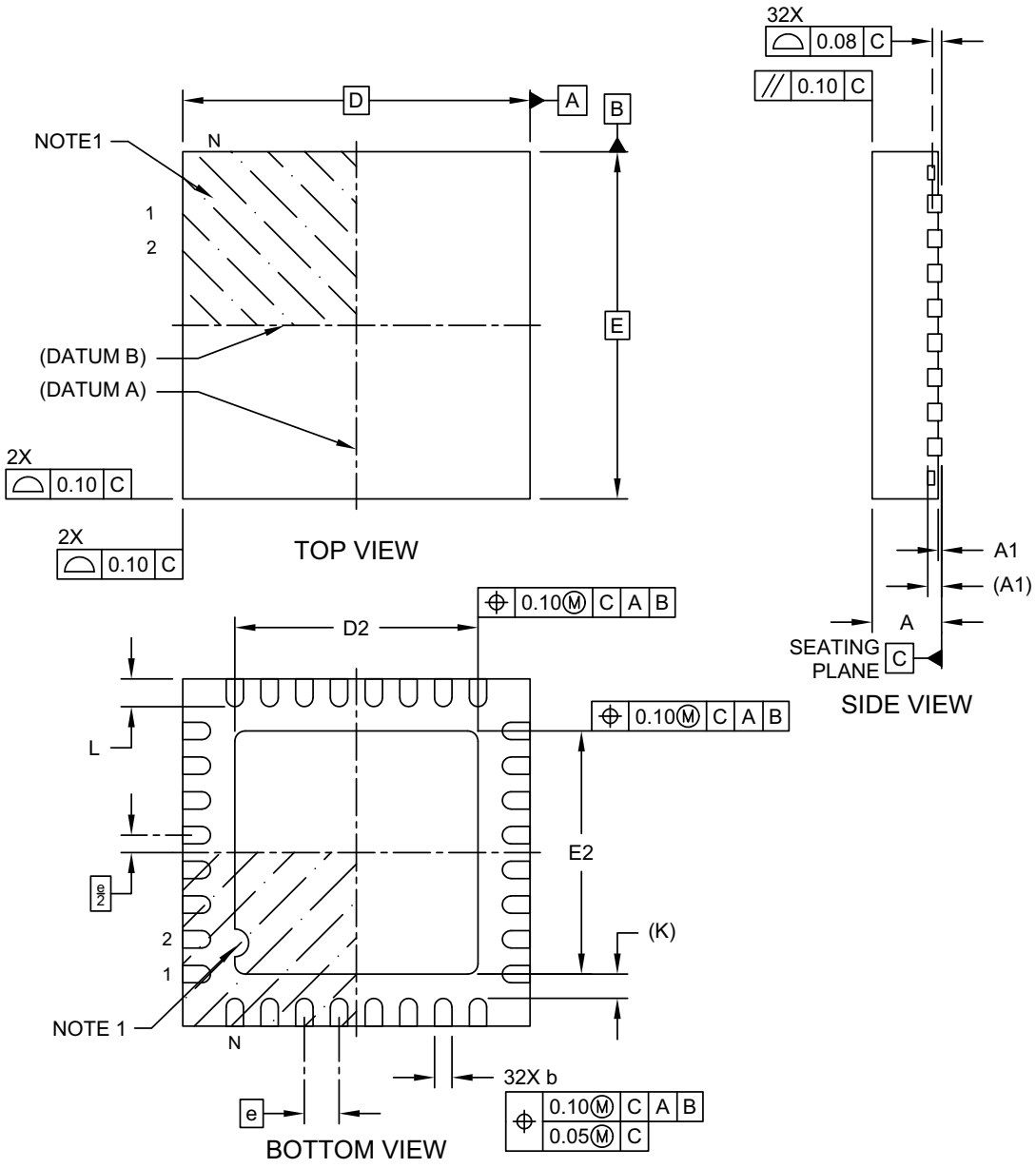
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

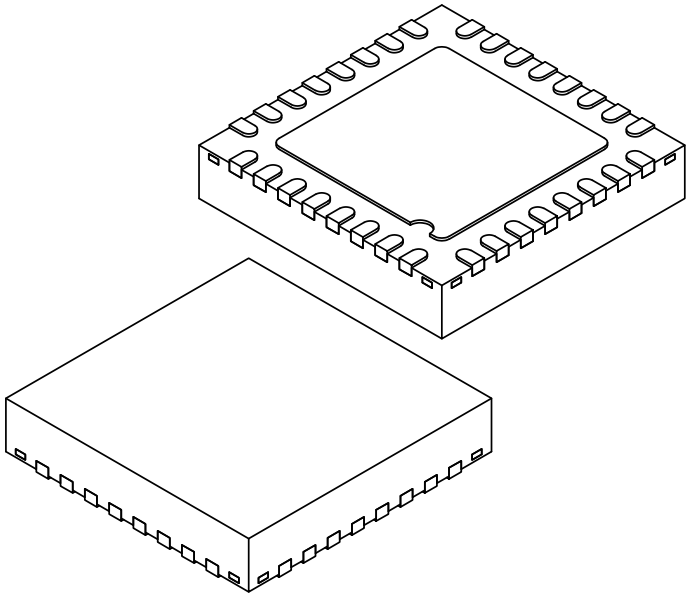
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25401 Rev A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.40	3.50	3.60
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.40	3.50	3.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.35 REF	

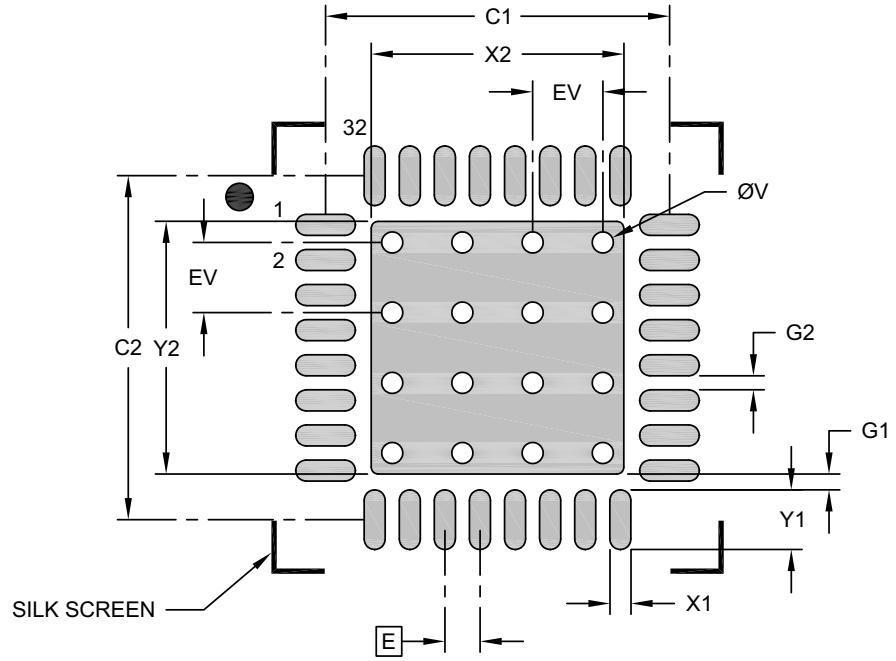
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25401 Rev A Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (M4C) - 5x5x1 mm Body [VQFN] With 3.50 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.60
Optional Center Pad Length	Y2			3.60
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27401 Rev A

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006736A (09-29-22)	—	Converted Microsemi data sheet ZL30281 to Microchip DS20006736A. Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL30281: Three-Output PCIe Clock Generator
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 32-Lead 5 mm x 5 mm VQFN
Media Type:	F = 4,000/Reel G = 490/Tray
Finish:	1 = Pb Free with Matte Sn lead finish, RoHS e3 Compliant

Examples:

a) ZL30281LDF1:

Three-Output PCIe Clock Generator, Leadless Chip Carrier, 32-Lead VQFN, 4,000/Reel, Pb Free with Matte Sn lead finish, RoHS e3 Compliant

b) ZL30281LDG1:

Three-Output PCIe Clock Generator, Leadless Chip Carrier, 32-Lead VQFN, 490/Tray, Pb Free with Matte Sn lead finish, RoHS e3 Compliant

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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