ZL30282

6-Output PCIe Clock Generator

Features

- 50 MHz Crystal or CMOS Input
- Generates PCIe 1, 2, 3, 4, 5 Compliant Clocks
- Spread-Spectrum Clocks (SSC) and Regular Clocks at the Same Time (Configs 5-8)
- Output Jitter <0.3 ps_{RMS} 12 kHz - 20 MHz Typical for Non-Spread-Spectrum Outputs
- Up to 6 Output Clocks with 8 Default Configurations Selected by Hardware Pins at Reset: (Configs 0-3 no SSC, Configs4-7 SSC for OC3-6)
  - **Config0/4**: OC1 100 MHz HCSL, OC2_P 25 MHz LVCMOS, OC3/4/5 unused, OC6 100 MHz HCSL
  - **Config1/5**: OC1 100 MHz HCSL, OC2_P 25 MHz LVCMOS, OC3/4/5/6 100 MHz HCSL
  - **Config2/6**: OC1 100 MHz HCSL, OC2_P 75 MHz LVCMOS, OC3/4/5/6 100 MHz HCSL
  - **Config3/7**: OC1/2 100 MHz HCSL, OC3/4/5/6 100 MHz HCSL
- Per-Output Control via SPI or I^2C Interface
  - Precise Output Alignment Circuitry and Per-Output Phase Adjustment
  - Per-Output Enable/Disable and Glitchless Start/Stop (Stop High or Low)
  - Spread-Spectrum Enable/Disable for DIV2
- Core Supply Voltage Options: 2.5V only, 3.3V only, 1.8V+2.5V or 1.8V+3.3V
- Space-Saving 8 mm x 8 mm 56-Lead QFN (0.5 mm Pitch)

Applications

- PCIe Gen1-5 Clock Generation for JBOF, Riser Card and Storage System

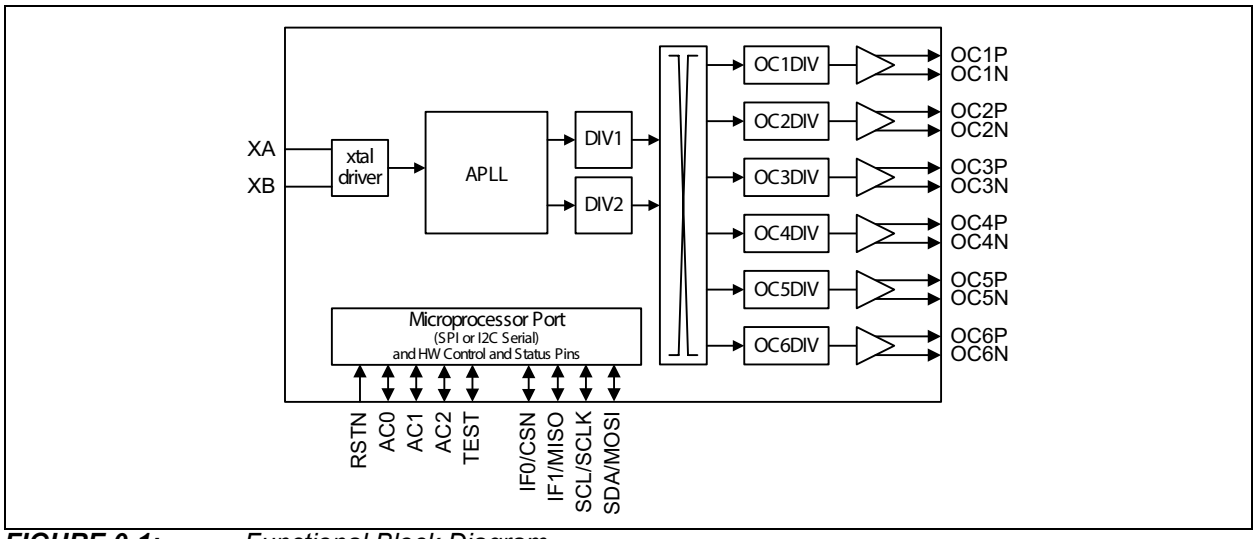

FIGURE 0-1: *Functional Block Diagram.*

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TABLE OF CONTENTS

List of Figures

List of Tables

NOTES:

1.0 PIN DESCRIPTION AND CONFIGURATION

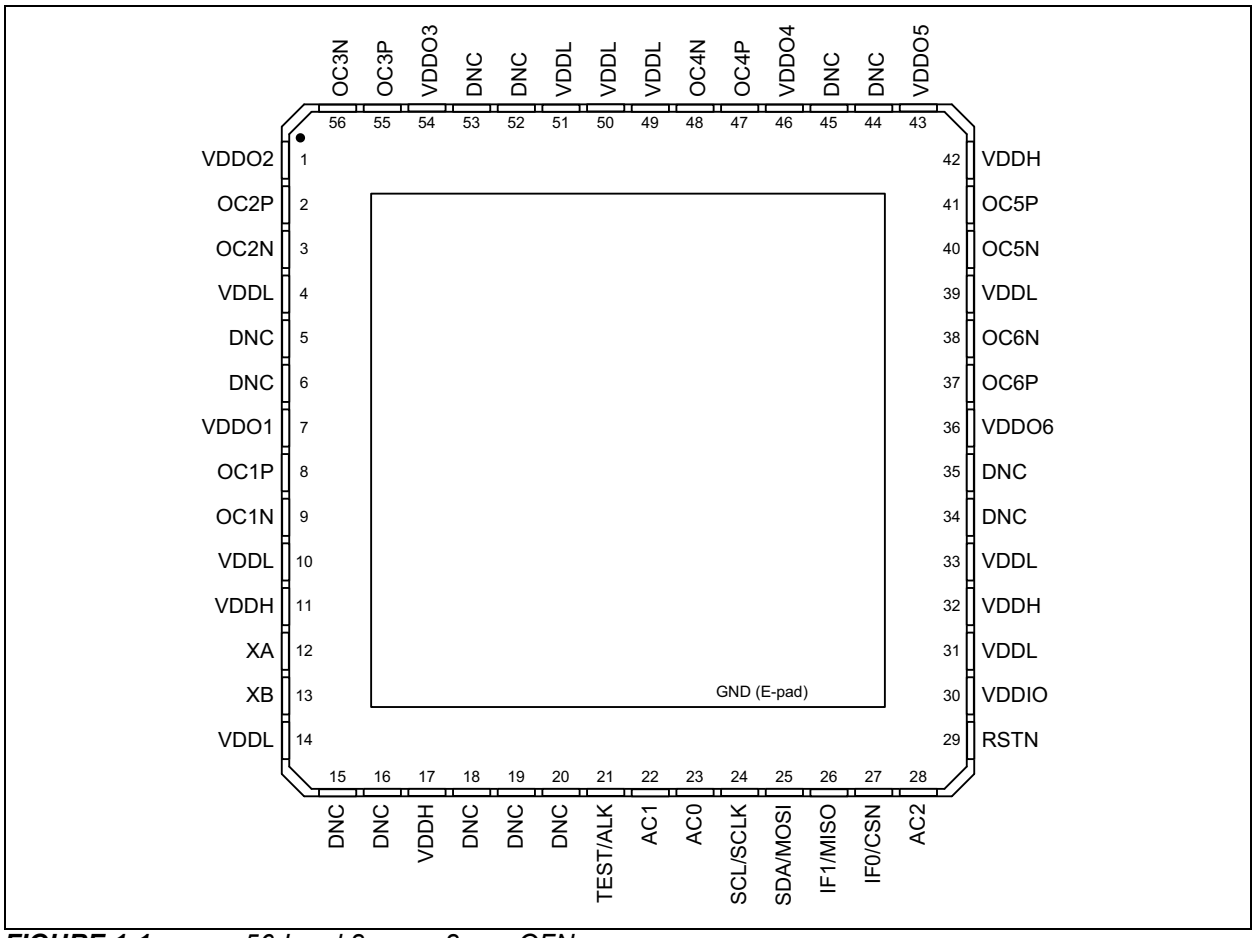


FIGURE 1-1: *56-Lead 8 mm x 8 mm QFN.*

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – Input, O – Output, A – Analog, P – Power Supply pin. All SPI/I^2C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

TABLE 1-1: PIN DESCRIPTIONS

Pin Number	Name	Type	Description
12 13	XA XB	A/I	**Crystal or Input Clock Pins** *Crystal:* MCR2.XAB=01. An on-chip crystal driver circuit is designed to work with an external crystal connected to the XA and XB pins. See Section 2.2.2 for crystal characteristics and recommended external components. *Input Clock:* MCR2.XAB=10. An external local oscillator or clock signal can be connected to the XA pin. The XB pin must be left unconnected. The signal on XA can be as large as 3.3V even when VDDH is only 2.5V.
8,9 2,3 55,56 47,48 41,40 37,38	OC1P,OC1N OC2P,OC2N OC3P,OC3N OC4P,OC4N OC5P,OC5N OC6P,OC6N	O	**Output Clock Pins** HCSL or CMOS. Programmable drive strength in CMOS mode. See Figure 9 for example external interface circuitry. See Table 9 for electrical specifications for HCSL. See Table 10 for electrical specifications for interfacing to CMOS inputs on neighboring devices.

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Name	Type	Description
29	RSTN	I	**Reset (Active-Low)** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. Minimum low time is 1 µs.
23 22 28	AC0 AC1 AC2	I/O	**Auto-Configure [2:0]** On the rising edge of RSTN these pins specify the device configuration. See Section 2.1.
21	TEST/ALK	I/O	**Factory Test** *Factory Test:* For normal operation this pin must be low on the rising edge of RSTN. *APLL Lock:* After reset this pin is an output that indicates APLL lock. 0 = Not locked, 1 = Locked.
27	IF0/CSN	I/O	**Interface Mode 0/SPI Chip Select (Active-Low)** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF0 and, together with IF1, specifies the interface mode for the device. See Section 2.1. *SPI Chip Select:* After reset this pin is CSN. An external SPI master must assert (low) CSN to access device registers. CSN should not be allowed to float.
26	IF1/MISO	I/O	**Interface Mode 1/SPI Master-In-Slave-Out** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF1 and, together with IF0, specifies the interface mode for the device. See Section 2.1. *SPI MISO:* After reset this pin is MISO. The device outputs data to an external SPI master on MISO during SPI read transactions.
24	SCL/SCLK	I/O	**I^2C Clock/SPI Clock** *I^2C Clock:* An external I^2C master must provide the I^2C clock signal on the SCL pin. In I^2C mode this pin should be externally pulled high by a 1 kΩ to 5 kΩ resistor. *SPI Clock:* An external SPI master must provide the SPI clock signal on SCLK.
25	SDA/MOSI	I/O	**I^2C Data/SPI Master-Out-Slave-In** *I^2C Data:* SDA is the bidirectional data line between the device and an external I^2C master. In I^2C mode this pin should be externally pulled high by a 1 kΩ to 5 kΩ resistor. *SPI MOSI:* An external SPI master sends commands, addresses, and data to the device on MOSI.
11,17 32,42	VDDH	P	**Higher Core Power Supply** 2.5V or 3.3V ±5%. When VDDH = 3.3V the device has additional internal power supply regulators enabled.
4,10,14, 31,33, 39,49, 50,51	VDDL	P	**Lower Core Power Supply** 1.8V ±5% or same voltage as VDDH.
30	VDDIO	P	**Digital Power Supply for Non-Clock I/O Pins** 1.8V to VDDH.
7	VDDO1	P	**Power Supply for OC1P/N** 1.5V to VDDH.
1	VDDO2	P	**Power Supply for OC2P/N** 1.5V to VDDH.
54	VDDO3	P	**Power Supply for OC3P/N** 1.5V to VDDH.

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Name	Type	Description
46	VDDO4	P	**Power Supply for OC4P/N** 1.5V to VDDH.
43	VDDO5	P	**Power Supply for OC5P/N** 1.5V to VDDH.
36	VDDO6	P	**Power Supply for OC6P/N** 1.5V to VDDH.
5,6,15, 16,18, 19,20, 34,35, 44,45, 52,53	DNC	—	**Do Not Connect** Leave these pins floating.
ePad	VSS	P	**Ground** 0 volts.

Note: The voltages on VDDL, VDDIO, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

2.0 FUNCTIONAL DESCRIPTION

2.1 Pin-Controlled Automatic Configuration at Reset

The device configuration is determined at reset (i.e. on the rising edge of RSTN) by the signal levels on these device pins: TEST/ALK, AC2, AC1, AC0, IF1/MISO, and IF0/CSN. For these pins, the first name (TEST, AC2, AC1, AC0, IF1, IF0) indicates their function when they are sampled by the rising edge of the RSTN pin. The second name refers to their function after reset. The values of these pins are latched into the CFGSR register when RSTN goes high. To ensure the device properly samples the reset values of these pins, the following guidelines should be followed:

1. Any pull-up or pull-down resistors used to set the value of these pins at reset should be 1 kΩ.
2. RSTN must be asserted at least as long as specified in Section 2.5.

The hardware configuration pins are grouped into three sets:

1. TEST – Manufacturing test mode
2. IF[1:0] – Microprocessor interface mode and I^2C address
3. AC[2:0] – Auto-config configuration number (0 to 7)

The TEST pin selects manufacturing test modes when TEST = 1 at the deassertion of RSTN. Therefore TEST must be low when RSTN is deasserted.

For all of these pins Microchip recommends that board designs include component sites for both pull-up and pull-down resistors (only one or the other populated per pin).

The IF[1:0] pins specify the processor interface mode and the I^2C slave address. The AC[2:0] pins specify one of eight device configurations.

Note: All eight device configurations require either:

a) A 50 MHz crystal between the XA and XB pins or

b) A 50 MHz XO driving the XA pin.

TABLE 2-1: IF PINS PROCESSOR INTERFACE MODES

IF1	IF0	Processor Interface
0	X	I^2C, slave address 111 0111
1	0	I^2C, slave address 111 0111
1	1	SPI slave

TABLE 2-2: AC PINS DEVICE CONFIGURATIONS

AC2	AC1	AC0	Configuration
0	0	0	Config0: 100 MHz HCSL on OC1, 25 MHz CMOS on OC2P, OC3/4/5 unused, 100 MHz HCSL on OC6, no SSC, all from DIV1
0	0	1	Config1: 100 MHz HCSL on OC1, 25 MHz CMOS on OC2P, 100 MHz HCSL on OC3-OC6, no SSC, all from DIV1
0	1	0	Config2: 100 MHz HCSL on OC1, 75 MHz CMOS on OC2P, 100 MHz HCSL on OC3-OC6, no SSC, all from DIV1
0	1	1	Config3: 100 MHz HCSL on OC1 and OC2, 100 MHz HCSL on OC3-OC6, no SSC, all from DIV1
1	0	0	Config4: Same as Config0 but OC6 SSC from DIV2
1	0	1	Config5: Same as Config1 but OC3-OC6 SSC from DIV2
1	1	0	Config6: Same as Config2 but OC3-OC6 SSC from DIV2
	1	1	Config7: Same as Config3 but OC3-OC6 SSC from DIV2

2.2 Local Oscillator or Crystal

Section 2.2.1 describes how to connect an external oscillator and the required characteristics of the oscillator. Section 2.2.2 describes how to connect an external crystal to the on-chip crystal driver circuit and the required characteristics of the crystal.

2.2.1 EXTERNAL OSCILLATOR

A 50 MHz signal from an external oscillator can be connected to the XA pin (XB must be left unconnected). To minimize jitter, the signal must be properly terminated and must have very short trace length. A poorly terminated single-ended signal can greatly increase output jitter, and long single-ended trace lengths are more susceptible to noise. When MCR2.XAB=10, XA is enabled as a single-ended input.

The jitter on output clock signals depends on the phase noise and frequency of the external oscillator.

2.2.2 EXTERNAL CRYSTAL AND ON-CHIP DRIVER CIRCUIT

The on-chip crystal driver circuit is designed to work with a fundamental mode, AT-cut crystal resonator. See Table 2-1 for recommended crystal specifications. To enable the crystal driver, set MCR2.XAB=01.

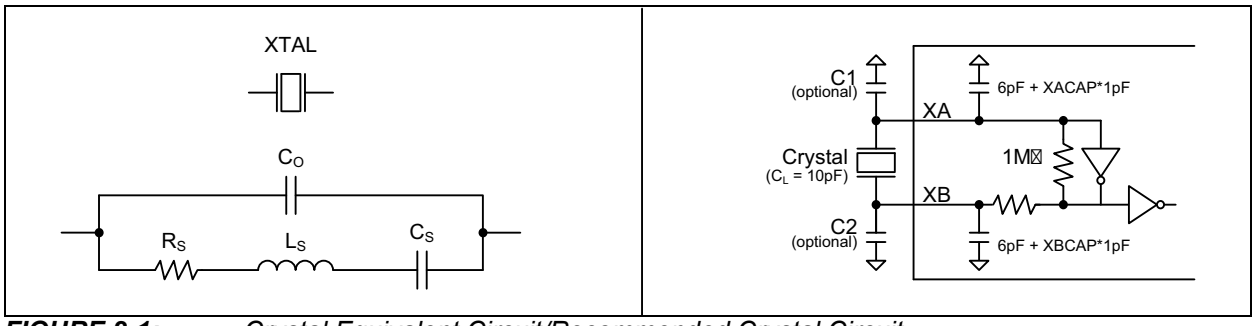


FIGURE 2-1: *Crystal Equivalent Circuit/Recommended Crystal Circuit.*

Figure 2-1 shows the crystal equivalent circuit and the recommended external component connections. The driver circuit design includes configurable internal load capacitors. For a 10 pF crystal the total capacitance on each of XA and XB should be 2 x 10 pF = 20 pF. To achieve these loads without external capacitors, register field XACR3.XACAP should be set to 20 pF minus actual XA external board trace capacitance minus XA's minimum internal capacitance of 6 pF. For example, if external trace capacitance is 2 pF then XACAP should be set to 20 pF – 2 pF – 6 pF = 12 pF. Register field XACR3.XBCAP should be set in a similar manner for XB load capacitance. Crystals with nominal load capacitance other than 10 pF usually can be supported with only internal load capacitance. If the XACAP and XBCAP fields do not have sufficient range for the application, capacitance can be increased by using external caps C1 and C2.

Note: For this device, the default XA pin and XB pin internal capacitive load is 13 pF. The GUI displays XACAP+6 pF and XBCAP+6 pF, which means that XACR3.XACAP = 7 pF and XACR3.XBCAP = 7 pF.

Users should also note that on-chip capacitors are not nearly as accurate as discrete capacitors (which can have 1% accuracy). If tight frequency accuracy is required for the crystal driver circuit then set XACAP and XBCAP both to 0 and choose appropriate C1 and C2 capacitors with 1% tolerance.

The crystal, traces, and two external capacitors sites (if included) should be placed on the board as close as possible to the XA and XB pins to reduce crosstalk of active signals into the oscillator. Also no active signals should be routed under the crystal circuitry.

Note: Crystals have temperature sensitivities that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO or TCXO should be used instead.

TABLE 2-3: CRYSTAL SELECTION PARAMETERS

Parameter		Symbol	Min.	Typ.	Max.	Units
Crystal Oscillator Frequency (Note 1)		f_{OSC}	—	50	—	MHz
Shunt Capacitance		C_O	—	2	5	pF
Load Capacitance (Note 2)		C_L	8	10	16	pF
Equivalent Series Resistance (ESR) (Note 3)	f_{OSC} < 40 MHz	R_S	—	—	60	Ω
	f_{OSC} > 40 MHz	R_S	—	—	50	Ω
Maximum Crystal Drive Level		—	100	100, 200, 300	—	µW
Crystal Frequency Stability vs. Power Supply		f_{FVD}	—	0.2	0.5	ppm per 10% Δ in VDD

Note 1: Crystal must be 50 MHz nominal.

2: For crystals with 100 µW max drive level C_L ≥ 16 pF is not supported. Crystals with max drive level of 200 µW or higher do not have these limitations.

3: These ESR limits are chosen to constrain crystal drive level to less than 100 µW. If the crystal can tolerate a drive level greater than 100 µW, then proportionally higher ESR is acceptable.

4: By the default the device is configured to drive 100 µW max drive level. For crystals with 200 µW or 300 µW max drive level, the XACR2 register should be set as described in the XACR2 register description.

2.3 Output Clock Configuration

The device has six output clock signal pairs. Each output has individual enable, start/stop and alignment controls. The outputs can be aligned relative to each other, and the phases of output signals can be adjusted dynamically with high resolution.

2.3.1 OUTPUT SIGNAL FORMAT, VOLTAGE, AND INTERFACING

The signal format of each output is determined by the configuration number specified by the AC[2:0] pins at device reset (see Table 2-2). The clock to the output driver can inverted by setting OCxCR2.POL=1. The CMOS output driver can be set to any of four drive strengths using OCxCR2.DRIVE.

Each output has its own power supply pin to allow CMOS signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components. Note that HCSL outputs must have a power supply voltage of 2.5V or 3.3V. Also note that VDDO voltage must not exceed VDDH voltage.

Each HCSL output requires a DC path through a 50Ω resistor to ground on each of OCxP and OCxN.

2.3.2 OUTPUT PHASE ADJUSTMENT

The phase of an output signal can be shifted by 180° by setting OCxCR2.POL=1. In addition, the phase can be adjusted using the OCxPH.PHADJ register field. The adjustment is in units of DIV1 or DIV2 clock periods. For outputs from DIV1, the DIV1 frequency is 600 MHz and resolution is half of one period, i.e. 0.833 ns. For outputs from DIV2 (OC3-OC6 in Configs4-7), the DIV2 frequency is 200 MHz and resolution is half of one period, i.e. 2.5 ns.

2.3.3 OUTPUT-TO-OUTPUT PHASE ALIGNMENT

A 0-to-1 transition of the ACR1.DALIGN bit causes a simultaneous reset of the dividers for all output clocks where OCx-CR1.PHEN=1. After this reset, all PHEN=1 output clocks with frequencies that are exactly integer multiples of one another are rising-edge aligned, with the phase of each output clock signal adjusted as specified by its OCxPH.PHADJ register field. The device does not support alignment of outputs from DIV1 with outputs from DIV2. The alignment function should only be applied to outputs from DIV1 or to outputs from DIV2 but not a mix of both.

Alignment is not glitchess; i.e. it may cause a short high time or low time on participating output clock signals. A glitchless alignment can be accomplished by first stopping the clocks, then aligning them, then starting them. Output clock start and stop is described in Section 2.3.4.

2.3.4 OUTPUT CLOCK START, STOP, AND HIGH-IMPEDANCE

Output clocks can be stopped high, low, or high-impedance. One use for this behavior is to ensure glitchless output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an OCxSTOP register with fields to control this behavior. The OCxSTOP.MODE field specifies whether the output clock signal stops high, low, or high-impedance. The OCxSTOP.SRC field specifies the source of the stop signal. When OCxSTOP.SRC=0001 the output clock is stopped when the corresponding bit is set in the STOPCR registers OR the MCR1.STOP bit is set.

When the stop mode is Stop High (OCxSTOP.MODE=x1) and the stop signal is asserted, the output clock is stopped after the next rising edge of the output clock. When the stop mode is Stop Low (OCxSTOP.MODE=x0) and the stop signal is asserted, the output clock is stopped after the next falling edge of the output clock. When the output is stopped, the output driver can optionally go high-impedance (OCxSTOP.MODE=1x). Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on.

When OCxCR2.POL=1 the output stops on the opposite polarity that is specified by the OCxSTOP.MODE field.

Each output has a status register (OCxSR) with several stop/start status bits. The STOPD bit is a real-time status bit indicating stopped or not stopped. The STOPL bit is a latched status bit that is set when the output clock has stopped. The STARTL bit is a latched status bit that is set when the output clock has started.

2.4 Microprocessor Interface

The device can communicate over a SPI interface or an I^2C interface.

In SPI mode the device can only be configured as a SPI slave to a processor master. The device is always a slave on the I^2C bus.

Section 2.1 describes reset pin settings required to configure the device for these interfaces.

2.4.1 SPI SLAVE

The device can present a SPI slave port on the CSN, SCLK, MOSI, and MISO pins. SPI is a widely used master/slave bus protocol that allows a master and one or more slaves to communicate over a serial bus. SPI masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master, which also generates the SCLK signal. The device receives serial data on the Master Out Slave In (MOSI) pin and transmits serial data on the Master In Slave Out (MISO) pin. MISO is high impedance except when the device is transmitting data to the bus master.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MOSI on the rising edge of SCLK and updates data on MISO on the falling edge of SCLK. SCLK does not have to toggle between accesses, i.e., when CSN is high.

Device Selection. Each SPI device has its own chip-select line. To select the device, the bus master drives its CSN pin low.

Command and Address. After driving CSN low, the bus master transmits an 8-bit command followed by a 16-bit register address. The available commands are shown below.

TABLE 2-4: SPI COMMANDS

Command	Hex	Bit Order, Left to Right
Write	0x02	0000 0010
Read	0x03	0000 0011

Read Transactions. After driving CSN low, the bus master transmits the read command followed by the 16-bit address. The device then responds with the requested data byte on MISO, increments its address counter, and pre-fetches the next data byte. If the bus master continues to demand data, the device continues to provide the data on MISO, increment its address counter, and pre-fetch the following byte. The read transaction is completed when the bus master drives CSN high. See Figure 2-2.

Write Transactions. After driving CSN low, the bus master transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device receives the first data byte on MOSI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the device continues to write the data received and increment its address counter. The write transaction is completed when the bus master drives CSN high. See Figure 2-3.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling CSN high. In response to early terminations, the device resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, the data byte is not written.

Design Option. Wiring MOSI and MISO Together. Because communication between the bus master and the device is half-duplex, the MOSI and MISO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the MOSI/MISO line when the device is transmitting.

AC Timing. See Table 13 and Figure 10 for AC timing specifications for the SPI interface.

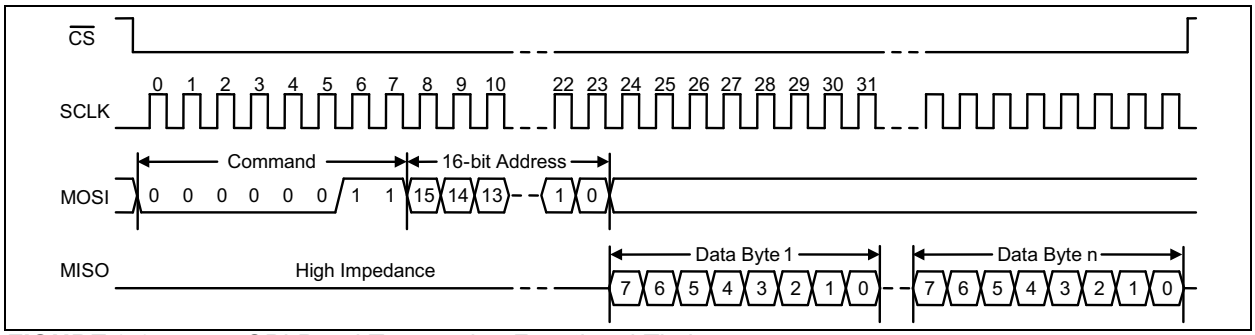


FIGURE 2-2: *SPI Read Transaction Functional Timing.*

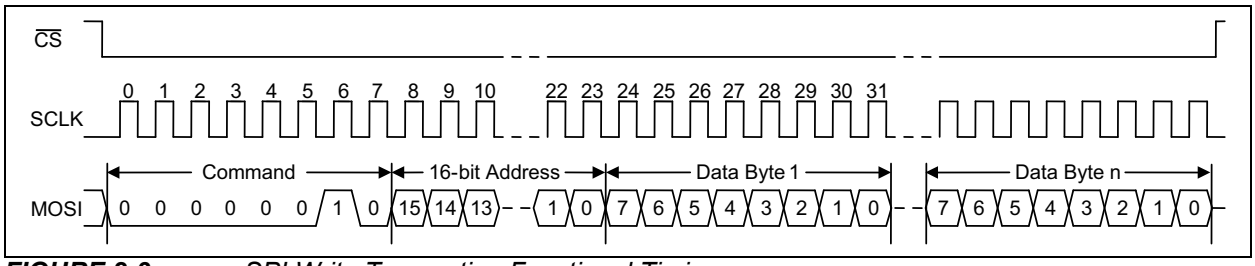


FIGURE 2-3: *SPI Write Transaction Functional Timing.*

2.4.2 I²C SLAVE

The device can present a fast-mode (400 kbit/s) I²C slave port on the SCL and SDA pins. I²C is a widely used master/slave bus protocol that allows one or more masters and one or more slaves to communicate over a two-wire serial bus. I²C masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master, which also generates the SCL signal. The device is compliant with version 2.1 of the I²C specification.

The I²C interface on the device is a protocol translator from external I²C transactions to internal SPI transactions. This explains the slightly increased protocol complexity described in the paragraphs that follow.

Read Transactions. The bus master first does an I²C write to the device. In this transaction three bytes are written: the SPI Read command (see Table 2-4), the upper byte of the register address, and the lower byte of the register address. The bus master then does an I²C read. During each acknowledge (A) bit the device fetches data from the read address and then increments the read address. The device then transmits the data to the bus master during the next 8 SCL cycles. The bus master terminates the read with a not-acknowledge (NA) followed by a STOP condition (P). See Figure 2-4. After the I²C write there can be unlimited idle time on the bus before the I²C read, but the device cannot tolerate other I²C bus traffic between the I²C write and the I²C read. Care must be taken to ensure that the I²C read is the first command on the bus after the I²C write to ensure the two-part read transaction happens correctly.

Write Transactions. The bus master does an I²C write to the device. The first three bytes of this transaction are the SPI Write command (see Table 2-4), the upper byte of the register address, and the lower byte of the register address. Subsequent bytes are data bytes to be written. After each data byte is received, the device writes the byte to the write address and then increments the write address. The bus master terminates the write with a STOP condition (P). See Figure 2-5.

I²C Features Not Supported by the Device. The I²C specification has several optional features that are not supported by the device. These are: 3.4 Mbit/s high-speed mode (Hs-mode), 10-bit device addressing, general call address, software reset, and device ID. The device does not hold SCL low to force the master to wait.

I²C Slave Address. The device's 7-bit slave address can be pin-configured for any of three values. These values are show in the table in Section 2.1.

Bit Order. The I²C specification requires device address, register address and all data bytes to be transmitted most significant bit first on the SDA signal.

Note: As required by the I²C specification, when power is removed from the device, the SDA and SCL pins are left floating so they don't obstruct the bus lines.

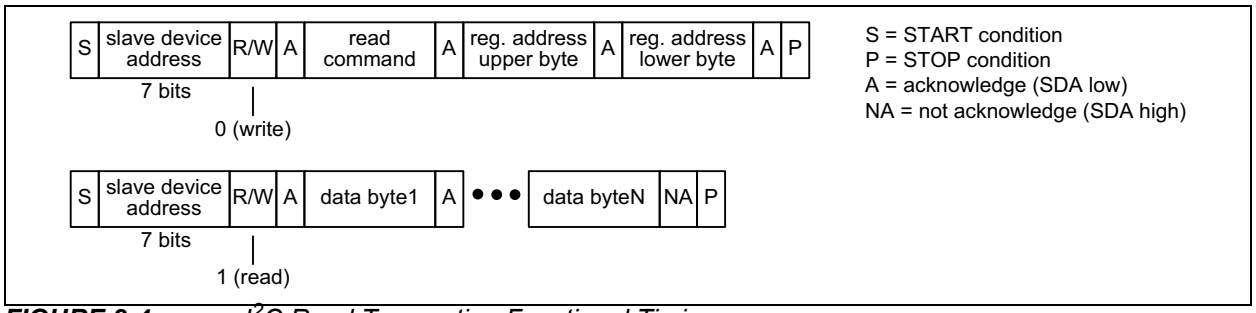


FIGURE 2-4: *I²C Read Transaction Functional Timing.*

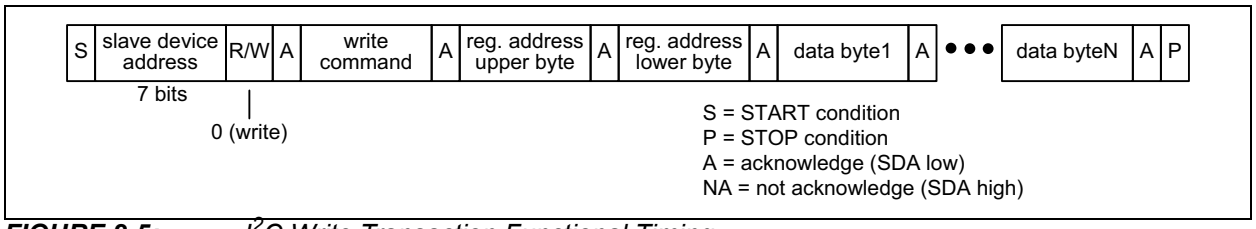


FIGURE 2-5: *I²C Write Transaction Functional Timing.*

Note: In Figure 2-4 and Figure 2-5, a STOP condition (P) immediately followed by a START condition (S) can be replaced by a repeated START condition (Sr) as described in the I2C specification.

2.5 Reset Logic

The device has three reset controls: the RSTN pin, and the hard reset (HRST) and soft reset (SRST) bits in MCR1. The RSTN pin asynchronously resets the entire device. When the RSTN pin is low all internal registers are reset to their default values. When RSTN returns high the device configures itself as specified by the AC[2:0] pins. *The RSTN pin must be asserted once after power-up.* Reset should be asserted for at least 1 µs. See Section 2.5.1 for important details about using an external RC reset circuit with the RSTN pin.

Asserting the MCR1.HRST (hard reset) bit is functionally similar to asserting the RSTN pin. The HRST bit resets the entire device except for the microprocessor interface, the HRST bit itself, and CFGSR.IF[1:0]. While HRST=1 the device accepts register writes so that HRST can be set back to 0, but register reads are not allowed. When HRST is set back to 0, the TEST and AC[2:0] pins are sampled as described in Section 2.1, but, unlike when RSTN is deasserted, the IF[1:0] pins are not sampled so that the device remains in the same interface mode (SPI or I²C) and maintains the same slave address when in I²C mode. When HRST is set back to 0, the device configures itself as specified by the AC[2:0] pins after a 1 µs to 3 µs delay.

The MCR1.SRST (soft reset) bit resets the entire device except for the microprocessor interface, the SRST bit itself, the MCR1.HRST bit, and the CFGSR register. When the SRST bit is asserted the device does not configure itself.

Important: System software must wait at least 100 µs after RSTN is deasserted and wait for GLOBISR.BCDONE=1 before configuring the device.

2.5.1 DESIGN CONSIDERATIONS FOR USING AN EXTERNAL RC RESET CIRCUIT

When the power supply arrangement for the device has VDDH = VDDL (3.3V or 2.5V), an external RC reset circuit can be used to reset the device during power-up with no additional considerations.

When the power supply arrangement for the device has VDDH > VDDL, then the board designer should choose one of two options: (a) a power-on-reset (POR) chip such as a Texas Instruments TPS3839 should be used instead of an external RC reset circuit, or (b) the device's VDDIO pin *must* be wired to VDDL.

The possible disadvantage of option (b) is that VDDIO, the power supply for all SPI/I^2C pins and the TEST/ALK pin, could be too low if neighboring devices operate at power supply voltages higher than VDDL. One exception to this disadvantage would be the I^2C interface. Because I^2C's logic-high voltage is set by pull-up resistors, those resistors can be externally wired to a voltage higher than VDDIO up to 3.3V. The SCL/SCLK and SDA/MOSI pins are 3.3V tolerant.

2.6 Power Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a lower-voltage supply and a higher-voltage supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latch-up. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the lower voltage supply and the higher voltage supply to force the higher voltage supply to be within one parasitic diode drop of the lower voltage supply. The second method is to ramp up the higher voltage supply first and then ramp up the lower voltage supply.

Important Note: The voltages on VDDL, VDDIO, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

2.7 Choosing Among Core Power Supply Options

The device supports the following core supply voltage options:

TABLE 2-5: SUPPORTED CORE SUPPLY VOLTAGES

VDDH	VDDL
3.3V	3.3V
3.3V	1.8V
2.5V	2.5V
2.5V	1.8V

Choosing the best option depends on several factors including supply voltages available on the board, willingness to use low-dropout (LDO) linear regulators to make local power supplies for the device, board power supply noise and mitigation strategies, target jitter performance, and how many device resources are enabled.

Starting with the VDDH = VDDL = 3.3V option, the advantages of this option are (1) the device only requires a single power supply voltage (assuming all output driver VDDOx supplies are also 3.3V), and (2) internal regulation is used for the APLL, maximizing power supply noise rejection. The disadvantage is that power consumption is higher than other options.

The VDDH = 3.3V, VDDL = 1.8V option does require two core power supply voltages, but internal regulation is used for the APLL, maximizing power supply noise rejection. Also this option has lower power consumption than the VDDH = VDDL = 3.3V option. If the application can provide 3.3V and 1.8V supplies to the device, this option is highly recommended as a good balance of lower power consumption and better power supply noise rejection.

The VDDH = VDDL = 2.5V option is for applications that do not have a 3.3V power supply and do not want to provide an LDO to make a 3.3V supply. The advantages of this option are (1) the device only requires a single power supply voltage (assuming all output driver VDDOx supplies are also 2.5V), and (2) lower power consumption than the VDDH = VDDL = 3.3V option. The disadvantage is that internal APLL regulators are bypassed and the APLL runs directly from the VDDH supply, which leaves the device more susceptible to power supply noise. This susceptibility can be mitigated using good power supply noise filtering and further mitigated with a dedicated LDO for the device.

The VDDH = 2.5V, VDDL = 1.8V option provides even lower power consumption than the VDDH = VDDL = 2.5V option. The disadvantages are (1) it requires two core power supply voltages, and (2) just like the VDDH = VDDL = 2.5V case, internal APLL regulators are bypassed and the APLL runs directly from the VDDH supply, which leaves the device more susceptible to power supply noise. This susceptibility can be mitigated using good power supply noise filtering and further mitigated with a dedicated LDO for the device.

NOTES:

3.0 REGISTER MAP

Table 3-1 shows the register map. In each register, bit 7 is the MSb and bit 0 is the LSb. Register addresses not listed are reserved. Bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode, resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 3-1.

3.1 Register Types

3.1.1 STATUS BITS

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. Status bits marked "—" are reserved and must be ignored.

3.1.2 CONFIGURATION FIELDS

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

3.2 Register Map

TABLE 3-1: REGISTER MAP

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Configuration Registers									
01	MCR1	SRST	HRST	STOP	—	—	—	ODMISO	—
02	MCR2	—	—	—	—	—	—	XAB[1:0]	
09	STOPCR1	OC5STP	—	OC4STP	—	OC3STP	OC2STP	—	OC1STP
0A	STOPCR2	—	—	—	—	—	—	—	OC6STP
11	ISCA	—	I2CA[6:0]						
Status Registers									
30	ID1	IDU[7:0]							
31	ID2	IDL[3:0]				REV[3:0]			
40	CFGSR	CFGD	—	IF[1:0]		TEST	AC[2:0]		
43	GLOBISR	BCDONE	—	—	—	—	—	—	—
48	APLL1SR	AIFLL	AIFL	AIFHL	AIFH	ALKL	ALK	—	—
50	OC1SR	—	—	—	—	STARTL	—	STOPL	STOPD
52	OC2SR	—	—	—	—	STARTL	—	STOPL	STOPD
53	OC3SR	—	—	—	—	STARTL	—	STOPL	STOPD
55	OC4SR	—	—	—	—	STARTL	—	STOPL	STOPD
57	OC5SR	—	—	—	—	STARTL	—	STOPL	STOPD
58	OC6SR	—	—	—	—	STARTL	—	STOPL	STOPD
Alignment Configuration Register									
100	ACR1	—	DALIGN	—	—	—	—	—	—
Output Clock Configuration Registers									
	OC1 Registers								
200	OC1OR1	PHEN	—	—	—	—	—	—	—
201	OC1CR2	—	POL	DRIVE[1:0]		—	—	—	—
209	OC1PH	—	—	—	—	PHADJ[3:0]			
20A	OC1STOP	—	SRC[3:0]				—	MODE[1:0]	

TABLE 3-1: REGISTER MAP (CONTINUED)

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OC2 Registers								
220	OC2CR1	Same as OC1 Registers							
...	...								
22A	OC2STOP								
	OC3 Registers								
230	OC3CR1	Same as OC1 Registers							
...	...								
23A	OC3STOP								
	OC4 Registers								
250	OC4CR1	Same as OC1 Registers							
...	...								
25A	OC4STOP								
	OC5 Registers								
270	OC5CR1	Same as OC1 Registers							
...	...								
27A	OC5STOP								
	OC6 Registers								
280	OC6CR1	Same as OC1 Registers							
...	...								
28A	OC6STOP								
Input Clock Configuration									
300	XACR1	—	POL	—	—	—	—	—	—
301	XACR2	XOAMP[7:0]							
302	XACR3	XBCAP[3:0]				XACAP[3:0]			

3.3 Register Definitions

3.3.1 GLOBAL CONFIGURATION REGISTERS

Register Name: MCR1

Register Description: Master Configuration Register 1

Register Address: 01h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SRST	HRST	STOP	—	—	—	ODMISO	—
Default	0	0	0	0	0	0	0	0

Bit 7: Soft Reset (SRST). This bit resets the entire device except for the microprocessor interface, the SRST bit itself, the MCR1.HRST bit, the I2CA register, and CFGSR bits 5:0. When SRST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. When the SRST bit is asserted the device's auto-configuration boot controller is not started. See Section 2.5.

0 = Normal operation

1 = Reset

Bit 6: Hard Reset (HRST). Asserting this bit is functionally equivalent to asserting the RSTN pin. The HRST bit resets the entire device except for the microprocessor interface and the HRST bit itself. Register fields with pin-programmed defaults latch their values from the corresponding input pins, and the device's auto-configuration boot controller is started. See Section 2.5.

0 = Normal operation

1 = Reset

Bit 5: Output Clock Stop (STOP). Asserting this bit stops all output clocks that are configured with OCx-STOP.SRC=0001. Note that this signal is ORed with the per-output stop control bit in the STOPCR registers to make each output's internal stop control signal. See Section 2.3.4.

Bit 1: Open Drain MISO Enable (ODMISO). This bit configures the MISO pin to be open-drain. When this bit is set, the MISO pin only drives low and must have an external pull-up resistor.

0 = Disable (MISO drives 0 and 1, high-impedance when not driven)

1 = Enable (MISO drives 0 only, high-impedance all other times)

Register Name: MCR2

Register Description: Master Configuration Register 2

Register Address: 02h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	XAB[1:0]	
Default	0	0	0	0	0	0	0	1

Bits 1 to 0: XA/XB Pin Mode (XAB[1:0]). This field specifies the behavior of the XA and XB pins. See Section 2.2.

00 = Crystal driver and input disabled/powered down
01 = Crystal driver and input enabled on XA/XB
10 = XA enabled as single-ended input for external oscillator signal; XB must be left floating
11 = {unused value}

Register Name: STOPCR1

Register Description: Output Clock Stop Control Register 1

Register Address: 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OC5STP	—	OC4STP	—	OC3STP	OC2STP	—	OC1STP
Default	0	0	0	0	0	0	0	0

Bit 7: OC5 Stop Control (OC5STP). When SRC=0001 in the OC5STOP register, setting this bit to 1 causes OC5 to stop. Note that this signal is ORed with MCR1.STOP to make OC5's internal stop control signal. See Section 2.3.4.

Bits 5, 3, 2, 0: These bits are similar to OC5STP above but for OC4 through OC1.

Register Name: STOPCR2

Register Description: Output Clock Stop Control Register 2

Register Address: 0Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	OC6STP
Default	0	0	0	0	0	0	0	0

Bit 0: This bit is similar to STOPCR1. OC5STP, but for OC6.

Register Name: I2CA

Register Description: I2C Address Register

Register Address: 11h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	I2CA[6:0]						
Default	0	1	1	1	0	1	1	1

Bits 6 to 0: I2C Address (I2CA[6:0]). This field specifies the device's address on the I2C bus.

3.3.2 STATUS REGISTERS

Register Name: ID1

Register Description: Device Identification Register, MSB

Register Address: 30h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IDU[7:0]							
Default	0	0	0	1	1	1	1	1

Bits 7 to 0: Device ID Upper (IDU[7:0]). This field is the upper eight bits of the device ID.

Register Name: ID2

Register Description: Device Identification Register, LSB and Revision

Register Address: 31h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IDL[3:0]				REV[3:0]			
Default	0	0	0	0	Contact factory.			

Bits 7 to 4: Device ID Lower (IDL[3:0]). This field is the lower four bits of the device ID.

Bits 3 to 0: Device Revision (REV[3:0]). These bits are the device hardware revision starting at 0.

Register Name: CFGSR

Register Description: Configuration Status Register

Register Address: 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CFGD	—	IF[1:0]		TEST	AC[2:0]		
Default	0	0	See below		See below	See below		

Bit 7: Configured (CFGD). This read-only bit is cleared by assertion of RSTN, MCR1.HRST or MCR1.SRST and set when any register is written (by auto-configuration or through the processor interface). CFGD=1 indicates that the device register set is no longer in factory-default state.

Bits 5 to 4: Interface Mode (IF[1:0]). These read-only bits are the latched state of the IF1/MISO and IF0/CSN pins when the RSTN pin transitions high. See Section 2.1.

Bit 3: Test Mode (TEST). This read-only bit is the latched state of the TEST pin when the RSTN pin transitions high or the MCR1.HRST bit is deasserted. For proper operation it should be 0. See Section 2.1.

Bits 2 to 0: Auto-Configuration (AC[2:0]). These bits are the latched state of the AC2, AC1 and AC0 pins when the RSTN pin transitions high or the MCR1.HRST bit is deasserted. See Section 2.1.

Register Name: GLOBISR

Register Description: Global Functions Interrupt Status Register

Register Address: 43h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	READY	—	—	—	—	—	—	—
Default	See below	0	0	0	0	0	0	0

Bit 7: Boot Controller Done (BCDONE). This bit indicates the status of the device after reset. It is cleared when the device is reset and set when the device is ready for operation.

Register Name: APPL1SR

Register Description: APLL1 Status Register

Register Address: 48h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	AIFLL	AIFL	AIFHL	AIFH	ALKL	ALK	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: APLL Input Frequency Low Latched Status (AIFLL). This latched status bit is set to 1 when the AIFL status bit is set. AIFLL is cleared when written with a 1. When AIFLL is set it can cause an interrupt request if the AIFLIE interrupt enable bit is set.

Bit 6: APLL Input Frequency Low Status (AIFL). This real-time status bit indicates that the input frequency to the APLL is lower that expected.

0 = Input frequency okay
1 = Input frequency low

Bit 5: APLL Input Frequency High Latched Status (AIFHL). This latched status bit is set to 1 when the AIFH status bit is set. AIFHL is cleared when written with a 1. When AIFHL is set it can cause an interrupt request if the AIFHIE interrupt enable bit is set.

Bit 4: APLL Input Frequency High Status (AIFH). This real-time status bit indicates that the input frequency to the APLL is higher that expected.

0 = Input frequency okay
1 = Input frequency high

Bit 3: APLL Lock Latched Status (ALKL). This latched status bit is set to 1 when the ALK status bit changes state (set or cleared). ALKL is cleared when written with a 1. When ALKL is set it can cause an interrupt request if the ALKIE interrupt enable bit is set.

Bit 2: APLL Lock Status (ALK). This real-time status bit indicates the lock status of the APLL.

0 = Not locked
1 = Locked

Register Name: OCxSR

Register Description: Output Clock x Status Register

Register Address: OC1: 50h, OC2: 52h, OC3: 53h, OC4: 55h, OC5: 57h, OC6: 58h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	STARTL	—	STOPL	STOPD
Default	0	0	0	0	0	0	0	0

Bit 3: (STARTL). This latched status bit is set when the output clock signal has been started after being stopped. Writing a 1 to this bit clears it. See Section 2.3.4.

0 = Output clock signal has not resumed from being stopped
1 = Output clock signal has resumed from being stopped

Bit 1: (STOPL). This latched status bit is set when the output clock signal has been stopped. Writing a 1 to this bit clears it. See Section 2.3.4.

0 = Output clock signal has not stopped
1 = Output clock signal has stopped

Bit 0: (STOPD). This real-time status bit is high when the output clock signal is stopped and low when the output clock is not stopped. See Section 2.3.4.

0 = Output clock signal is not stopped
1 = Output clock signal is stopped

3.3.3 ALIGNMENT CONFIGURATION REGISTER

Register Name: ACR1

Register Description: Align Configuration Register 1

Register Address: 100h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	DALIGN	—	—	—	—	—	—
Default	0	0	0	0	0	1	0	0

Bit 6: Align Output Dividers (DALIGN). A 0-to-1 transition on this bit causes a simultaneous reset of the medium-speed dividers and the low-speed dividers for all output clocks where OCxCR1.PHEN=1. After this reset all PHEN=1 output clocks with frequencies that are exactly integer multiples of one another will be rising-edge aligned as specified by their OCxPH registers. This bit should be set then cleared once during system startup. Setting this bit during normal system operation can cause phase jumps in the output clock signals.

3.3.4 OUTPUT CLOCK CONFIGURATION REGISTERS

Register Name: OCxCR1

Register Description: Output Clock x Configuration Register 1

Register Address: OC1: 200h, OC2: 220h, OC3: 230h, OC4: 250h, OC5: 270h, OC6: 280h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHEN	—	—	—	—	—	—	—
Default	1	Varies with Output Number and Config Number						

Bit 7: Phase Alignment Enable (PHEN). This bit enables this output to participate in phase alignment. See Section 2.3.3.

0 = Phase alignment disabled for this output
1 = Phase alignment enabled for this output

Register Name: OCxCR2

Register Description: Output Clock x Configuration Register 2

Register Address: OC1: 201h, OC2: 221h, OC3: 231h, OC4: 251h, OC5: 271h, OC6: 281h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	POL	DRIVE[1:0]		—	—	—	—
Default	0	0	See below		Varies with Output Number and Config Number			

Bit 6: Clock Path Polarity (POL). The clock path to the output driver is inverted when this bit set. This does not invert the LSDIV path to the CMOS OCxN pin if that path is enabled. See Section 2.3.1.

Bits 5 to 4: CMOS Output Drive Strength (DRIVE[1:0]). The CMOS output drivers have four equal sections that can be enabled or disabled to achieve four different drive strengths from 1x to 4x. When the output power supply VDDOx is 3.3V or 2.5V, the user should start with 1x and only increase drive strength if the output is highly loaded and signal transition time is unacceptable. When VDDOx is 1.8V or 1.5V the user should start with 4x and only decrease drive strength if the output signal has unacceptable overshoot. For output OC2 the default value of this field is 10=3x for all configs. For all other outputs this field is ignored. See Section 2.3.1.

00 = 1x
01 = 2x
10 = 3x
11 = 4x

Register Name: OCxPH

Register Description: Output Clock x Phase Adjust Register

Register Address: OC1: 209h, OC2: 229h, OC3: 239h, OC4: 259h, OC5: 279h, OC6: 289h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	PHADJ[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Phase Adjust Value (PHADJ[3:0]). This field can be used to adjust the phase of an output clock vs. the phase of other clock outputs. The adjustment is in units of DIV1 or DIV2 clock periods. For outputs from DIV1, the DIV1 frequency is 600 MHz and resolution is half of one period, i.e. 0.833 ns. For outputs from DIV2 (OC3-OC6 in Configs4-7), the DIV2 frequency is 200 MHz and resolution is half of one period, i.e. 2.5 ns. Negative values mean earlier in time (leading) and positive values mean later in time (lagging). See Section 2.3.2.

0000 = 0 DIVx periods
0001 = 0.5
0010 = 1.0
0011 = 1.5
0100 = 2.0
0101 = 2.5
0110 = 3.0
0111 = 3.5
1000 = –1.0 DIVx periods
1001 = –0.5
1010 = –2.0
1011 = –1.5
1100 = –3.0
1101 = –2.5
1110 = –4.0
1111 = –3.5

Register Name: OCxSTOP

Register Description: Output Clock x Start Stop Register

Register Address: OC1: 20Ah, OC2: 22Ah, OC3: 23Ah, OC4: 25Ah, OC5: 27Ah, OC6: 28Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	SRC[3:0]				—	MODE[1:0]	
Default	0	0	0	0	1	1	0	0

Bits 6 to 3: Output Clock Stop Source (SRC[3:0]). This field specifies the source of the stop signal. See Section 2.3.4.

0000 = Never stop
0001 = Logical OR of (the global MCR1.STOP bit) or (the OCx stop bit in the STOPCR registers)
0010 to 1111 = {unused values}

Bits 1 to 0: Output Clock Stop Mode (MODE[1:0]). This field selects the mode of the start-stop function. See Section 2.3.4.

00 = Stop Low: stop after falling edge of output clock, start after rising edge of output clock
01 = Stop High: stop after rising edge of output clock, start after falling edge of output clock
10 = Stop Low then go high-impedance: stop after falling edge, start after rising edge
11 = Stop High then go high-impedance: stop after rising edge, start after falling edge

3.3.5 INPUT CLOCK CONFIGURATION REGISTERS

Register Name: XACR1

Register Description: XA Input Clock Configuration Register 1

Register Address: 300h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	POL	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 6: Input Polarity (POL). This field specifies which input clock edge the APLL will lock to.

0 = Rising edge
1 = Falling edge

Register Name: XACR2

Register Description: XA Input Clock Configuration Register 2

Register Address: 301h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	XOAMP[7:0]							
Default	0	0	0	1	0	0	0	0

Bits 7 to 0: XO Amplifier Control (XOAMP[7:0]). For the recommended 10 pF crystal the default value of 0x10 is appropriate for crystal with 100 µW max drive. For 10 pF crystal with 200 µW max drive set this register to 0x58. For 10 pF crystal with 300 µW max drive set this register to 0x88.

Register Name: XACR3

Register Description: XA Input Clock Configuration Register 3

Register Address: 302h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	XBCAP[3:0]				XACAP[3:0]			
Default	0	1	1	1	0	1	1	1

Bits 7 to 4: XB Internal Capacitor Selection (XBCAP[3:0]). Actual internal capacitance on the XB pin in pF is approximately 6 + XBCAP. See Section 2.2.2.

Bits 3 to 0: XA Internal Capacitor Selection (XACAP[3:0]). Actual internal capacitance on the XA pin in pF is approximately 6 + XACAP. See Section 2.2.2.

NOTES:

4.0 ELECTRICAL CHARACTERISTICS

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Min.	Max.	Units
Supply voltage, nominal 1.5V	VDD15	–0.3	1.65	V
Supply voltage, nominal 1.8V	VDD18	–0.3	1.98	V
Supply voltage, nominal 2.5V	VDD25	–0.3	2.75	V
Supply voltage, nominal 3.3V	VDD33	–0.3	3.63	V
Voltage on XA, any OCxP/N pin	VANAPIN	–0.3	3.63	V
Voltage on any digital I/O pin	VDIGPIN	–0.3	3.63	V
Storage Temperature Range	T_{ST}	–55	+125	°C

Note 1: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Voltages are with respect to ground (VSS) unless otherwise stated.

2: The typical values listed in the tables of the Electrical Characteristics section are not production tested.

3: Specifications to –40°C and +85°C are guaranteed by design or characterization and not production tested.

TABLE 4-2: RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage, Higher Core (choose 1 row)	VDDH	2.375	2.5	2.625	V
		3.135	3.3	3.465	
Supply Voltage, Lower Core (choose 1 row)	VDDL	1.71	1.8	1.89	V
		Same as VDDH			
Supply Voltage, Non-Clock I/O Pins (choose 1 row)	VDDIO	1.71	1.8	1.89	V
		2.375	2.5	2.625	
		Same as VDDH			
Supply Voltage, OCx Outputs (x=1, 2, 3, 4, 5, or 6) (choose 1 row)	VDDOx	1.425	1.5	1.575	V
		1.71	1.8	1.89	
		2.375	2.5	2.625	
		Same as VDDH			
Operating Temperature	T_A	–40	—	+85	°C

TABLE 4-3: SUPPLY CURRENTS

Characteristics	Symbol	Min.	Typ. (Note 1)	Max.	Units	Notes
Total VDDH Current, All Configs 0-7	I_{DDH}	—	113	—	mA	Note 2
Config0 Total VDDL Current	I_{DDL}	—	191	—	mA	Note 2
Config1 Total VDDL Current	I_{DDL}	—	247	—	mA	Note 2
Config2 Total VDDL Current	I_{DDL}	—	247	—	mA	Note 2
Config3 Total VDDL Current	I_{DDL}	—	247	—	mA	Note 2
Config4 Total VDDL Current	I_{DDL}	—	229	—	mA	Note 2
Config5 Total VDDL Current	I_{DDL}	—	278	—	mA	Note 2
Config6 Total VDDL Current	I_{DDL}	—	278	—	mA	Note 2
Config7 Total VDDL Current	I_{DDL}	—	278	—	mA	Note 2
VDDOx Current for an HCSL Output	I_{DDOHC}	—	20	—	mA	Note 3
VDDOx Current for a CMOS Output	I_{DDOC}	—	4	—	mA	Note 4

Note 1: Typical values measured at nominal supply voltages and 25°C ambient temperature.

2: Typical I_{DD} measured with VDDH = VDDL = VDDOx = VDDIO = 3.3V.

3: 50Ω to ground on each OCxP and OCxN.

4: VDDOx = 3.3V, 1x drive strength, f_O = 250 MHz, 2 pF load.

TABLE 4-4: NON-CLOCK CMOS PINS

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input High Voltage	V_{IH}	0.7 x VDDIO	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.3 x VDDIO	V	—
Input Leakage Current, All Digital Inputs	I_{IL}	–10	—	10	µA	Note 1
Input Capacitance	C_{IN}	—	3	10	pF	—
Input Capacitance, SCL/SCLK, SDA/MOSI	C_{IN}	—	3	11	pF	—
Input Hysteresis, SCL and SDA in I^2C Bus Mode	—	0.05 x VDDIO	—	—	mV	—
Output Leakage (When High Impedance)	I_{LO}	–10	—	10	µA	Note 1
Output High Voltage	V_{OH}	0.8 x VDDIO	—	—	V	I_O = –3 mA
Output Low Voltage	V_{OL}	—	—	0.2 x VDDIO	V	I_O = 3 mA

Note 1: $0V < V_{IN} <$ VDDIO for all other non-clock inputs.

2: V_{OH} does not apply for SCL and SDA in I^2C interface mode because they are open-drain.

TABLE 4-5: XA CLOCK INPUT

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input High Voltage, XA	V_{IH}	1.2	—	VDDH	V	V_{DDH} = 2.5V or 3.3V
Input Low Voltage, XA	V_{IL}	—	—	0.8	V	V_{DDH} = 2.5V or 3.3V
Input Frequency, XA Pin	f_{IN}	50			MHz	—
Input Leakage Current	I_{IL}	–10	—	10	µA	—
Input Duty Cycle	—	40	—	60	%	—

Note: This table covers the case when there is no external crystal connected and an external oscillator or clock signal is connected to the XA pin.

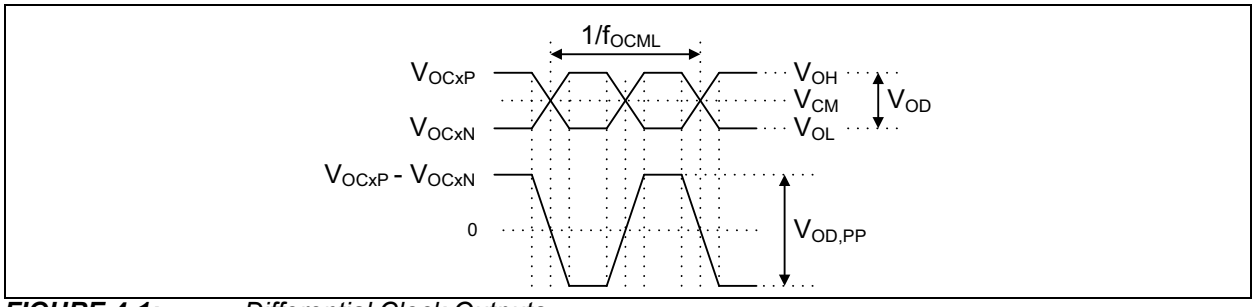


FIGURE 4-1: *Differential Clock Outputs.*

TABLE 4-6: HCSL CLOCK OUTPUTS

VDDOx = VDDH = 3.3V±5% or VDDOx = VDDH = 2.5V±5% for HCSL operation.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output Frequency	f_{OCHC}	—	250	250	MHz	—
Output Common Mode Voltage	V_{CM}		$V_{OD}/2$		V	Note 1, Figure 4-1
Output Differential Voltage	V_{OD}	0.6	0.75	0.95	V	Note 1, Figure 4-1
Output Rise/Fall Time	t_r/t_f	—	250	—	ps	20% - 80%
Output Duty Cycle	—	45	50	55	%	—

Note 1: Each of OCxP and OCxN with 50Ω termination resistor to ground.

TABLE 4-7: CMOS CLOCK OUTPUTS

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output Frequency	f_{OCMOS}		25, 75		MHz	—
Output High Voltage	V_{OH}	VDDOx – 0.4	—	VDDOx	V	Note 1
Output Low Voltage	V_{OL}	0	—	0.4	V	Note 1
Output Rise/Fall Time, VDDOx = 1.8V, OCxCR2.DRIVE = 4x	t_r/t_f	—	0.4	—	ns	2 pF load
Output Rise/Fall Time, VDDOx = 1.8V, OCxCR2.DRIVE = 4x		—	1.2	—	ns	15 pF load
Output Rise/Fall Time, VDDOx = 3.3V, OCxCR2.DRIVE = 1x		—	0.7	—	ns	2 pF load
Output Rise/Fall Time, VDDOx = 3.3V, OCxCR2.DRIVE = 1x		—	2.2	—	ns	15 pF load
Output Duty Cycle	—	45	50	55	%	Note 2
Output Duty Cycle, OCxNEG Single-Ended	—	—	50	—	%	—
Output Duty Cycle, OCxPOS Single-Ended	—	—	50	—	%	—
Output Current When Output Disabled	I_{OH}	—	300	—	µA	OCxCR2.OCSF = 0

Note 1: For VDDOx = 3.3V and OCxCR2.DRIVE = 1x, I_O = 4 mA. For VDDOx = 1.5V and OCxCR2.DRIVE = 4x, I_O = 8 mA.

2: VDDOx ≥ 1.8V.

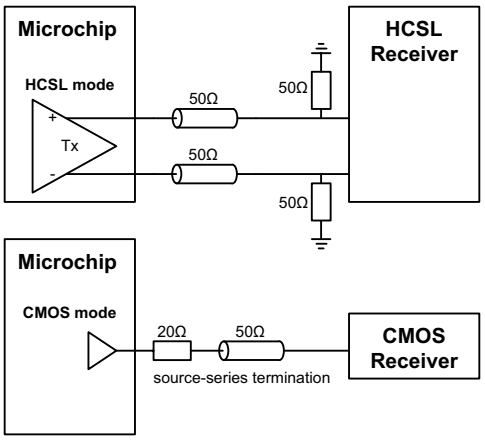


FIGURE 4-2: *Example External Components for Differential Output Signals.*

TABLE 4-8: JITTER AND SKEW SPECIFICATIONS

Characteristics	Test Conditions	Min	Typ.	Max.	Units
Output-to-Output Skew	Note 1	—	—	100	ps
OC2 25 MHz Jitter, Config0	Note 4	—	0.315	—	ps_{RMS}
OC2 75 MHz Jitter, Config2	Note 4	—	0.367	—	ps_{RMS}
PCI Express 1.1, Common Refclk Jitter	Total jitter, Note 2, Note 3	—	7.65	—	ps_{PP}
PCI Express 2.1, Common Refclk Jitter	10 kHz to 1.5 MHz, Note 2	—	0.060	—	ps_{RMS}
	1.5 MHz to 50 MHz, Note 2	—	0.780	—	ps_{RMS}
PCI Express 3.0, Common Refclk Jitter	Note 2	—	0.280	—	ps_{RMS}
PCI Express 4.0, Common Refclk Jitter	Note 2	—	0.280	—	ps_{RMS}
PCI Express 5.0, Common Refclk Jitter	Note 2	—	0.050	—	ps_{RMS}

Note 1: Requires phase alignment capability described in Section 2.3.3. Only applies for outputs that have the same signal format, VDDO voltage. drive strength, and loading/termination.

2: Jitter is from the PCIe jitter filter combination that produces the highest jitter. Applies for non-spread-spectrum signals.

3: N = 10000

4: 25 MHz measured 12 kHz to 5 MHz. 75 MHz measured 12 kHz to 20 MHz.

TABLE 4-9: TYPICAL INPUT-TO-OUTPUT CLOCK DELAY

Mode	Delay, Input Clock Edge to Output Clock Edge
All Modes	Non-deterministic but constant as long as the APLL remains locked and output clock phases are not adjusted as described in Section 2.3.2.

TABLE 4-10: SPI SLAVE INTERFACE TIMING

VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%

Characteristics (Note 1, Note 2, Note 3)	Symbol	VDDIO 3.3V or 2.5V		VDDIO 1.8V		Units
		Min.	Max.	Min.	Max.	
SCLK Frequency	f_{BUS}	—	23	—	15	MHz
SCLK Cycle Time	t_{CYC}	43.5	—	66	—	ns
CSN Setup to First SCLK Edge	t_{SUC}	10	—	10	—	ns
CSN Hold Time after Last SCLK Edge	t_{HDC}	10	—	10	—	ns
CSN High Time	t_{CSH}	25	—	25	—	ns
SCLK High Time	t_{CLKH}	10	—	33	—	ns
SCLK Low Time	t_{CLKL}	21.75	—	33	—	ns
MOSI Data Setup Time	t_{SUI}	2	—	10	—	ns
MOSI Data Hold Time	t_{HDI}	2	—	10	—	ns
MISO Enable Time from SCLK Edge	t_{EN}	0	—	0	—	ns
MISO Disable Time from CSN High	t_{DIS}	—	80	—	80	ns
MISO Data Valid Time	t_{DV}	—	20.5	—	32	ns
MISO Data Hold Time from SCLK Edge	t_{HDO}	0	—	0	—	ns
CSN, MOSI Input Rise Time, Fall Time	t_r/t_f	—	10	—	10	ns

Note 1: All timing is specified with 100 pF load on all SPI pins.

2: All parameters in this table are guaranteed by design or characterization.

3: See timing diagram in Figure 4-3.

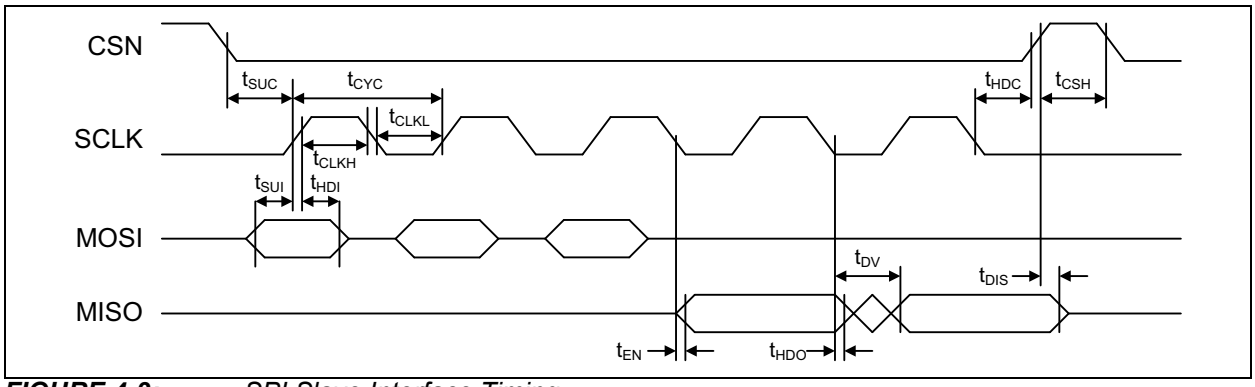


FIGURE 4-3: *SPI Slave Interface Timing.*

TABLE 4-11: I²C SLAVE INTERFACE TIMING

VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
SCL Clock Frequency	f_{SCL}	—	—	400	kHz	Note 1
Hold Time, START Condition	$t_{HD:STA}$	0.6	—	—	µs	—
Low Time, SCL	t_{LOW}	1.3	—	—	µs	—
High Time, SCL	t_{HIGH}	0.6	—	—	µs	—
Setup Time, START Condition	$t_{SU:STA}$	0.6	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	0	—	0.9	µs	Note 2, Note 3
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	—
Rise Time	t_r	—	—	—	ns	Note 4
Fall Time	t_f	$20 + 0.1C_b$	—	300	ns	C_b is cap. of one bus line
Setup Time, STOP Condition	$t_{SU:STO}$	0.6	—	—	µs	—
Bus Free Time between STOP/START	t_{BUF}	1.3	—	—	µs	—
Pulse Width of Spikes that Must be Suppressed by the Input Filter	t_{SP}	0	—	50	ns	—

Note 1: The timing parameters in this table are specifically for 400 kbps Fast Mode. Fast Mode devices are downward-compatible with 100 kbps Standard Mode I²C bus timing. All parameters in this table are guaranteed by design or characterization. All values referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels (see Table 7).

2: The device internally provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.

3: The I²C specification indicates that the maximum $t_{HD:DAT}$ spec only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. The device does not stretch the low period of the SCL signal.

4: Determined by choice of pull-up resistor.

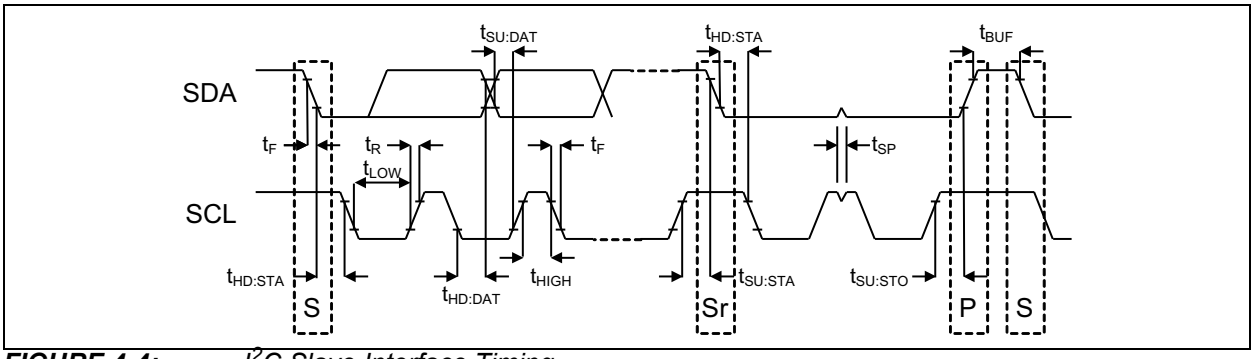


FIGURE 4-4: *I²C Slave Interface Timing.*

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Ambient Temperature	$T_{A(MAX)}$	—	—	+85	°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	—
Package Thermal Resistance, 8x8 QFN-56Ld						
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	—	15.1	—	°C/W	Still-air
		—	12.4	—	°C/W	1 m/s airflow
		—	10.6	—	°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance	θ_{JB}	—	3.2	—	°C/W	—
Junction to Case Thermal Resistance	θ_{JC}	—	7.3	—	°C/W	—
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	—	0.9	—	°C/W	Still-air
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	—	0.1	—	°C/W	Still-air

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 8-layer JEDEC standard test board and dissipating maximum power.

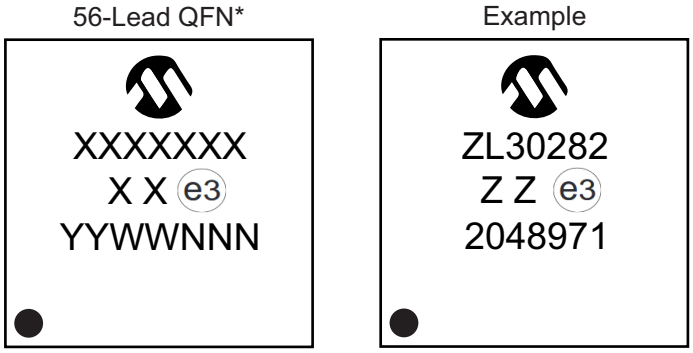
2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

3: For all numbers in the table, the exposed pad is connected to the ground plane with a 9x9 array of thermal vias; via diameter 0.33 mm; via pitch 0.76 mm.

NOTES:

5.0 PACKAGE OUTLINE

5.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

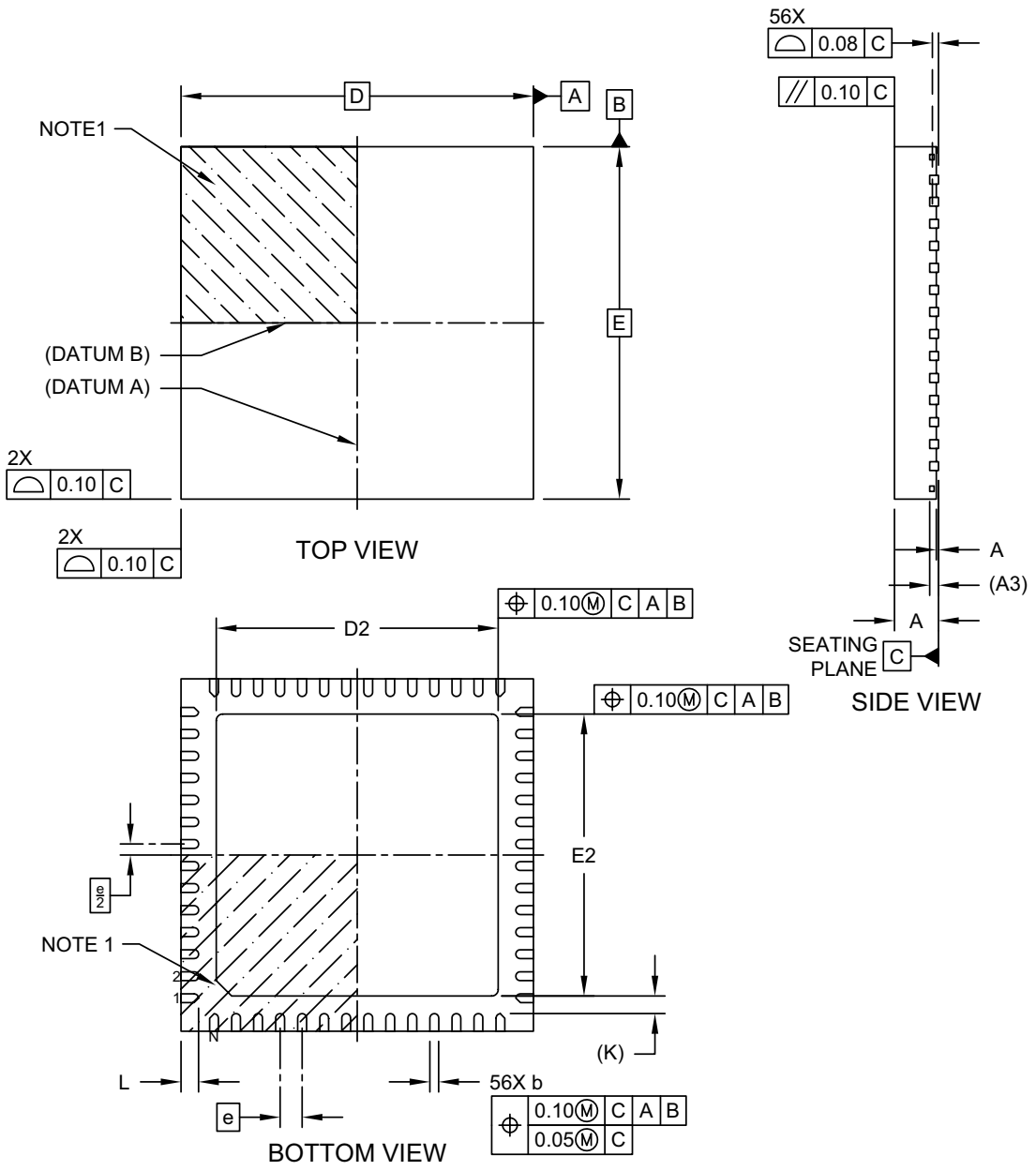
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

56-Lead 8 mm x 8 mm VQFN Package Outline and Recommended Land Pattern

56-Lead Very Thin Plastic Quad Flat, No Lead Package (MEC) - 8x8x1 mm Body [VQFN] With 6.5 mm Exposed Pad; Microsemi Legacy Package

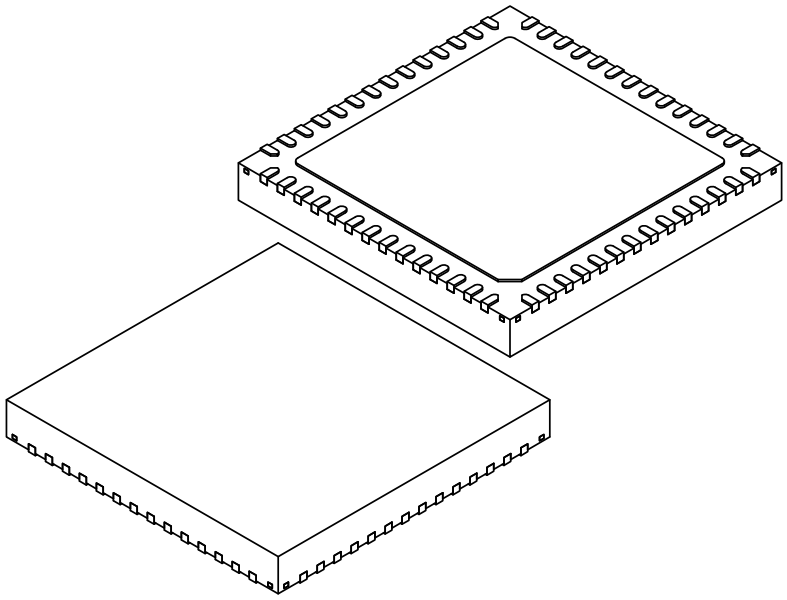
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25411 Rev A Sheet 1 of 2

56-Lead Very Thin Plastic Quad Flat, No Lead Package (MEC) - 8x8x1 mm Body [VQFN] With 6.5 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		56	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.40	6.50
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.40	6.50
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.40 REF	

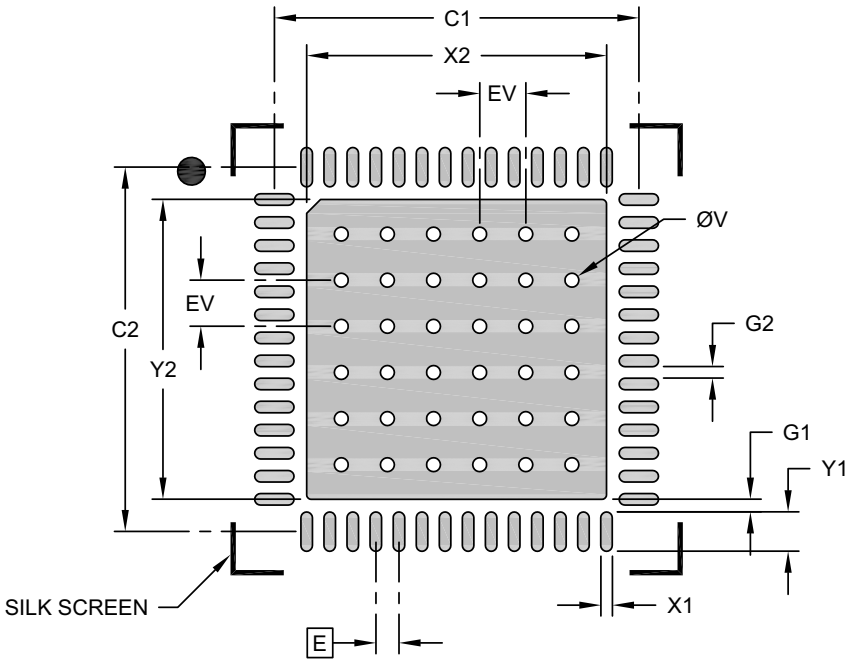
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25411 Rev A Sheet 2 of 2

56-Lead Very Thin Plastic Quad Flat, No Lead Package (MEC) - 8x8x1 mm Body [VQFN] With 6.5 mm Exposed Pad; Microsemi Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			6.50
Optional Center Pad Length	Y2			6.50
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (Xnn)	X1			0.25
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.28		
Contact Pad to Contact Pad (Xnn)	G2	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27411 Rev A

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006397A (08-11-20)	—	Converted Microsemi data sheet ZL30282 to Microchip DS20006397A. Minor text changes throughout.
DS20006397B (11-23-20)	Table 4-6	Updated values for Output Common Mode Voltage and Output Differential Voltage.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL30282: 6-Output PCIe Clock Generator
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 56-Lead 8 mm x 8 mm VQFN
Media Type:	G = 260/Tray F = 2,700/Reel
Finish:	1 = Pb-Free Matte (Sn) Tin

Examples:

a) ZL30282LDG1:

6-Output PCIe Clock Generator, Leadless Chip Carrier, 56-Lead VQFN, 260/Tray, Pb-Free Matte (Sn) Tin

b) ZL30282LDF1:

6-Output PCIe Clock Generator, Leadless Chip Carrier, 56-Lead VQFN, 2,700/Reel, Pb-Free Matte (Sn) Tin

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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