ZL38001

Low-Voltage Acoustic Echo Canceller with Low ERL Compensation

Data Sheet

June 2004

Features

- Contains two echo cancellers: 112 ms acoustic echo canceller
- Works with low cost voice codec. ITU-T G.711 or signed mag μ/A-Law, or linear 2's comp
- Each port may operate in different format
- Advanced NLP design - full duplex speech with no switched loss on audio paths
- Fast re-convergence time: tracks changing echo environment quickly
- Adaptation algorithm converges even during Double-Talk
- Designed for exceptional performance in high background noise environments
- Provides protection against narrow-band signal divergence
- Howling prevention stops uncontrolled oscillation in high loop gain conditions
- Offset nulling of all PCM channels
- Serial micro-controller interface

Ordering Information

ZL38001DGA 36 Pin QSOP
ZL38001QDC 48 Pin TQFP

-40°C to +85°C

- ST-BUS, GCI, or variable-rate SSI PCM interfaces
- User gain control provided for speaker path (-24 dB to +48 dB in 3 dB steps)
- 18 dB gain at Sout to compensate for high ERL environments
- AGC on speaker path
- Handles up to 0 dB acoustic echo return loss
- Transparent data transfer and mute options
- 20 MHz master clock operation
- Low power mode during PCM Bypass
- Bootloadable for future factory software upgrades
- 2.7 V to 3.6 V supply voltage; 5 V-tolerant inputs

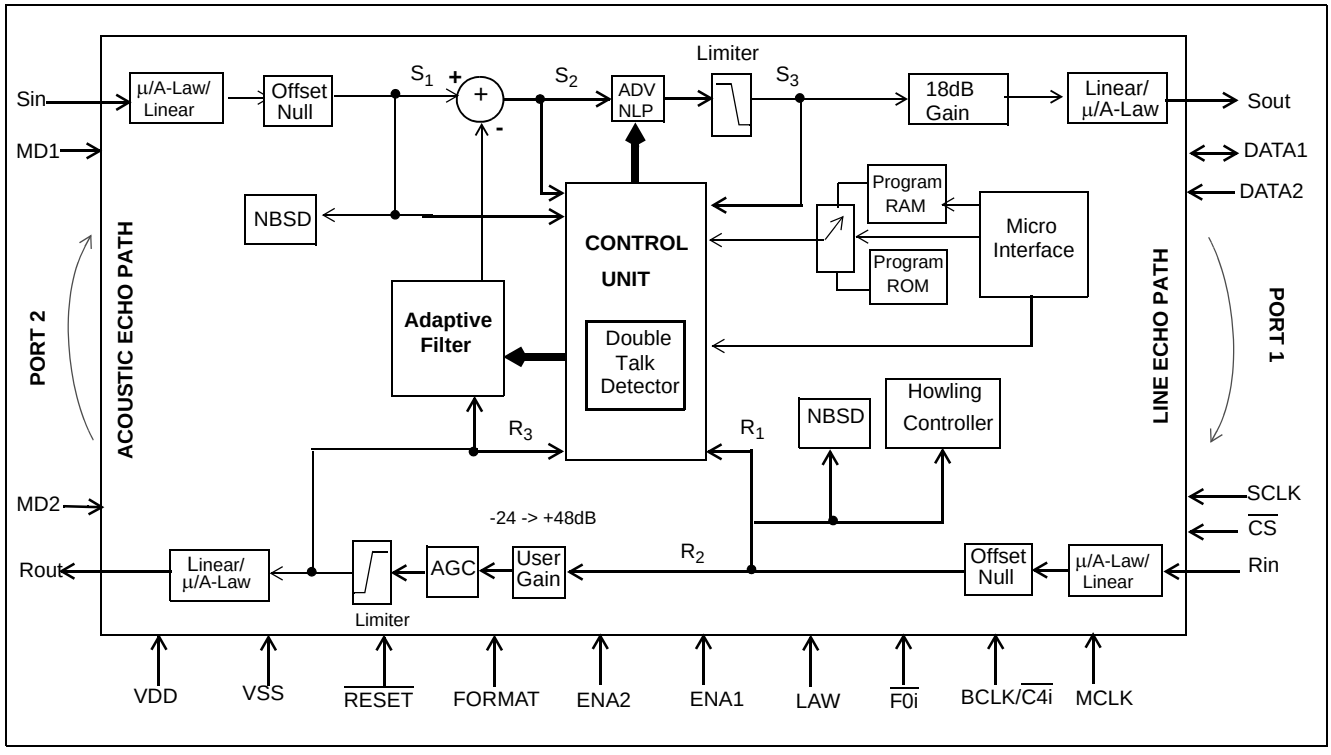


Figure 1 - Functional Block Diagram

Applications

- Handsfree in automobile applications

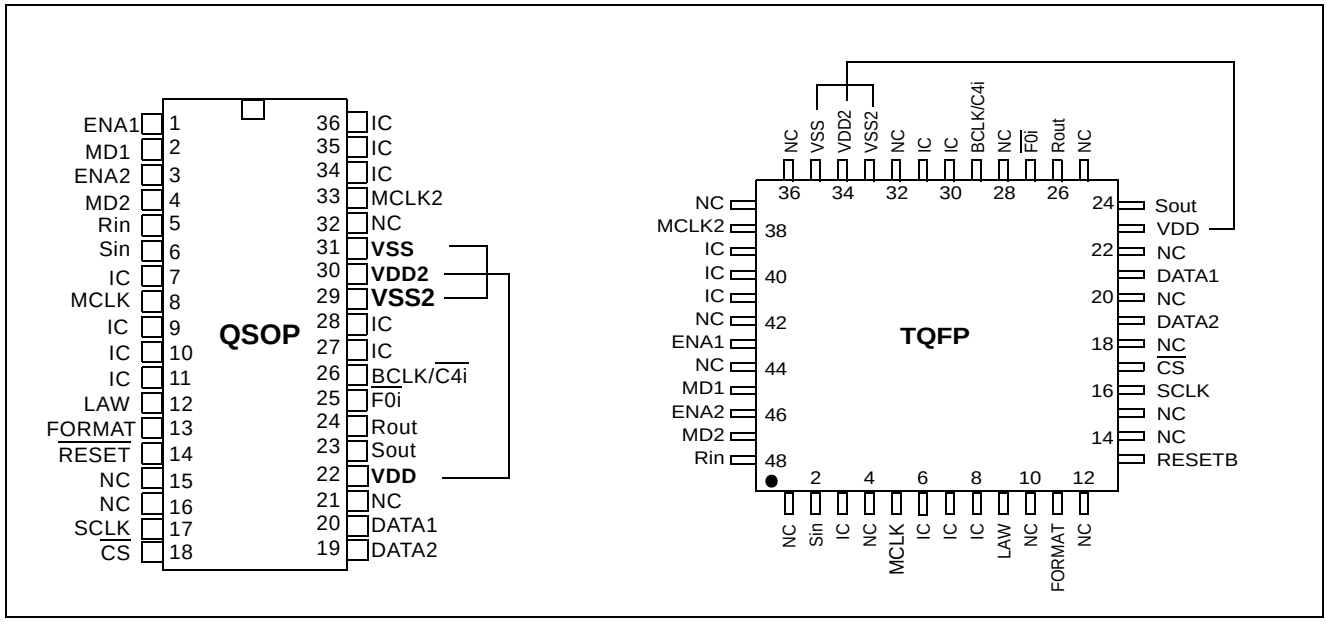


Figure 2 - Pin Connections

Pin Description

QSOP Pin #	TQFP Pin #	Name	Description
1	43	ENA1	**SSI Enable Strobe/ST-BUS & GCI Mode for Rin/Sout (Input).** This pin has dual functions depending on whether SSI or ST-BUS/GCI is selected. For SSI, this strobe must be present for frame synchronization. This is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer for on Rin/Sout pins. Strobe period is 125 microseconds. For ST-BUS or GCI, this pin, in conjunction with the MD1 pin, selects the proper mode for Rin/Sout pins (see ST-BUS and GCI Operation description).
2	45	MD1	**ST-BUS & GCI Mode for Rin/Sout (Input).** When in ST-BUS or GCI operation, this pin, in conjunction with the ENA1 pin, will select the proper mode for Rin/Sout pins (see ST-BUS and GCI Operation description). Connect this pin to Vss in SSI mode.
3	46	ENA2	**SSI Enable Strobe /ST-BUS & GCI Mode for Sin/Rout (Input).** This pin has dual functions depending on whether SSI or ST-BUS/GCI is selected. For SSI, this is an active high channel enable strobe, 8 or 16 data bits wide, enabling serial PCM data transfer on Sin/Rout pins. Strobe period is 125 microseconds. For ST-BUS/GCI, this pin, in conjunction with the MD2 pin, selects the proper mode for Sin/Rout pins (see ST-BUS and GCI Operation description).
4	47	MD2	**ST-BUS & GCI Mode for Sin/Rout (Input).** When in ST-BUS or GCI operation, this pin in conjunction with the ENA2 pin, selects the proper mode for Sin/Rout pins (see ST-BUS and GCI Operation description). Connect this pin to Vss in SSI mode.
5	48	Rin	**Receive PCM Signal Input (Input).** 128 kbps to 4096 kbps serial PCM input stream. Data may be in either companded or 2's complement linear format. This is the Receive Input channel from the line (or network) side. Data bits are clocked in following SSI, GCI or ST-BUS timing requirements.
6	2	Sin	**Send PCM Signal Input (Input).** 128 kbps to 4096 kbps serial PCM input stream. Data may be in either companded or 2's complement linear format. This is the Send Input channel (from the microphone). Data bits are clocked in following SSI, GCI or ST-BUS timing requirements.
7	3	IC	**Internal Connection (Input).** Must be tied to Vss.
8	5	MCLK	**Master Clock (Input).** Nominal 20 MHz Master Clock input (may be asynchronous relative to 8 KHz frame signal.) Tie together with MCLK2 (pin 33).
9,10,11	6, 7, 8	IC	**Internal Connection (Input).** Must be tied to Vss.
12	9	LAW	**A/$\overline{\mu}$ Law Select (Input).** When low, selects μ–Law companded PCM. When high, selects A-Law companded PCM. This control is for both serial pcm ports.
13	11	FORMAT	**ITU-T/$\overline{\text{Sign Mag}}$ (Input).** When low, selects sign-magnitude PCM code. When high, selects ITU-T (G.711) PCM code. This control is for both serial pcm ports.
14	13	$\overline{\text{RESET}}$	**Reset / Power-down (Input).** An active low resets the device and puts the ZL38001 into a low-power stand-by mode.

Pin Description (continued)

QSOP Pin #	TQFP Pin #	Name	Description
17	16	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for the serial microport interface.
18	17	$\overline{CS}$	**Serial Port Chip Select (Input).** Enables serial microport interface data transfers. Active low.
19	19	DATA2	**Serial Data Receive (Input).** In Motorola/National serial microport operation, the DATA2 pin is used for receiving data. In Intel serial microport operation, the DATA2 pin is not used and must be tied to Vss or Vdd.
20	21	DATA1	**Serial Data Port (Bidirectional).** In Motorola/National serial microport operation, the DATA1 pin is used for transmitting data. In Intel serial microport operation, the DATA1 pin is used for transmitting and receiving data.
22	23	VDD	**Positive Power Supply (Input**). Nominally 3.3 volts.
23	24	Sout	**Send PCM Signal Output (Output).** 128 kbps to 4096 kbps serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. This is the Send Out signal after acoustic echo cancellation and non-linear processing. Data bits are clocked out following SSI, ST-BUS or GCI timing requirements.
24	26	Rout	**Receive PCM Signal Output (Output).** 128 kbps to 4096 kbps serial PCM output stream. Data may be in either companded or 2's complement linear PCM format. This is the Receive out signal after line echo cancellation non-linear processing, AGC and gain control. Data bits are clocked out following SSI, ST-BUS or GCI timing requirements.
25	27	$\overline{F0i}$	**Frame Pulse (Input).** In ST-BUS (or GCI) operation, this is an active-low (or active-high) frame alignment pulse, respectively. SSI operation is enabled by connecting this pin to Vss.
26	29	BCLK/$\overline{C4i}$	**Bit Clock/ST-BUS Clock (Input).** In SSI operation, BCLK pin is a 128 kHz to 4.096 MHz bit clock. This clock must be synchronous with ENA1 and ENA2 enable strobes. In ST-BUS or GCI operation, $\overline{C4i}$ pin must be connected to the 4.096 MHz ($\overline{C4}$) system clock.
27, 28	30, 31	IC	**Internal Connection (Input).** Tie to Vss.
29	33	VSS2	**Digital Ground (Input).** Nominally 0 volts.
30	34	VDD2	**Positive Power Supply (Input).** Nominally 3.3 volts (tie together with VDD, pin 22).
31	35	VSS	**Digital Ground (Input).** Nominally 0 volts (tie together with VSS2, pin 29).
33	38	MCLK2	**Master Clock (Input).** Nominal 20 MHz master clock (tie together with MCLK, pin 8).
34,35,36	39, 40, 41	IC	**Internal Connection (Input).** Tie to Vss.
15, 16, 21, 32	1, 4, 10, 12, 14, 15, 18, 20, 22, 25, 28, 32, 36, 37, 42, 44	NC	**No Connect (Output).** This pin should be left unconnected.

Table of Contents

List of Figures

List of Tables

List of Register Tables

1.0 Functional Description

The ZL38001 device contains an acoustic echo cancellers, as well as the many control functions necessary to operate the echo canceller. The ZL38001 provides clear signal transmission in both audio path directions to ensure reliable voice communication, even with low level signals. The ZL38001 does not use variable attenuators during double-talk or single-talk periods of speech, as do many other acoustic echo cancellers for speakerphones. Instead, the ZL38001 provides high performance full-duplex operation similar to network echo cancellers, so that users experience clear speech and uninterrupted background signals during the conversation. This prevents subjective sound quality problems associated with “noise gating” or “noise contrasting”.

The ZL38001 uses an advanced adaptive filter algorithm that is double-talk stable, which means that convergence takes place even while both parties are talking[1]. This algorithm allows continual tracking of changes in the echo path, regardless of double-talk, as long as a reference signal is available for the echo canceller.

The echo tail cancellation capability of the acoustic echo canceller has been sized appropriately (112 ms) to cancel echo in an average sized office with a reverberation time of less than 112 ms.

In addition to the echo cancellers, the following functions are supported:

- Control of adaptive filter convergence speed during periods of double-talk, far end single-talk and near-end echo path changes
- Control of Non-Linear Processor thresholds for suppression of residual non-linear echo
- Howling detector to identify when instability is starting to occur and to take action to prevent oscillation
- Narrow-Band Detector for preventing adaptive filter divergence caused by narrow-band signals
- Offset Nulling filters for removal of DC components in PCM channels
- Limiters that introduce controlled saturation levels
- Serial controller interface compatible with Motorola, National and Intel microcontrollers
- PCM encoder/decoder compatible with μ/A-Law ITU-T G.711, μ/A-Law Sign-Mag or linear 2’s complement coding
- Automatic gain control on the receive speaker path

1.1 Adaptation Speed Control

The adaptation speed of the acoustic echo canceller is designed to optimize the convergence speed versus divergence caused by interfering near-end signals. Adaptation speed algorithm takes into account many different factors such as relative double-talk condition, far end signal power, echo path change and noise levels to achieve fast convergence.

1.2 Advanced Non-Linear Processor (ADV-NLP)[1]

After echo cancellation, there is likely to be residual echo which needs to be removed so that it will not be audible. The ZL38001 uses an NLP to remove low level residual echo signals which are not comprised of background noise. The operation of the NLP depends upon a dynamic activation threshold, as well as a double-talk detector which disables the NLP during double-talk periods.

The ZL38001 keeps the perceived noise level constant, without the need for any variable attenuators or gain switching that causes audible “noise gating”. The noise level is constant and identical to the original background noise even when the NLP is activated.

The NLP can be disabled by setting the NLP- bit to 1 in the AEC control registers.

1. Patent pending.

1.3 Narrow Band Signal Detector (NBSD)[1]

Single or multi-frequency tones (e.g,. DTMF, or signalling tones) present in the reference input of an echo canceller for a prolonged period of time may cause the adaptive filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this divergence by detecting single or multi-tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, the filter adaptation process is stopped but the echo canceller continues to cancel echo.

The NBSD can be disabled by setting the NB- bit to 1 in the MC control registers.

1.4 Howling Detector (HWLD)[1]

The Howling detector is part of an Anti-Howling control, designed to prevent oscillation as a result of positive feedback in the audio paths.

The HWLD can be disabled by setting the AH- bit to 1 in the (MC) control register.

1.5 Offset Null Filter

To ensure robust performance of the adaptive filters at all times, any DC offset that may be present on either the Rin signal or the Sin signal, is removed by highpass filters. These filters have a corner frequency placed at 40 Hz.

The offset null filters can be disabled by setting the HPF- bit to 1 in the AEC control registers.

1.6 Limiters

To prevent clipping in the echo paths, two limiters with variable thresholds are provided at the outputs.

The Rout limiter threshold is in Rout Limiter Register 1 and 2. The Sout limiter threshold is in Sout Limiter Register. Both output limiters are always enabled.

1.7 User Gain

The user gain function provides the ability for users to adjust the audio gain in the receive path (speaker path). This gain is adjustable from -24 dB to +48 dB in 3 dB steps. It is important to use ONLY this user gain function to adjust the speaker volume. The user gain function in the ZL38001 is optimally placed between the two echo cancellers such that no reconvergence is necessary after gain changes.

The gain can be accessed through Receive Gain Control Register.

1. Patent Pending

1.8 AGC

The AGC function is provided to limit the volume in the speaker path. The gain of the speaker path is automatically reduced during the following conditions:

- When clipping of the receive signal occurs
- When initial convergence of the acoustic echo canceller detects unusually large echo return
- When howling is detected
- The AGC can be disabled by setting the AGC- bit to 1 in MC control register

1.9 18 dB Gain Pad at Sout

The purpose of the 18 dB gain pad is to improve the subjective quality in low ERL environments. The ZL38001 can cancel echo with a ERL as low as 0 dB (attenuation from Rout to Sin). In many hand free applications, the ERL can be low (or negative). This is due to both speaker and microphone gain setting. The speaker gain has to be set high enough for the speaker to be heard properly and the microphone gain needs to be set high enough to ensure sufficient signal is sent to the far end. If the ERL (Acoustic Attenuation - speaker gain - microphone gain) is greater than 0 dB, then the echo canceller cannot cancel echo. To overcome this limitation, the ZL38001 has a 18 dB gain pad at Sout. The microphone gain can be reduced by 18 dB to allow either the speaker gain and/or the acoustic coupling to be increased by a total of 18 dB allowing more flexibility in the design.

1.10 Mute Function

A pcm mute function is provided for independent control of the Receive and Send audio paths. Setting the MUTE_R or MUTE_S bit in the MC register, causes quiet code to be transmitted on the Rout or Sout paths respectively.

Quiet code is defined according to the following table.

	LINEAR 16 bits 2's complement	SIGN/ MAGNITUDE μ-Law A-Law	CCITT (G.711)	
			μ-Law	A-Law
+Zero (quiet code)	0000h	80h	FFh	D5h

Table 1 - Quiet PCM Code Assignment

1.11 Bypass Control

A PCM bypass function is provided to allow transparent transmission of pcm data through the ZL38001. When the bypass function is active, pcm data passes transparently from Rin to Rout and from Sin to Sout, with bit-wise integrity preserved.

When the Bypass function is selected, most internal functions are powered down to provide low power consumption.

The BYPASS control bit is located in the main control MC register.

1.12 Adaptation Enable/Disable

Adaptation control bits are located in the AEC and LEC control registers. When the ADAPT- bit is set to 1, the adaptive filter is frozen at the current state. In this state, the device continues to cancel echo with the current echo model.

When the ADAPT- bit is set to 0, the adaptive filter is continually updated. This allows the echo canceller to adapt and track changes in the echo path. This is the normal operating state.

1.13 ZL38001 Throughput Delay

In all modes, voice channels always have 2 frames of delay. In ST-BUS/GCI operation, the D and C channels have a delay of one frame.

1.14 Power Down / Reset

Holding the $\overline{\text{RESET}}$ pin at logic low will keep the ZL38001 device in a power-down state. In this state all internal clocks are halted, and the DATA1, Sout and Rout pins are tristated.

The user should hold the $\overline{\text{RESET}}$ pin low for at least 200 msec following power-up. This will insure that the device powers up in a proper state. Following any return of $\overline{\text{RESET}}$ to logic high, the user must wait for 8 complete 8 KHz frames prior to writing to the device registers. During this time, the initialization routines will execute and set the ZL38001 to default operation (program execution from ROM using default register values).

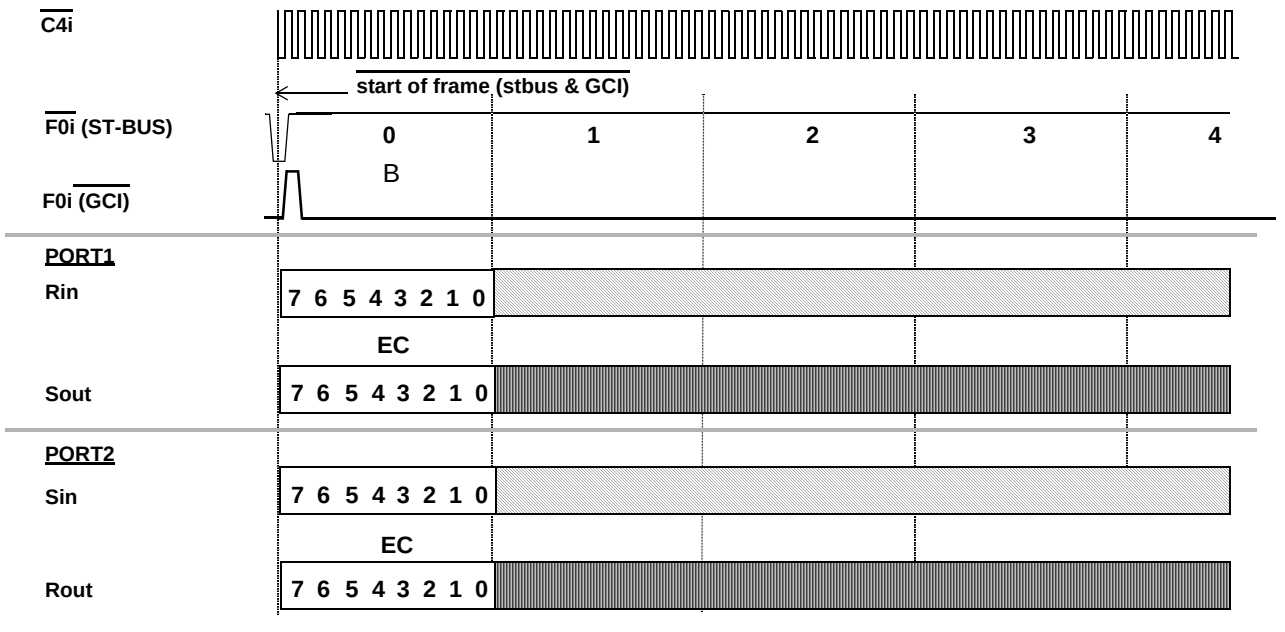
2.0 PCM Data I/O

The PCM data transfer for the ZL38001 is provided through two PCM ports. One port consists of Rin and Sout pins while the second port consists of Sin and Rout pins. The data are transferred through these ports according to either ST-BUS, GCI or SSI conventions and the device automatically detects the correct convention. The device determines the convention by monitoring the signal applied to the F0i pin. When a valid ST-BUS (active low) frame pulse is applied to the F0i pin, the ZL38001 will assume ST-BUS operation. When a valid GCI (active high) frame pulse is applied to the F0i pin, the device will assume GCI operation. If F0i is tied continuously to Vss, the device will assume SSI operation. Figures 11 to 13 show timing diagrams of these 3 PCM-interface operation conventions.

2.1 ST-BUS and GCI Operation

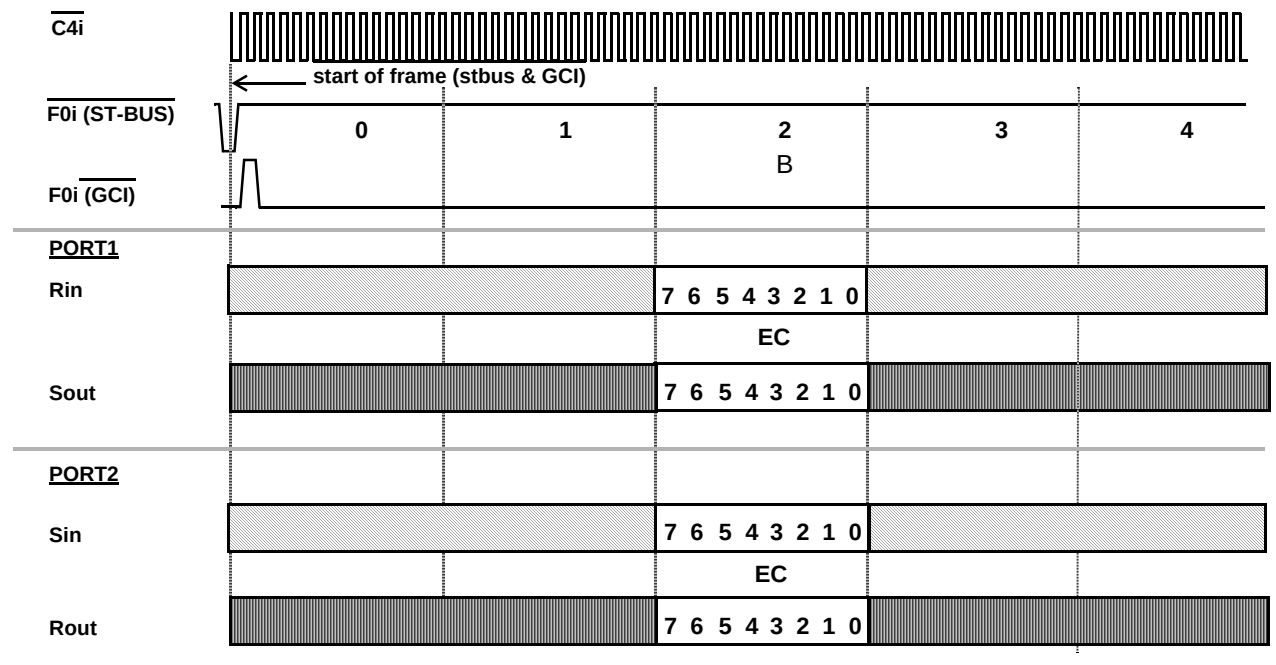
The ST-BUS PCM interface conforms to Zarlink's ST-BUS standard with an active-low frame pulse. Input data is clocked in by the rising edge of the bit clock (C4i) three-quarters of the way into the bitcell and output data bit boundaries (Rout, Sout) occur every second falling edge of the bit clock (see Figure 11.) The GCI PCM interface corresponds to the GCI standard commonly used in Europe with an active-high frame pulse. Input data is clocked in by the falling edge of the bit clock (C4i) three-quarters of the way into the bitcell and output data bit boundaries (Rout, Sout) occur every second rising edge of the bit clock (see Figure 12.)

Either of these interfaces (STBUS or GCI) can be used to transport 8 bit companded PCM data (using one timeslot) or 16 bit 2's complement linear PCM data (using two timeslots). The MD1/ENA1 pins select the timeslot on the Rin/Sout port while the MD2/ENA2 pin selects the timeslot on the Sin/Rout port, as in Table 2. Figures 3 to 6 illustrate the timeslot allocation for each of these four modes.



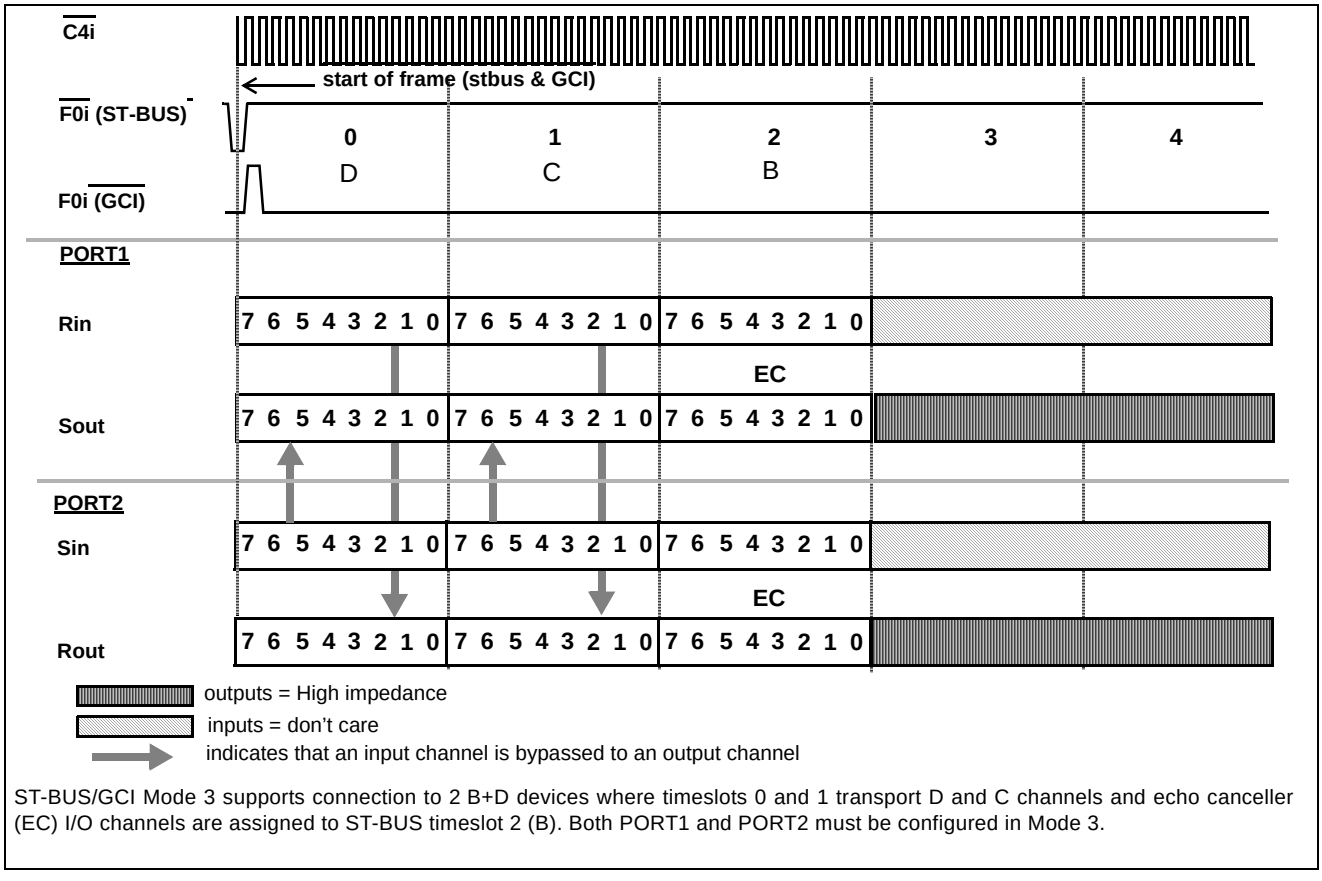
In ST-BUS/GCI Mode 1, echo canceller I/O channels are assigned to ST-BUS/GCI timeslot 0. Note that the user can configure PORT1 and PORT2 into different modes.

Figure 3 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 0 (Mode 1)



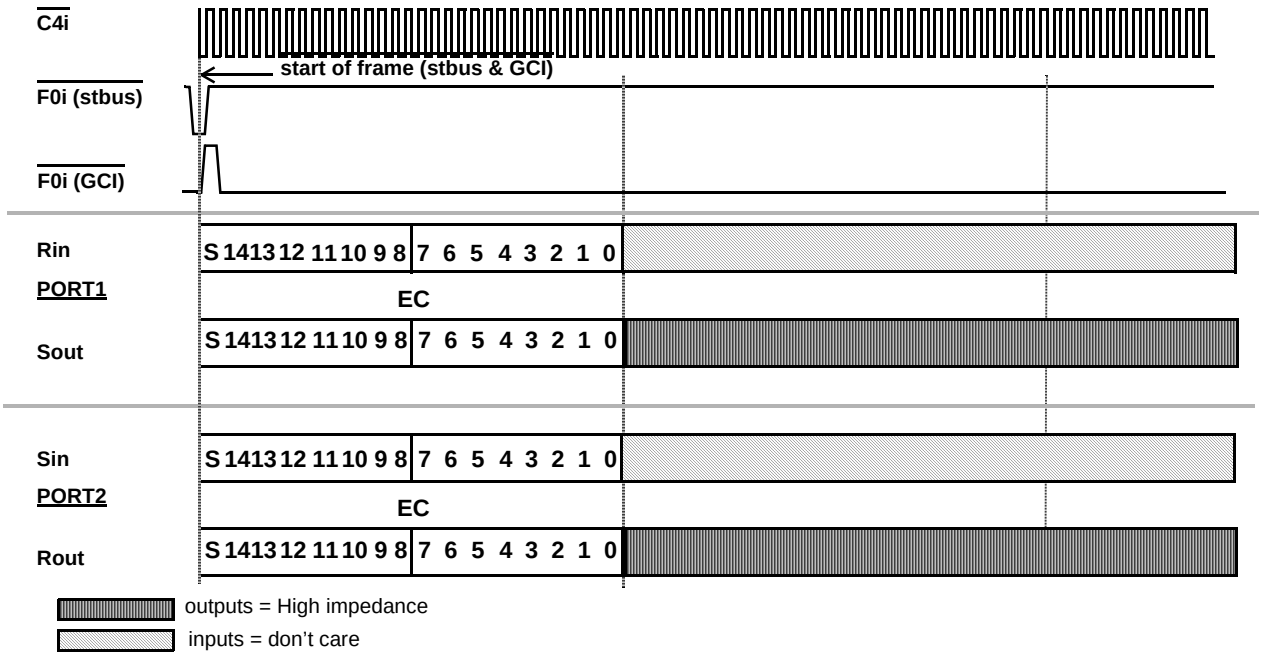
In ST-BUS/GCI Mode 2, echo canceller I/O channels are assigned to ST-BUS/GCI timeslot 2. Note that the user can configure PORT1 and PORT2 into different modes.

Figure 4 - ST-BUS and GCI 8-Bit Companded PCM I/O on Timeslot 2 (Mode 2)



ST-BUS/GCI Mode 3 supports connection to 2 B+D devices where timeslots 0 and 1 transport D and C channels and echo canceller (EC) I/O channels are assigned to ST-BUS timeslot 2 (B). Both PORT1 and PORT2 must be configured in Mode 3.

Figure 5 - ST-BUS and GCI 8-Bit Companded PCM I/O with D and C channels (Mode 3)



ST-BUS/GCI Mode 4 allows 16 bit 2's complement linear data to be transferred using ST-BUS/GCI I/O timing. Note that PORT1 and PORT2 need not necessarily both be in mode 4.

Figure 6 - ST-BUS and GCI 16-Bit 2's Complement Linear PCM I/O (Mode 4)

PORT1 Rin/Sout		ST-BUS/GCI Mode Selection	PORT2 Sin/Rout	
Enable Pins			Enable Pins	
MD1	ENA1		MD2	ENA2
0	0	Mode 1. 8 bit companded PCM I/O on timeslot 0	0	0
0	1	Mode 2. 8 bit companded PCM I/O on timeslot 2.	0	1
1	0	Mode 3. 8 bit companded PCM I/O on timeslot 2. Includes D & C channel bypass in timeslots 0 & 1.	1	0
1	1	Mode 4. 16-bit 2's complement linear PCM I/O on timeslots 0 & 1.	1	1

Table 2 - ST-BUS & GCI Mode Select

2.2 SSI Operation

The SSI PCM interface consists of data input pins (Rin, Sin), data output pins (Sout, Rout), a variable rate bit clock (BCLK), and two enable pins (ENA1, ENA2) to provide strobes for data transfers. The active high enable may be either 8 or 16 BCLK cycles in duration. Automatic detection of the data type (8 bit companded or 16-bit 2's complement linear) is accomplished internally. The data type cannot change dynamically from one frame to the next.

In SSI operation, the frame boundary is determined by the rising edge of the ENA1 enable strobe (see Figure 7). The other enable strobe (ENA2) is used for parsing input/output data and it must pulse within 125 microseconds of the rising edge of ENA1.

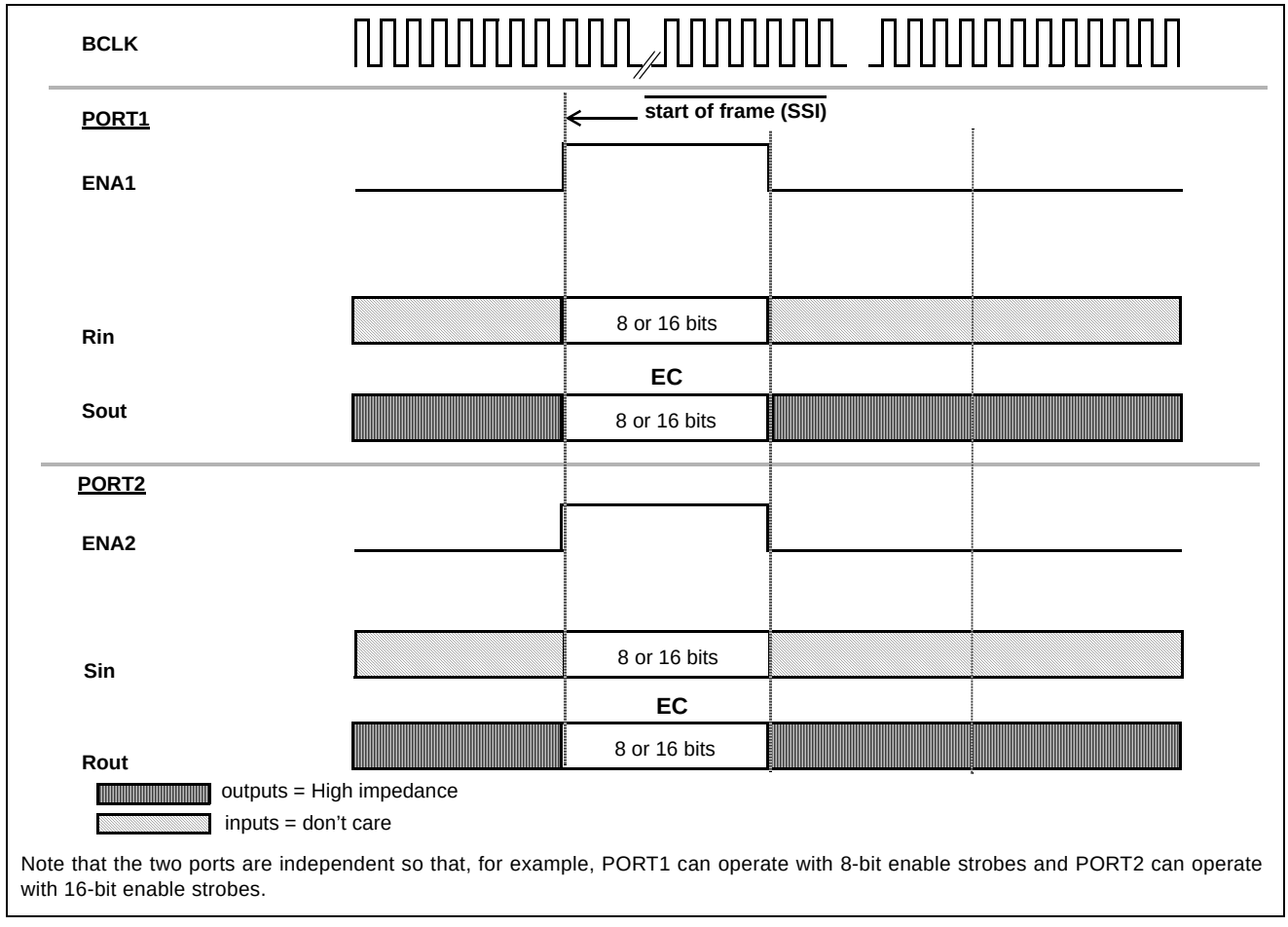
In SSI operation, the enable strobes may be a mixed combination of 8 or 16 BCLK cycles allowing the flexibility to mix 2's complement linear data on one port (e.g., Rin/Sout) with companded data on the other port (e.g., Sin/Rout).

Enable Strobe Pin	Designated PCM I/O Port
ENA1	Line Side Echo Path (PORT 1)
ENA2	Acoustic Side Echo Path (PORT 2)

Table 3 - SSI Enable Strobe Pins

2.3 PCM Law and Format Control (LAW, FORMAT)

The PCM companding/coding law used by the ZL38001 is controlled through the LAW and FORMAT pins. ITU-T G.711 companding curves for μ-Law and A-Law are selected by the LAW pin. PCM coding ITU-T G.711 and Sign-Magnitude are selected by the FORMAT pin. See Table 4.



Note that the two ports are independent so that, for example, PORT1 can operate with 8-bit enable strobes and PORT2 can operate with 16-bit enable strobes.

Figure 7 - SSI Operations

PCM Code	Sign-Magnitude FORMAT=0	ITU-T (G.711) FORMAT=1	
	μ/A-LAW LAW = 0 or 1	μ-LAW LAW = 0	A-LAW LAW =1
+ Full Scale	1111 1111	1000 0000	1010 1010
+ Zero	1000 0000	1111 1111	1101 0101
- Zero	0000 0000	0111 1111	0101 0101
- Full Scale	0111 1111	0000 0000	0010 1010

Table 4 - Companded PCM

2.4 Linear PCM

The 16-bit 2's complement PCM linear coding permits a dynamic range beyond that which is specified in ITU-T G.711 for companded PCM. The echo-cancellation algorithm will accept 16-bits 2's complement linear code which gives a maximum signal level of +15 dBm0.

2.5 Bit Clock (BCLK/$\overline{C4i}$)

The BCLK/$\overline{C4i}$ pin is used to clock the PCM data for GCI and ST-BUS ($\overline{C4i}$) interfaces, as well as for the SSI (BCLK) interface.

In SSI operation, the bit rate is determined by the BCLK frequency. This input must contain either eight or sixteen clock cycles within the valid enable strobe window. BCLK may be any rate between 128 KHz to 4.096 MHz and can be discontinuous outside of the enable strobe windows defined by ENA1, ENA2 pins. Incoming PCM data (Rin, Sin) are sampled on the falling edge of BCLK while outgoing PCM data (Sout, Rout) are clocked out on the rising edge of BCLK. See Figure 13.

In ST-BUS and GCI operation, connect the system $\overline{C4}$ (4.096 MHz) clock to the $\overline{C4i}$ pin.

2.6 Master Clock (MCLK)

A nominal 20 MHz, continuously-running master clock (MCLK) is required. MCLK may be asynchronous with the 8 KHz frame.

3.0 Microport

The serial microport provides access to all ZL38001 internal read and write registers, plus write-only access to the bootloadable program RAM (see next section for bootload description.) This microport is compatible with Intel MCS-51 (mode 0), Motorola SPI (CPOL=0, CPHA=0) and National Semiconductor Microwire specifications. The microport consists of a transmit/receive data pin (DATA1), a receive data pin (DATA2), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK).

The ZL38001 automatically adjusts its internal timing and pin configuration to conform to Intel or Motorola/National requirements. The microport dynamically senses the state of the SCLK pin each time $\overline{CS}$ pin becomes active (i.e., high to low transition). If SCLK pin is high during $\overline{CS}$ activation, then Intel mode 0 timing is assumed. In this case DATA1 pin is defined as a bi-directional (transmit/receive) serial port and DATA2 is internally disconnected. If SCLK is low during $\overline{CS}$ activation, then Motorola/National timing is assumed and DATA1 is defined as the data transmit pin while DATA2 becomes the data receive pin. The ZL38001 supports Motorola half-duplex processor mode (CPOL=0

and CPHA=0). This means that during a write to the ZL38001, by the Motorola processor, output data from the DATA1 pin must be ignored. This also means that input data on the DATA2 pin is ignored by the ZL38001 during a valid read by the Motorola processor.

All data transfers through the microport are two bytes long. This requires the transmission of a Command/Address byte followed by the data byte to be written to or read from the addressed register. CS must remain low for the duration of this two-byte transfer. As shown in Figures 8 and 9, the falling edge of CS indicates to the ZL38001 that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of CS are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and at what address. The next 8 clock cycles are used to transfer the data byte between the ZL38001 and the microcontroller. At the end of the two-byte transfer, $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the DATA1 pin. The DATA1 pin will remain tri-stated as long as $\overline{CS}$ is high.

Intel processors utilize Least Significant Bit (LSB) first transmission while Motorola/National processors use Most Significant Bit (MSB) first transmission. The ZL38001 microport automatically accommodates these two schemes for normal data bytes. However, to ensure timely decoding of the R/W and address information, the Command/Address byte is defined differently for Intel and Motorola/National operations. Refer to the relative timing diagrams of Figure 8 and Figure 9. Receive data bits are sampled on the rising edge of SCLK while transmit data is clocked out on the falling edge of SCLK. Detailed microport timing is shown in Figure 14 and Figure 15.

3.1 Bootload Process and Execution from RAM

A bootloadable program RAM (BRAM) is available on the ZL38001 to support factory-issued software upgrades to the built-in algorithm. To make use of this bootload feature, users must include 4096 X 8 bits of memory in their microcontroller system (i.e., external to the ZL38001), from which the ZL38001 can be bootloaded. Registers and program data are loaded into the ZL38001 in the same fashion via the serial microport. Both employ the same command / address / data byte specification described in the previous section on serial microport. Either intel or motorola mode may be transparently used for bootloading. There are also two registers relevant to bootloading (BRC=control and SIG=signature, see Register Summary). The effect of these register values on device operation is summarized in Table 5.

Bootload mode is entered and exited by writing to the bootload bit in the Bootload RAM Control (BRC) register at address 3fh (see Register Summary). During bootload mode, any serial microport "write" (R/$\overline{W}$ command bit =0) to an address other than that of the BRC register will contribute to filling the program BRAM. Call these transactions "BRAM-fill" writes. Although a command/address byte must still precede each data byte (as described for the serial microport), the values of the address fields for these "BRAM-fill" writes are ignored (except for the value 3fh, which designates the BRC register.) Instead, addresses are internally generated by the ZL38001 for each "BRAM-fill" write. Address generation for "BRAM-fill" writes resumes where it left off following any read transaction while bootload mode is enabled. The first 4096 such "BRAM-fill" writes while bootload is enabled will load the memory, but further ones after that are ignored. Following the write of the first 4096 bytes, the program BRAM will be filled. Before bootload *mode is disabled*, it is recommended that users then read back the value from the signature register (SIG) and compare it to the one supplied by the factory along with the code. Equality verifies that the correct data has been loaded. The signature calculation uses an 8-bit MISR which only incorporates input from "BRAM-fill" writes. Resetting the bootload bit (**C_2**) in the BRC register to 0 (see Register Summary) exits bootload mode, resetting the signature (SIG) register and internal address generator for the next bootload. A hardware reset ($\overline{RESET}$=0) similarly returns the ZL38001 to the ready state for the start of a bootload.

FUNCTIONAL DESCRIPTION FOR USING THE BOOTABLE RAM			
	BOOTLOAD MODE - Microport Access is to bootload RAM (BRAM)		
BRC Register Bits $C_3C_2C_1C_0$ X 1 0 0	R/W	Address	Data
	W	3fh (= 1 1 1 1 1 1 b)	Writes "data" to BRC reg. - Bootload frozen; BRAM contents are NOT affected.
	W	other than 3fh	Writes "data" to next byte in BRAM (bootloading.)
	R	1 x x x x x b	Reads back "data" = BRC reg value. - Bootload frozen; BRAM contents are NOT affected.
	R	0 x x x x x b	Reads back "data" = SIG reg value. - Bootload frozen; BRAM contents are NOT affected.
	NON-BOOTLOAD MODE - Microport Access is to device registers (DREGs)		
BRC Register Bits $C_3C_2C_1C_0$ X 0 0 0	R/W	Address	Data
	W	any (= a_5 a_4 a_3 a_2 a_1 a_0 b)	Writes "data" to corresponding DREG.
	R	any (= a_5 a_4 a_3 a_2 a_1 a_0 b)	Reads back "data" = corresponding DREG value.
PROGRAM EXECUTION MODES			
$C_3C_2C_1C_0$ 0 0 0 0	Execute program in ROM, bootload mode disabled. - BRAM address counter reset to initial (ready) state. - SIG reg reseeded to initial (ready) state		
$C_3C_2C_1C_0$ 0 1 0 0	Execute program in ROM, while bootloading the RAM. - BRAM address counter increments on microport writes (except to 3fh) - SIG reg recalculates signature on microport writes (except to 3fh)		
$C_3C_2C_1C_0$ 1 0 0 0	Execute program in RAM, bootload mode disabled. - BRAM address counter reset to initial (ready) state. - SIG reg reseeded to initial (ready) state		
$C_3C_2C_1C_0$ 1 1 0 0	- NOT RECOMMENDED - (Execute program in RAM, while bootloading the RAM)		

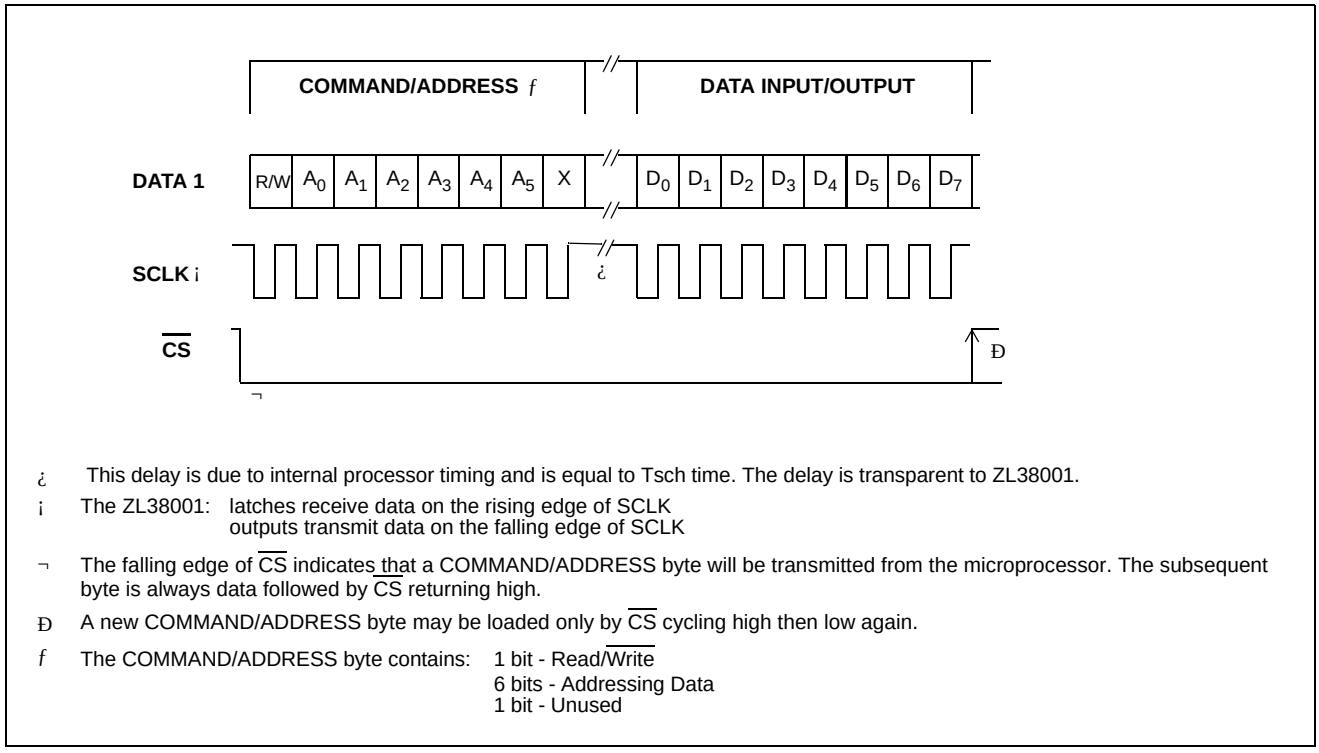
Table 5 - Bootload RAM Control (BRC) Register States

Note: bits C_1 C_0 are reserved, and must be set to zero.

Once the program has been loaded, to begin execution from RAM, bootload mode must be disabled (BOOT bit, C_2=0) and execution from RAM enabled (RAM_ROMb bit, C_3=1) by setting the appropriate bits in the BRC register. During the bootload process, however, ROM program execution (RAM_ROMb bit, C_3=0) should be selected. See Table 5 for the effect of the BRC register settings on Microport accesses and on program execution.

Following program loading and enabling of execution from RAM, it is recommended that users set the software reset bit in the Main Control (MC) register, to ensure that the device updates the default register values to those of the new program in RAM. Note: it is important to use a software reset rather than a hardware ($\overline{RESET}$=0) reset, as the latter will return the device to its default settings (which includes execution from program ROM instead of RAM.)

To verify which code revision is currently running, users can access the Firmware Revision Code (FRC) register (see Register Summary). This register reflects the identity code (revision number) of the last program to run register initialization (which follows a software or hardware reset.)



¿ This delay is due to internal processor timing and is equal to Tsch time. The delay is transparent to ZL38001.

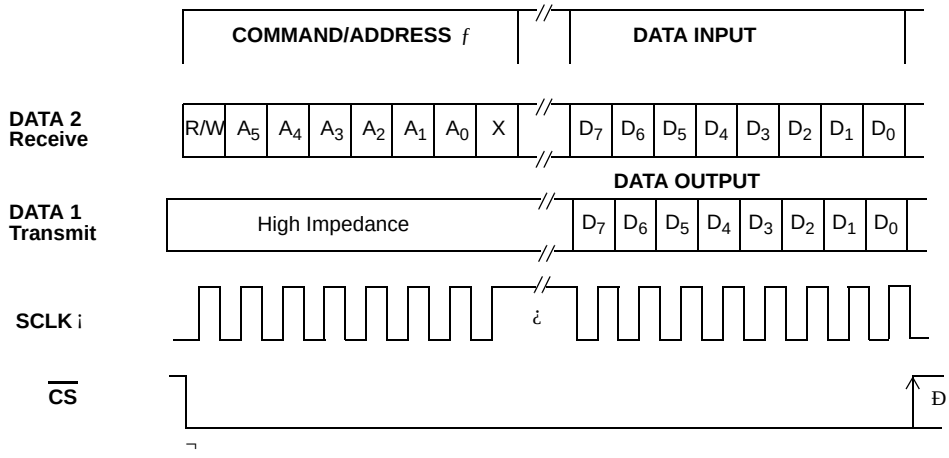
¡ The ZL38001: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

¬ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

Ð A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

f The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
6 bits - Addressing Data
1 bit - Unused

Figure 8 - Serial Microport Timing for Intel Mode 0



¿ This delay is due to internal processor timing and is equal to Tsch time. The delay is transparent to ZL38001.

¡ The ZL38001: latches receive data on the rising edge of SCLK
outputs transmit data on the falling edge of SCLK

¬ The falling edge of $\overline{CS}$ indicates that a COMMAND/ADDRESS byte will be transmitted from the microprocessor. The subsequent byte is always data followed by $\overline{CS}$ returning high.

Ð A new COMMAND/ADDRESS byte may be loaded only by $\overline{CS}$ cycling high then low again.

f The COMMAND/ADDRESS byte contains: 1 bit - Read/$\overline{Write}$
6 bits - Addressing Data
1 bit - Unused

Figure 9 - Serial Microport Timing for Motorola Mode 00 or National Microwire

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}-V_{SS}	-0.5	5.0	V
2	Input Voltage	V_i	V_{SS}-0.3	5.5	V
3	Output Voltage Swing	V_o	V_{SS}-0.3	5.5	V
4	Continuous Current on any digital pin	$I_{i/o}$		±20	mA
5	Storage Temperature	T_{ST}	-65	150	°C
6	Package Power Dissipation	P_D		90 (typ)	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	2.7	3.3	3.6	V	
2	Input High Voltage		1.4		V_{DD}	V	
3	Input Low Voltage		V_{SS}		0.4	V	
4	Operating Temperature	T_A	-40		+85	°C	

Echo Return Limits

	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
1	Acoustic Echo Return			0	dB	Measured from Rout -> Sin
2	Line Echo Return			0	dB	Measured from Sout -> Rin

DC Electrical Characteristics*- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions/Notes
1	Standby Supply Current:	I_{CC}		3	70	µA	$\overline{\text{RESET}}$ = 0
	Operating Supply Current:	I_{DD}		20		mA	$\overline{\text{RESET}}$ = 1, clocks active
2	Input HIGH voltage	V_{IH}	0.7V_{DD}			V	
3	Input LOW voltage	V_{IL}			0.3V_{DD}	V	
4	Input leakage current	I_{IH}/I_{IL}		0.1	10	µA	V_{IN}=V_{SS} to V_{DD}
5	High level output voltage	V_{OH}	0.8V_{DD}			V	I_{OH}=2.5 mA
6	Low level output voltage	V_{OL}			0.4V_{DD}	V	I_{OL}=5.0 mA
7	High impedance leakage	I_{OZ}		1	10	µA	V_{IN}=V_{SS} to V_{DD}
8	Output capacitance	C_o		10		pF	
9	Input capacitance	C_i		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
*DC Electrical Characteristics are over recommended temperature and supply voltage.

AC Electrical Characteristics† - Serial Data Interfaces - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Notes
1	MCLK Frequency	f_{CLK}	19.15		20.5	MHz	
2	BCLK/$\overline{C4i}$ Clock High	t_{BCH}, t_{C4H}	90			ns	
3	BCLK/$\overline{C4i}$ Clock Low	t_{BLL}, t_{C4L}	90			ns	
4	BCLK/$\overline{C4i}$ Period	t_{BCP}	240		7900	ns	
5	SSI Enable Strobe to Data Delay (first bit)	t_{SD}	80			ns	C_L = 150 pF
6	SSI Data Output Delay (excluding first bit)	t_{DD}	80			ns	C_L = 150 pF
7	SSI Output Active to High Impedance	t_{AHZ}	80			ns	C_L = 150 pF
8	SSI Enable Strobe Signal Setup	t_{SSS}	10		t_{BCP} -15	ns	
9	SSI Enable Strobe Signal Hold	t_{SSH}	15		t_{BCP} -10	ns	
10	SSI Data Input Setup	t_{DIS}	10			ns	
11	SSI Data Input Hold	t_{DIH}	15			ns	
12	ST-BUS/GCI $\overline{F0i}$ Setup	t_{F0iS}	20		150	ns	
13	ST-BUS/GCI $\overline{F0i}$ Hold	t_{F0iH}	20		150	ns	
14	ST-BUS/GCI Data Output delay	t_{DSD}	80			ns	C_L = 150 pF
15	ST-BUS/GCI Output Active to High Impedance	t_{ASHZ}	80			ns	C_L = 150 pF
16	ST-BUS/GCI Data Input Hold time	t_{DSH}	20			ns	
17	ST-BUS/GCI Data Input Setup time	t_{DSS}	20			ns	

† Timing is over recommended temperature and power supply voltages.

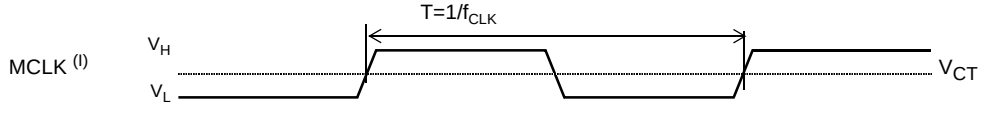
AC Electrical Characteristics† - Microport Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Notes
1	Input Data Setup	t_{IDS}	30			ns	
2	Input Data Hold	t_{IDH}	30			ns	
3	Output Data Delay	t_{ODD}	100			ns	C_L = 150 pF
4	Serial Clock Period	t_{SCP}	500			ns	
5	SCLK Pulse Width High	t_{SCH}	250			ns	
6	SCLK Pulse Width Low	t_{SCL}	250			ns	
7	CS Setup-Intel	t_{CSSI}	200			ns	
8	$\overline{CS}$ Setup-Motorola	t_{CSSM}	100			ns	
9	$\overline{CS}$ Hold	t_{CSH}	100			ns	
10	$\overline{CS}$ to Output High Impedance	t_{OHZ}	100			ns	C_L = 150 pF

† Timing is over recommended temperature range and recommended power supply voltages.

Characteristic	Symbol	CMOS Level	Units
CMOS reference level	V_{CT}	0.5*V_{DD}	V
Input HIGH level	V_H	0.9*V_{DD}	V
Input LOW level	V_L	0.1*V_{DD}	V
Rise/Fall HIGH measurement point	V_{HM}	0.7*V_{DD}	V
Rise/Fall LOW measurement point	V_{LM}	0.3*V_{DD}	V

Table 6 - Reference Level Definition for Timing Measurements



Notes: O. CMOS output
I. CMOS input (5 V tolerant)
(see Table 8 for symbol definitions)

Figure 10 - Master Clock - MCLK

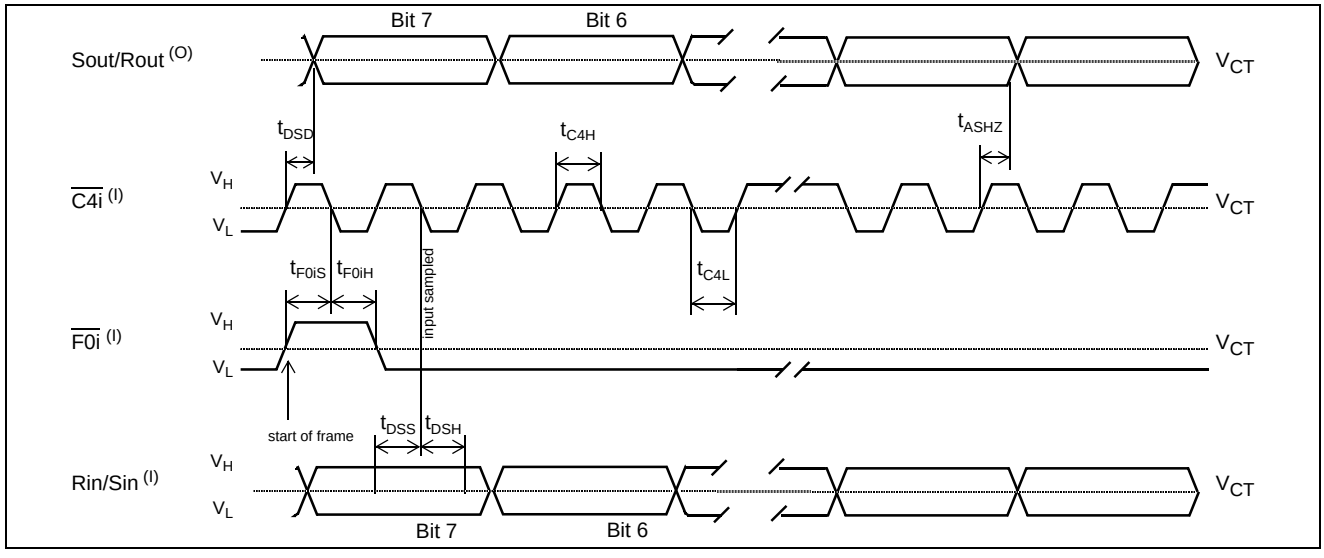


Figure 11 - GCI Data Port Timing

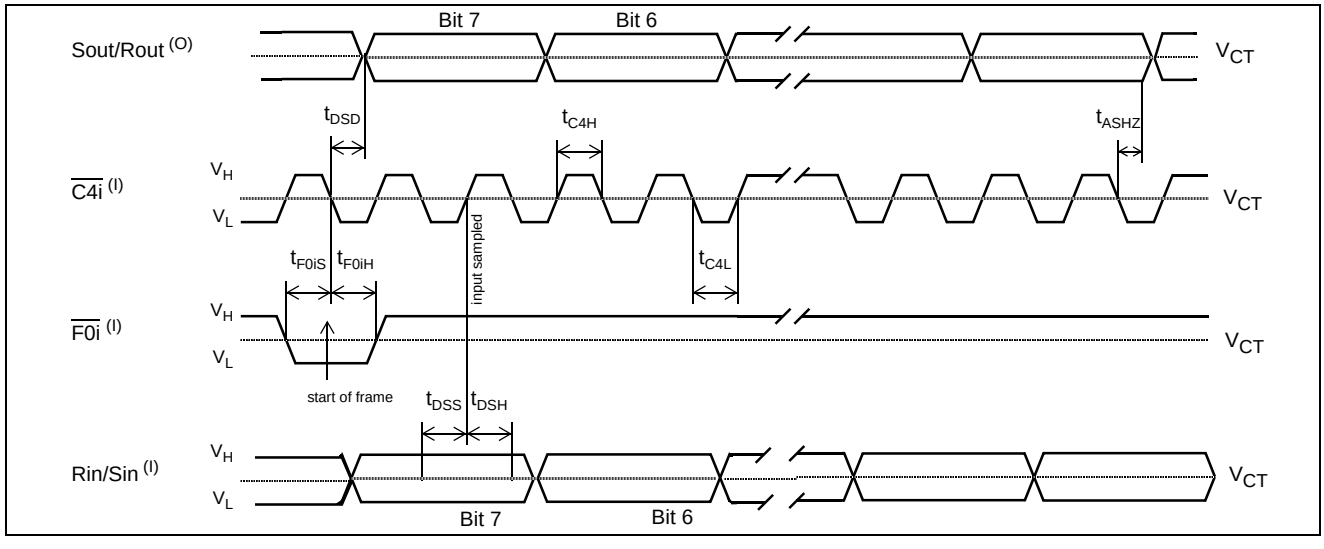


Figure 12 - ST-BUS Data Port Timing

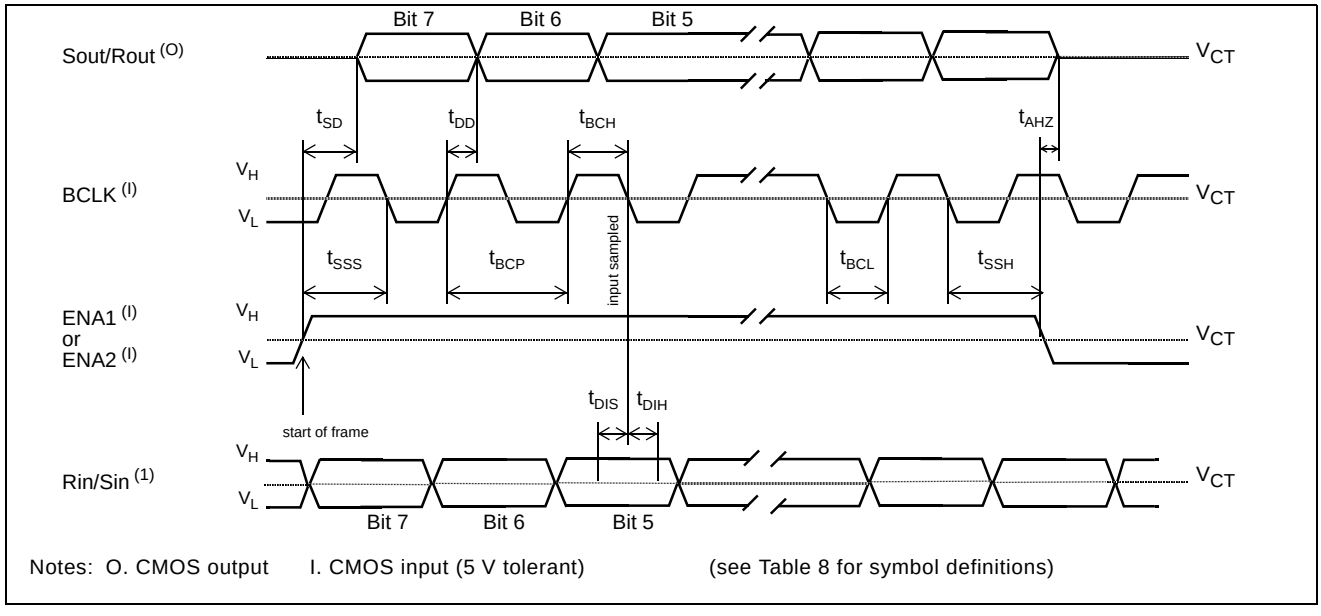


Figure 13 - SSI Data Port Timing

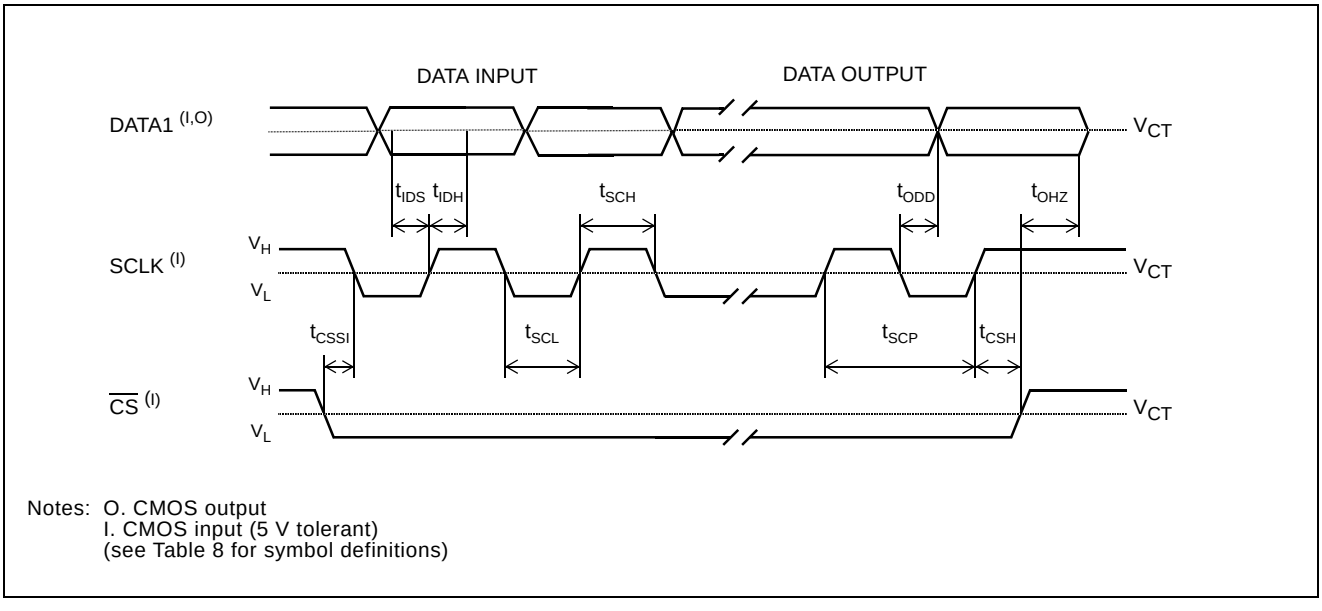
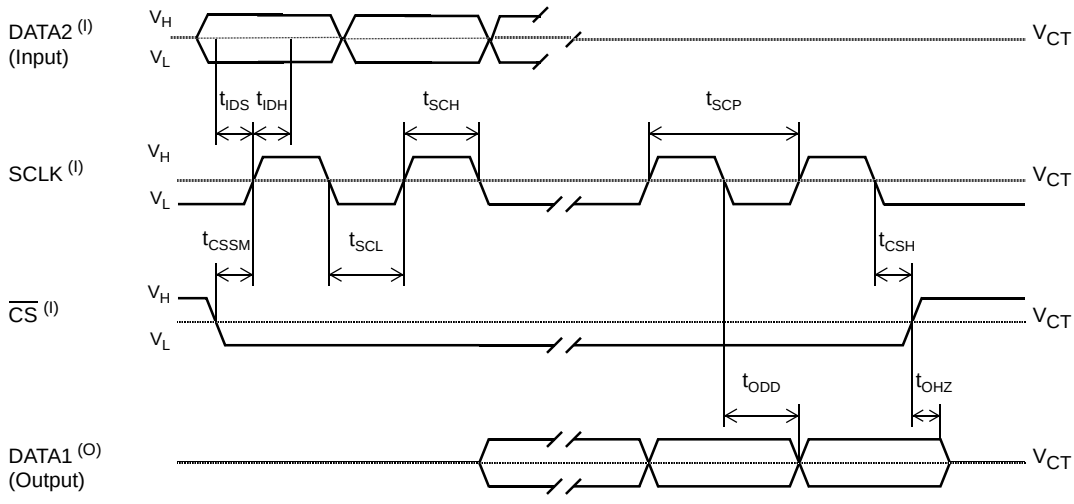


Figure 14 - INTEL Serial Microport Timing



Notes: O. CMOS output
I. CMOS input (5 V tolerant)
(see Table 8 for symbol definitions)

Figure 15 - Motorola Serial Microport Timing

4.0 Register Summary

External Read/Write Address: 00_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
LIMIT	MUTE_R	MUTE_S	BYPASS	NB-	AGC-	AH-	RESET

Bit	Name	Description
7	LIMIT	When high, the 2-bit shift mode is enabled in conjunction with bit 7 of LEC register and when low 2-bit shift mode is disabled. Default limit for Rin and Sin is 3.14 dBm0.
6	MUTE_R	When high, the Rin path is muted to quite code (after the NLP) and when low the Rin path is not muted.
5	MUTE_S	When high, the Sin path is muted to quite code (after the NLP) and when low the Sin path is not muted.
4	BYPASS	When high, the Send and Receive paths are transparently by-passed from input to output and when low the Send and Receive paths are not bypassed.
3	NB-	When high, Narrowband signal detectors in Rin and Sin paths are disabled and when low the signal detectors are enabled.
2	AGC-	When high, AGC is disabled and when low AGC is enabled.
1	AH-	When high, the Howling detector is disabled and when low the Howling detector is enabled.
0	RESET	When high, the power initialization routine is executed presetting all registers to default values. This bit automatically clears itself to ’0’ when reset is complete.

Register Table 1 - Main Control Register (MC)

External Read/Write Address:21_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
P-	ASC-	NLP-	INJ-	HPF-	HCLR	ADAPT-	ECBY

Bit	Name	Description
7	P-	When high, the Exponential weighting function for the adaptive filter is disabled and when low the weighting function is enabled
6	ASC-	When high, the Internal Adaptation speed control is disabled and when low the Adaptation speed is enabled.
5	NLP-	When high, the Non Linear Processor is disabled in the Sin/Sout path and when low the NLP is enabled.

Register Table 2 - Acoustic Echo Canceller Control Register (AEC)

External Read/Write Address:21_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
P-	**ASC-**	**NLP-**	**INJ-**	**HPF-**	**HCLR**	**ADAPT-**	**ECBY**

Bit	Name	Description
4	INJ-	When high, the Noise filtering process is disabled in the NLP and when low the Noise filtering process is enabled.
3	HPF-	When high, Offset nulling filter is bypassed in the Sin/Sout path and when low the Offset nulling filter in not bypassed.
2	HCLR	When high, Adaptive filter coefficients are cleared and when low the filter coefficients are not cleared
1	ADAPT-	When high, the Echo canceller adaptation is disabled and when low the adaptation is enabled.
0	ECBY	When high, the Echo estimate from the filter is not subtracted from the input (Sin), when low the estimate is subtracted.

Register Table 2 - Acoustic Echo Canceller Control Register (AEC) (continued)

External Read/Write Address: 01_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
SHFT	**ASC-**	**NLP-**	**INJ-**	**HPF-**	**HCLR**	**ADAPT-**	**ECBY**

Bit	Name	Description
7	SHFT	When high the 16-bit linear mode, inputs Sin, Rin, are shift right by 2 and outputs Sout, Rout are shift left by 2. This bit is ignored when 16-bit linear mode is not selected in both ports. This bit is also ignored if bit 7 of MC register is set to zero.
6	ASC-	When high, the Internal Adaptation speed control is disabled and when low the Adaptation speed is enabled.
5	NLP-	When high, the Non Linear Processor is disabled in the Rin/Rout path and when low the NLP is enabled.
4	INJ-	When high, the Noise filtering process is disabled in the NLP and when low the Noise filtering process is enabled.
3	HPF-	When high, Offset nulling filter is bypassed in the Rin/Rout path and when low the Offset nulling filter in not bypassed.
2	HCLR	When high, Adaptive filter coefficients are cleared and when low the filter coefficients are not cleared.

Register Table 3 - Line Echo Canceller Control Register (LEC)

External Read/Write Address: 01_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
SHFT	**ASC-**	**NLP-**	**INJ-**	**HPF-**	**HCLR**	**ADAPT-**	**ECBY**

Bit	Name	Description
1	ADAPT-	When high, the Echo canceller adaptation is disabled and when low the adaptation is enabled.
0	ECBY	When high, the Echo estimate from the filter is not substracted from the input (Rin), when low the estimate is substracted.

Register Table 3 - Line Echo Canceller Control Register (LEC) (continued)

External Read Address: 22_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
-	**ACMUND**	**HWLNG**	**-**	**NLPDC**	**DT**	**NB**	**NBS**

Bit	Name	Description
7	-	RESERVED.
6	ACMUND	When low, No active signal in the Rin/Rout path.
5	HWLNG	When high, Howling is occurring in the loop and when low, no Howling is detected.
4	-	RESERVED.
3	NLPDC	When high, the NLP is activated and when low the NLP is not activated.
2	DT	When high the Double Talk is detected and when low, the Double talk is not detected.
1	NB	LOGICAL OR of the status bit NBS + NBR from LSR Register.
0	NBS	When high, the Narrowband signal has been detected in the Sin/Sout path and when low, the Narrowband signal has not been detected in the Sin/Sout path.

Register Table 4 - Acoustic Echo Canceller Status Register (ASR) (* Do not write to this register)

External Read Address: 02_H
Reset Value: 00_H

7	6	5	4	3	2	1	0

Bit	Name	Description
7	-	RESERVED.
6	-	
5	-	
4	-	
3	NLPC	When high, NLP is activated and when low NLP is not activated.
2	DT	When high, double-talk is detected and when low double-talk is not detected.
1	NB	This bit indicates a LOGICAL-OR of Status bits NBR + NBS (from ASR Register).
0	NBR	When high, a narrowband signal has been detected in the Receive (Rin) path. When low no narrowband signal is not detected in the Rin path.

Register Table 5 - Line Echo Canceller Status Register (LSR) (* Do not write to this register)

External Read/Write Address:20_H
Reset Value: $6D_H$

7	6	5	4	3	2	1	0
-	-	-	G4	G3	G2	G1	G0

Bit	Name	Description
7	Reserved	Must keep as Logic 0.
6	Reserved	Must keep as Logic 1.
5	Reserved	Must keep as Logic 1.
4-0	G4-0	User Gain Control on the Rin/Rout path (Tolerance of gains: +/- 0.15 dB). The hexadecimal number represents G3 to G0 value in the table below.

Register Value	Gain		Register Value	Gain
0h	-24 dB		10h	+24 dB
1h	-21 dB		11h	+27 dB
2h	-18 dB		12h	+30 dB
3h	-15 dB		13h	+33 dB
4h	-12 dB		14h	+36 dB
5h	-9 dB		15h	+39 dB
6h	-6 dB		16h	+42 dB
7h	-3 dB		17h	+45 dB
8h	0 dB		18h	+48 dB
9h	+3 dB		19h	Reserved
Ah	+6 dB		1Ah	Reserved
Bh	+9 dB		1Bh	Reserved
Ch	+12 dB		1Ch	Reserved
Dh	+15 dB		1Dh	Reserved
Eh	+18 dB		1Eh	Reserved
Fh	+21 dB		1Fh	Reserved

Register Table 6 - Receive Gain Control Register

External Read/Write Address: 32_H
Reset Value: 25_H

7	6	5	4	3	2	1	0
HG_2	HG_1	HG_0	DTGain	-	-	-	-

Bit	Name	Description
7	-	RESERVED. Must keep as 0.
6	-	RESERVED. Must keep as 0.
5	-	RESERVED. Must keep as 1.
4	DTRGain	This bit controls the gain level at Rout during double talk. When this bit is high 12 dB of attenuation is injected into the Rout path during double talk. When this bit is low the gain pad is disabled.
3	-	RESERVED. Must keep as 0.
2	-	RESERVED. Must keep as 1.
1	-	RESERVED. Must keep as 0.
0	-	RESERVED. Must keep as 1.

Register Table 7 - Double Talk Gain Control Register 1 (DTGCR1)

External Read/Write Address: 12_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
-	-	-	DTSGain		-	-	

Bit	Name	Description
7	-	RESERVED. Must keep as 0.
6	-	RESERVED. Must keep as 0.
5	-	RESERVED. Must keep as 0.
4	DTSGain	This bit controls the gain level at Sout during double talk. When this bit is high 12 dB of attenuation is injected into the Sout path during double talk. When this bit is low the gain pad is disabled.
3	-	RESERVED. Must keep as 0.
2	-	RESERVED. Must keep as 0.
1	-	RESERVED. Must keep as 0.
0	-	RESERVED. Must keep as 0.

Register Table 8 - Double Talk Gain Control Register 2 (DTGCR2)

External Read/Write Address: 31_H
Reset Value: 21_H

7	6	5	4	3	2	1	0
$DTDT_2$	**$DTDT_1$**	**$DTDT_0$**	-	-	-	-	-

Bit	Name	Description
7	$DTDT_2$	
6	$DTDT_1$	
5	$DTDT_0$	
4	-	RESERVED. Must keep as 0.
3	-	RESERVED. Must keep as 0.
2	-	RESERVED. Must keep as 0.
1	-	RESERVED. Must keep as 0.
0	-	RESERVED. Must keep as 1.

$DTDT_2$, $DTDT_1$, $DTDT_0$ Value	DTDT	**$DTDT_2$, $DTDT_1$, $DTDT_0$** Value	DTDT
000	-12 dB	100	+12 dB
001	-6 dB	101	+18 dB
010	0 dB	110	+24 dB
011	+6 dB	111	+30 dB

Register Table 9 - Double Talk detection Threshold Register (DTDT)

External Read Address: 16_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$RIPD_7$	**$RIPD_6$**	**$RIPD_5$**	**$RIPD_4$**	**$RIPD_3$**	**$RIPD_2$**	**$RIPD_1$**	**$RIPD_0$**

Bit	Name	Description
7	$RIPD_7$	These peak detector registers allow the user to monitor the receive in signal (Rin) peak level at reference point R1 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$RIPD_6$	
5	$RIPD_5$	
4	$RIPD_4$	
3	$RIPD_3$	
2	$RIPD_2$	
1	$RIPD_1$	
0	$RIPD_0$	

Register Table 10 - Receive (Rin) Peak Detect Register 1 (RIPD1)

External Read Address: 17_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$RIPD_{15}$	**$RIPD_{14}$**	**$RIPD_{13}$**	**$RIPD_{12}$**	**$RIPD_{11}$**	**$RIPD_{10}$**	**$RIPD_9$**	**$RIPD_8$**

Bit	Name	Description
7	$RIPD_{15}$	These peak detector registers allow the user to monitor the receive in signal (Rin) peak level at reference point R1 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$RIPD_{14}$	
5	$RIPD_{13}$	
4	$RIPD_{12}$	
3	$RIPD_{11}$	
2	$RIPD_{10}$	
1	$RIPD_9$	
0	$RIPD_8$	

Register Table 11 - Receive (Rin) Peak Detect Register 2 (RIPD2)

External Read Address: 18_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$REPD_7$	**$REPD_6$**	**$REPD_5$**	**$REPD_4$**	**$REPD_3$**	**$REPD_2$**	**$REPD_1$**	**$REPD_0$**

Bit	Name	Description
7	$REPD_7$	These peak detector registers allow the user to monitor the error signal peak level at reference point R2 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$REPD_6$	
5	$REPD_5$	
4	$REPD_4$	
3	$REPD_3$	
2	$REPD_2$	
1	$REPD_1$	
0	$REPD_0$	

Register Table 12 - Receive (Rin) ERROR Peak Detect Register 1 (REPD1)

External Read Address: 19_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$REPD_{15}$	**$REPD_{14}$**	**$REPD_{13}$**	**$REPD_{12}$**	**$REPD_{11}$**	**$REPD_{10}$**	**$REPD_9$**	**$REPD_8$**

Bit	Name	Description
7	$REPD_{15}$	These peak detector registers allow the user to monitor the error signal peak level at reference point R2 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$REPD_{14}$	
5	$REPD_{13}$	
4	$REPD_{12}$	
3	$REPD_{11}$	
2	$REPD_{10}$	
1	$REPD_9$	
0	$REPD_8$	

Register Table 13 - Receive (Rin) ERROR Peak Detect Register 2 (REPD2)

External Read Address: $3A_H$
Reset Value: 00_H

7	6	5	4	3	2	1	0
$ROPD_7$	**$ROPD_6$**	**$ROPD_5$**	**$ROPD_4$**	**$ROPD_3$**	**$ROPD_2$**	**$ROPD_1$**	**$ROPD_0$**

Bit	Name	Description
7	$ROPD_7$	These peak detector registers allow the user to monitor the receive out signal (Rout) peak level at reference point R3 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$ROPD_6$	
5	$ROPD_5$	
4	$ROPD_4$	
3	$ROPD_3$	
2	$ROPD_2$	
1	$ROPD_1$	
0	$ROPD_0$	

Register Table 14 - Receive (Rout) Peak Detect Register 1 (ROPD1)

External Read Address: $3B_H$
Reset Value: 00_H

7	6	5	4	3	2	1	0
$ROPD_{15}$	**$ROPD_{14}$**	**$ROPD_{13}$**	**$ROPD_{12}$**	**$ROPD_{11}$**	**$ROPD_{10}$**	**$ROPD_9$**	**$ROPD_8$**

Bit	Name	Description
7	$ROPD_{15}$	These peak detector registers allow the user to monitor the receive out signal (Rout) peak level at reference point R3 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$ROPD_{14}$	
5	$ROPD_{13}$	
4	$ROPD_{12}$	
3	$ROPD_{11}$	
2	$ROPD_{10}$	
1	$ROPD_9$	
0	$ROPD_8$	

Register Table 15 - Receive (Rout) Peak Detect Register 2 (ROPD2)

External Read Address: 36_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$SIPD_7$	**$SIPD_6$**	**$SIPD_5$**	**$SIPD_4$**	**$SIPD_3$**	**$SIPD_2$**	**$SIPD_1$**	**$SIPD_0$**

Bit	Name	Description
7	$SIPD_7$	These peak detector registers allow the user to monitor the receive in signal (Sin) peak level at reference point S1 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$SIPD_6$	
5	$SIPD_5$	
4	$SIPD_4$	
3	$SIPD_3$	
2	$SIPD_2$	
1	$SIPD_1$	
0	$SIPD_0$	

Register Table 16 - Send (Sin) Peak Detect Register 1 (SIPD1)

External Read Address: 37_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$SIPD_{15}$	**$SIPD_{14}$**	**$SIPD_{13}$**	**$SIPD_{12}$**	**$SIPD_{11}$**	**$SIPD_{10}$**	**$SIPD_9$**	**$SIPD_8$**

Bit	Name	Description
7	$SIPD_{15}$	These peak detector registers allow the user to monitor the receive in signal (Sin) peak level at reference point S1 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$SIPD_{14}$	
5	$SIPD_{113}$	
4	$SIPD_{12}$	
3	$SIPD_{11}$	
2	$SIPD_{10}$	
1	$SIPD_9$	
0	$SIPD_8$	

Register Table 17 - Send (Sin) Peak Detect Register 2 (SIPD2)

External Read Address: 38_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$SEPD_7$	**$SEPD_6$**	**$SEPD_5$**	**$SEPD_4$**	**$SEPD_3$**	**$SEPD_2$**	**$SEPD_1$**	**$SEPD_0$**

Bit	Name	Description
7	$SEPD_7$	These peak detector registers allow the user to monitor the error signal peak level in the send path at reference point S2 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$SEPD_6$	
5	$SEPD_5$	
4	$SEPD_4$	
3	$SEPD_3$	
2	$SEPD_2$	
1	$SEPD_1$	
0	$SEPD_0$	

Register Table 18 - Send ERROR Peak Detect Register 1 (SEPD1)

External Read Address: 39_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
$SEPD_{15}$	**$SEPD_{14}$**	**$SEPD_{13}$**	**$SEPD_{12}$**	**$SEPD_{11}$**	**$SEPD_{10}$**	**$SEPD_9$**	**$SEPD_8$**

Bit	Name	Description
7	$SEPD_{15}$	These peak detector registers allow the user to monitor the error signal peak level in the send path at reference point S2 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$SEPD_{14}$	
5	$SEPD_{13}$	
4	$SEPD_{12}$	
3	$SEPD_{11}$	
2	$SEPD_{10}$	
1	$SEPD_9$	
0	$SEPD_8$	

Register Table 19 - Send ERROR Peak Detect Register 2 (SEPD2)

External Read Address: $1A_H$
Reset Value: 00_H

7	6	5	4	3	2	1	0
$SOPD_7$	**$SOPD_6$**	**$SOPD_5$**	**$SOPD_4$**	**$SOPD_3$**	**$SOPD_2$**	**$SOPD_1$**	**$SOPD_0$**

Bit	Name	Description
7	$SOPD_7$	These peak detector registers allow the user to monitor the Send out signal (Sout) peak level at reference point S3 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$SOPD_6$	
5	$SOPD_5$	
4	$SOPD_4$	
3	$SOPD_3$	
2	$SOPD_2$	
1	$SOPD_1$	
0	$SOPD_0$	

Register Table 20 - Send (Sout) Peak Detect Register 1 (SOPD1)

External Read Address: $1B_H$
Reset Value: 00_H

7	6	5	4	3	2	1	0
$SOPD_{15}$	**$SOPD_{14}$**	**$SOPD_{13}$**	**$SOPD_{12}$**	**$SOPD_{11}$**	**$SOPD_{10}$**	**$SOPD_9$**	**$SOPD_8$**

Bit	Name	Description
7	$SOPD_{15}$	These peak detector registers allow the user to monitor the Send out signal (Sout) peak level at reference point S3 (see Figure 1). The information is in 16-bit 2's complement linear coded format presented in two 8-bit registers. The high byte is in Register 2 and the low byte is in Register 1.
6	$SOPD_{14}$	
5	$SOPD_{13}$	
4	$SOPD_{12}$	
3	$SOPD_{11}$	
2	$SOPD_{10}$	
1	$SOPD_9$	
0	$SOPD_8$	

Register Table 21 - Send (Sout) Peak Detect Register 2 (SOPD2)

External Read Address: 24_H
Reset Value: 80_H

7	6	5	4	3	2	1	0
L_0	**-**	**-**	**-**	**-**	**-**	**-**	**-**

Bit	Name	Description
7	L_0	This bit is used in conjunction with Rout Limiter Register 2. (See description below.)
6	-	RESERVED
5	-	
4	-	
3	-	
2	-	
1	-	
0	-	

Register Table 22 - Rout Limiter Register 1 (RL1)

External Read Address: 25_H
Reset Value: $3E_H$

7	6	5	4	3	2	1	0
L_8	L_7	L_6	L_5	L_4	L_3	L_2	L_1

Bit	Name	Description
7	L_8	In conjunction with bit 7 (L_0) of the above (RL1) register, this register (RL2) allows the user to program the output Limiter threshold value in the Rout path. Default value is (07D)h which is equal to 3.14 dBmo Maximum value is (1FF)h = 15 dBmo Minimum value is (001)h = -38 dBmo
6	L_7	
5	L_6	
4	L_5	
3	L_4	
2	L_3	
1	L_2	
0	L_1	

Register Table 23 - Rout Limiter Register 2 (RL2)

External Read Address: 26_H
Reset Value: $3D_H$

7	6	5	4	3	2	1	0
L_4	L_3	L_2	L_1	L_0			

Bit	Name	Description
7	L_4	This register allows the user to program the output Limiter threshold value in the Rout path. Default value is (1D)h which is equal to 3.14 dBmo Maximum value is (1F)h
6	L_3	
5	L_2	
4	L_1	
3	L_0	
2	-	RESERVED. Must be keep as 1.
1	-	RESERVED. Must be keep as 0.
0	-	RESERVED. Must be keep as 1.

Register Table 24 - Sout Limiter Register (SL)

External Read Address: 03_H
Reset Value: 00_H

7	6	5	4	3	2	1	0
FRC_2	**FRC_1**	**FRC_0**	**-**	**-**	**-**	**-**	**-**

Bit	Name	Description
7	FRC_2	Revision code of the firmware program currently being run (default=rom=00).
6	FRC_1	
5	FRC_0	
4	-	RESERVED
3	-	
2	-	
1	-	
0	-	

Register Table 25 - Firmware Revision Code Register (FRC)

External Read Address: $3F_H$
Reset Value: 00_H

7	6	5	4	3	2	1	0
-	-	-	-	C_3	C_2	C_1	C_0

Bit	Name	Description
7	-	RESERVED
6	-	
5	-	
4	-	
3	C_3	RAM_ROMb bit. When high, device executes from RAM. When low, device executes from ROM.
2	C_2	BOOT bit. When high, puts device in bootload mode. When low, bootload is disabled.
1	C_1	RESERVED. Must be set to zero.
0	C_0	RESERVED. Must be set to zero.

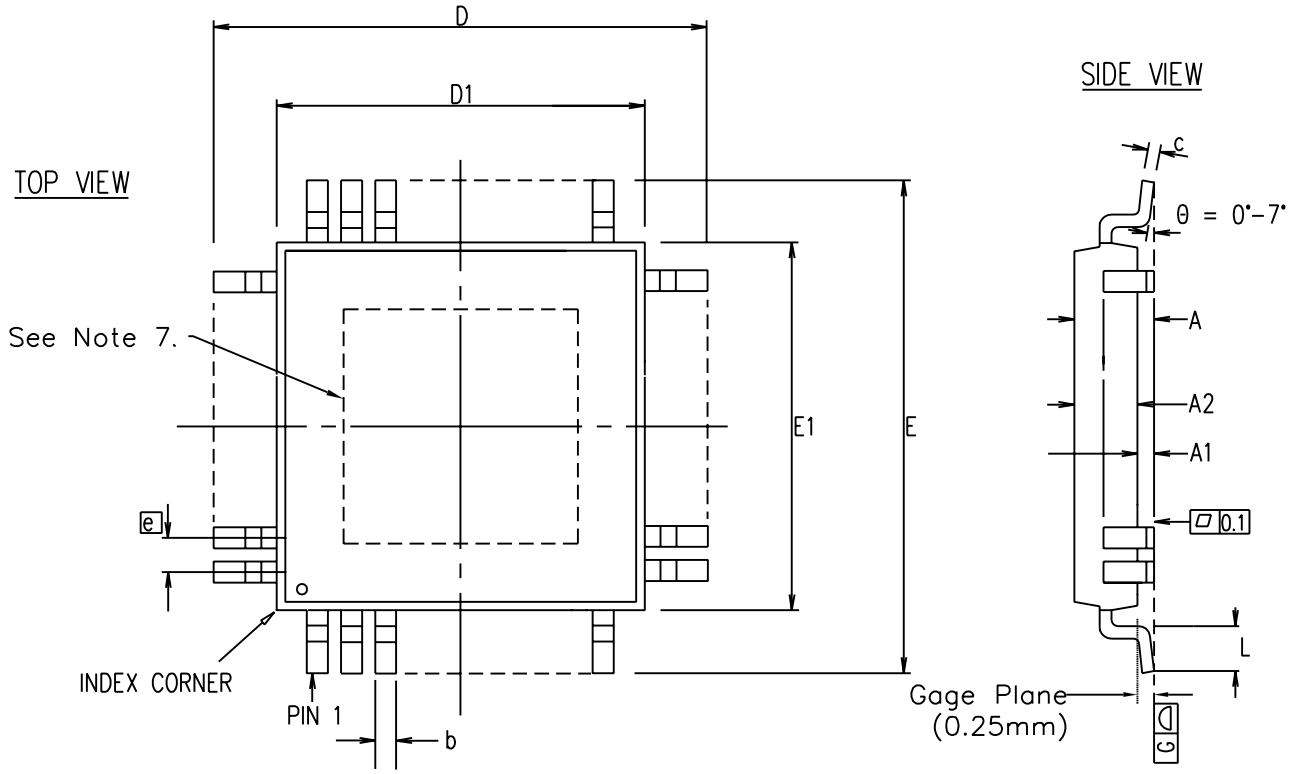
Register Table 26 - Bootload RAM Control Register (BRC)

External Read Address: 07_H
Reset Value: 10_H

7	6	5	4	3	2	1	0
SIG_7	SIG_6	SIG_5	SIG_4	SIG_3	SIG_2	SIG_1	SIG_0

Bit	Name	Description
7	SIG_7	This register provides the signature of the bootloaded data to verify error-free delivery into the device. Note: this register is only accessible if BOOT bit is high (bootload mode enabled) in the above BRC register. While bootload is disabled, the register value is held constant at its reset seed value of FFh.
6	SIG_6	
5	SIG_5	
4	SIG_4	
3	SIG_3	
2	SIG_2	
1	SIG_1	
0	SIG_0	

Register Table 27 - Bootload RAM Signature Register (SIG)



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	9.00 BSC			0.354 BSC	
D1	7.00 BSC			0.276 BSC	
E	9.00 BSC			0.354 BSC	
E1	7.00 BSC			0.276 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	48				
ND	12				
NE	12				
NOTE	SQUARE				

Conforms to JEDEC MS-026 ABC Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.
7. Dashed area represents exposed paddle for e-PAD Packages only.
   - See leadframe drawing for e-Pad dimension.
   - Metal area of exposed die pad shall be within 0.30mm of nominal pad size.

This drawing supersedes 418/ED/51612/002 (Swindon)

ISSUE	1	2	3	4
ACN	201365	207083	208007	212441
DATE	28Oct96	6Jul99	14Dec99	25Mar02
APPRD.				

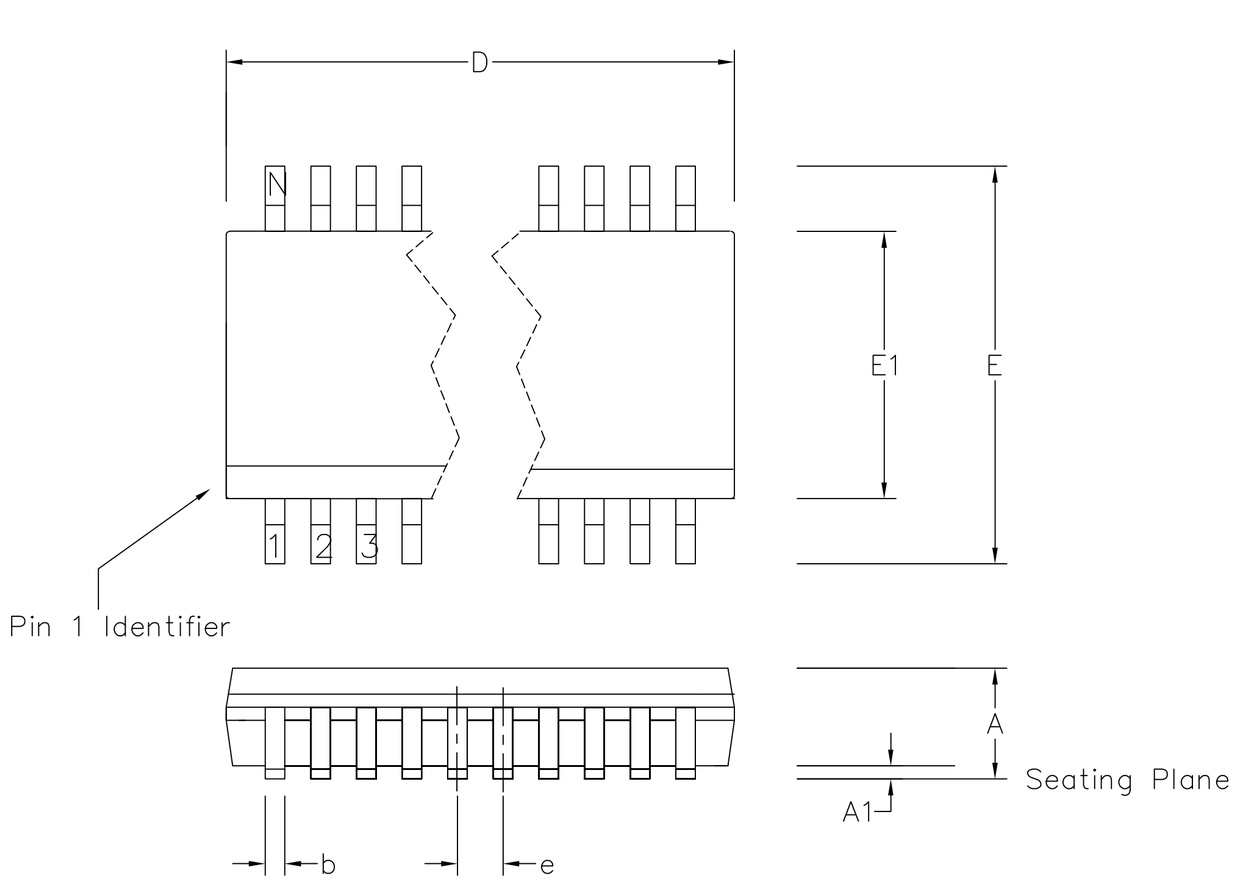
ZARLINK SEMICONDUCTOR

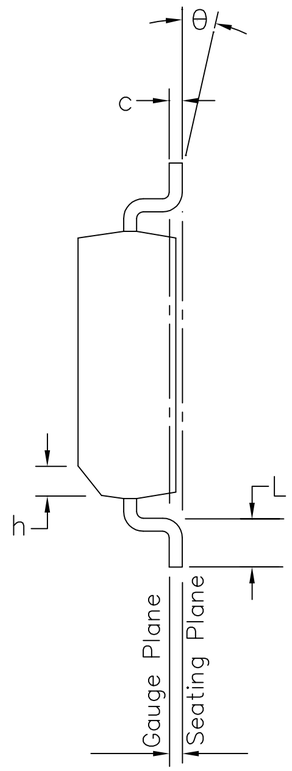
Previous package codes
TP / TH / F

Package Code QD

Package Outline for 48 lead TQFP / E-Pad TQFP (7x7x1.0mm) 2.0mm Footprint

GPD00249





Symbol	Altern. Dimensions in inches		Control Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.096	0.104	2.44	2.64
A1	0.004	0.012	0.10	0.30
D	0.598	0.612	15.20	15.40
E1	0.291	0.299	7.40	7.60
E	0.398	0.414	10.11	10.51
L	0.016	0.050	0.40	1.27
e	0.0315 BSC.		0.80 BSC.	
b	0.011	0.020	0.28	0.51
c	0.009	0.013	0.23	0.32
θ	0°	8°	0°	8°
h	0.018	0.0216	0.45	0.55
	Pin features			
N	36			
NON JEDEC STANDARD DRAWING				

Notes:
1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located at pin 1 position.
2. Controlling dimensions are in millimeters
3. D & E1 do not include mould flash or protrusion. But do include mold mismatch.
4. Dimension E1 does not include inter-lead flash or protrusion.
5. Dimension b does not include dambar protrusion/intrusion.
6. Not to Scale

ISSUE	1			
ACN				
DATE	09-02-04			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Q

Package Code DG

Package Outline for 36 lead QSOP, 300 mil (7.5mm) Body width

103461

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE