Timberwolf Digital Signal Processor family, powered by *AcuEdge*™ Technology

Advanced Multi-Channel Super Wideband Audio Processor

ZL38042

Preliminary Data Sheet

Description

The ZL38042 is part of Microsemi's new Timberwolf audio processor family of products that feature the company's innovative *AcuEdge* acoustic technology, which is a set of highly-complex and integrated algorithms. These algorithms are incorporated into a powerful DSP platform that allow the user to extract intelligible information from the audio environment from which they are communicating.

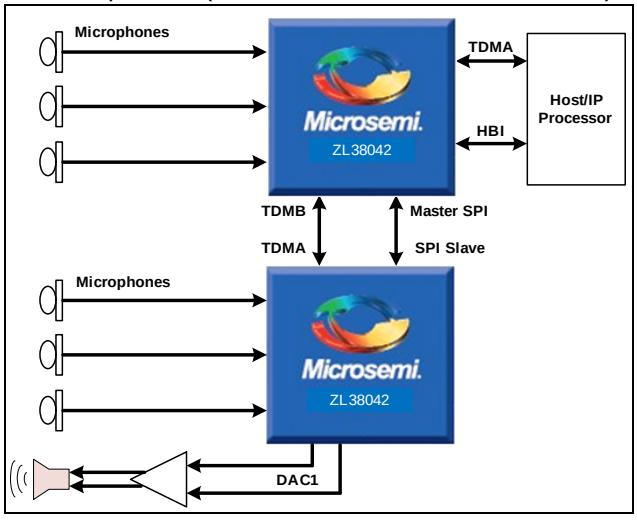
The ZL38042 device supports 4 digital microphones and provides advanced Acoustic Echo Cancellation (AEC) and non-stationary Noise Reduction (NR) for up to 3 parallel microphone paths for Super Wideband conference phone applications. For additional mics, a ZL38042 device can be configured as a master to control up to 4 slave ZL38042 devices.

The Microsemi *AcuEdge* Technology license-free, royalty-free intelligent audio Firmware provides AEC, NR and a variety of other voice enhancements to improve both the intelligibility and subjective quality of voice in harsh acoustic environments.

The *MiTuner*™ Automatic Tuning Kit and ZLS38508 *MiTuner* GUI provide automatic tuning and easy control for manual fine tuning adjustments. Further, the ZLS38508 *MiTuner* GUI provides easy graphical control of the various interconnections required to meet the needs of your application.

Applications

- Wideband Conference phone with satellite microphones (one slave ZL38042 shown below)



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Ordering Information

Device OPN	Package	Packing
ZL38042LDF1	64-pin QFN (9x9)	Tape & Reel
ZL38042LDG1	64-pin QFN (9x9)	Tray

These packages meet RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

Microsemi *AcuEdge* Technology ZLS38042 Firmware

- Super Wideband, Wideband and Narrowband Acoustic Echo Cancellation (of 3 microphone paths simultaneously)
- Up to 15 microphones can be supported by using multiple ZL38042 devices
- Full or Half duplex operation
- AEC supports long tail length:
  - 256 ms for Narrowband and Wideband
  - 170 ms for Super Wideband
- Howling detection/cancellation
  - Prevents oscillation in the AEC audio paths
- Audio Compressor/Limiter/Expander
- Non-linear echo cancellation provides higher tolerance for speaker distortions
- Advanced noise reduction reduces background noise from the near-end speech signal
- Provisions for 48 kHz stereo audio mixing and stereo music record and playback with 8/16/24 kHz voice processing
- Continuous double talk convergence
- Comfort noise generation
- Programmable tone generation (DTMF)
- Various encoding/decoding options:
  - 16-bit linear
  - G.722
  - G.711 A/μ law
- Send and receive path 8-band parametric equalizers
- 48 kHz bypass mode
- Configurable Cross-Point Switch

ZL38042 Hardware Features

- DSP with Voice Hardware Accelerators
- Dual ΔΣ 16-bit digital-to-analog converters (DAC)
  - Sampling up to 48 kHz and internal output drivers
  - Headphone amps capable of 4 single-ended or 2 differential outputs
  - 32 mW output drive power into 16 ohms
  - Impulse pop/click protection
- 2 Digital Microphone inputs supporting up to 4 Microphones on a single ZL38042 device
- 2 TDM ports supporting PCM or Inter-IC Sound (I^2S)
  - Each port provides sample rate conversion and synchronous TDM bus operation
- SPI Slave port for host processor interface
- Master SPI port for serial Flash interface
- 14 General Purpose Input/Output (GPIO) pins
- General purpose UART port
- Boots from SPI, UART, or Flash allowing easy firmware updates
- Ultra-low power and Reset operation mode power

Performance

- 3 AEC channels, Tail Length:
  - 256 ms in Narrowband and Wideband modes
  - 170 ms in Super Wideband mode
- AEC sampling rates: 8 kHz, 16 kHz, and 24 kHz
- Single Talk TCLw: > 60 dB
- Double Talk TCLw: > 40 dB
- Double Talk Attenuation: < 3 dB
- Non-stationary noise reduction up to 30 dB

The *MiTuner*™ Automatic Tuning Kit and ZLS38508 MiTuner GUI

Microsemi's *MiTuner* kit provides hardware, software and support for the automatic tuning of Microsemi's *AcuEdge* Technology audio processors.

Features include:

- Auto tuner allows user to automatically tune key parameters of the system
- Visual representation of the audio paths allow variations in the audio routing configuration
- Visual representation of the key building blocks in the transmit (Tx) and receive (Rx) audio paths with drop-down menus to program block parameters
- Set the analog and digital gains
- Configure parameters allows users to “fine tune” the performance

Tools

- ZLE38000 Evaluation Kit
- *MiTuner*™ Automatic Tuning Kit
- *MiTuner*™ ZLS38508 and ZLS38508LITE GUI

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1.0 Overview

The Microsemi *AcuEdge*™ Technology ZL38042 is an advanced audio processing device with peripherals and interfaces tuned for multi-microphone conference phones. The ZL38042 will automatically switch between each microphone to provide a low noise path to users situated at different places in a room. The microphones may be fixed in a single unit or may be mobile and tethered only by a cable.

Additionally, ZL38042 devices are configured to operate in a slave and master mode where up to four slave ZL38042 devices may be interconnected to a ZL38042 master, allowing for more than three microphones in a system. The connected devices act as one device, allowing a single Flash loading of the system.

The Microsemi *AcuEdge*™ Technology ZLS38042 Firmware offers a sophisticated audio compressor/limiter/ expander with adjustable attack and decay time. Three microphone audio paths may be routed to the voice processing algorithms for simultaneous AEC processing. The ZL38042 provides super wideband (>10 kHz bandwidth) communication which utilizes a sampling rate of 24 kHz.

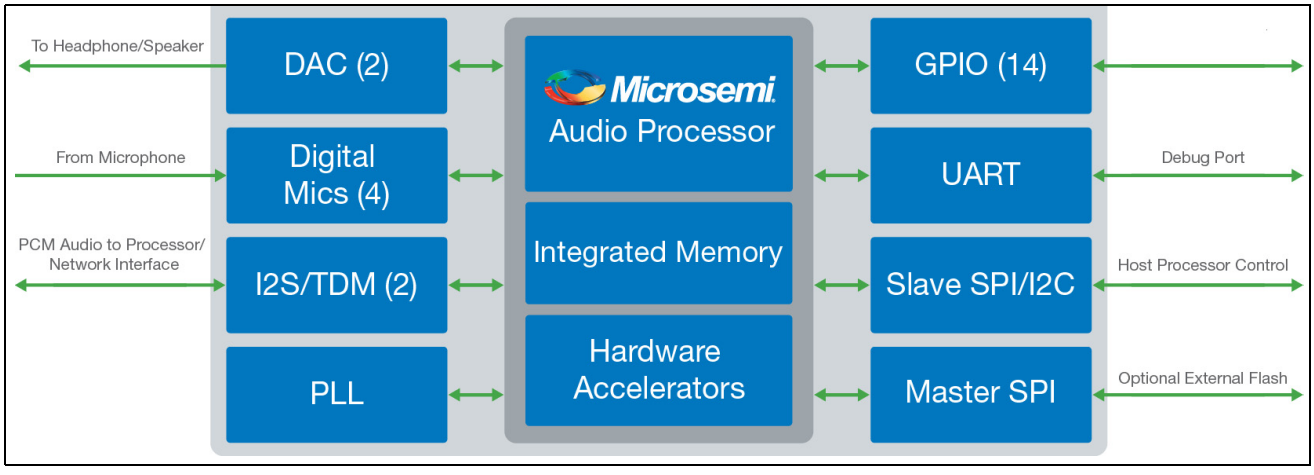


Figure 1 - ZL38042 Advanced Multi-Channel Super Wideband Audio Processor Block Diagram

2.0 Analog Interfaces

The ZL38042 provides the following peripheral analog ports:

- 2 digital microphone interfaces allowing sampling of up to 4 digital microphones
- 2 independent headphone drivers
  - Dual 16-bit digital-to-analog converters (DACs)
  - 16 ohms single-ended or differential drive capability
  - 32 mW output drive power into 16 ohms

2.1 Digital Microphone Interface

The ZL38042 can support up to four digital microphones using the DMIC_CLK, DMIC_IN1, and DMIC_IN2 interface pins. The ZL38042 digital microphone clock output is variable depending on the selected data rate. Selecting an 8 kHz or 16 kHz data rate corresponds to a 1.024 MHz digital microphone clock. Selecting the super wideband 24 kHz data rate corresponds to a 1.536 MHz digital microphone clock. Selecting a 48 kHz data rate corresponds to a 3.072 MHz digital microphone clock.

AEC can be performed on up to three microphones selected to go to the ZL38042 voice processing section. Alternatively, the microphones may be routed to the TDM bus for use by the host or an external Codec.

Electret condenser microphones can be used with the digital microphone interface by using a Digital Electret Microphone Pre-Amplifier device as shown in Figure 35. External Codecs can also be used to connect to analog microphones via the TDM buses.

See "Digital Microphone Interface" on page 50 for digital microphone connections.

2.2 Headphone Output

The ZL38042 has two 16-bit fully differential delta-sigma digital-to-analog converters. The two output DACs independently drive an analog output subsystem. Each subsystem is able to drive two output pins, representing four independent single-ended headphone outputs that can be driven by two independent data streams.

The output pins can be independently configured as shown in "Output Driver Interface" on page 52. Four analog gains on each headphone output are provided and can be set to: 1x, 0.5x, 0.333x, and 0.25x.

The headphone amplifiers are self-protecting so that a direct short from the output to ground or a direct short across the terminals does not damage the device.

The ZL38042 provides audible pop suppression which eliminates pop noise in the headphone earpiece when the device is powered on/off or when the device channel configurations are changed. This is especially important when driving a headphone single-ended through an external capacitor. The external coupling capacitor value can vary from 10 µf to 470 µf depending on the type of earpiece used and the frequency response desired.

The DACs and headphone amplifiers will be powered down if they are not required for a given application.

3.0 Digital Interfaces

The ZL38042 provides the following peripheral digital ports:

- SPI – The device provides 2 Serial Peripheral Interface (SPI) ports
  - The SPI Slave port can be used as the main communication port with a host processor, and can be used to download the device's firmware
  - The Master SPI port can be used to boot load the devices' firmware from an external Flash, or it can be used by the master ZL38042 to boot load and control additional ZL38042 devices configured as slaves
- I^2C - The device provides an Inter-Integrated Circuit (I^2C) port. (pins are shared with the SPI Slave port)
  - The I^2C port can be used as the main communication port with a host processor, and can be used to download the device's firmware
- TDM – The device provides 2 Time-Division Multiplexing buses (TDM-A and TDM-B)
  - The ports can be configured for Pulse-Code Modulation (PCM) or Inter-IC Sound (I^2S) operation
  - TDM-A supports up to four bi-directional streams when configured in PCM mode or two bi-directional streams when configured for I^2S mode at frequencies up to 6.144 MHz
  - TDM-B is used by the master ZL38042 to interconnect with the slave ZL38042 devices via their TDMA interface
  - Sample rate conversions are automatically done when data is sent/received at different rates than is processed internally
- UART – The device provides a Universal Asynchronous Receiver/Transmitter (UART) port
  - The UART port can be used as a debug tool, a booting option, and/or as the host control interface operating at 115.2K baud
- GPIO – The device provides 14 General Purpose Input/Output (GPIO) ports
  - GPIO ports can be used for interrupt and event reporting, bootstrap options, as well as being used for general purpose I/O for communication and controlling external devices. Certain GPIO pins have dedicated functions based on your configuration, and other GPIO ports are used as chip selects when using slave and master mode.

3.1 ZL38042 Slave and Master Mode Operation

The ZL38042 devices can be operated as a slave or as a master device. The ZL38042 device which is controlled by the host can control between one to four slave ZL38042 devices.

Control of four slave devices is illustrated in Figure 2. GPIO_3 through GPIO_6 of the master device are used as chip selects for the slave devices. If less than 4 slave devices are used, the unused GPIO are free for general I/O use.

The 3.3 Kohm pull-up on GPIO_3 defines the ZL38042 device as the master. The 3.3 Kohm pull-ups on GPIO_4, GPIO_5, and GPIO_6 of the slave ZL38042 devices define its slave number (using boolean algebra).

If a Flash memory device is used, it is tied to the Master SPI of the master ZL38042 device.

To make provisions for Audio Interface Box (AIB) use, wire the AIB connector to the TDMA port of the master ZL38042 device. The host control lines should be high impedance or disconnected when using the AIB.

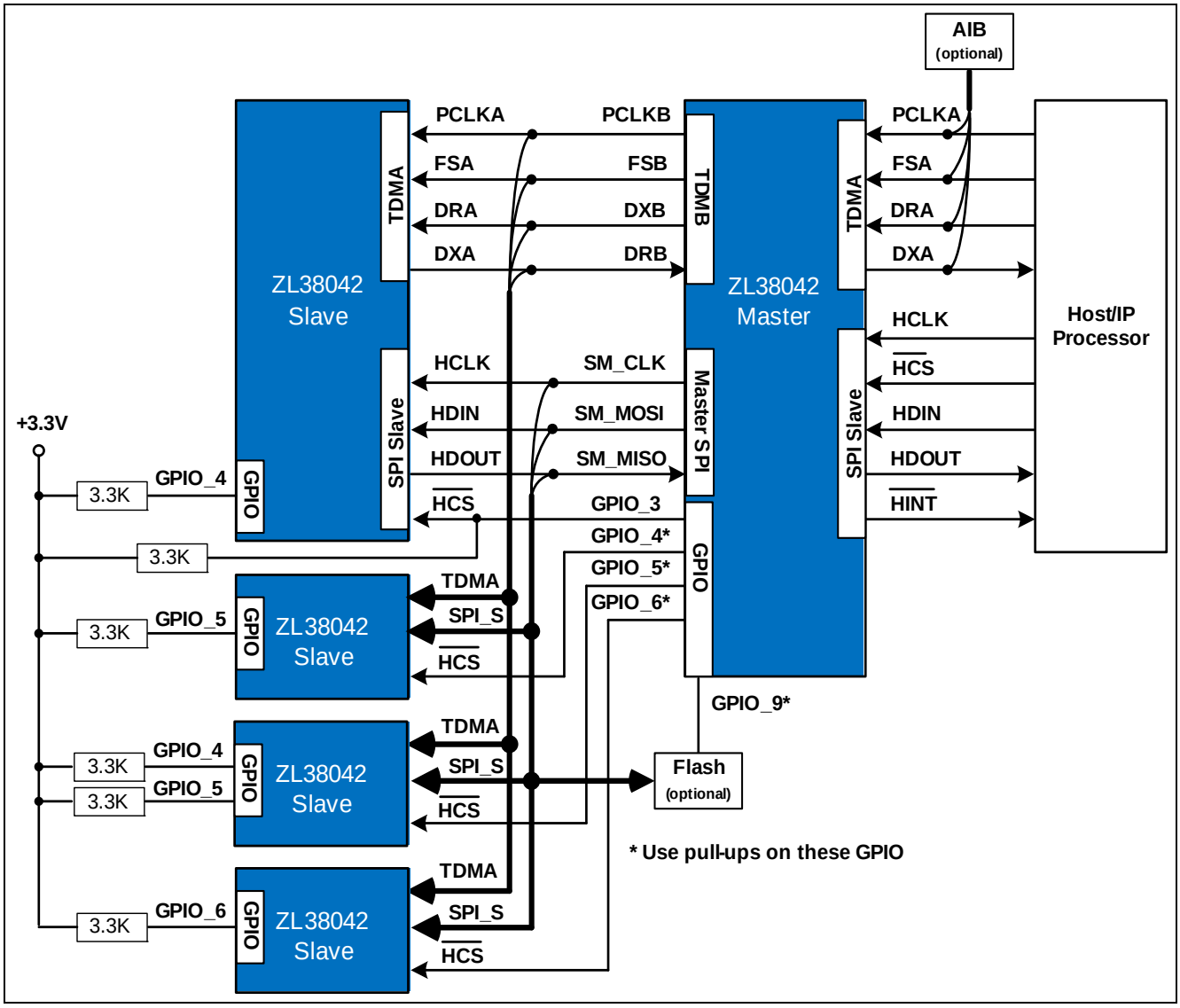


Figure 2 - ZL38042 Slave and Master Mode Operation

3.2 TDM Interface

The ZL38042 device has two TDM interfaces, TDM-A and TDM-B. The TDM-A block is capable of being a master or a slave and supports up to four bi-directional input and output streams. The TDM-B block is used to control other ZL38042 devices when using slave and master mode. TDM-B can also be configured as a PCM highway, I^2S, GCI, as well as a variety of specialized configurations for talking to external codecs.

The TDM interface supports bit reversal (LSB first <– –> MSB first) and loopbacks within the TDM interface and from one interface to another (see "Input Cross-Point Switch" on page 17).

The ZL38042 firmware supports up to four simultaneous channels (bi-directional) on the TDM-A port. Each of the TDM channels can be assigned an independent timeslot. The timeslots can be any 8-bit timeslot up to the maximum supported by the PCLK rate being used. Each timeslot can be configured for A-law/µ-Law or linear PCM or G.722 encoding. Linear PCM will be sent on consecutive timeslots (e.g. N, programmed in the timeslot registers, and N+1 or N+2). The PCM interface can transmit/receive 8-bit compressed with 8 kHz sampling (narrowband), or 16-bit linear data with 16 kHz sampling (wideband), or 16-bit linear data with 24 kHz sampling (super wideband).

Wideband audio usually means the TDM bus is operating at a 16 kHz frame sync (FS), but there are two other operating modes that support wideband audio using an 8 kHz FS:

- G.722 supports wideband audio with an 8 kHz FS. This uses a single 8-bit timeslot on the TDM bus.
- "Half-FS Mode" supports wideband audio with an 8 kHz FS signal. In this mode, 16-bit linear audio is received on two timeslot pairs; the first at the specified timeslot (N,N+1) and the second a half-frame later. In total, four 8-bit timeslots are used per frame, timeslots (N, N+1) and ((N + ((bits_per_frame)/16)), (N + 1 + ((bits_per_frame)/16))). The user programs the first timeslot and the second grouping is generated automatically 125/2 µs from the first timeslot.

Table 1 shows a list of allowable TDM-A configurations when the ZL38042 is a master device and TDM-A operates as a slave port.

Case	Crystal	TDM-A Eminence	TDM-A FS Rate (kHz)	TDM-A PCLK Rates (MHz)	TDM-A Direction
1	Yes	Slave	8, 16, 24	0.128, 0.256, 0.512. 1.024, 2.048, 4.096, 8.192	In/Out
2	Yes	Slave	48	1.536, 3.072, 6.144	In/Out

Table 1 - TDM-A Configurations when Operating as a Slave Port

A single ZL38042 device can accommodate 3 mics. If only 3 mics are required, the ZL38042 TDM-B port can be configured as a master port with functionality as shown in Table 2.

When more than 3 mics are used, the TDM-B port of the ZL38042 master is used as an interconnect to slave ZL38042 device(s). TDM-B on the first slave device can then be configured as the master port with functionality as shown in Table 2.

Case	Crystal	TDM-B Eminence	TDM-B FS Rate (kHz)	TDM-B PCLK Rates (MHz)	TDM-B Direction
1	Yes	Master	8, 16, 24	0.128, 0.256, 0.512. 1.024, 2.048, 4.096, 8.192	In/Out
2	Yes	Master	48	1.536, 3.072, 6.144	In/Out

Table 2 - TDM-B Configurations when Operating as a Master Port

The TDM interface supports a variety of interface and timing options, as follows:

- GCI mode or I^2S Left-Justified mode – First data bits are aligned with the rising edge of the frame sync pulse
- PCM mode with PCM transmit on negative edge (XEDX = 0) – First output data bit aligned with a ½ clock cycle delay from the frame sync pulse, first input data bit aligned with a 1 clock cycle delay from the frame sync pulse
- PCM mode with PCM transmit on positive edge (XEDX = 1) or normal I^2S interface mode – First data bits are aligned with a 1 clock cycle delay from the frame sync pulse

Note: Using the clock slot delay, up to 7 clock cycles of delay can be realized.

3.2.1 GCI Mode

The GCI voice/data bytes can occupy any of the available timeslots. The GCI block can be configured as a master or a slave and supports a clock that has the same frequency as the data rate.

Note: Traditional GCI Monitor, Signalling, and Control channel bytes and double data rate are not supported.

Figure 3 illustrates the GCI format with slave timing, FS and PCLK are provided by the host. Slave mode accommodates frame sync pulses with various widths (see "GCI and PCM Timing Parameters" on page 37).

Figure 4 illustrates the GCI format with master timing, FS and PCLK are provided by the ZL38042. Master mode outputs a frame sync pulse equal to one PCLK cycle.

For both, first data bits are aligned with the rising edge of the frame sync pulse.

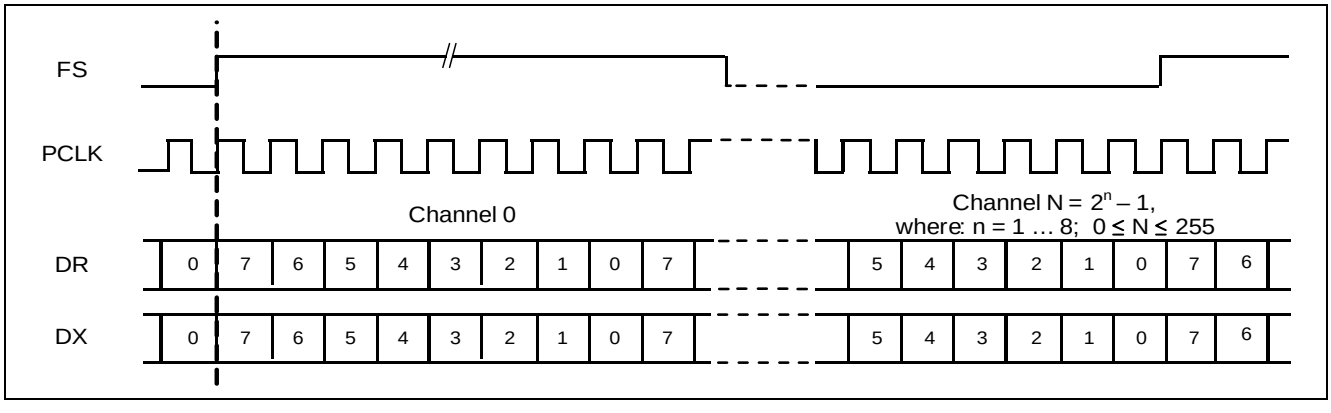


Figure 3 - TDM – GCI Slave Functional Timing Diagram

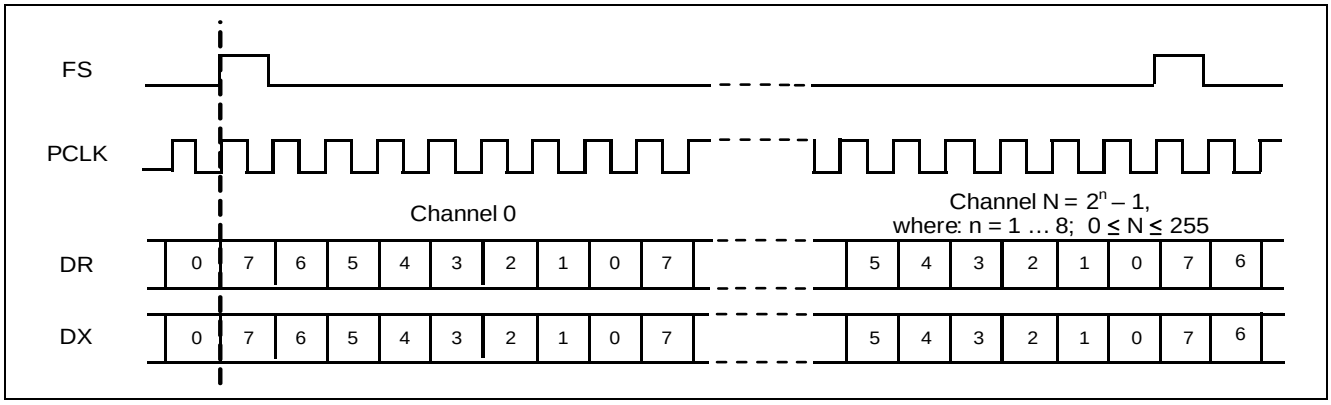


Figure 4 - TDM – GCI Master Functional Timing Diagram

3.2.2 PCM Mode

The PCM voice/data bytes can occupy any of the available timeslots. The PCM block can be configured as a master or a slave and is compatible with the Texas Instruments Inc. McBSP mode timing format.

Figure 5 and Figure 6 illustrate the PCM format with slave timing, FS and PCLK are provided by the host. Slave mode accommodates frame sync pulses with various widths (see "GCI and PCM Timing Parameters" on page 37).

Figure 7 and Figure 8 illustrate the PCM format with master timing, FS and PCLK are provided by the ZL38042. Master mode outputs a frame sync pulse equal to one PCLK cycle.

Diagrams for PCM transmit on negative edge (XEDX = 0) and PCM transmit on positive edge (XEDX = 1) are shown for both slave and master timing.

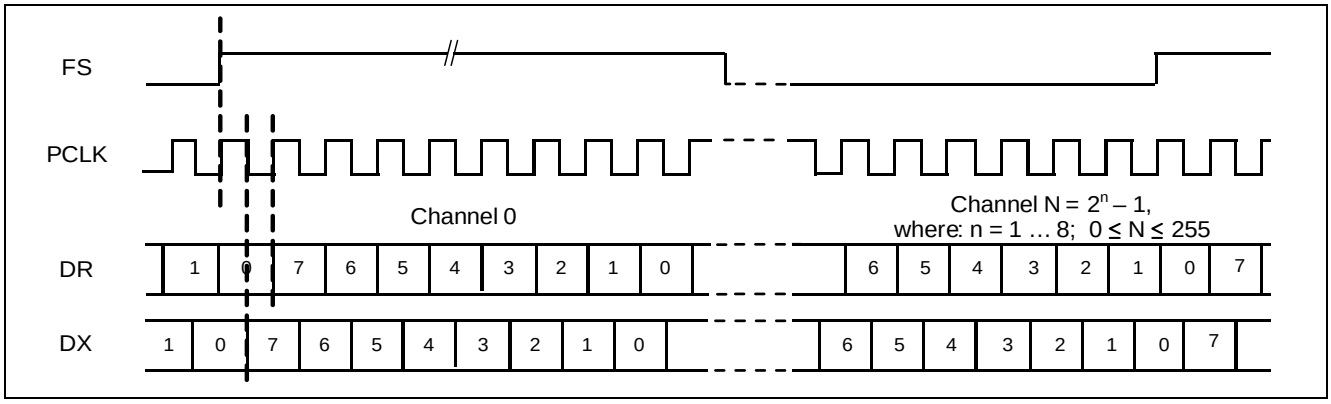


Figure 5 - TDM – PCM Slave Functional Timing Diagram (8-bit, XEDX = 0)

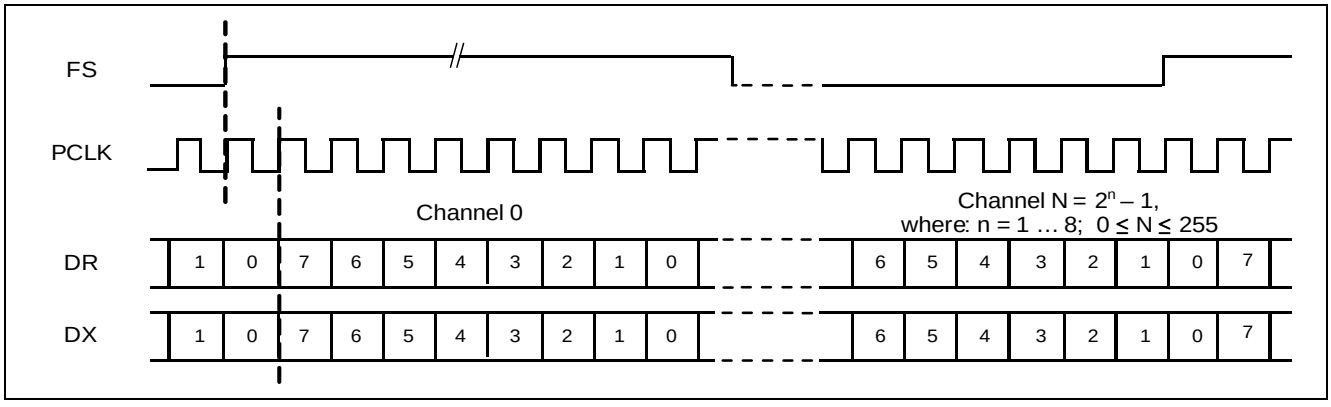


Figure 6 - TDM – PCM Slave Functional Timing Diagram (8-bit, XEDX = 1)

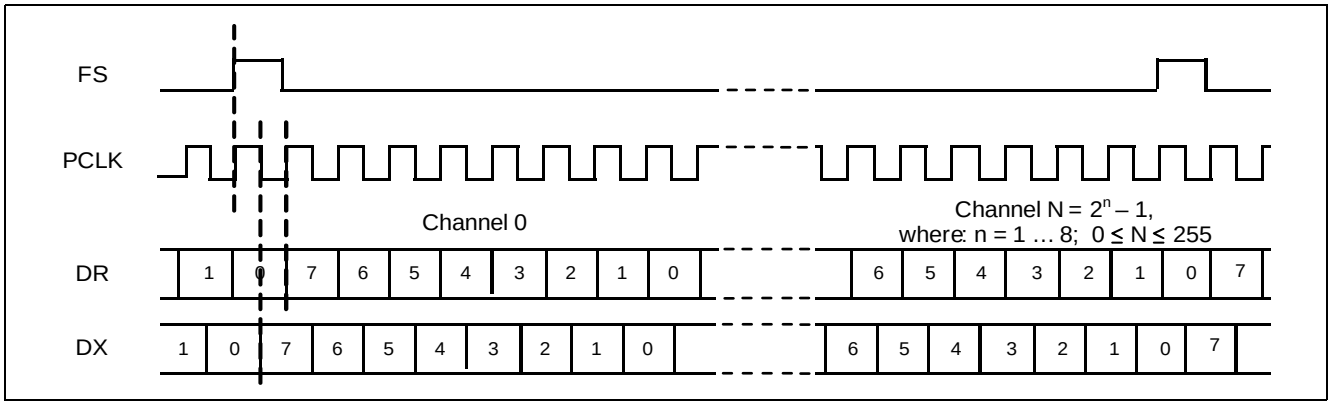


Figure 7 - TDM – PCM Master Functional Timing Diagram (8-bit, XEDX = 0)

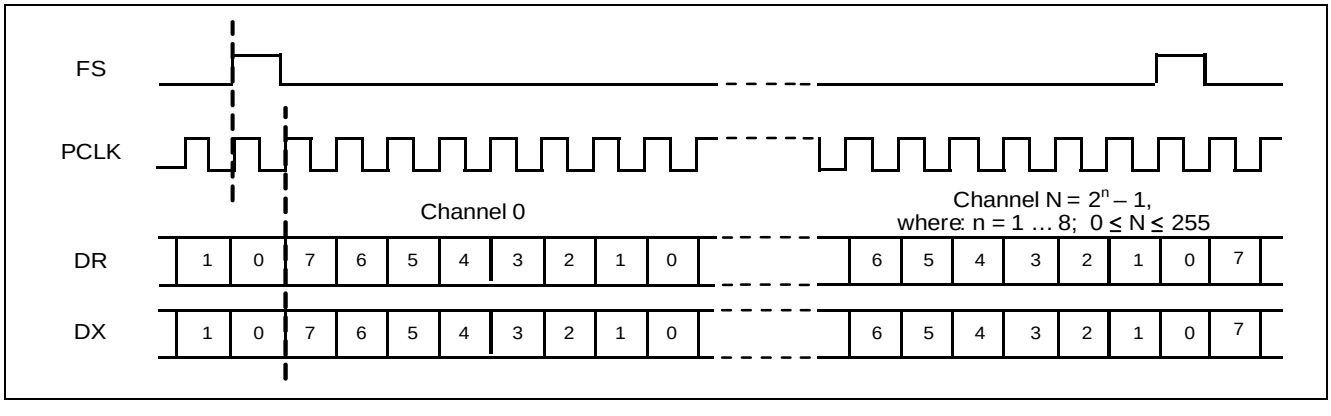


Figure 8 - TDM – PCM Master Functional Timing Diagram (8-bit, XEDX = 1)

3.2.3 I²S Interface

The I²S bus is a sub-mode of the very flexible TDM bus. In I²S mode, the 4-wire TDM port conforms to the I²S protocol and the port pins become I2S_SCK, I2S_WS, I2S_SDI, and I2S_SDO (refer to Table 10 for pin definitions). Both TDM buses have I²S capability.

An I²S bus supports two bi-directional data streams, left and right channel, by using the send and receive data pins utilizing the common clock and word signals. The send data is transmitted on the I2S_SDO line and the receive data is received on the I2S_SDI line.

The TDM-B I²S port on the first slave device can be used to connect external analog-to-digital converters or Codecs. The port can operate in master mode where the ZL38042 is the source of the port clocks.

The I²S ports operate at 8, 16, 24, and 48 kHz sampling rates as a master or a slave.

The I²S port operates in two frame alignment modes (I²S and left justified) which determine the data start in relation to the word select line. The serial data streams (SD) can be inputs or outputs. Per the I²S standard, the WS line is output using a 50% duty cycle.

Note: Right justified mode, where the data is padded with zeroes before the data, is not supported.

Figure 9 illustrates the I²S mode, which is left channel first associated with I2S_WS (Left/Right Clock signal) low, followed by the right channel associated with I2S_WS high. The MSB of the data is clocked out starting on the second falling edge of I2S_SCK following the I2S_WS transition and clocked in starting on the second rising edge of I2S_SCK following the I2S_WS transition. See the *Microsemi AcuEdge™ Technology ZLS38042 Firmware Manual* for I²S port setup.

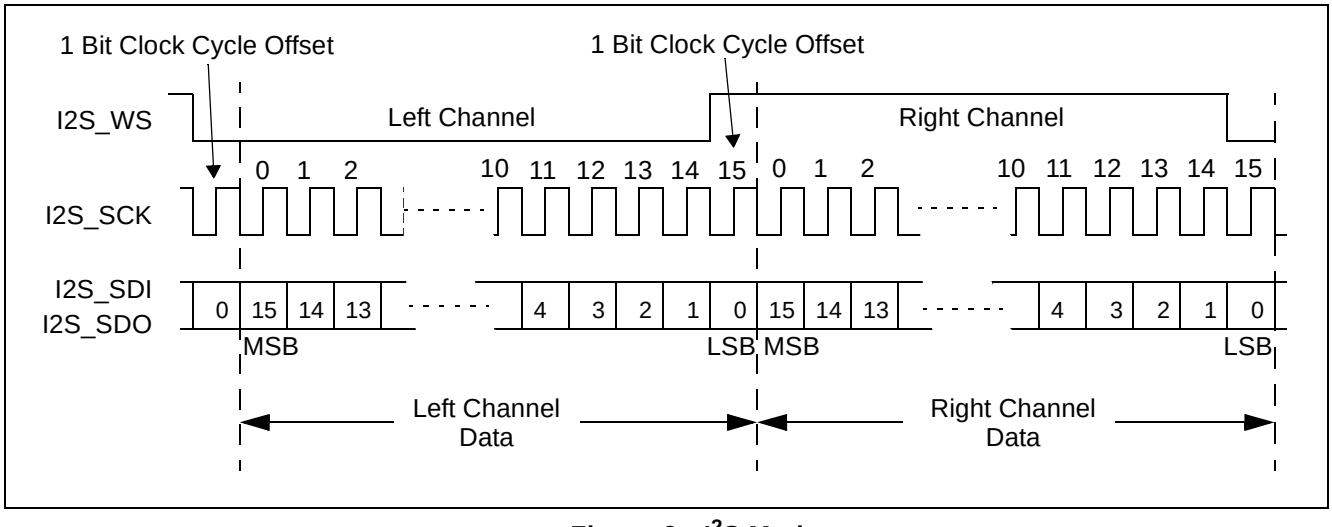


Figure 9 - I²S Mode

Figure 10 illustrates the left justified mode, which is left channel first associated with I2S_WS (Left/Right Clock signal) high, followed by the right channel associated with I2S_WS low. The MSB of the data is clocked out starting on the falling edge of I2S_SCK associated with the I2S_WS transition, and clocked in starting on the first rising edge of I2S_SCK following the I2S_WS transition. See the *Microsemi AcuEdge™ Technology ZLS38042 Firmware Manual* for I²S port setup.

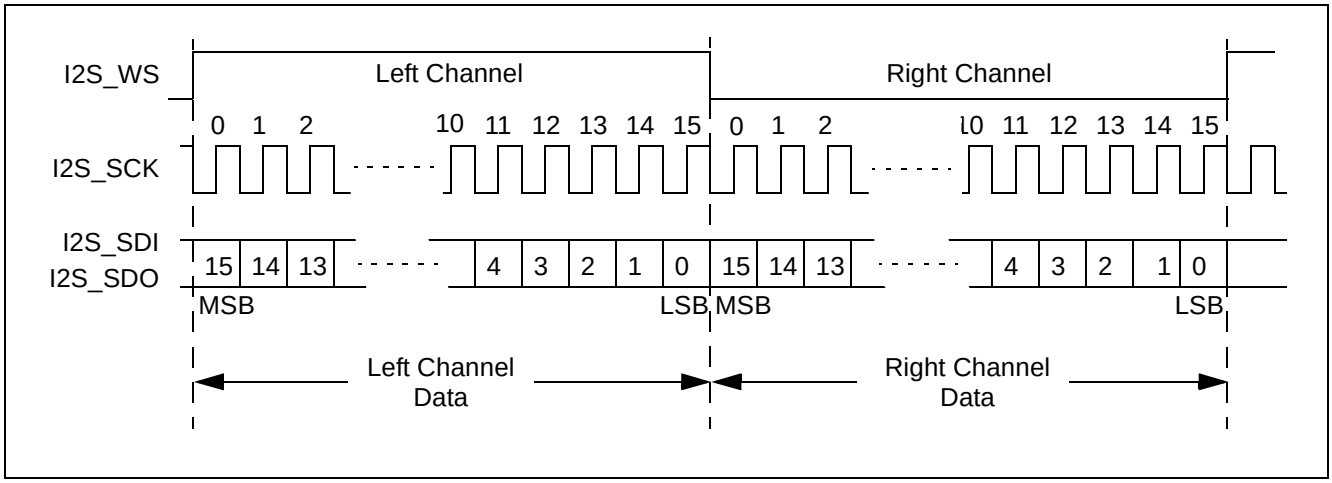


Figure 10 - Left Justified Mode

Each I^2S interface can support one dual channel Codec (Figure 11). The four 16-bit channel processing capacity of the DSP is spread across the two input channels from the ADCs of Codec(0) and Codec(1), and the two output channels to the DACs of Codec(0) and Codec(1). See the *Microsemi AcuEdge™ Technology ZLS38042 Firmware Manual* for I^2S port setup.

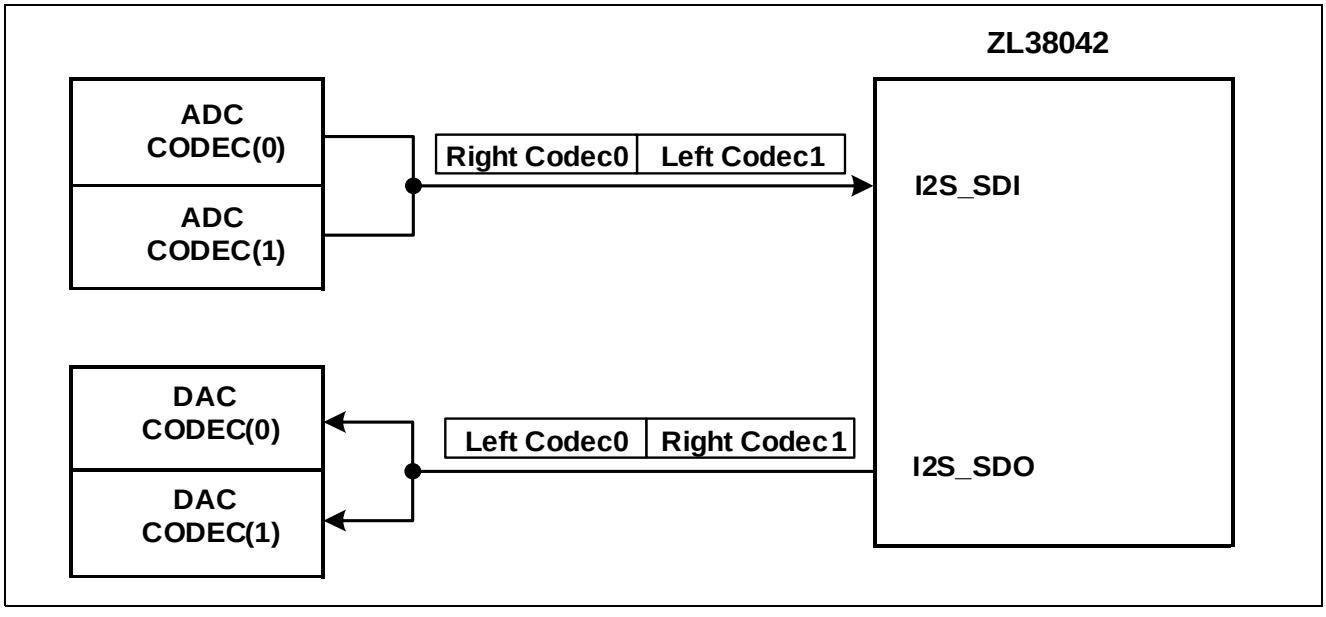


Figure 11 - Dual Codec Configuration

Both I^2S bus modes can support full bi-directional stereo communication.

The device supports I^2S loopback. See the *Microsemi AcuEdge™ Technology ZLS38042 Firmware Manual* for configuration details.

3.3 Input Cross-Point Switch

The ZL38042 contains a Cross-Point Switch that allows any of the various timeslots of the TDM buses to be routed to various paths and connection points in the signal processing chain. All timeslots in each TDM bus can be routed to all other timeslots within that bus. Furthermore, when both TDM buses are running at the same frame sync speed, all timeslots from one TDM bus can be routed to all timeslots of the other bus.

The Cross-Point Switch allows each TDM bus to connect to the receive path signal processing chain for echo cancellation, equalization, etc. at a 16 kHz sampling rate. The signal processing chain can also be bypassed and the TDM data can be routed straight to the DAC at either 8 kHz or 16 kHz sampling rates. Additionally, the send channel signal processing chain and decimated microphone data can be routed to the TDM at 8 kHz and 16 kHz sampling rates. The Cross-Point Switch provides the ability to use an external Codec as the acoustic front end.

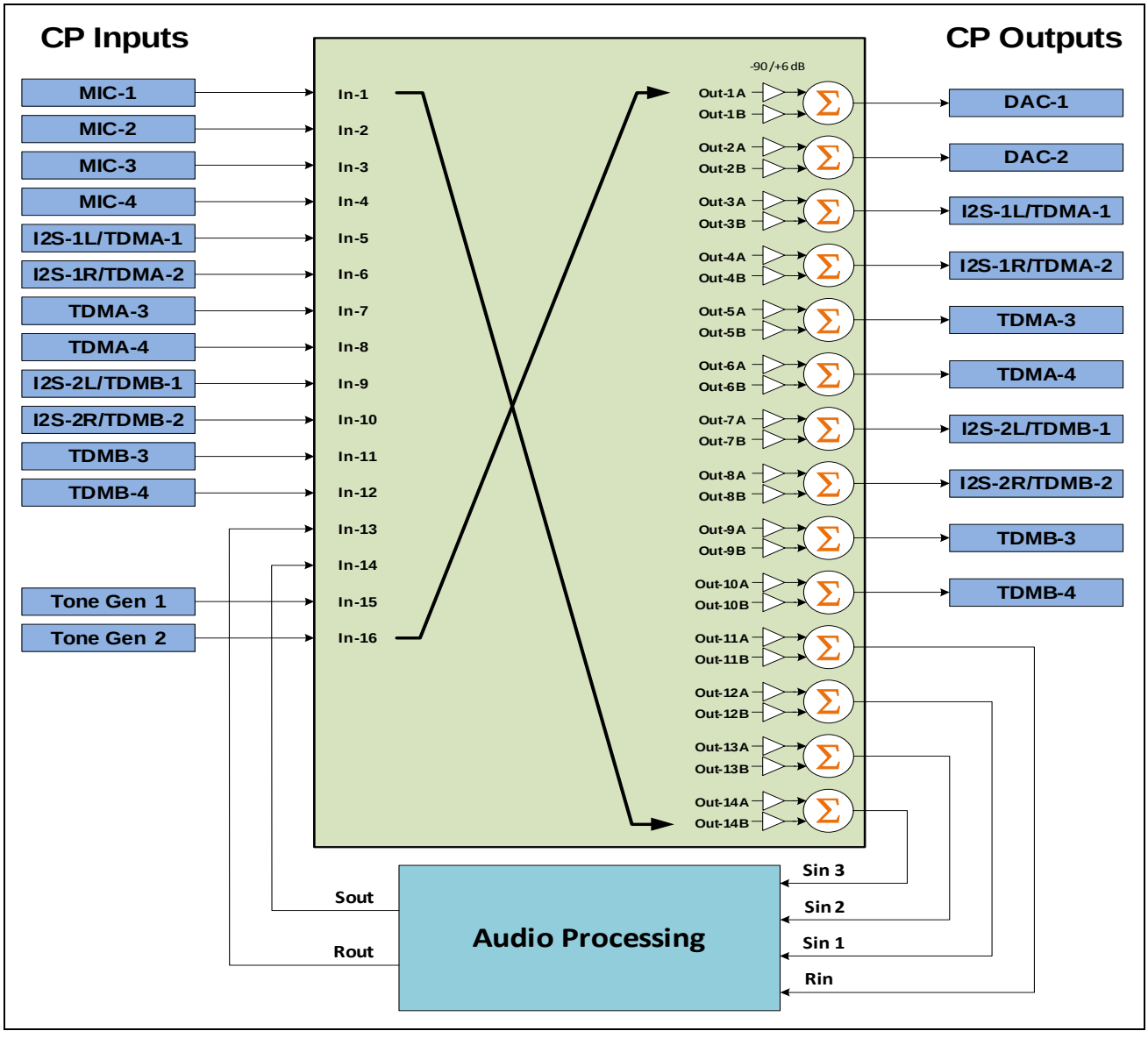


Figure 12 - Cross-Point Switch

3.4 Host Bus Interface

The host bus interface (HBI) is the main communication port from a host processor to the ZL38042. It can be configured to be either a SPI slave or a I^2C slave port, either of which can be used to program or query the device.

The ZL38042 allows for automatic configuration between SPI and I^2C operation. For the HBI port, if the HCLK toggles for two cycles, the HBI will default to the SPI Slave, otherwise it will remain configured as I^2C (see Table 3). The HBI comes up listening in both SPI and I^2C modes, but with I^2C inputs selected. If HCLK is present, it switches the data selection before the first byte is complete so that no bits are lost. Once the port is determined to be SPI, a hardware reset is needed to change back to I^2C.

This port can read and write all of the memory and registers on the ZL38042. Refer to the *Microsemi AcuEdge™ Technology ZLS38042 Firmware Manual* for proper configuration of the HBI.

Description	Condition	Operating Mode	Notes
HBI Slave interface selection.	HCLK toggling	Host SPI bus	
	HDIN tied to VSS	Host I^2C bus. Slave address 45h (7-bit).	1
	HDIN tied to DVDD33	Host I^2C bus. Slave address 52h (7-bit).	

Table 3 - HBI Slave Interface Selection

Note 1: By default, the HBI comes up as an I^2C interface. Toggling the HCLK pin will cause the host interface to switch to a SPI interface. If an I^2C interface is desired, HCLK needs to be tied to ground.

3.4.1 SPI Slave

The physical layer is a 4-wire SPI interface. Chip select and clock are both inputs. The SPI Slave port can support byte, word, or command framing. The outbound interrupt can be configured to be open drain or actively driven. In either mode, the signal is active low. The SPI Slave chip select polarity, clock polarity, and sampling phase are fixed.

The ZL38042 command protocol is half duplex, allowing the serial in and serial out to be shorted together for a 3-wire connection. The chip select is active low. The data is output on the falling edge of the clock and sampled on the rising edge of the clock.

The SPI Slave supports access rates up to 25 MHz.

3.4.2 I^2C Slave

The I^2C bus is similar to the Philips Semiconductor (NXP) 1998 Version 2.0, I^2C standard. The ZL38042 I^2C bus supports 7-bit addressing and transfer rates up to 400 kHz. External pull-up resistors are required on I2C_SCLK and I2C_SDA when operating in this mode (note, the I^2C slave pins are 3.3 V pins and are not 5 V tolerant).

The selection of the I^2C slave address is performed at bootup by the strapping of the HDIN and HCLK pins, see Table 3.

3.4.3 UART

The ZL38042 device incorporates a two-wire UART (Universal Asynchronous Receiver Transmitter) interface with transfer rates up to 115.2K baud. TX and RX pins allow bi-directional communication with a host. The UART is primarily used as a debug port during system development, but can be used as the host processor interface instead of the SPI Slave or I^2C port.

The UART port may be used by an external host microprocessor to Read/Write the ZL38042's internal control/status registers. The ZL38042 will set up the initial parameters of this port (i.e., baud rate, stop bits, parity bit etc.) during the boot process.

The UART pins should be made accessible on the PCB in case they are required for debug purposes.

3.4.4 Host Interrupt Pin

An internal host interrupt controller controls the active low interrupt pin which is part of the host bus interface. Associated with the interrupt controller is an event queue which reports status information about which event caused the interrupts.

The events listed in Table 4 can cause an interrupt. Upon sensing the interrupt, the host can read the event queue to determine which event caused the interrupt. Specific events are enabled by the host processor.

Event	Interrupt Source
PLL CFAIL	Clock fail - An Interrupt is generated when the PLL goes out of lock.
PCM Highway A CFAIL	Clock fail - A clock failure has been detected on the clock source PCLKA.
PCM Highway B CFAIL	Clock fail - A clock failure has been detected on the clock source PCLKB.
Event Queue Overflow	An interrupt is generated if the event queues overflow.
Boot complete	A boot - An interrupt is sent when configured for host boot. When the device is powered up and ready to receive commands.

Table 4 - External Host Interrupt Events

The firmware is configured to send the "boot complete" event to the host – so that after a reset for any condition, the host will be notified.

The ZL38042 also has a watchdog timer. Should a watchdog event occur, the device resets and the host is notified. If operating with Flash and external Flash is selected, the ZL38042 will reboot and the host will be notified when the re-boot is complete.

3.5 Master SPI

Like the HBI SPI Slave, the physical layer of the Master SPI is a 4-wire SPI interface supporting half duplex communication. The 4-wire Master SPI port supports one chip select which is multiplexed with GPIO_9.

The ZL38042 uses the Master SPI port to communicate to an external Flash via GPIO_9 or to communicate with slave ZL38042 devices (acting as a "host" to them) via their slave SPI port.

When communicating to an external Flash, the ZL38042 can automatically read the Flash data (program code and configuration record) through this interface upon the release of reset, depending on the value of the bootstrap options. Refer to "Flash Interface" on page 49 for application information.

When acting as a host to ZL38042 slave devices, GPIO_3 – GPIO_6 are used as chip selects for the interface.

3.6 GPIO

The ZL38042 64-pin QFN package has 14 GPIO (General Purpose Input/Output) pins.

The GPIO can be individually configured as either inputs or outputs, and have associated maskable interrupts reported to the host processor through the interrupt controller and event queue. The GPIO pins are intended for low frequency signalling.

When a GPIO pin is defined as an input, the state of that pin is sampled and latched into the GPIO Read Register. A transition on a GPIO input can cause an interrupt and event to be passed to the host processor.

Certain GPIO pins are used as chip selects when using slave and master mode operation, others have special predefined functions, such as volume up/down, associated with that pin. Individual GPIO pins may also be defined as status outputs with associated enable/disable control. See the *Microsemi AcuEdge™ Technology ZLS38042 Firmware Manual* for control and status programming.

Immediately after any power-on or hardware reset the GPIO pins are defined as inputs and their state is captured in the GPIO Configuration Register. The state of this register is used to determine which options are selected for the device.

4.0 Reset

The device has a hardware reset pin ($\overline{\text{RESET}}$) that places the entire device into a known low power state. The device will perform either a digital or an analog reset depending on the duration of the reset pulse.

- Digital reset – When the reset pin is brought low for a duration of between 100 ns and 1 µs, a digital reset occurs and all device states and registers are reset by this pin.
- Analog reset –When the reset pin is brought low for a duration greater than 10 µs, both a digital and an analog reset will occur. The analog reset will deactivate the internally generated +1.2 V by shutting off the external FET and the internal PLL. Raising the reset pin high will immediately turn back on these supplies (requiring a corresponding PLL startup time).

For both digital and analog reset cases when reset is released, the device will go though its boot process and the firmware will be reloaded. If the reset had been an analog reset, then the boot process will take longer waiting for the system clocks to power back on.

GPIO sensing will occur with either type of reset.

A 10 KΩ pull-up resistor is required on the $\overline{\text{RESET}}$ pin to DVDD33 if this pin is not continuously driven.

5.0 Power Supply

5.1 Power Supply Sequencing/Power up

No special power supply sequencing is required. The +3.3 V or +1.2 V power rails can be applied in either order.

Upon power-up, the ZL38042 begins to boot and senses the external resistors on the GPIO to determine the bootstrap settings. After 3 ms, the ZL38042 digital section will become stable. The boot process then begins and takes less than 1 second to become fully operational (when auto-booting from Flash, including the time it takes to load the firmware).

In order to properly boot, the clocks to the device must be stable. This requires either the 12.000 MHz crystal or oscillator to be active, or the PCLK and frame sync of TDM-A be present and stable before the ZL38042's reset is released.

5.2 +1.2 V Power Supply

The DSP core power rail (DVDD12) requires +1.2 V to operate. Refer to "Power Supply Considerations" on page 53 in the Applications section for various supply and control options.

6.0 Device Booting

6.1 Boot Loader

The ZL38042 device contains a built-in boot-loader that gets executed after a hardware reset or when power is initially applied to the part. The Boot loader performs the following actions:

- Reads the GPIO bootstrap information and stores it in a user-accessible register
- Loads external serial Flash device contents into Program RAM, or waits for the host to load Program RAM (depending on bootstrap setting)
- Programs the ZL38042 configuration registers to their proper default values
- Jumps to Program RAM to execute the firmware (depending on bootstrap setting)
- Slave devices can have external Flash, or can be booted by the Master ZL38042

6.2 Loadable Device Code

In order for the ZL38042 to operate, it must be loaded with code that resides externally. This code can either be auto-booted from an external Flash memory through the Master SPI, or can be loaded into the ZL38042 by the host processor through the HBI or UART ports. An external resistor pull-up or an internal resistor pull-down determines which boot mode will be used.

The external code consists of two logical segments, the firmware code itself and the configuration record. The firmware is a binary image which contains all of the executable code allowing the ZL38042 to perform voice processing and establishes the user command set. The configuration record contains settings for all of the user registers and defines the power-up operation of the device.

For an application that has no host and no way of externally programming the ZL38042, the configuration record is setup so that the registers are set to their desired values for normal operation.

A GUI development tool is provided to create and modify a configuration record and create a bootable Flash image which can then be duplicated for production of the end product.

When auto-booting from a Flash device the boot sequence lasts less than 1 second. When booting through the HBI SPI/I^2C the boot time will vary depending on the host's communications speed. If boot speed is important, then SPI is recommended over I^2C.

6.3 Bootup Procedure

Valid clocks (PCLKA/FSA or a crystal or oscillator) must be present before the ZL38042 device can exit its reset state. After the reset line is released, the ZL38042's internal voltage regulator will be enabled (if the EXT_SEL pin is strapped low). Once the +1.2 V supply is established, the PLL will be also be enabled. Based on the GPIO bootstrap options, the ZL38042 will select the appropriate PLL source and system parameters and the PLL will lock to the desired operating frequency. An output prompt will be sent from the UART, an event will be placed in the event-queue and the interrupt pin pulled low to signal the host when it's OK to load boot code.

If the GPIO strapping pins indicate that the ZL38042 will auto-boot, it will begin reading data from the external Flash.

For situations where the host is loading the ZL38042, the host SPI, I^2C or UART ports can be used. The port that initiates the loading process becomes the boot master.

The ZL38042 allows for automatic configuration between SPI and I^2C operation. For the HBI port, if the HCLK toggles for two cycles, the HBI will default to the SPI Slave, otherwise it will remain configured as I^2C.

When using the HBI to boot (either as a SPI or I^2C), the host should wait at least 3 ms after reset is released and then begin polling the ZL38042 to see that it is OK to begin downloading boot code (or simply wait until the boot complete event is received). The host should not try to address the part while the part is being held in reset.

The ZL38042 does not support communication over the HBI while booting from the UART and vice-versa.

7.0 GPIO Functionality

Table 5 lists the different boot options that can be selected by using external resistors. These GPIOs have internal pull-down resistors, thereby defaulting to a 0 setting. A resistor to DVDD33 is required to select a 1 option. The external pull-up resistors must have a value of 3.3 KΩ. A GPIO with a bootstrap pull-up can be used for other functionality following the power-up boot sense process.

GPIO							Pertains to GPIO on:	Operating Mode	Description	Notes
6	5	4	3	2	1	0				
					0	0	Master or Slave device	Crystal or clock oscillator 12 MHz source (default)	Clock source	
				0				Host boot (default)	Boot source selection	1
				1				External Flash		2
			1				Master device	Master	Defines ZL38042 as a master device	3
0	0	1	0				Slave device	Slave and master	Sets ZL38042 as slave device 1	4
0	1	0	0						Sets ZL38042 as slave device 2	5
0	1	1	0						Sets ZL38042 as slave device 3	4, 5
1	0	0	0						Sets ZL38042 as slave device 4	6

0 = No connection or a pull-down resistor.

Table 5 - Bootstrap Modes

Note 1: If operating ZL38042 as a slave device in slave and master mode, set the slave device for Host boot.

Note 2: Apply a 3.3 KΩ resistor from GPIO_2 to DVDD33.

Note 3: Apply a 3.3 KΩ resistor from GPIO_3 to DVDD33. This pull-up is required for ZL38042 operation. The device is defined as a master but it can also be used standalone without any slave devices attached.

Note 4: Apply a 3.3 KΩ resistor from GPIO_4 to DVDD33.

Note 5: Apply a 3.3 KΩ resistor from GPIO_5 to DVDD33.

Note 6: Apply a 3.3 KΩ resistor from GPIO_6 to DVDD33.

7.1 Hot Key Functionality

The GPIOs can be used to generate an interrupt to the host where the host can take a predefined action as defined by the product. Additionally, if enabled, some of the GPIOs can be used to perform certain predefined functions. Refer to the *Microsemi AcuEdge™ Technology ZLS38042 Firmware Manual*.

8.0 Device Pinout - 64-Pin QFN

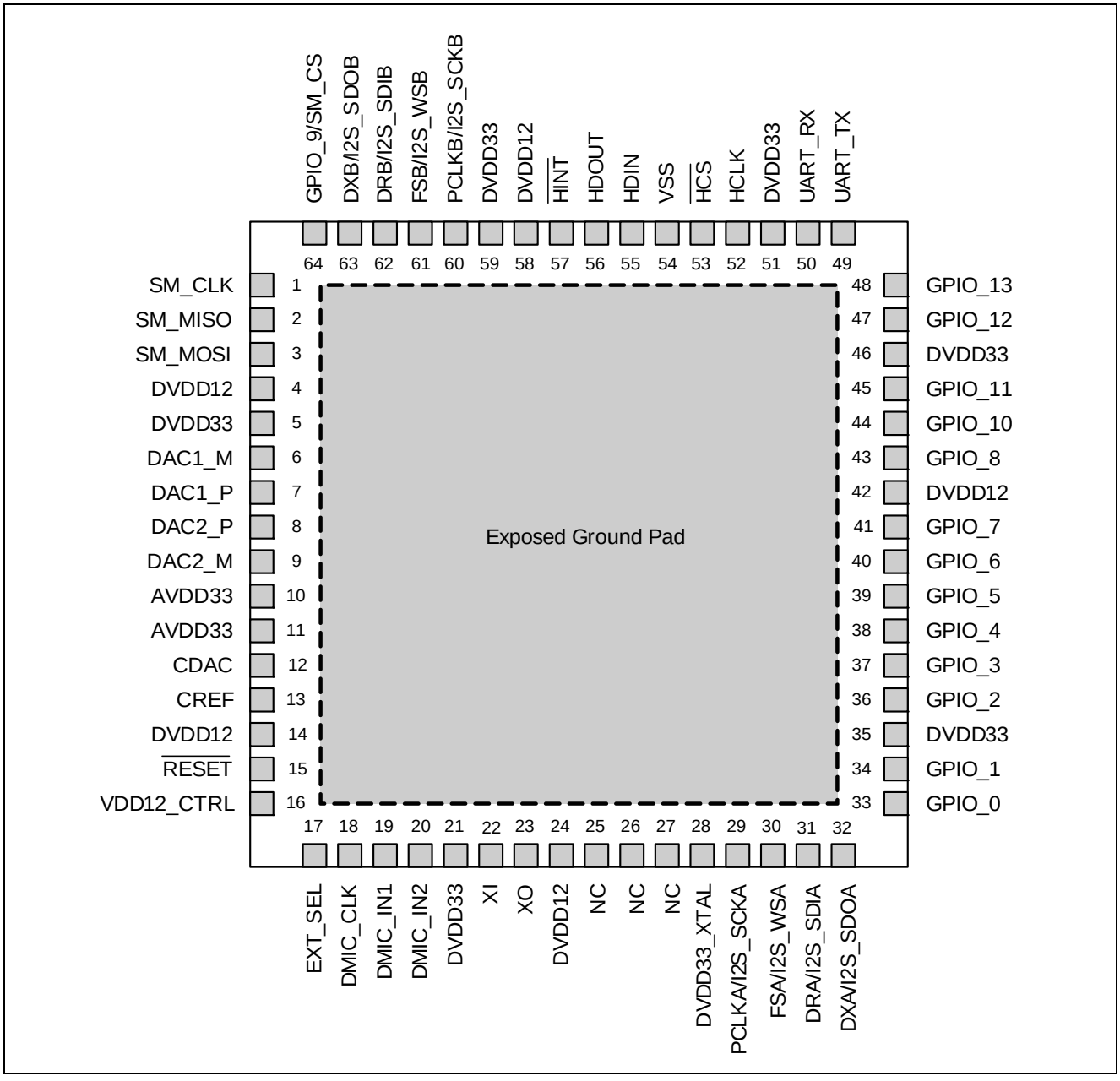


Figure 13 - ZL38042 64-Pin QFN – Top View

9.0 Pin Descriptions

QFN Pin #	Name	Type	Description
15	$\overline{\text{RESET}}$	Input	**Reset.** When low the device is in its reset state and all tristate outputs will be in a high impedance state. This input must be high for normal device operation. A 10 KΩ pull-up resistor is required on this node to DVDD33 if this pin is not continuously driven. Refer to "Reset" on page 20 for an explanation of the various reset states and their timing.

Table 6 - Reset Pin Description

QFN Pin #	Name	Type	Description
6	DAC1_M	Output	**DAC 1 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 1.
7	DAC1_P	Output	**DAC 1 Plus Output.** This is the positive output signal of the differential amplifier of the DAC 1.
9	DAC2_M	Output	**DAC 2 Minus Output.** This is the negative output signal of the differential amplifier of the DAC 2.
8	DAC2_P	Output	**DAC 2 Plus Output.** This is the positive output signal of the differential amplifier of the DAC 2.
12	CDAC	Output	**DAC Reference.** This node requires capacitive decoupling. Refer to "DAC Bias Circuit" on page 55.
13	CREF	Output	**Common Mode Reference.** This node requires capacitive decoupling. Refer to "DAC Bias Circuit" on page 55.

Table 7 - DAC Pin Descriptions

QFN Pin #	Name	Type	Description
18	DMIC_CLK	Output	**Digital Microphone Clock Output.** Clock output for digital microphones and digital electret microphone pre-amplifier devices.
19	DMIC_IN1	Input	**Digital Microphone Input 1.** Stereo or mono digital microphone input. *Tie to VSS if unused.*
20	DMIC_IN2	Input	**Digital Microphone Input 2.** Stereo or mono digital microphone input. *Tie to VSS if unused.*

Table 8 - Microphone Pin Descriptions

QFN Pin #	Name	Type	Description
29	PCLKA/ I2S_SCKA	Input/ Output	**PCM Port A Clock (Input/Tristate Output).** When TDM operation is selected this clock operates as specified in Table 1. PCLKA is equal to the data rate of signals DRA/DXA. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I^2S Port A Serial Clock (Input/Tristate Output).** This is the I^2S port bit clock and operates at selectable rates of 256, 512, 1411.2 and 1536 KHz. In I^2S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I^2S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal is an input in I^2S slave mode. *Tie this pin to VSS if unused.*
30	FSA/ I2S_WSA	Input/ Output	**PCM Port A Frame Pulse (Input/Tristate Output).** This is an 8/16 kHz TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I^2S Port A Word (Left/Right) Clock (Input/Tristate Output**). This is the I^2S port left or right word select clock and operates at selectable rates of 8, 16, or 48 kHz, which is equal to the f_S (sampling frequency) of the peripheral device. In I^2S master mode this clock is an output which drives the left/right clock input of the external slave device's peripheral converters. In I^2S slave mode this clock is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I^2S slave mode. *Tie this pin to VSS if unused.*
31	DRA/ I2S_SDIA	Input	**PCM Port A Serial Data Stream Input.** This serial data stream operates at PCLK data rates as specified in Table 1. Each 8 kHz frame supports 2, 4, 8, 16, 32, 64, or 128 slots of 8-bit or half as many 16-bit slots. **I^2S Port A Serial Data Input.** This is the I^2S port serial data input. *Tie this pin to VSS if unused.*
32	DXA/ I2S_SDOA	Output	**PCM Port A Serial Data Stream Output.** This serial data stream operates at PCLK data rates as specified in Table 1. Each 8 kHz frame supports 2, 4, 8, 16, 32, 64, or 128 slots of 8-bit or half as many 16-bit slots. **I^2S Port A Serial Data Output.** This is the I^2S port serial data output.

Table 9 - TDM and I^2S Port A Pin Description

QFN Pin #	Name	Type	Description
60	PCLKB/ I2S_SCKB	Input/ Output	**PCM Port B Clock (Input/Tristate Output).** When TDM operation is selected this clock operates as specified in Table 1. PCLKB is equal to the data rate of signals DRB/DXB. In TDM master mode this clock is an output and in TDM slave mode this clock is an input. **I²S Port B Serial Clock (Input/Tristate Output).** This is the I²S port bit clock and operates at selectable rates of 256, 512, 1411.2 and 1536 KHz. In I²S master mode this clock is an output and drives the bit clock input of the external slave device's peripheral converters. In I²S slave mode this clock is an input and is driven from a converter operating in master mode. After power-up, this signal is an input in I²S slave mode. *Tie this pin to VSS if unused.*
61	FSB/ I2S_WSB	Input/ Output	**PCM Port B Frame Pulse (Input/Tristate Output).** This is an 8/16 kHz TDM frame alignment reference. This signal is an input for applications where the PCM bus is frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. **I²S Port B Word (Left/Right) Clock (Input/Tristate Output**). This is the I²S port left or right word select clock and operates at selectable rates of 8, 16, or 48 kHz, which is equal to the f_S (sampling frequency) of the peripheral device. In I²S master mode this clock is an output which drives the left/right clock input of the external slave device's peripheral converters. In I²S slave mode this clock is an input which is driven from a converter operating in master mode. After power-up, this signal defaults to be an input in I²S slave mode. *Tie this pin to VSS if unused.*
62	DRB/ I2S_SDIB	Input	**PCM Port B Serial Data Stream Input.** This serial data stream operates at PCLK data rates as specified in Table 1. Each 8 kHz frame supports 2, 4, 8, 16, 32, 64, or 128 slots of 8-bit or half as many 16-bit slots. **I²S Port B Serial Data Input.** This is the I²S port serial data input. *Tie this pin to VSS if unused.*
63	DXB/ I2S_SDOB	Output	**PCM Port B Serial Data Stream Output.** This serial data stream operates at PCLK data rates as specified in Table 1. Each 8 kHz frame supports 2, 4, 8, 16, 32, 64, or 128 slots of 8-bit or half as many 16-bit slots. **I²S Port B Serial Data Output.** This is the I²S port serial data output.

Table 10 - TDM and I²S Port B Pin Description

QFN Pin #	Name	Type	Description
52	HCLK	Input	**HBI SPI Slave Port Clock Input.** Clock input for the SPI Slave port. Maximum frequency = 25 MHz. This input should be tied to VSS in I^2C mode, refer to Table 3. *Tie this pin to VSS if unused.*
53	$\overline{HCS}$	Input	**HBI SPI Slave Chip Select Input.** This active low chip select signal activates the SPI Slave port. This port functions as a peripheral interface for an external controller, and supports access to the internal registers and memory of the device. **HBI I^2C Serial Clock Input.** This pin functions as the I2C_SCLK input in I^2C mode. A pull-up resistor is required on this node for I^2C operation. *Tie this pin to VSS if unused.*
55	HDIN	Input	**HBI SPI Slave Port Data Input.** Data input signal for the SPI Slave port. This input selects the slave address in I^2C mode, refer to Table 3. *Tie this pin to VSS if unused.*
56	HDOUT	Input/ Output	**HBI SPI Slave Port Data Output (Tristate Output).** Data output signal for the SPI Slave port. **HBI I^2C Serial Data (Input/Output).** This pin functions as the I2C_SDA I/O in I^2C mode. A pull-up resistor is required on this node for I^2C operation.
57	$\overline{HINT}$	Output	**HBI Interrupt Output.** This output can be configured as either CMOS or open drain by the host.

Table 11 - HBI – SPI Slave Port Pin Descriptions

QFN Pin #	Name	Type	Description
1	SM_CLK	Output	**Master SPI Port Clock (Tristate Output).** Clock output for the Master SPI port. Maximum frequency = 25 MHz.
2	SM_MISO	Input	**Master SPI Port Data Input.** Data input signal for the Master SPI port.
3	SM_MOSI	Output	**Master SPI Port Data Output (Tristate Output).** Data output signal for the Master SPI port.
64	GPIO_9/ SM_CS	Input/ Output	**Master SPI Port Chip Select (Input Internal Pull-Up/Tristate Output).** Chip select output for the Master SPI port. Shared with GPIO_9, see Table 14.

Table 12 - Master SPI Port Pin Descriptions

QFN Pin #	Name	Type	Description
50	UART_RX	Input	**UART (Input).** Receive serial data in. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.
49	UART_TX	Output	**UART (Tristate Output).** Transmit serial data out. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.

Table 13 - UART Pin Description

QFN Pin #	Name	Type	Description
33, 34, 36	GPIO_[0:2]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling.
37, 38, 39, 40, 41, 43	GPIO_[3:8]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling. In slave and master mode, GPIO_3 through GPIO_6 may be used as chip selects. See 3.1, “ZL38042 Slave and Master Mode Operation“.
64	GPIO_9/ SM_CS	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** This pin can be configured as an input or output and is intended for low-frequency signalling. Alternate functionality with SM_CS, see Table 12.
44, 45, 47, 48	GPIO_ [10:13]	Input/ Output	**General Purpose I/O (Input Internal Pull-Down/Tristate Output).** These pins can be configured as an input or output and are intended for low-frequency signalling.

Table 14 - GPIO Pin Descriptions

QFN Pin #	Name	Type	Description
22	XI	Input	**Crystal Oscillator Input.** Refer to “External Clock Requirements” on page 47.
23	XO	Output	**Crystal Oscillator Output.** Refer to “External Clock Requirements” on page 47.

Table 15 - Oscillator Pin Description

QFN Pin #	Name	Type	Description
17	EXT_SEL	Input	**VDD +1.2 V Select.** Select external +1.2 V supply. Tie to DVDD33 if the +1.2 V supply is to be provided externally. Tie to VSS (0 V) if the +1.2 V supply is to be generated internally. Refer to "Power Supply Considerations" on page 53 for more information.
16	VDD12_CTRL	Output	**VDD +1.2 V Control.** Analog control line for the voltage regulator external FET when EXT_SEL is tied to VSS. When EXT_SEL is tied to DVDD33, the VDD12_CTRL pin becomes a CMOS output which can drive the shutdown input of an external LDO.
4, 14, 24, 42, 58	DVDD12	Power	**Core Supply.** Connect to a +1.2 V ±5% supply. Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.
5, 21, 35, 46, 51, 59	DVDD33	Power	**Digital Supply.** Connect to a +3.3 V ±5% supply. Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.
28	DVDD33_ XTAL	Power	**Crystal Digital Supply.** For designs using a crystal or external oscillator, this pin must be connected to a +3.3 V supply source capable of delivering 10 mA. For designs that do not use a crystal or external oscillator this pin can be tied to VSS in order to save power.
10, 11	AVDD33	Power	**Analog Supply.** Connect to a +3.3 V ±5% supply. Place a 100 nF, 20%, 10 V, ceramic capacitor on each pin decoupled to the VSS plane.
54	VSS	Ground	**Ground.** Connect to digital ground plane.
	Exposed Ground Pad	Ground	**Exposed Pad Substrate Connection.** Connect to VSS. This pad is at ground potential and must be soldered to the printed circuit board and connected via multiple vias to a heatsink area on the bottom of the board and to the internal ground plane.

Table 16 - Supply and Ground Pin Description

QFN Pin #	Name	Type	Description
25, 26, 27	NC		**No Connection.** These pins are to be left unconnected, do not use as a tie point.

Table 17 - No Connect Pin Description

10.0 Electrical Characteristics

10.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Digital supply voltage (DVDD33)	-0.5 to +4.0 V
Core supply voltage (DVDD12)	-0.5 to +1.32 V
Input voltage	-0.5 to +4.0 V
Continuous current at digital outputs	15 mA
Package power dissipation, continuous (1), T_A = 85°C, P_D	1.8 W
Junction to ambient thermal resistance (1), θ_{JA}	22.1 °C/W
Junction to exposed pad thermal resistance (1), θ_{JC}	2.0 °C/W
Reflow temperature, 10 sec., MSL3, per *JEDEC J-STD-020*	260 °C
Storage temperature	-55 to +125 °C
ESD immunity (Human Body Model)	JESD22 Class 1C compliant

Notes:

1. *The thermal specifications assume that the device is mounted on an effective thermal conductivity test board (4 layers, 2s2p) per JEDEC JESD51-7 and JESD51-5.*

10.2 Operating Ranges

Microsemi guarantees the performance of this device over the industrial (-40 ºC to 85 ºC) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the *Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.*

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient temperature	T_{OP}	-40		+85	°C
Analog supply voltage	V_{AVDD33}	3.135	3.3	3.465	V
Digital supply voltage	V_{DVDD33}				V
Crystal Digital supply voltage	V_{DVDD33_XTAL}				V
Crystal I/O voltage	V_{XI}		2.5	2.625	V
Core supply voltage	V_{DVDD12}	1.14	1.2	1.26	V

10.3 Power Consumption

Device power consumption can vary with the firmware load. Common values are listed here using an external +1.2 V supply for the core power supply with PCLKA as the external clock source for the PLL and a 3.3 KΩ resistor from GPIO_2 to DVDD33 (external Flash selected), unless otherwise noted.

	+3.3 V [1]		+1.2 V [2]			
Operational Mode	**Typ.**	**Max.**	**Typ.**	**Max.**	**Units**	**Notes / Conditions**
Normal Wideband and Super Wideband Narrowband	 55 45		 148 88		mW	Firmware active, 1 DAC active[3] 2 MICs active[4].
Low power Wideband and Super Wideband Narrowband	 48 45		 94 58			
Sleep	7		3			Analog blocks disabled and Firmware made inactive.
Reset	0.35		0			Device in reset (reset > 10 µS), DVDD12 not present.
Ultra-low power	0.01		0			Crystal or crystal oscillator in use. Device in reset (reset > 10 µS), DVDD12 not present, DVDD33_XTAL held low.

Note 1: Table values include all current entering DVDD33, AVDD33, and DVDD33_XTAL pins. Add 3.3 mW to Normal, Low power, and Sleep modes if the internal voltage regulator is used. Add 3.6 mW to Normal, Low power, and Sleep modes if a crystal or crystal oscillator is used.

Note 2: Core supply voltage. Table values include all current entering DVDD12 pins. Multiply the +1.2 V power values by 2.75 if the internal regulator is used.

Note 3: For 2 DACs active, add 12 mW to +3.3 V power.

Note 4: If 3 or 4 MICs are active, add 1 mW to +1.2 V power.

10.4 DC Specifications

Typical values are for TA = 25 ºC and nominal supply voltage. Minimum and maximum values are over the industrial -40 ºC to 85 ºC temperature range and supply voltage range as shown in "Operating Ranges" on page 31, except as noted. A 12 MHz crystal oscillator is active.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
Input high voltage	V_{IH}	0.7 * V_{DVDD33}		V_{DVDD33} + 0.3	V	All digital inputs
Input low voltage	V_{IL}	V_{VSS} - 0.3		0.3 * V_{DVDD33}	V	All digital inputs
Input hysteresis voltage	V_{HYS}	0.4			V	
Input leakage (input pins)	I_{IL}			5	µA	0 to +3.3 V
Input leakage (bi-directional pins)	I_{BL}			5	µA	0 to +3.3 V
Weak pull-up current	I_{PU}	38	63	101	µA	Input at 0 V
Weak pull-down current	I_{PD}	19	41	158	µA	Input at +3.3 V
Input pin capacitance	C_I		5		pF	
Output high voltage	V_{OH}	2.4			V	At 12 mA
Output low voltage	V_{OL}			0.4	V	At 12 mA
Output high impedance leakage	I_{OZ}			5	µA	0 to +3.3 V
Pin capacitance (output & input/tristate pins)	C_O		5		pF	
Output rise time	t_{RT}		1.25		ns	10% to 90%, C_{LOAD} = 20 pF
Output fall time	t_{FT}		1.25		ns	90% to 10%, C_{LOAD} = 20 pF

10.5 AC Specifications

For all AC specifications, typical values are for TA = 25 ºC and nominal supply voltage. Minimum and maximum values are over the industrial -40 ºC to 85 ºC temperature range and supply voltage ranges as shown in "Operating Ranges" on page 31, except as noted. 12 MHz crystal oscillator active.

10.5.1 Microphone Interface

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
Microphone clock output (DMIC_CLK), 8 kHz, 16 kHz data rate 24 kHz data rate 48 kHz data rate			 1.024 1.536 3.072		MHz	
DMIC_CLK, Output high current	I_{OH}		20		mA	V_{OH} = DVDD33 - 0.4 V
DMIC_CLK, Output low current	I_{OL}		30		mA	V_{OL} = 0.4 V
DMIC_CLK, Output rise and fall time	t_R, t_F		5		ns	C_{LOAD} = 100 pF

10.5.2 DAC

Measurements taken using PCM mode. THD+N versus output power for speaker drive applications presented in Figure 14; THD+N versus output voltage for amplifier drive applications presented in Figure 15.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
DAC output level: Full scale: Differential Single-ended 0 dBm0 : Differential Single-ended	V_{DACFS}		 4.8 2.4 2.8 1.4		V_{PP}	DAC gain = 1, 1 KΩ load.
PCM full scale level (V_{ppd} value)			9		dBm0	DAC gain = 1, 600 Ω load
DAC output power: Single-ended, 32 ohm load Single-ended, 16 ohm load Differential, 32 ohm load			 20.6 37.5 86.0	 24 47 94	mW	*1.*, Single-ended loads driven capacitively to ground
Frequency response: Sample rate = 48 KS/s	f_R	20		20000	Hz	*1.*, 3 dB cutoff includes external AC coupling, without AC coupling the response is low pass.
Dynamic range: Sample rate = 48 KS/s			 92		 dBFS	20 Hz - 20 kHz
Total harmonic distortion plus noise	THD + N		-82		dBFS	Differential output, input = -3 dBFS.
Signal to Noise Ratio	SNR		85		dB	1004 Hz, C-message weighted
Allowable capacitive load to ground	C_L			100	pF	*1.*, At each DAC output.
Power supply rejection ratio	PSRR	50	70		dB	*1.*, 20 Hz - 100 kHz, 100 mVpp supply noise.
Crosstalk			-85	-70	dB	*1.*, Between DAC outputs.
Note 1: Guaranteed by design, not tested in production.						

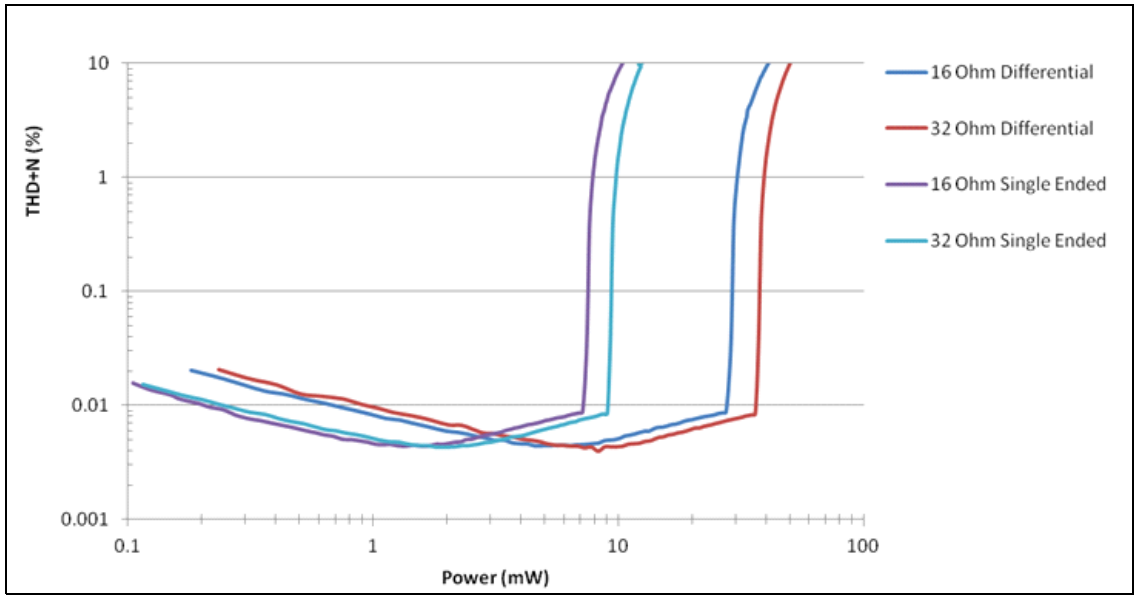


Figure 14 - THD+N Ratio versus Output Power – Driving Low Impedance

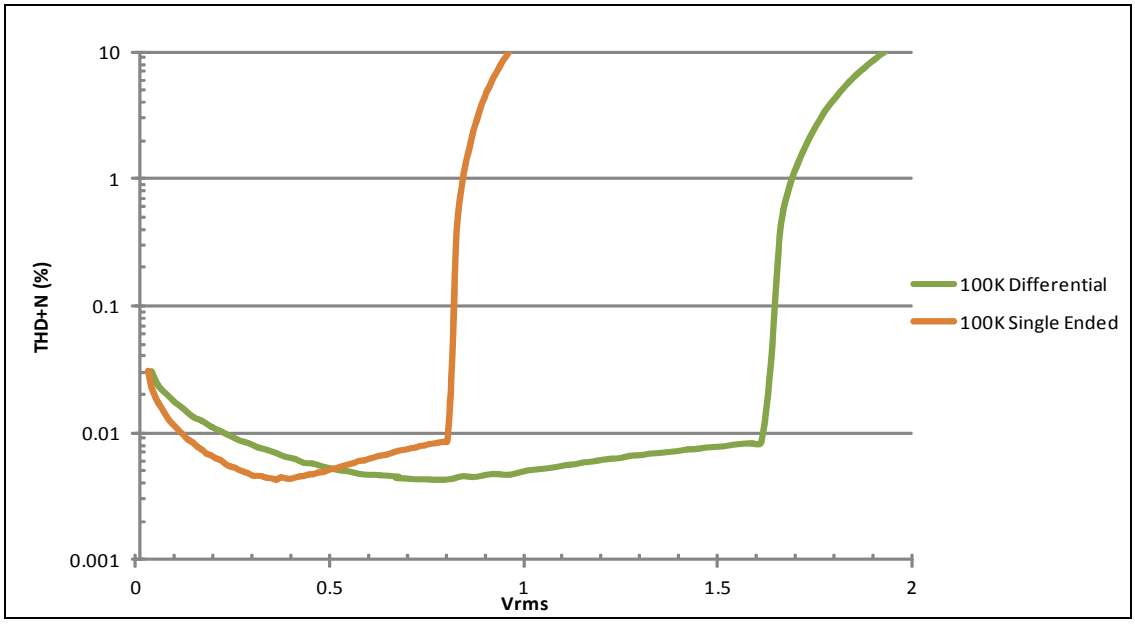


Figure 15 - THD+N Ratio versus V_{RMS} – Driving High Impedance

10.5.3 AC Specifications - External Oscillator Requirements

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
External oscillator frequency accuracy	A_{OSC}	-50		50	ppm	Not tested in production
External oscillator duty cycle	DC_{OSC}	40		60	%	
Jitter on PCLKA (master mode)				0.75	ns_{pp}	
PCLK lock time			200		µs	
Holdover accuracy				50	ppm	

11.0 Timing Characteristics

Figure 16 depicts the timing reference points that apply to the timing diagrams shown in this section. For all timing characteristics, typical values are for TA = 25 ºC and nominal supply voltage. Minimum and maximum values are over the industrial -40 ºC to 85 ºC temperature range and supply voltage ranges as shown in "Operating Ranges" on page 31, except as noted.

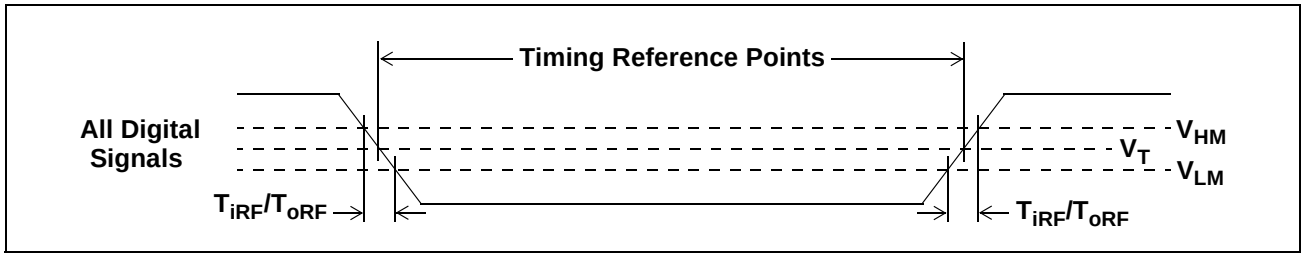


Figure 16 - Timing Parameter Measurement Digital Voltage Levels

11.1 TDM Interface Timing Parameters

11.1.1 GCI and PCM Timing Parameters

Specifications for GCI and PCM timing modes are presented in the following table. The specifications apply to both port A and port B in slave operation.

A timing diagram that applies to GCI timing of the TDM interface is illustrated in Figure 17.

Timing diagrams that apply to PCM timing of the TDM interface are illustrated in Figure 18 and Figure 19.

Parameter	Symbol	Min	Typ	Max	Unit	Notes / Conditions
PCLK period	t_{PCY}	122		7812.5	ns	1, 2, 4
PCLK High pulse width	t_{PCH}	48				2
PCLK Low pulse width	t_{PCL}	48				2
Fall time of clock	t_{PCF}			8		
Rise time of clock	t_{PCR}			8		
FS delay (output rising or falling)	t_{FSD}	2		15		2
		2		25		3
FS setup time (input)	t_{FSS}	5				5
FS hold time (input)	t_{FSH}	0.5		125000 - $2t_{PCY}$		5
Data output delay	t_{DOD}	2		15		2
		2		25		3
Data output delay to High-Z	t_{DOZ}	0		10		6
Data input setup time	t_{DIS}	5				5
Data input hold time	t_{DIH}	0				5
Allowed PCLK jitter time	t_{PCT}			20		Peak-to-peak
Allowed Frame Sync jitter time	t_{FST}			20		Peak-to-peak

Note 1: PCLKA or PCLKB frequency must be an integer multiple of 512 kHz +/- 6000 ppm but must be specified to within 100 ppm. The minimum clock frequency is 128 kHz.

Note 2: C_{LOAD} = 40 pF

Note 3: C_{LOAD} = 150 pF

Note 4: If PCLKA is used to drive the main system clock, it's frequency must be a multiple of 2.048 MHz and it and FSA must be present at all times to maintain proper internal operation.

Note 5: Setup times based on 2 ns PCLK rise and fall times; hold times based on 0 ns PCLK rise and fall times.

Note 6: Guaranteed by design, not tested in production.

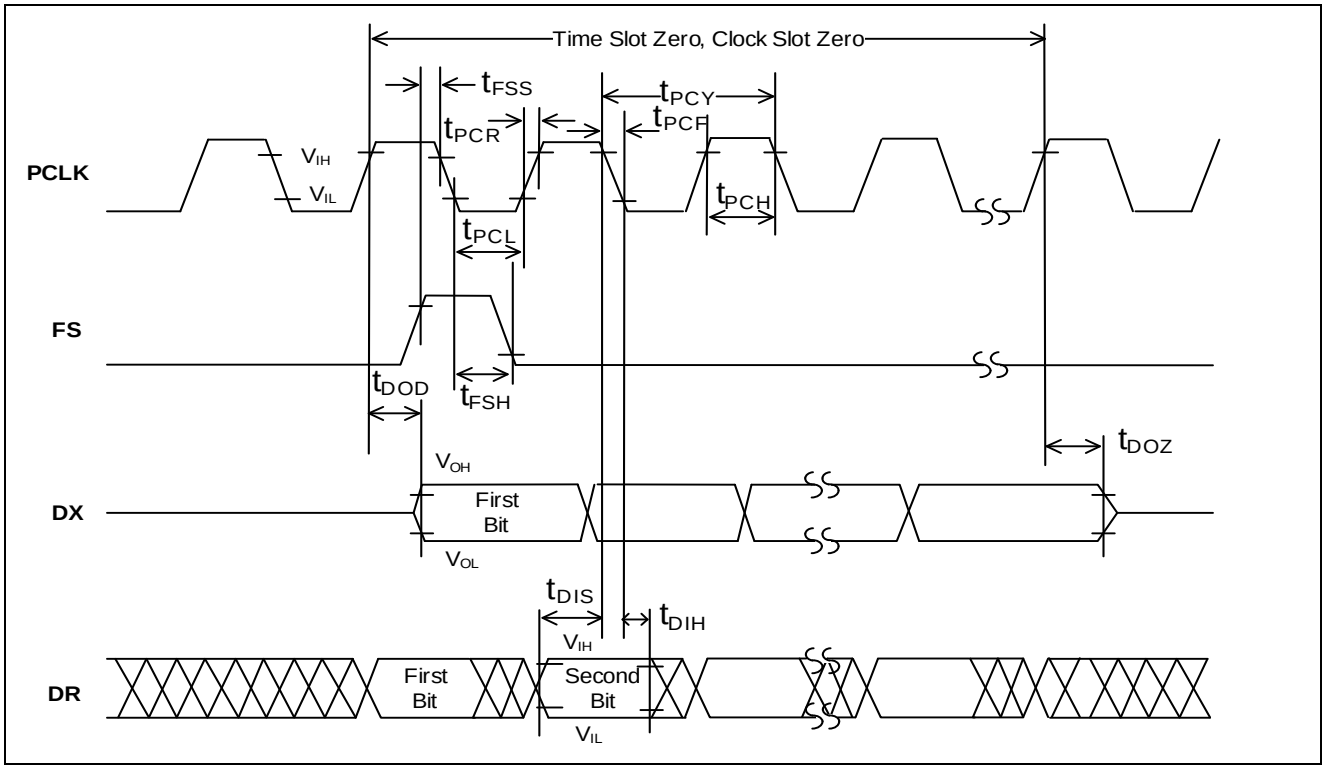


Figure 17 - GCI Timing, 8-bit

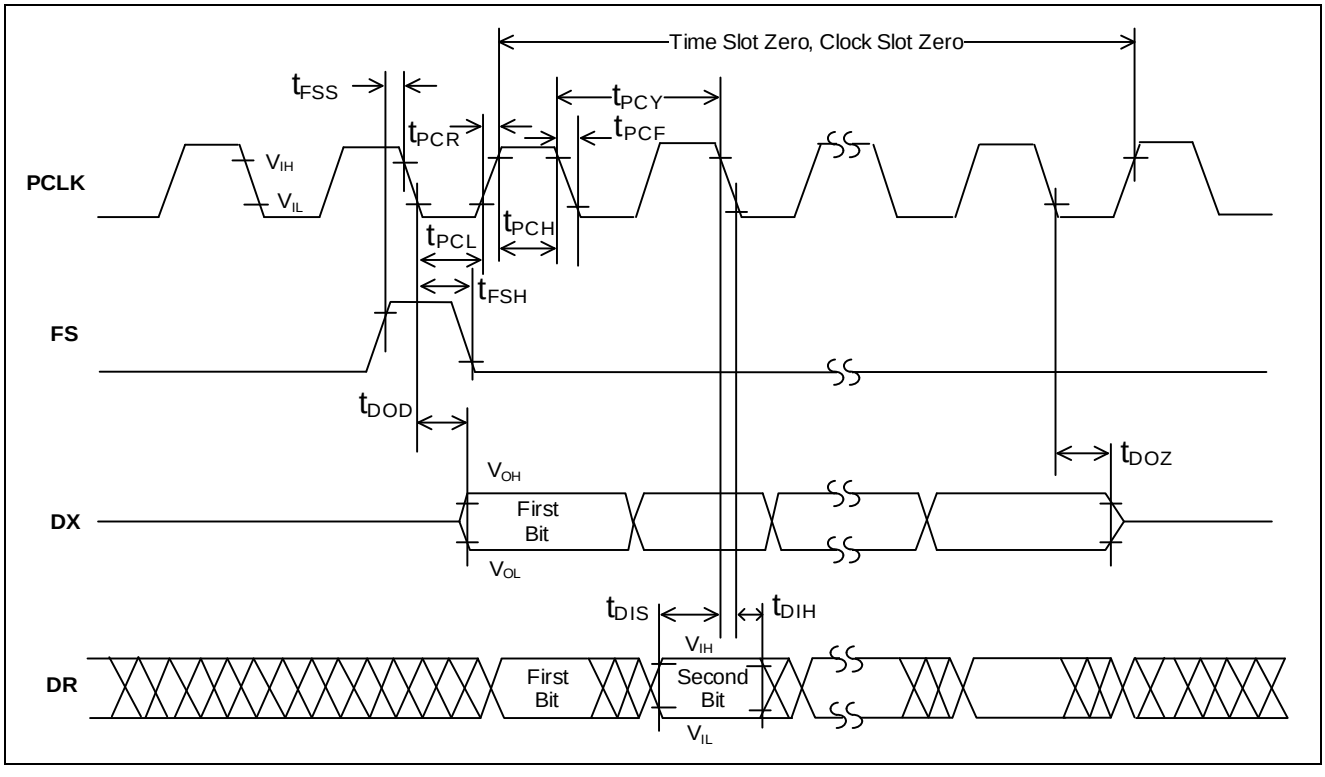


Figure 18 - PCM Timing, 8-bit with XEDX = 0 (Transmit on Negative PCLK Edge)

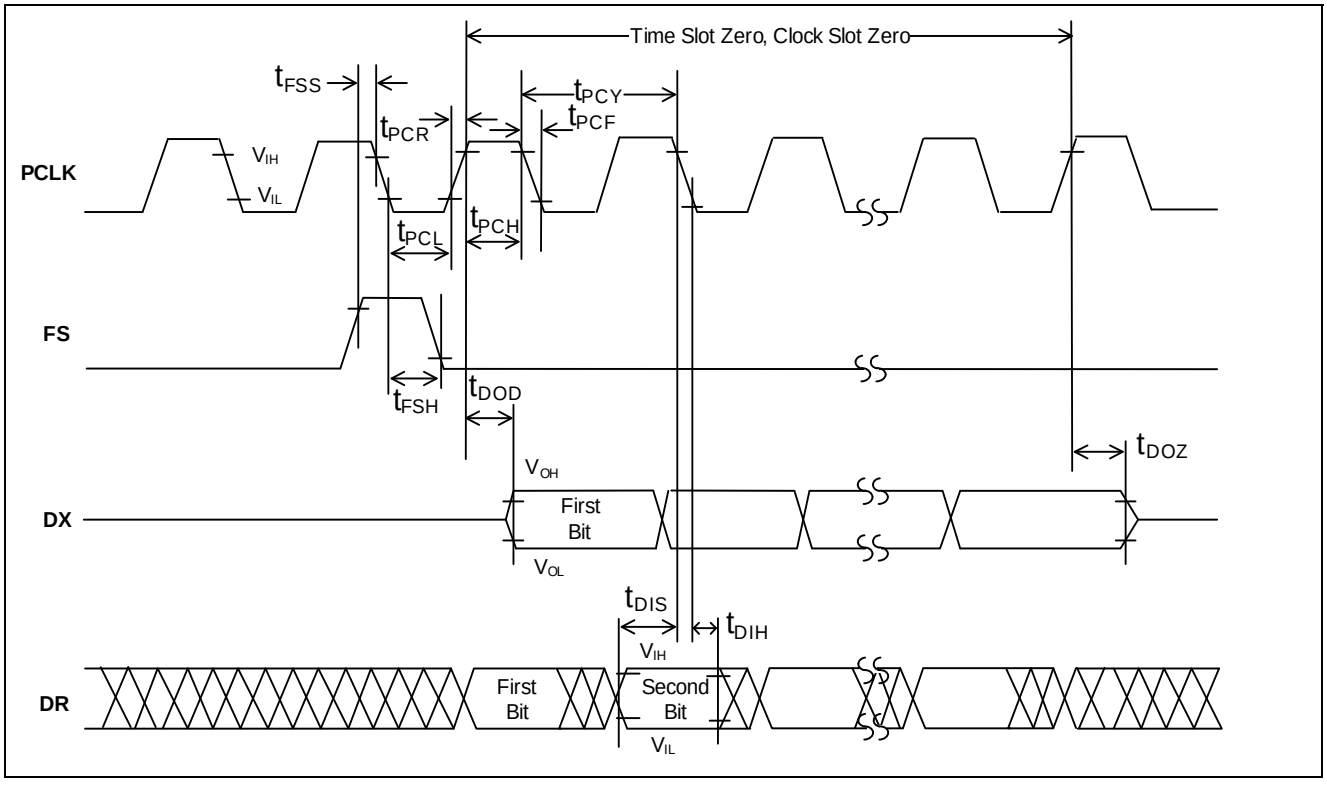


Figure 19 - PCM Timing, 8-bit with XEDX = 1 (Transmit on Positive PCLK Edge)

11.1.2 I²S Timing Parameters

11.1.2.1 I²S Slave

Specifications for I²S Slave timing are presented in the following table. The specifications apply to both port A and port B. A timing diagram for the I²S Slave timing parameters is illustrated in Figure 20.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
I2S_SCK Clock Period f_s = 48 kHz f_s = 8 kHz	t_{ISSCP}		651.04 3.91		ns µs	
I2S_SCK Pulse Width High f_s = 48 kHz f_s = 8 kHz	t_{ISSCH}	292.97 1.76		358.07 2.15	ns µs	
I2S_SCK Pulse Width Low f_s = 48 kHz f_s = 8 kHz	t_{ISSCL}	292.97 1.76		358.07 2.15	ns µs	
I2S_SDI Setup Time	t_{ISDS}	5			ns	
I2S_WS Setup Time	t_{ISDS}	5			ns	
I2S_SDI Hold Time	t_{ISDH}	0			ns	
I2S_WS Hold Time	t_{ISDH}	0.5			ns	
I2S_SCK Falling Edge to I2S_SDO Valid	t_{ISOD}	2		15	ns	C_{LOAD} = 40 pF

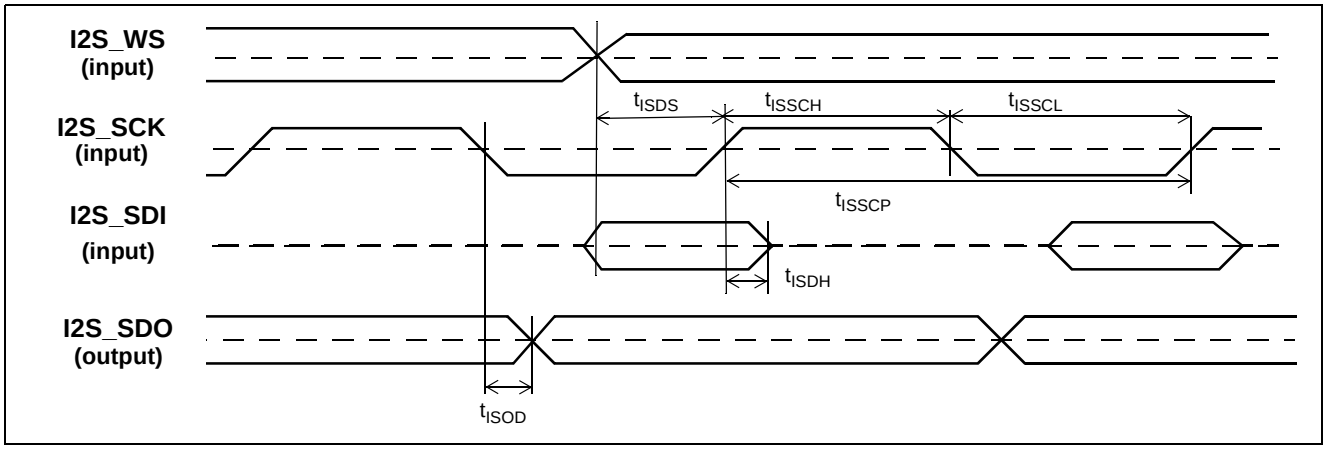


Figure 20 - Slave I²S Timing

11.1.2.2 I²S Master

Specifications for I²S Slave timing are presented in the following table. The specifications apply to both port A and port B. A timing diagram for the I²S Master timing parameters is illustrated in Figure 21.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes/Conditions
I2S_SCK Clock Period f_s = 48 kHz f_s = 8 kHz	t_{IMSCP}		651.04 3.91		ns µs	
I2S_SCK Pulse Width High f_s = 48 kHz f_s = 8 kHz	t_{IMSCH}	318.0 1.95		333.0 1.96	ns µs	
I2S_SCK Pulse Width Low f_s = 48 kHz f_s = 8 kHz	t_{IMSCL}	318.0 1.95		333.0 1.96	ns µs	
I2S_SDI Setup Time	t_{IMDS}	5			ns	
I2S_SDI Hold Time	t_{IMDH}	0			ns	
I2S_SCK Falling Edge to I2S_WS	t_{IMOD}	2		15	ns	C_{LOAD} = 40 pF
I2S_SCK Falling Edge to I2S_SDO Valid	t_{IMOD}	2		15	ns	C_{LOAD} = 40 pF

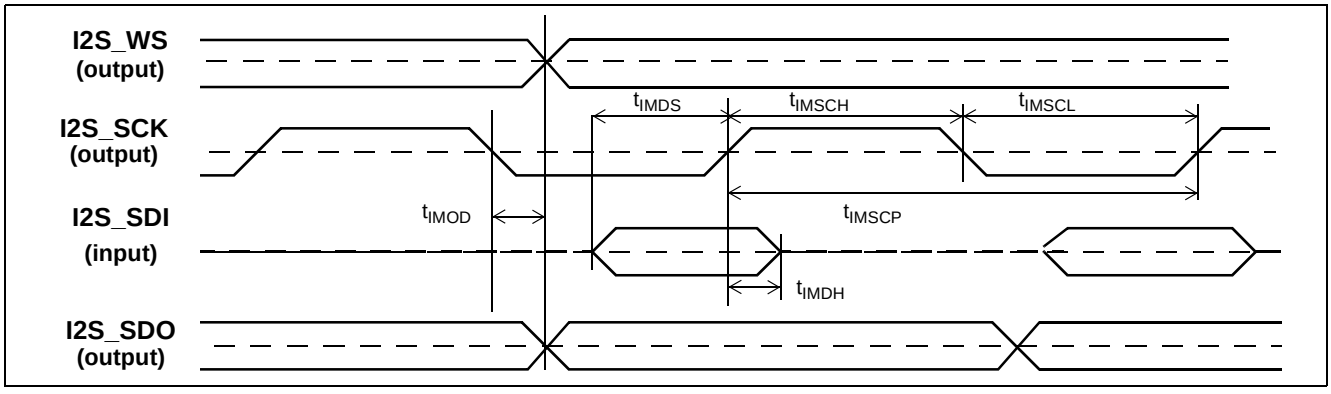


Figure 21 - Master I²S Timing

11.2 Host Bus Interface Timing Parameters

11.2.1 SPI Slave Port Timing Parameters

Specifications for SPI Slave timing are presented in the following table. A timing diagram for the SPI Slave timing parameters is illustrated in Figure 22.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
HCLK Clock Period	t_{SSCP}	40			ns	
HCLK Pulse Width High	t_{SSCH}	16	$t_{SSCP}/2$			1
HCLK Pulse Width Low	t_{SSCL}	16	$t_{SSCP}/2$			1
HDIN Setup Time	t_{SSDS}	5				
HDIN Hold Time	t_{SSDH}	0				
$\overline{HCS}$ Asserted to HCLK Sampling Edge	t_{SHCSC}	5	$t_{SSCP}/2$			
HCLK Driving Edge to HDOUT Valid	t_{SSOD}	2		15		C_{LOAD} = 40 pF
$\overline{HCS}$ Falling Edge to HDOUT Valid	t_{SSFD}	0		15		2, C_{LOAD} = 40 pF
$\overline{HCS}$ De-asserted to HDOUT Tristate	t_{SSOZ}	0		10		5, C_{LOAD} = 40 pF
$\overline{HCS}$ Pulse High	t_{SHCSH}	20	$t_{SSCP}/2$			1, 3
$\overline{HCS}$ Pulse low	t_{SHCSL}					4

Note 1: HCLK may be stopped in the high or low state indefinitely without loss of information. When $\overline{HCS}$ is at low state, every 16 HCLK cycles, the 16-bit received data will be interpreted by the SPI interface logic.

Note 2: The first data bit is enabled on the falling edge of $\overline{HCS}$ or on the falling edge of HCLK, whichever occurs last.

Note 3: The SPI Slave requires 61ns $\overline{HCS}$ off time just to make the transition of $\overline{HCS}$ synchronized with HCLK clock. In the command framing mode, there is no $\overline{HCS}$ off time between each 16-bit command/data, and $\overline{HCS}$ is held low until the end of command.

Note 4: If $\overline{HCS}$ is not held low for 8 or 16 HCLK cycles exactly, the SPI Slave will reset. During byte or word framing mode, $\overline{HCS}$ is held low for the whole duration of the command. Multiple commands can be transferred with $\overline{HCS}$ low for the whole duration of the multiple commands. The rising edge of the $\overline{HCS}$ indicates the end of the command sequence and resets the SPI Slave.

Note 5: Guaranteed by design, not tested in production.

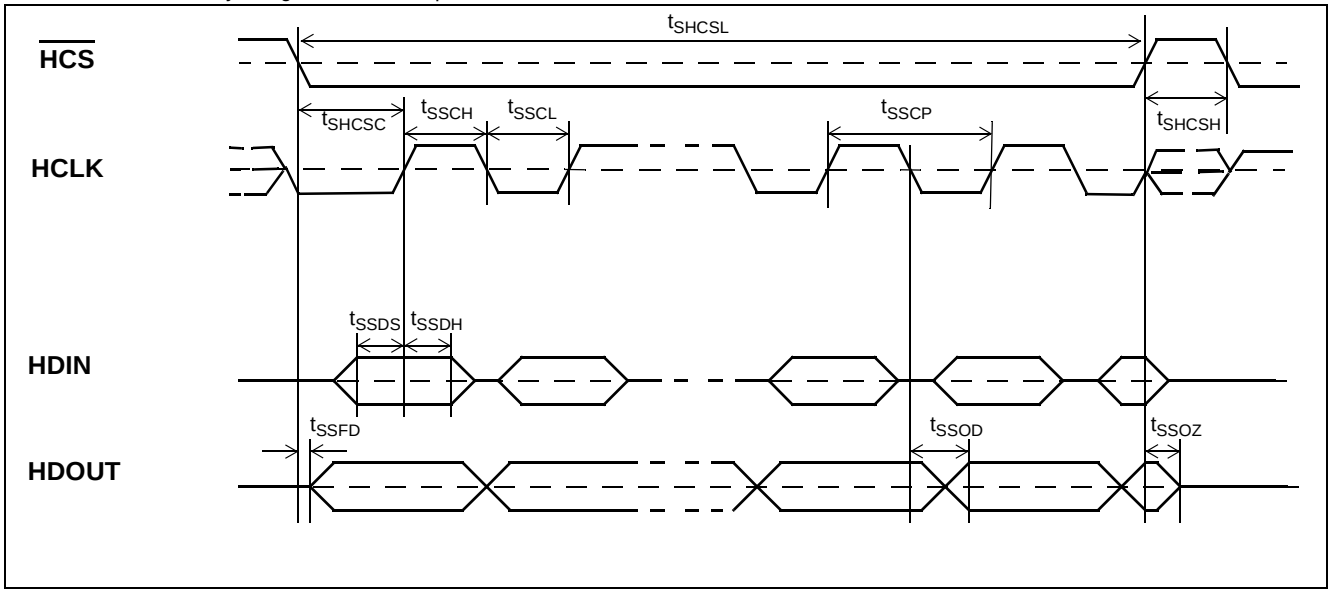


Figure 22 - SPI Slave Timing

11.2.2 I²C Slave Interface Timing Parameters

The I²C interface uses the SPI Slave interface pins.

Specifications for I²C interface timing are presented in the following table. A timing diagram for the I²C timing parameters is illustrated in Figure 23.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
SCLK Clock Frequency	f_{SCL}	0		400	kHz	
START Condition Hold Time	t_{STARTH}	0.6			µs	
SDA data setup time	t_{SDAS}	100			ns	
SDA Hold Time Input	t_{SDAH}	100			ns	
SDA Hold Time Output	t_{SDAH}	300			ns	
High period of SCLK	t_{SCLH}	0.6			µs	
Low period of SCLK	t_{SCLL}	1.3			µs	
STOP Condition Setup Time	t_{STOPS}	0.6			µs	
Repeated Start Condition Setup Time	t_{STARTS}	0.6			µs	
Pulse Width Spike Suppression, glitches ignored by input filter	t_{SP}	50			ns	

Table 18 - I²C Timing Parameters

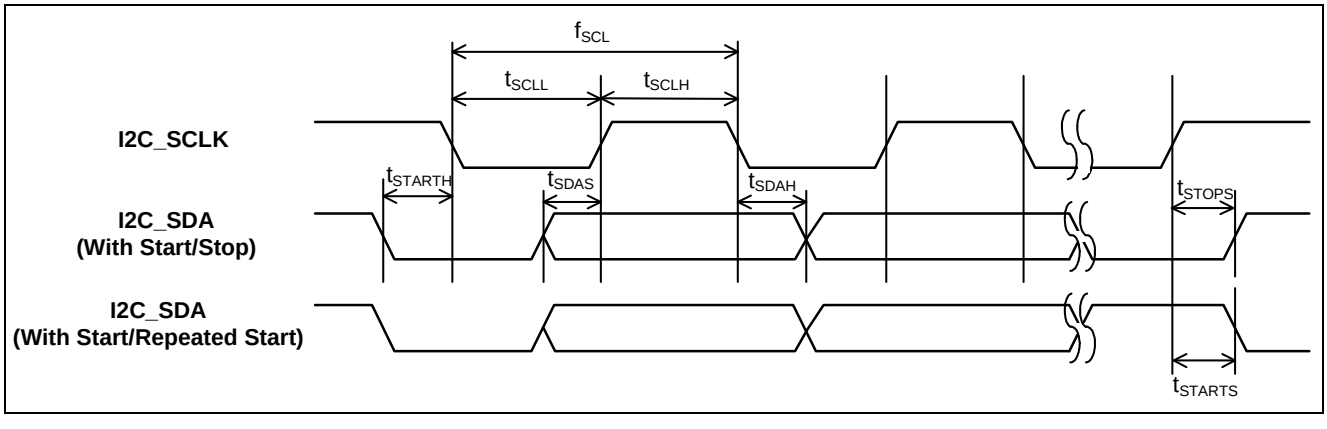


Figure 23 - I²C Timing Parameter Definitions

11.3 UART Timing Parameters

Specifications for UART timing are presented in the following table. Timing diagrams for the UART timing parameters are illustrated in Figure 24 and Figure 25.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes / Conditions
UART_RX and UART_TX bit width Baud rate = 9600 bps Baud rate = 115.2 kbps	t_{UP}		 104.17 8.68		 µs µs	
Allowed baud rate deviation 8 bits with parity 8 bits with no parity				 4.37 4.86	 % %	 Guaranteed by design, not tested in production.

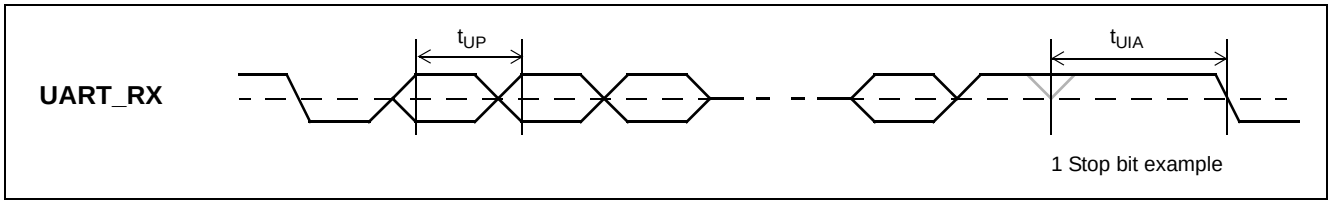


Figure 24 - UART_RX Timing

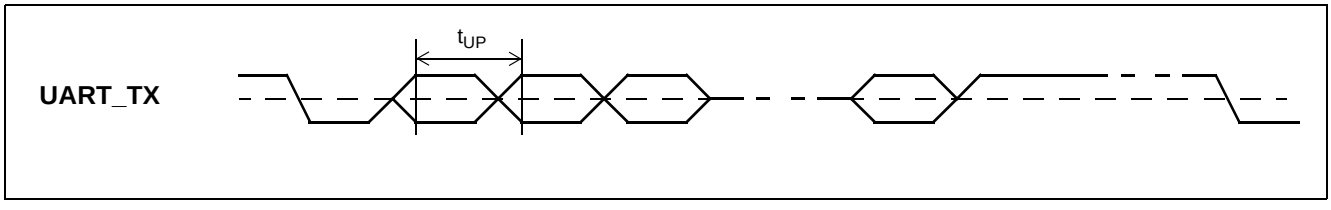


Figure 25 - UART_TX Timing

11.4 Master SPI Timing Parameters

Specifications for Master SPI timing are presented in the following table. A timing diagram for the Master SPI timing parameters is illustrated in Figure 26.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes/Conditions
SM_CLK Clock Period	t_{MSCP}	40		320		Max. 25.0 MHz
SM_CLK Pulse Width High	t_{MSCH}	(t_{MSCP}/2) - 2		160		
SM_CLK Pulse Width Low	t_{MSCL}	(t_{MSCP}/2) - 2		160		
SM_MISO Setup Time	t_{MSDS}	3				
SM_MISO Hold Time	t_{MSDHD}	0				
SM_CS Asserted to SM_CLK Sampling Edge	t_{MSCC}	(t_{MSCP}/2) - 4				
SM_CLK Driving Edge to SM_MOSI Valid	t_{MSOD}	-1		2	ns	C_{LOAD} = 40 pF
SM_MOSI Setup to SM_CLK Sampling Edge	t_{MSOS}	(t_{MSCP}/2) - 4				C_{LOAD} = 40 pF
SM_MOSI Hold Time to SM_CLK Sampling Edge	t_{MSOHD}	(t_{MSCP}/2) - 4				C_{LOAD} = 40 pF
SM_CS Hold Time after last SM_CLK Sampling Edge	t_{MSCSHD}	(t_{MSCP}/2) - 4				
SM_CS Pulse High	t_{MSCSH}	(t_{MSCP}/2) - 2				

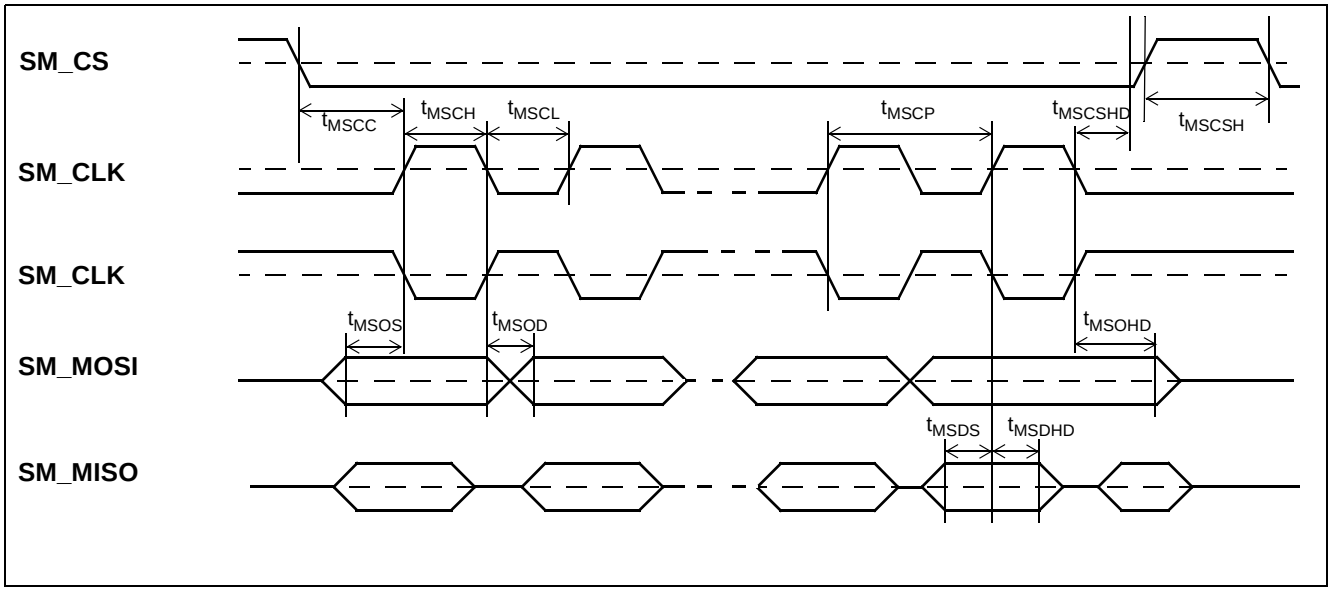


Figure 26 - Master SPI Timing

12.0 Applications

Hardware interfaces of the ZL38042 device that require external components are discussed in this section. Block diagrams showing typical ZL38042 applications are shown in Figure 27 and Figure 28.

Refer to the following sections for detailed information on the various hardware interfaces.

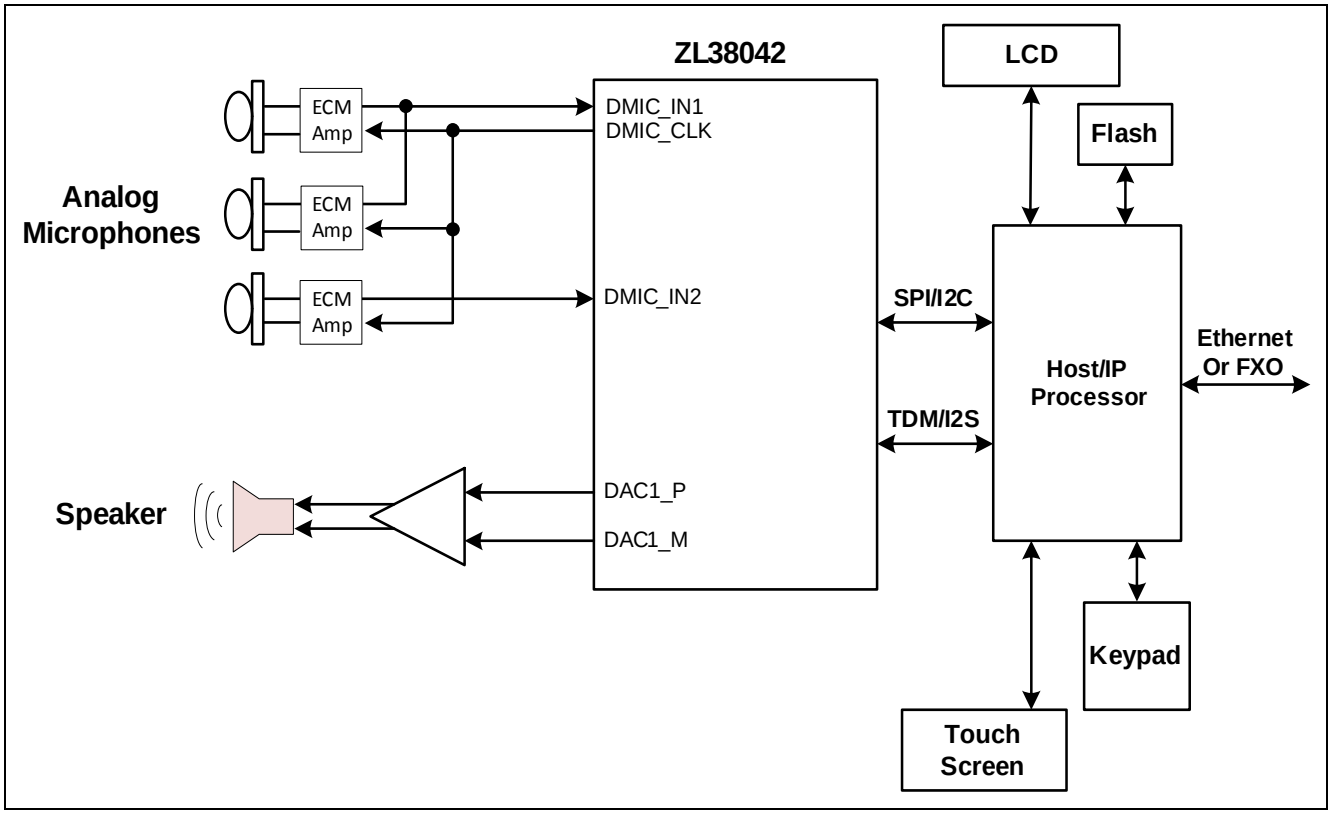


Figure 27 - Hardware Interface Block Diagram – Three Microphone Super Wideband Phone with Processor Boot

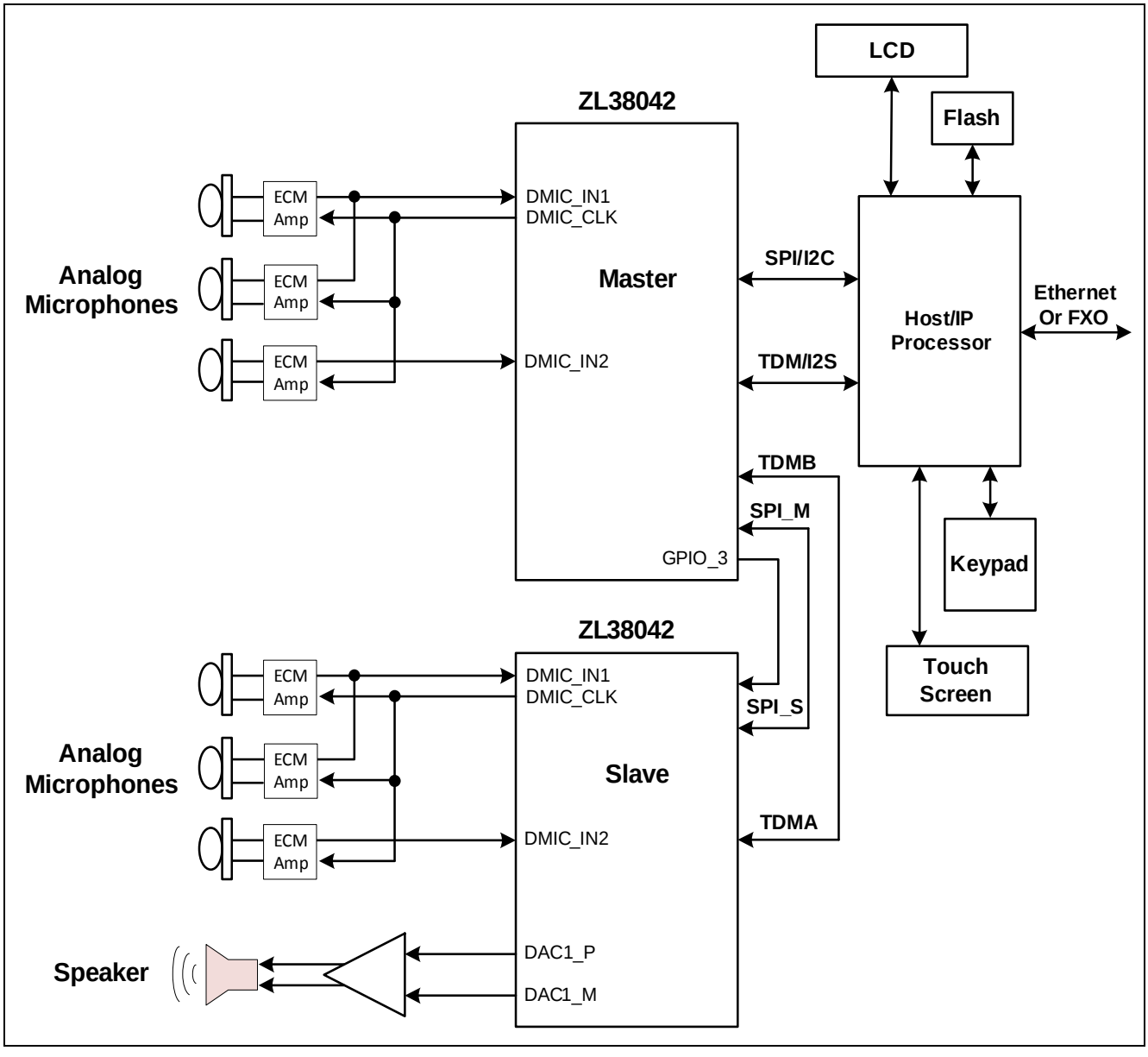


Figure 28 - Hardware Interface Block Diagram – Six Input Conference Phone using Two ZL38042 Devices

12.1 External Clock Requirements

In all modes of operation the ZL38042 requires an external clock source for the PLL, which is the source for internal timing signals. This external clock source may be either a crystal or a clock oscillator with a 2.5 V output. The frequency of the crystal or oscillator is required to be 12 MHz.

12.1.1 Crystal Application

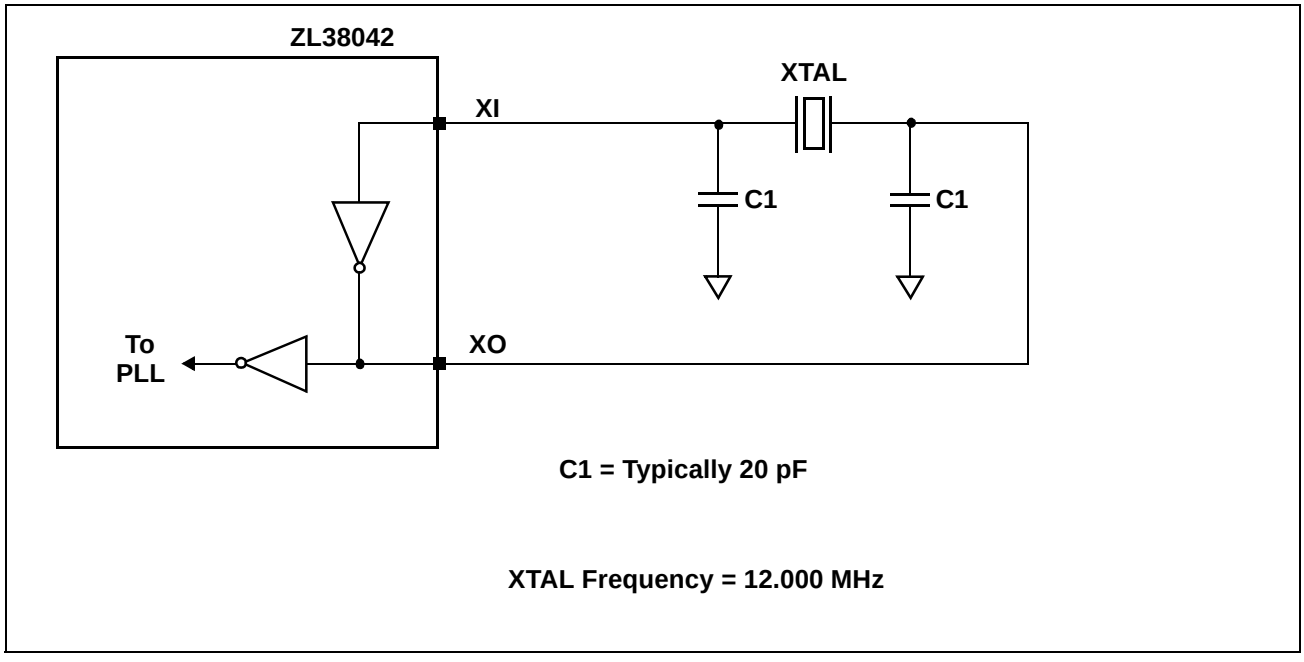


Figure 29 - Crystal Application Circuit

The oscillator circuit that is created across pins XI and XO require an external fundamental mode crystal that has a specified parallel resonance (f_P) at 12 MHz.

12.1.2 Clock Oscillator Application

Figure 30 illustrates the circuit that is used when the ZL38042 external clock source is a clock oscillator. The oscillator pins are 2.5 V compliant and should not be driven from 3.3 V CMOS without a level shifter or voltage attenuator.

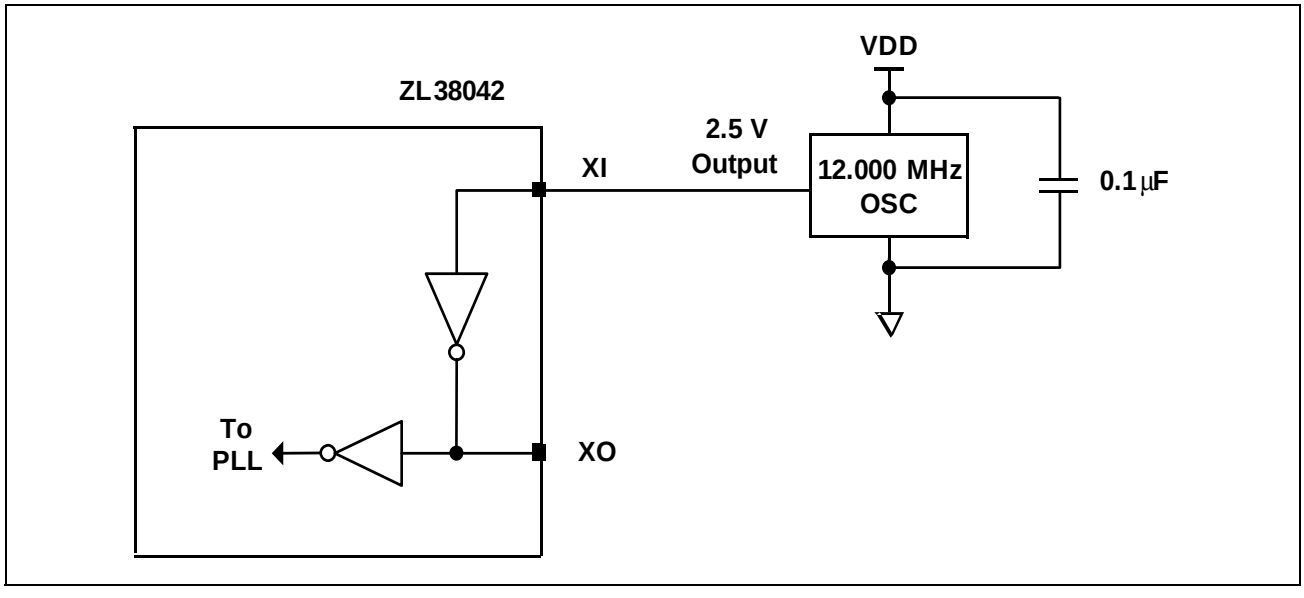


Figure 30 - Clock Oscillator Application Circuit

12.2 Flash Interface

After power-up the ZL38042 will run its resident boot code, which establishes the initial setup of the Master SPI port and then downloads the firmware from external Flash memory. This Flash firmware establishes the modes of all the ZL38042 ports and then installs the resident application.

Figure 31 illustrates the connection of Flash memory to the ZL38042 Master SPI port. If using slave and master mode, the Flash memory must be wired to the master ZL38042 device.

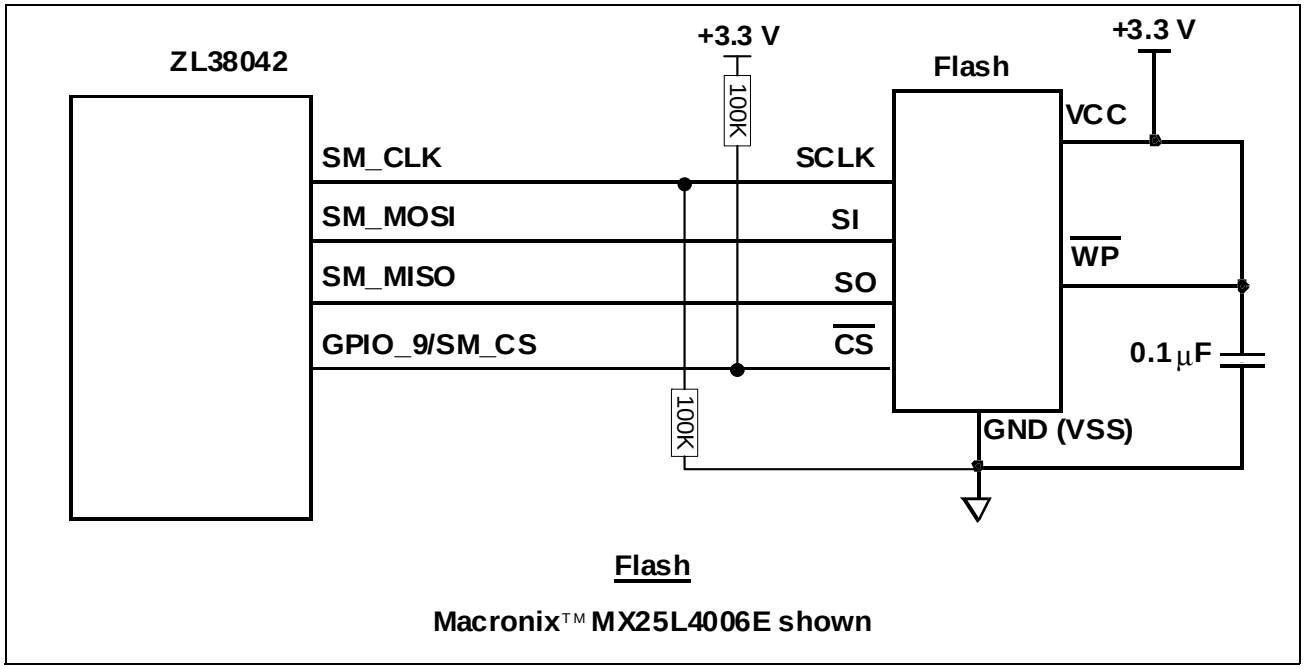


Figure 31 - Flash Interface Circuit

The ZL38042 supports a wide variety of Flash devices, the Macronix™ MX25L4006E 4 Mbit CMOS Serial Flash is used in the ZLE38042 demonstration hardware.

The ZL38042 identifies Flash devices (with a single binary image) with the ZL38042 boot ROM auto sensing the Flash type. The ZL38042 complies with JEDEC *Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices.* The ZL38042 is compatible with the *Serial Flash Discoverable Parameters* JEDEC standard JESD216A and the *Common Flash Interface* JESD68.01 JEDEC standard. The ZL38042 can identify devices by their JEDEC standard JEP106-K *Standard Manufacturer's Identification Code*.

12.3 Digital Microphone Interface

The digital microphone interface uses 3 pins (DMIC_IN1, DMIC_IN2, and DMIC_CLK) to interface with digital microphones. The ZL38042 digital microphone clock output is 1.024 MHz which corresponds to a digital microphone sample rate of 16 kHz. Microphone data is decimated and filtered to provide 8 kHz and 16 kHz audio inputs.

A stereo digital microphone, or two separate mono digital microphones, send two microphone channels on one pin by sending the data for one channel on the rising edge and one channel on the falling edge. The selection as to which clock edge is to clock in the microphone data (rising/falling) is done via an internal device register (host writable over the HBI) or in the configuration record (loaded from Flash).

Various digital microphone interfaces are presented in Figures 32 - 34.

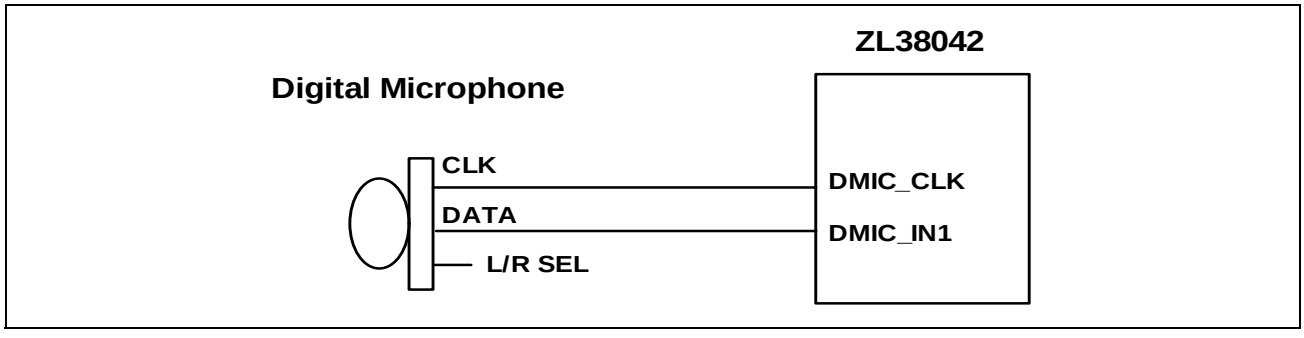


Figure 32 - Single Mono Digital Microphone Interface

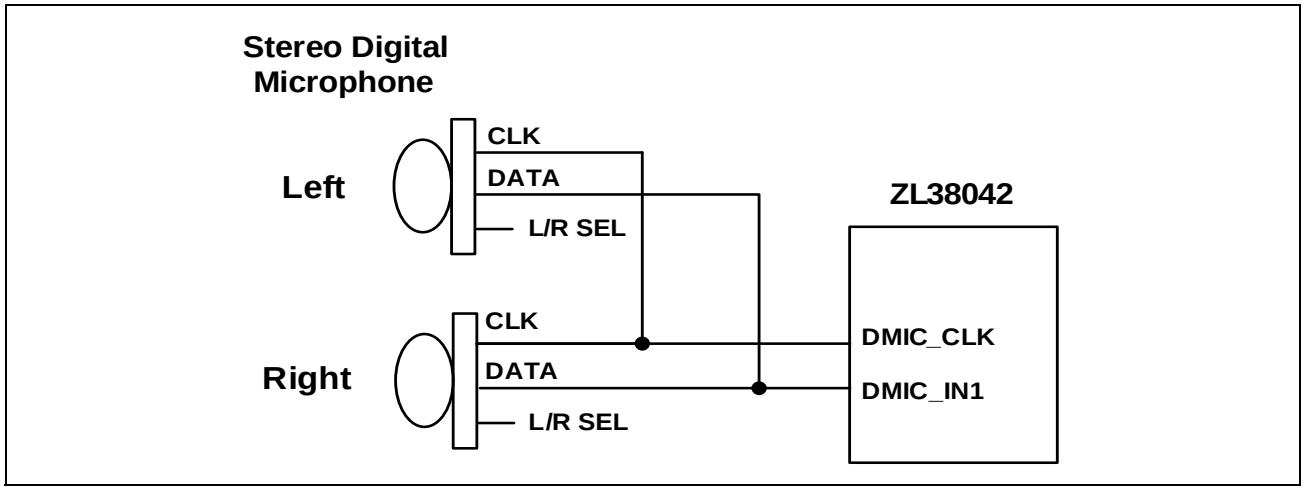


Figure 33 - Dual Microphone or Stereo Digital Microphone Interface

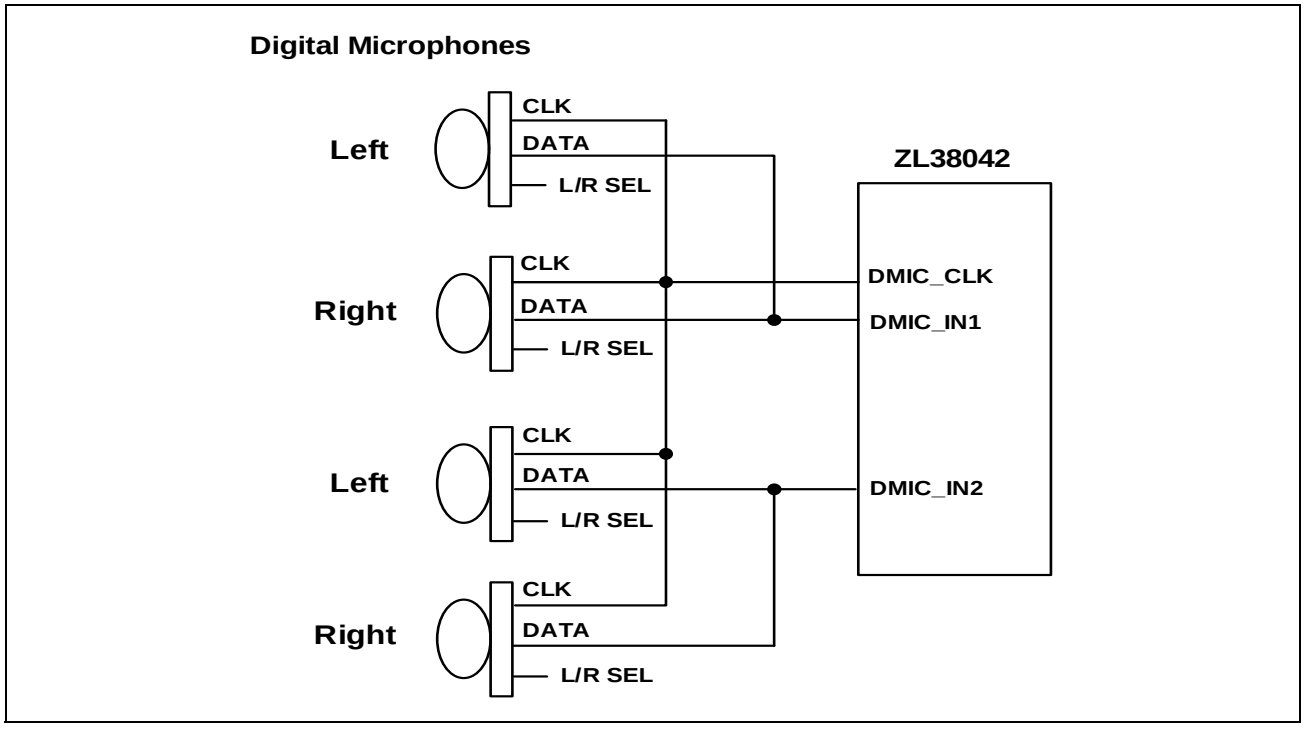


Figure 34 - Four Digital Microphone Interface

Analog electret condenser microphones (ECM) can also be used with the digital microphone interface, a Digital Electret Microphone Pre-Amplifier device as shown in Figure 35 is required.

The analog microphone in Figure 35 is wired to a differential amplifier which amplifies and converts the microphone signal to single-ended. The microphone signals are then further amplified and digitized through the Digital Electret Microphone Pre-Amplifiers and applied to the ZL38042 digital microphone input.

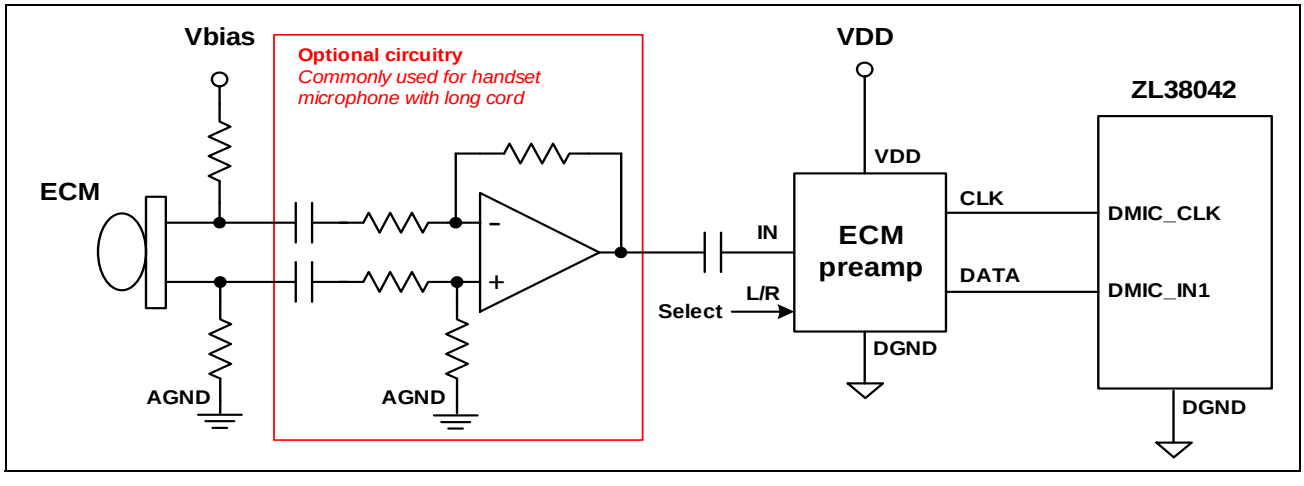


Figure 35 - ECM Circuit

12.4 Output Driver Interface

Figure 36 shows the different possible output driver configurations for the 64-pin QFN package.

The two output DACs independently drive positive and negative headphone driver amplifiers. The output pins can be independently configured in the following ways:

A. Direct differential drive of a speaker as low as 32 ohms. (Differentially driving a 16 ohm speaker is possible, but only with the same amount of power as in the single-ended case. The signal level must be reduced to not exceed ½ scale in this case.)

B. Direct differential drive of a high impedance power amplifier. A Class D amplifier is recommended for this speaker driver. Use an ON Semiconductor® NCP2820 or equivalent. A 1 µF coupling capacitor is generally used with the Class D amplifier.

C. Driving either a high impedance or a capacitively coupled speaker as low as 16 ohms single-ended. The coupling capacitance can be any value between 10 µF and 100 µF.

Four independent analog gains on each headphone output are provided and can be set to: 1x, 0.5x, 0.333x, and 0.25x.

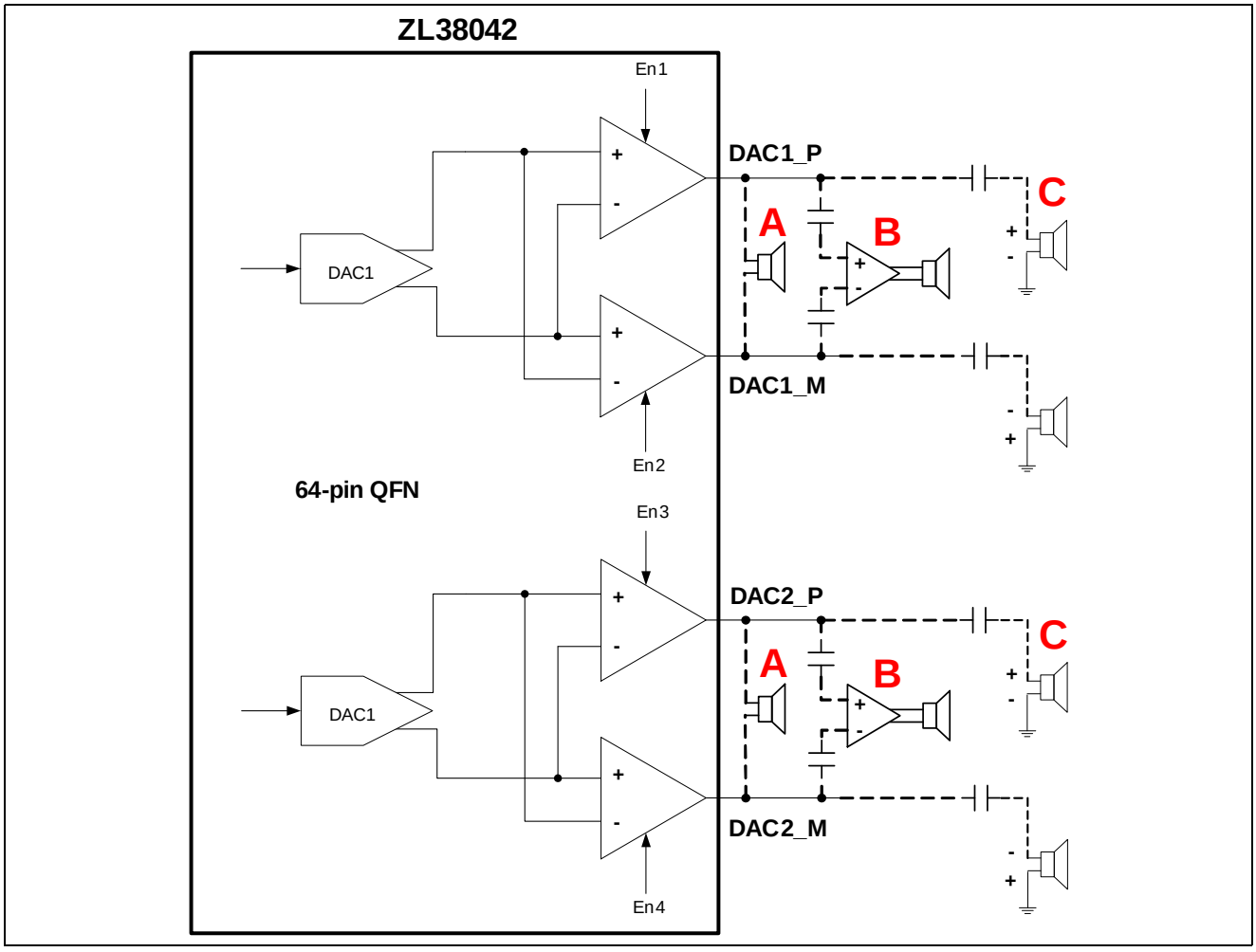


Figure 36 - Audio Output Configurations

12.5 Power Supply Considerations

The ZL38042 requires +1.2 V to power its core DSP power supply (DVDD12). To achieve optimum noise and power performance, supply DVDD12 from an external source. Use an LDO regulator like the Microsemi LX8213 to achieve low noise and low overall power consumption. The ZL38042 is designed to minimize power in its active states when DVDD12 is supplied externally.

To further reduce power when using a crystal or clock oscillator, the internal PLL can be shut-down as described in 12.5.3, “Ultra-Low Power Mode“ on page 55.

12.5.1 External +1.2 V Power

Figure 37 shows DVDD12 powered from an external supply. External supply use is selected when the EXT_SEL pin is tied to +3.3 V. The EXT_SEL pin can be pulled high or simply hard-wired to DVDD33.

VDD12_CTRL is a CMOS output which can be used to control the shutdown of the external supply. VDD12_CTRL will provide a steady +3.3 V output (with up to 4 mA of source current) for the external supply to be enabled and 0 V for the supply to be disabled.

For power savings when the ZL38042 does not need to be operational, the external voltage regulator can be turned off by pulling the $\overline{\text{RESET}}$ pin low for longer than 10 µS (Reset mode). This action will force the VDD12_CTRL pin low, shutting off the external LDO and allowing the +1.2 V supply to collapse to 0 V.

If shutdown of the external +1.2 V supply is not desired, simply leave the VDD12_CTRL output float.

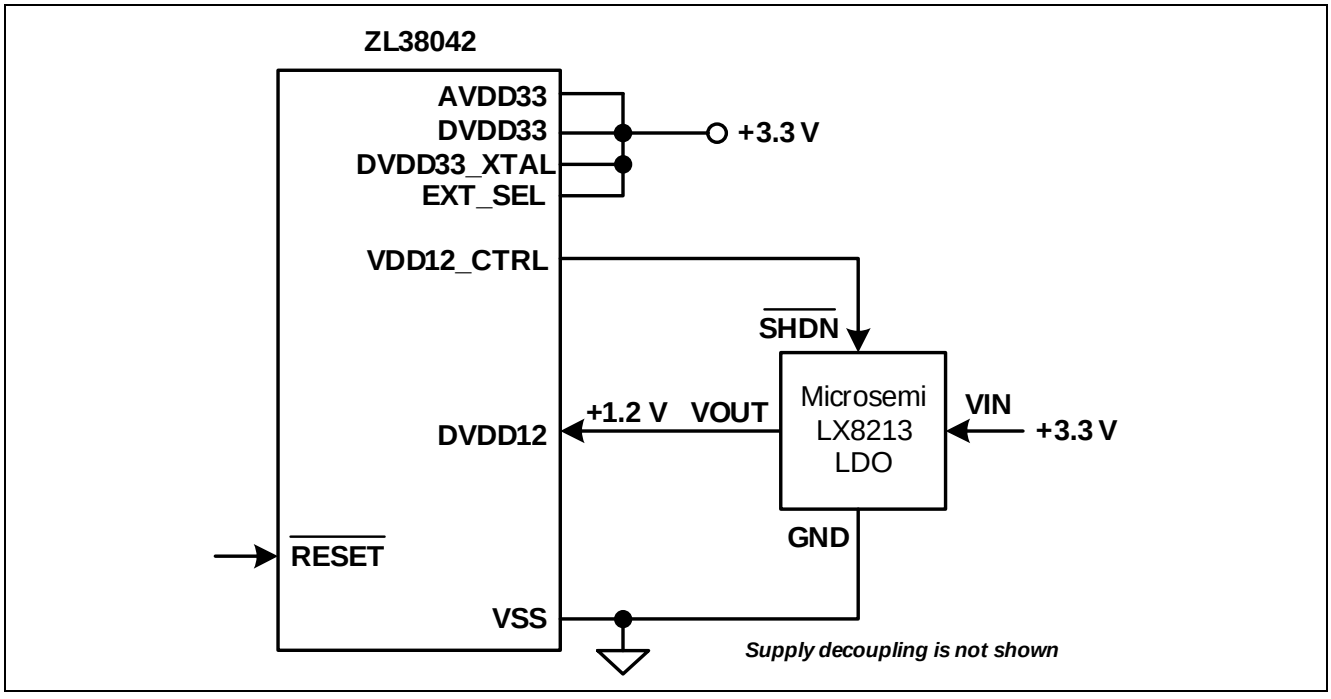


Figure 37 - External +1.2 V Power Supply Configuration

12.5.2 Internal +1.2 V Power

Alternatively, the ZL38042 has a built-in voltage regulator that can be used as the DVDD12 source. The internal voltage regulator requires an external N-channel FET device and a parallel 470 ohm resistor. Figure 38 shows DVDD12 powered from the internal supply. Power dissipation is higher with internal regulator use due to the constant current draw from the 470 ohm resistor and internal control circuitry and functional blocks being active.

Internal supply use is selected when the EXT_SEL pin is tied to VSS. With the built-in voltage regulator enabled, VDD12_CTRL will drive Q1 and generate +1.2 V at DVDD12. The parallel 470 ohm resistor is required to ensure supply start-up. Q1 can be any of the high power FETs shown in Table 19, or an equivalent.

For power savings when the ZL38042 does not need to be operational, the internal voltage regulator can be turned off by pulling the $\overline{\text{RESET}}$ pin low for longer than 10 µS (Reset mode). This action will force the VDD12_CTRL pin low, shutting off the FET and allowing the +1.2 V supply to collapse to 0 V.

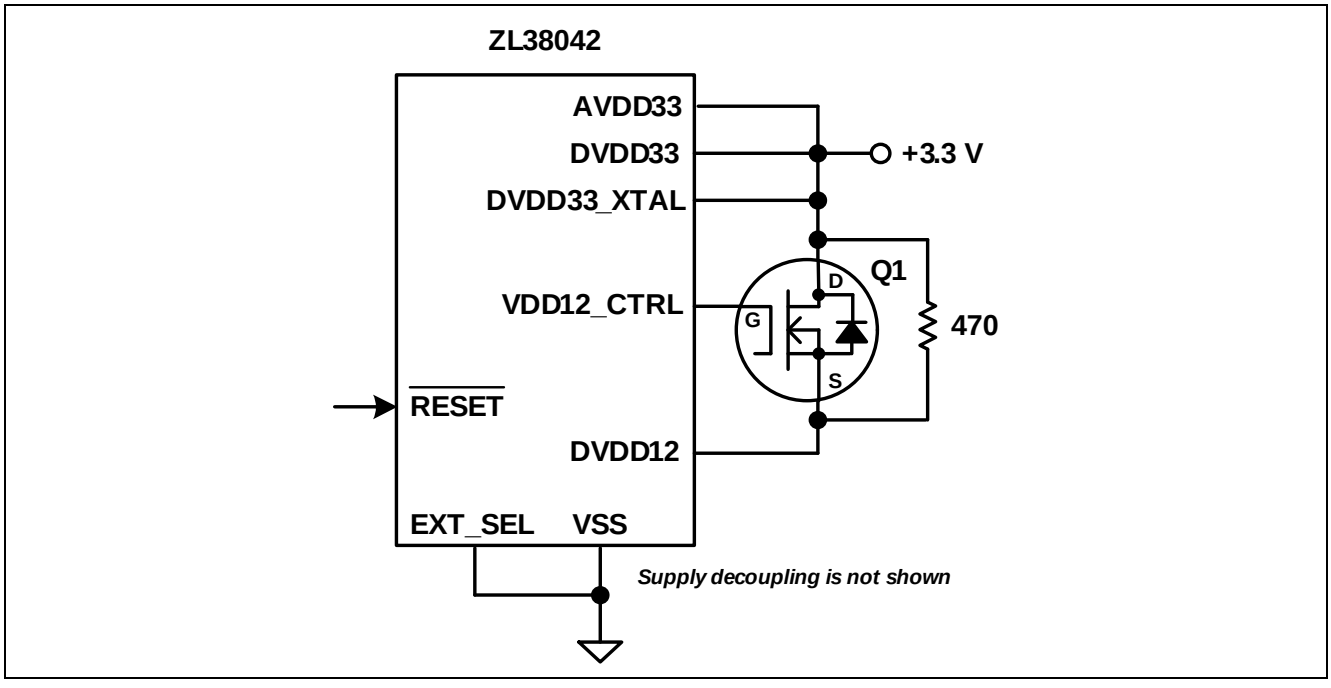


Figure 38 - Internal +1.2 V Power Supply Configuration

Manufacturer	Part Number
Vishay®	Si1422DH
International Rectifier	IRLMS2002
Diodes Inc.®	ZXMN2B03E6

Table 19 - Q1 Component Options

12.5.3 Ultra-Low Power Mode

When using a crystal or clock oscillator, the ZL38042 can be placed into an Ultra-low power state by turning off the internal PLL. The circuit required to perform this is shown in Figure 39.

The external circuit that drives the ZL38042 $\overline{\text{RESET}}$ pin can also be used to power the DVDD33_XTAL pin. The reset drive circuit (gate) needs to provide at least 10 mA of source current when reset is high. The series 100 ohm resistor provides a time delay to keep crystal power from reacting to short reset pulses. When the reset line goes low for longer than 10 µS, the crystal oscillator's internal regulator will turn off and the ZL38042 will draw Ultra-low power as specified in "Power Consumption" on page 32.

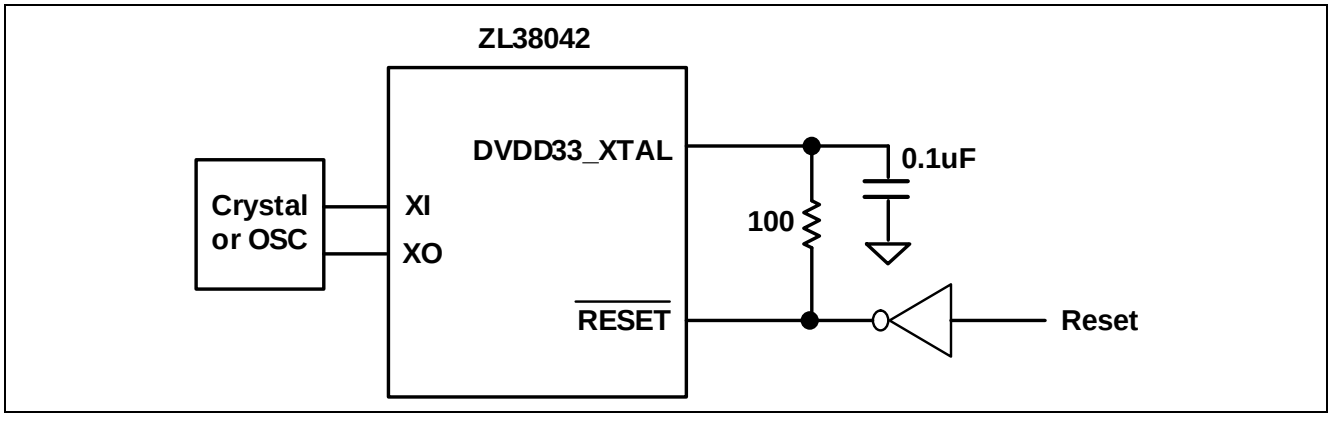


Figure 39 - Ultra-Low Power Operation Circuit

12.6 DAC Bias Circuit

The common mode bias voltage output signal (CREF) for the DAC output buffers must be decoupled through a 0.1 µF (C_{REF1}) and a 1.0 µF (C_{REF2}) ceramic capacitor to VSS. The positive DAC reference voltage output (CDAC) must be decoupled through a 0.1 µF (C_{DAC}) ceramic capacitor to VSS as shown in Figure 40.

All capacitors can have a 20% tolerance and a minimum voltage rating of 6.3 V.

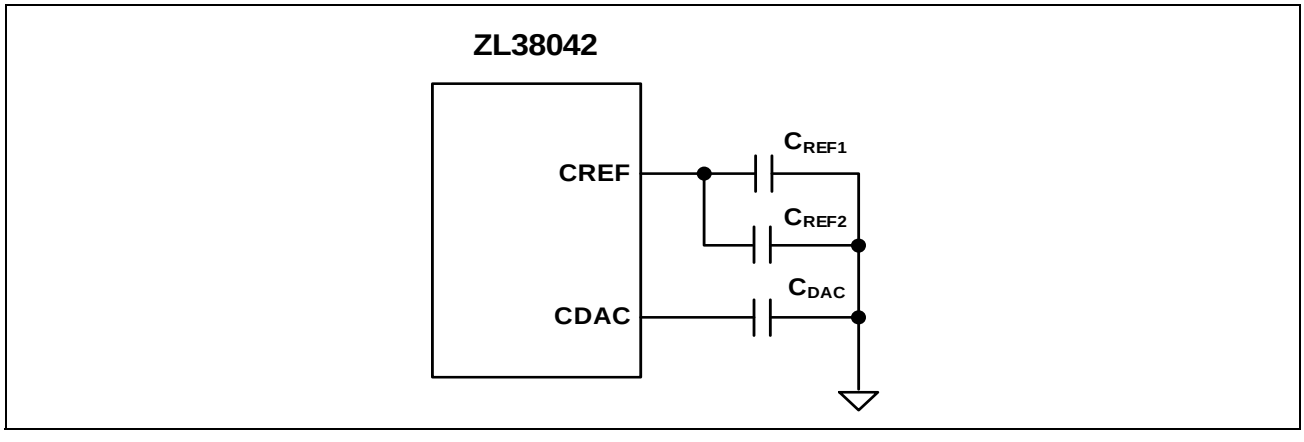


Figure 40 - ZL38042 Bias Circuit

12.7 AEC Auto-Tuning

To optimize the acoustic properties of a given system design, the Audio Processor firmware requires gain and level tuning. The mechanical design, including the speaker and microphone quality and placement, will all affect the system's acoustic performance. Microsemi has developed *MiTuner*™ GUI Software (ZLS38508) and the Microsemi Audio Interface Box (AIB) Evaluation Kit (ZLE38470BADA) to automatically optimize the firmware's tunable parameters for a given hardware design, facilitating the system design process and eliminating the need for tedious manual tuning. The *MiTuner* GUI Software provides step-by-step instructions that allow the software's algorithms to achieve a high level of acoustic performance for a given enclosure.

In order to perform auto-tuning, a mating header for the AIB hardware needs to be provided on the system board. The UART and I^2S (or PCM) ports of the ZL38042 are used for auto-tuning. Figure 41 illustrates the port interface and header details. I^2S port A is shown, but port B can be used instead. The header only needs to be populated on the system board(s) that are used for tuning evaluation.

Any connections to a host processor need to be isolated from the UART and I^2S ports during the auto-tuning process. If a host processor is connected to these ports, a resistor should be placed between the host and each ZL38042 port signal, so that the resistor can be removed to isolate the host from the ZL38042 without interfering with the ZL38042's connection to the AIB.

To interface between the header and the AIB, a 10-wire ribbon cable is used. The cable is terminated on both ends with a double row, 5 position, 100 mil (2.54 mm) female socket strip. Pin 10 on each socket is keyed to ensure proper signal connection. On the system board header pin 10 must be removed, or alternatively both pins 9 and 10 can be eliminated to reduce the space needed on the system board. Signal integrity series termination resistors are provided for the interface in the AIB.

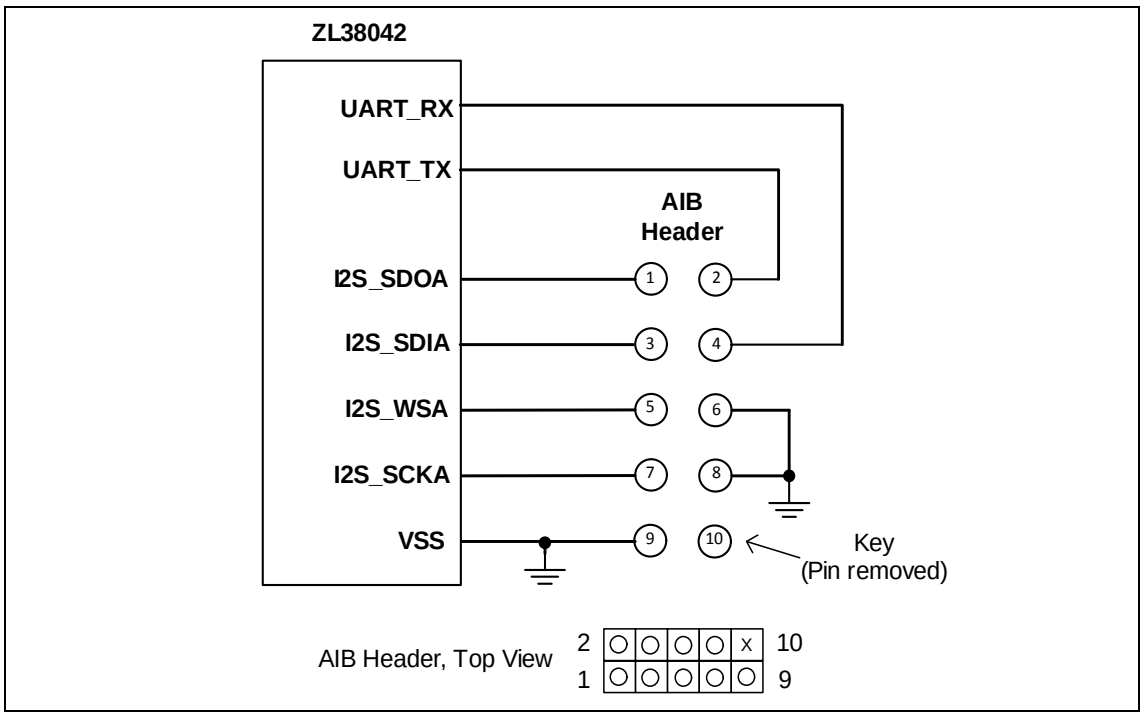
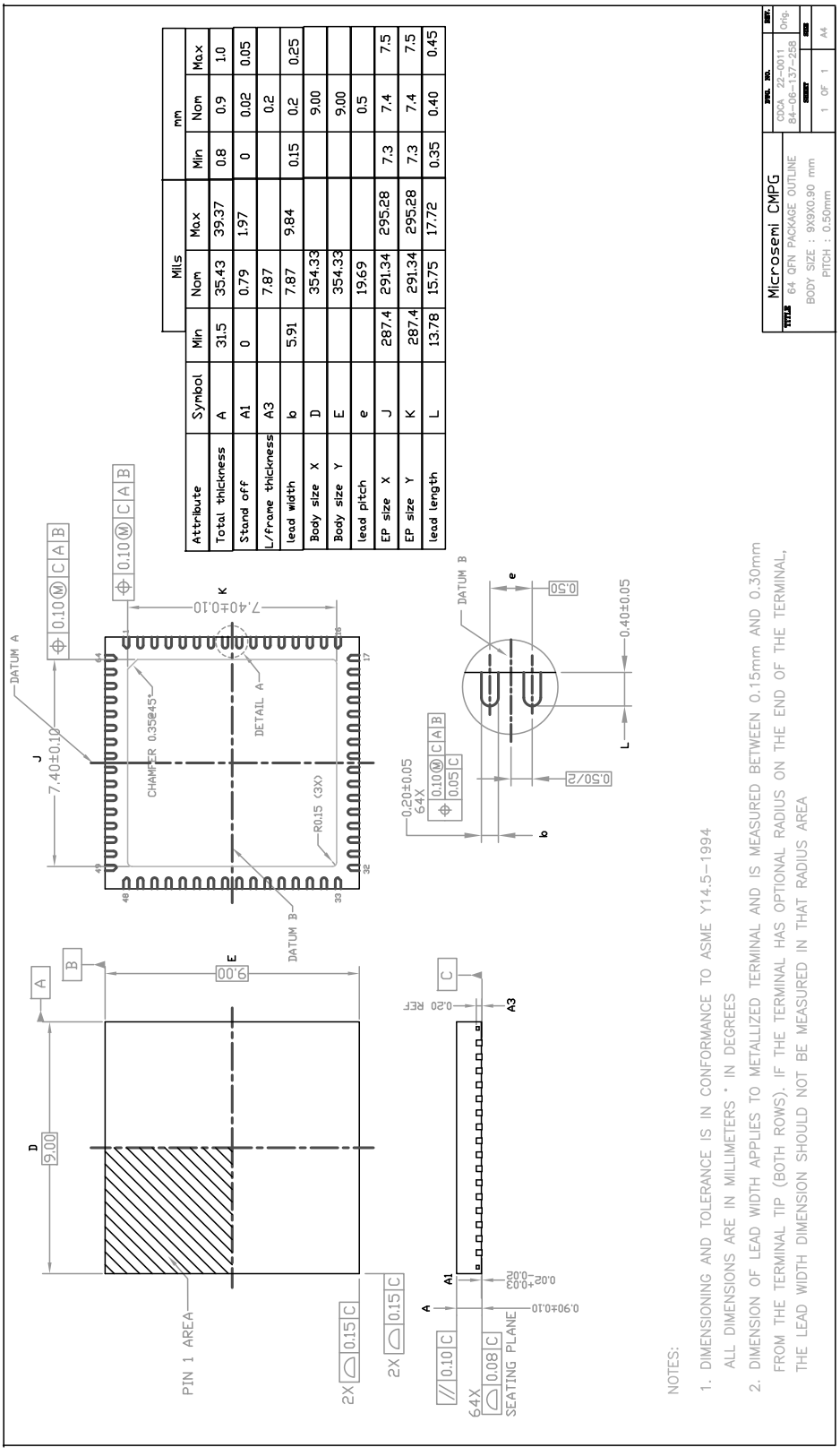


Figure 41 - AIB System Board Connection

Note: A Samtec TSW-105-07-L-D through-hole terminal strip, or a Samtec TSM-105-01-L-DV surface mount terminal strip, or a suitable equivalent can be used for the AIB Header. The header is a double row, 5 position, 10-pin male 100 mil (2.54 mm) unshrouded terminal strip with 25 mil (0.64 mm) square vertical posts that are 230 mils (5.84 mm) in length.

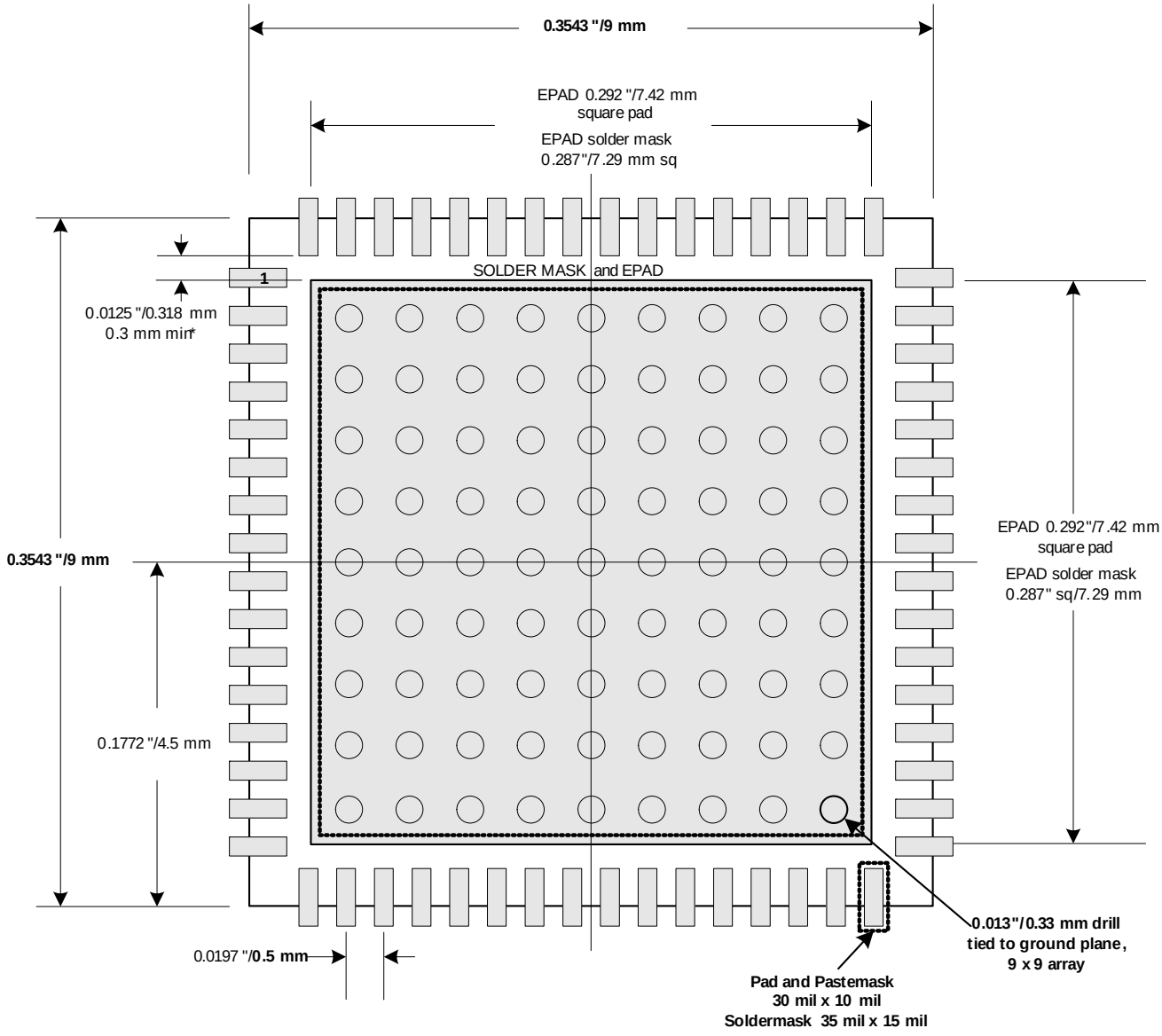
13.0 Package Outline Drawings



Attribute	Symbol	Mils Min	Mils Nom	Mils Max	mm Min	mm Nom	mm Max
Total thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/frame thickness	A3		7.87			0.2	
lead width	b	5.91	7.87	9.84	0.15	0.2	0.25
Body size X	D		354.33			9.00	
Body size Y	E		354.33			9.00	
lead pitch	e		19.69			0.5	
EP size X	J	287.4	291.34	295.28	7.3	7.4	7.5
EP size Y	K	287.4	291.34	295.28	7.3	7.4	7.5
lead length	L	13.78	15.75	17.72	0.35	0.40	0.45

Figure 42 - 64-Pin QFN

The recommended land pattern shows the maximum number of vias that should be used for the exposed pad, fewer vias can be used.



64-QFN
9 mm x 9 mm, 0.5 mm pitch

* Minimum spacing between pins and epad must be 0.3 mm

Recommended EPAD configuration uses 0.292"/7.42 mm square pad tied to a ground plane with a 9 x 9 array of 0.013"/0.33 mm vias. This is necessary for good thermal performance.

Figure 43 - Recommended 64-Pin QFN Land Pattern – Top View

14.0 Revision History

The following table lists substantive changes that were made to this revision of the ZL38042 data sheet.

Changes	Pages
Removed psychoacoustic technique from noise reduction bullet in , “Microsemi AcuEdge Technology ZLS38042 Firmware“.	1
Added Flash and AIB to 3.1, “ZL38042 Slave and Master Mode Operation“ and Figure 2 -, “ZL38042 Slave and Master Mode Operation“.	10
Added to Table 11 “HBI - SPI Slave Port Pin Descriptions“ pin description and fixed pin numbers in Table 16 “Supply and Ground Pin Description“ and Table 17 “No Connect Pin Description“	28, 30
10.5.2, “DAC“ descriptions changed.	34
Figure 30, “Clock Oscillator Application Circuit” drawing changed.	48

Table 20 - List of Changes to the Data Sheet

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