

ZL40122 High Speed, Current Feedback Quad Operational Amplifier

Data Sheet

March 2006

# Features

- 450 MHz small signal bandwidth
- 1500 V/μs slew rate
- 5.2 mA/channel static supply current
- 65 mA output current
- 120 MHz gain flatness to +/- 0. 1dB
- 14 pin SOIC

# Applications

- Video switchers/routers
- Video line drivers
- Twisted pair driver/receiver
- Active filters

# Description

The ZL40122 is a high speed, quad, current feedback operational amplifier offering high performance at a low cost. The device has a very high output current drive capability of 65 mA while requiring only 5.2 mA of static supply current. This feature makes the ZL40122

Ordering Information							
ZL40122/DCA ZL40122/DCB ZL40122DCF1 ZL40122DCE1	14 lead SOIC 14 lead SOIC 14 lead SOIC* 14 lead SOIC*	Tubes Tape & Reel Tape & Reel, Bake & Drypack Tubes, Bake & Drypack					
*Pb Free Matte Tin -40°C to +85°C							

the ideal choice where a high density of high speed devices is required.

The flat gain response to 120 MHz, 450 MHz small signal bandwidth and 1500 V/ $\mu$ s slew rate make the device an excellent solution for video applications such as driving video signals down significant cable lengths.

Other applications which may take advantage of the ZL40122 superior dynamic performance features include low cost high order active filters and twisted pair driver/receivers.

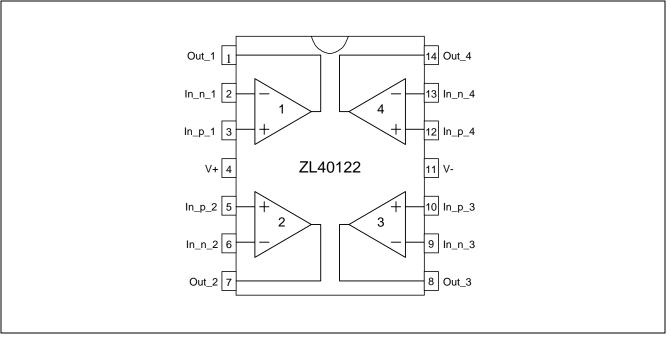


Figure 1 - Functional Block Diagram and Pin Connection

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1

# **Change Summary**

Changes from November 2004 Issue to March 2006 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1		Updated Ordering Information

# **Application Notes**

# **Current Feedback Op Amps**

Current feedback op amps offer several advantages over voltage feedback amplifiers:

- AC bandwidth not dependent on closed loop gain
- High Slew Rate
- Fast settling time

The architecture of the current feedback opamp consists of a high impedance non-inverting input and a low impedance inverting input which is always feedback connected. The error current is amplified by a transimpedance amplifier which can be considered to have gain

$$Z(f) = \frac{Z_o}{1 + j\left(\frac{f}{f_o}\right)}$$

where  $Z_0$  is the DC gain.

It can be shown that the closed loop non-inverting gain is given by

$$\frac{Vout}{Vin} = \frac{Av}{1 + j \left(\frac{fR_f}{f_o Z_o}\right)}$$

where Av is the DC closed loop gain, Rf is the feedback resistor. The closed loop bandwidth is therefore given by

$$BW_{CL} = \frac{f_o Z_o}{R_f} = \frac{GB_{OL}}{R_f}$$

and for low values of closed loop gain Av depends only on the feedback resistor R<sub>f</sub> and not the closed loop gain.

Increasing the value of R<sub>f</sub>

- Increases closed loop stability
- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Reduces overshoot

Using a resistor value of  $R_{f}$ =510  $\Omega$  for Av=+2 V/V gives good stability and bandwidth. However since requirements for stability and bandwidth vary it may be worth experimentation to find the optimal  $R_{f}$  for a given application.

#### **Layout Considerations**

Correct high frequency operation requires a considered PCB layout as stray capacitances have a strong influence over high frequency operation for this de0ice. The Zarlink evaluation board serves as a good example layout that should be copied. The following guidelines should be followed:

- Include 6.8 uF tantalum and 0.1 uF ceramic capacitors on both positive and negative supplies
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitances
- Minimize all trace lengths to reduce series inductance

# **Application Diagrams**

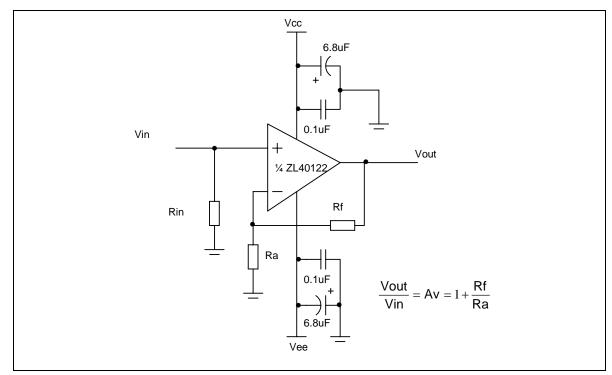


Figure 2 - Non-inverting Gain

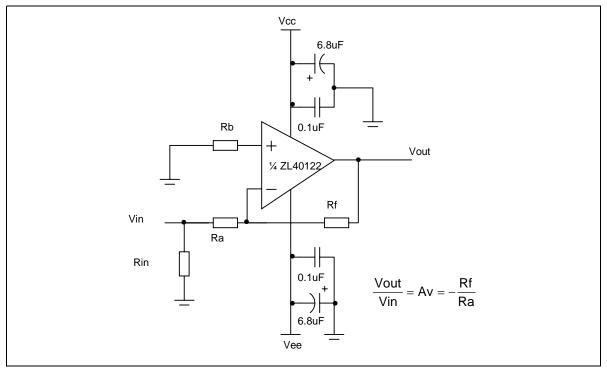


Figure 3 - Inverting Gain

# **Absolute Maximum Ratings**

	Parameter	Symbol	Min.	Max.	Units
1	Vin Differential	V <sub>IN</sub>		±1.2	V
2	Output Short Circuit Protection	V <sub>OS/C</sub>		See Apps Note in this data sheet	
3	Supply voltage	V+, V-		±6.5	V
4	Voltage at Input Pins	V <sub>(+IN)</sub> , V <sub>(-IN)</sub>	V-	V+	V
5	Voltage at Output Pins	Vo	V-	V+	V
6	EDS Protection (HBM Human Body Model) (see Note 2)		2	(see Note 3)	kV
7	Storage Temperature		-55	+150	°C
8	Latch-up test		±100 mA for 100 ms	(see Note 4)	
9	Supply transient test		20% pulse for 100 ms	(see Note 5)	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k $\Omega$  in series with 100 pF. Machine model, 20  $\Omega$ in series with 100 pF.

Note 3: 0.8 kV between the pairs of +INA, -INA and +INB pins only. 2 kV between supply pins, OUTA or OUTB pins and any input pin.

Note 4: ±100 mA applied to input and output pins to force the device to go into "latch-up". The device passes this test to JEDEC spec

Note 5: Positive and Negative supply transient testing increases the supplies by 20% for 100 ms.

# **Operating Range**

17.

Characteristic	Min.	Тур.	Max.	Units	Comments
Supply Voltage (Vcc)	±4.0		±6.0	V	
Operating Temperature (Ambient)	-40		+85	°C	
Junction to Ambient resistance	Rth(j-a)	150		°C	
				4 layer	
				FR4 board	
Junction to Case resistance	Rth(j-c)	60		°C	
				4 layer	
				FR4 board	

**Electrical Characteristics** - Vcc= $\pm$ 5 V, T<sub>amb</sub>=25C(typ.),T<sub>amb</sub>=-40C to +85C(min-max), Av=+2V/V, Rf=510  $\Omega$ , Rload=100  $\Omega$  unless specified.

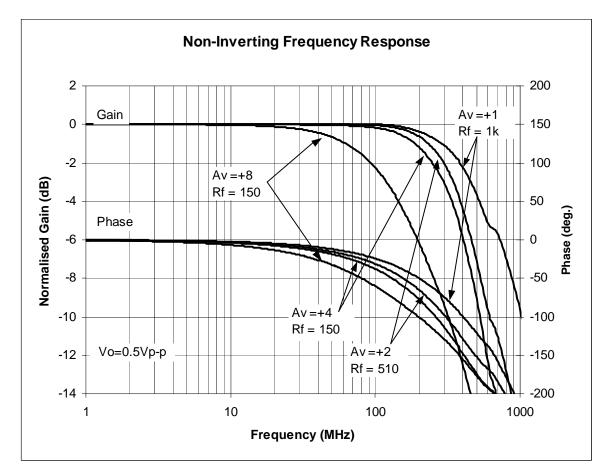
Characteristic	Conditions	Тур 25С	Min/ Max 25C	Min/ Max 40 to +85C	Units	Test Type <sup>1</sup>
Frequency Domain Response			1		1	
-3 dB Bandwidth	Av=+1; Vo < 0.5 Vp-p; Rf=1.5 kΩ	450	-	-	MHz	С
	Av=+2; Vo < 0.5 Vp-p; Rf=510 Ω	380	-	-	MHz	С
	Av=+2; Vo < 5 Vp-p; Rf=510 Ω	170	-	-	MHz	С
+/- 0.1 dB Flatness	Av=+2; Vo < 0.5 Vp-p; Rf=510 Ω	120	-	-	MHz	С
Differential Gain (NTSC)	Rload=150 Ω	0.01	-	-	%	С
Differential Phase (NTSC)	Rload=150 Ω	0.015	-	-	deg.	С
Time Domain Response	l					
Rise and Fall Time	Vout=0.5 V Step	1	-	-	ns	С
	Vout=5 V Step	2.8	-	-	ns	С
Settling Time to 0.1%	Vout=2 V Step	6	-	-	ns	С
Overshoot	Vout=0.5 V Step	4	-	-	%	С
Slew Rate	Vout=5 V Step	1500	-	-	V/µs	С
Noise and Distortion		•				
2 <sup>nd</sup> Harmonic Distortion	Vout=2 Vp-p, 1 MHz	-84	-	-	dBc	С
3 <sup>nd</sup> Harmonic Distortion	Vout=2 Vp-p, 1 MHz	-85	-	-	dBc	С
Equivalent Input Noise						
Voltage	>1 MHz	5.5	-	-	nV√Hz	С
Non-Inverting Current	>1 MHz	1.3	-	-	<sup>pV</sup> √Hz	С
Inverting Current	>1 MHz	11	-	-	<sup>pA</sup> √Hz	С
Static, DC Performance					•	
Input Offset Voltage		2.7	±6.3	±7.7	mV	А
Average Drift		-	-	15	μV/deg. C	С
Input Bias Current – Non-inverting		2.6	±5.6	±6	uA	А
Average Drift		-	-	6	nA/deg. C	С

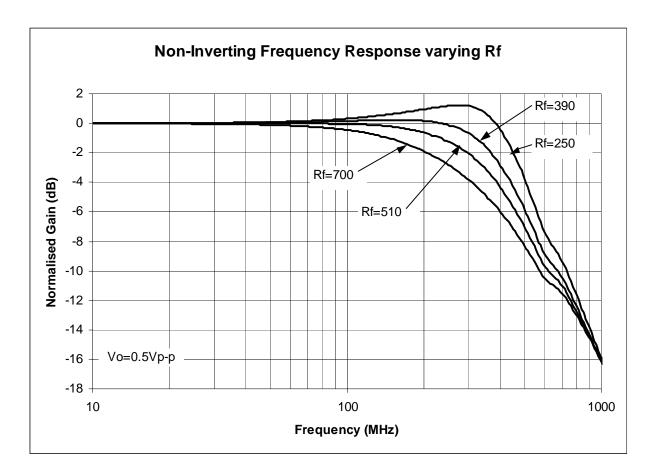
Characteristic	Conditions	Тур 25С	Min/ Max 25C	Min/ Max -40 to +85C	Units	Test Type <sup>1</sup>
Input Bias Current – Inverting		7.4	±25	±28	μΑ	А
Average Drift		-	-	15	nA/deg. C	С
Power Supply Rejection Ratio (+ve)	DC	61	58	57	dB	A
Power Supply Rejection Ratio (-ve)	DC	58	56	55	dB	A
Common Mode Rejection Ratio	DC	54	50	49	dB	А
Supply Current (per Channel)	Quiescent	5.2	6.5	6.7	mA	А
Miscellaneous Performance	•					
Input Resistance (Non-inverting)		8	-	-	MΩ	С
Input Capacitance (Non-inverting)		1	-	-	pF	С
Common Mode Input Range		±2.4	±2.2	±2.0	V	А
Output Voltage Range	Rload=100 $\Omega$	±2.8	±2.7	±2.6	V	А
Output Current (max)		65	-	-	mA	С
Output Resistance, Closed Loop	DC	90	-	-	mΩ	С

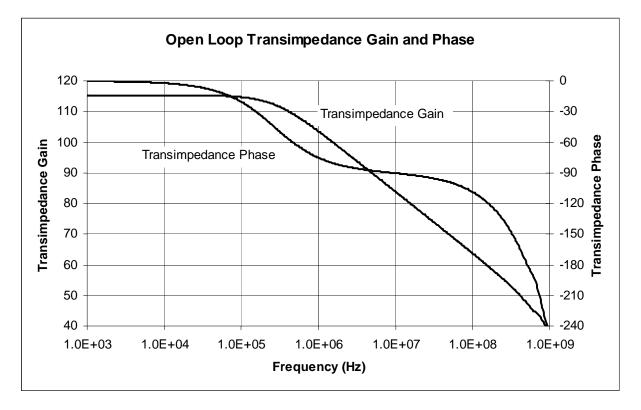
Note: Test Types:

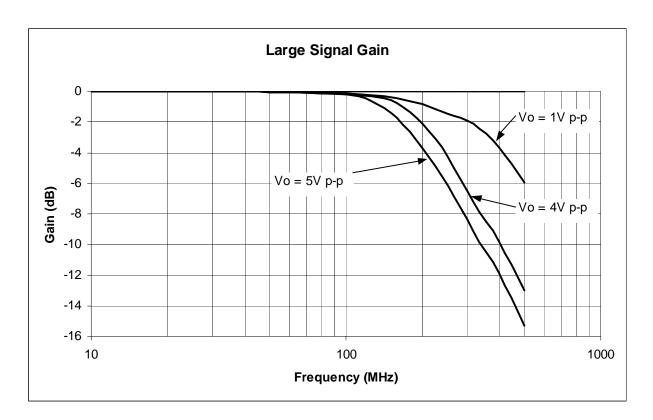
(A) 100% tested at 25°C. Over temperature limits are set by characterization and simulation.
(B) Limits set by characterization or simulation.
(C) Typical value only for information.

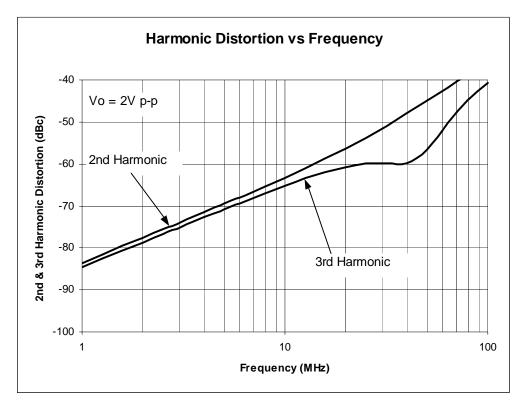
**Typical Performance Characteristics -**  $T_{amb}$ =25degC,  $V_{supply}$ =± 5 V, Rload=100  $\Omega$ , Av=+2V/V, Rf=510  $\Omega$ , unless otherwise specified.

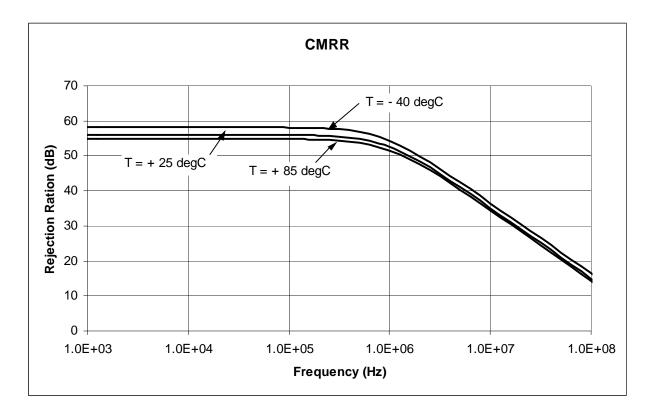


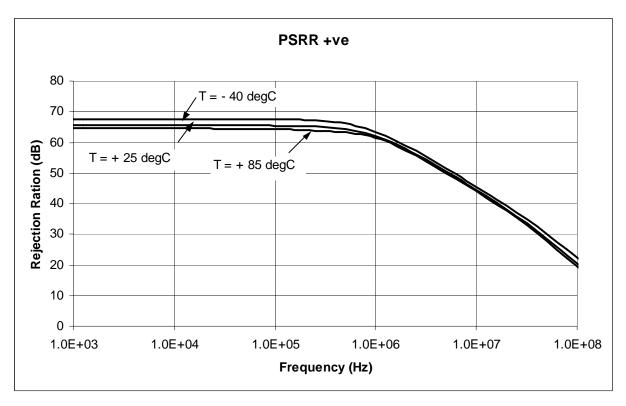


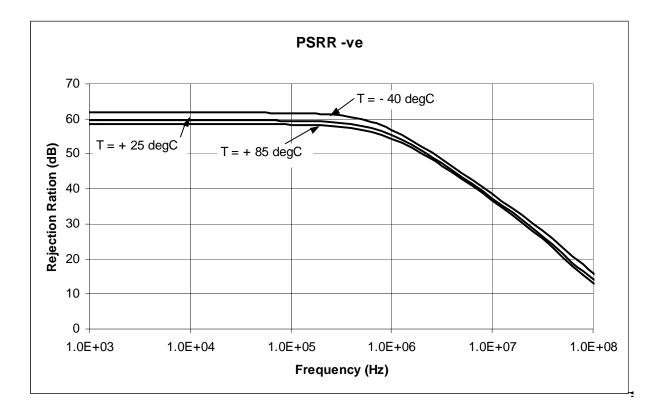


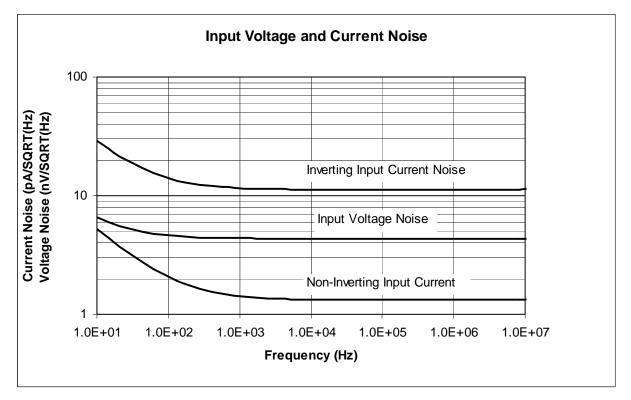


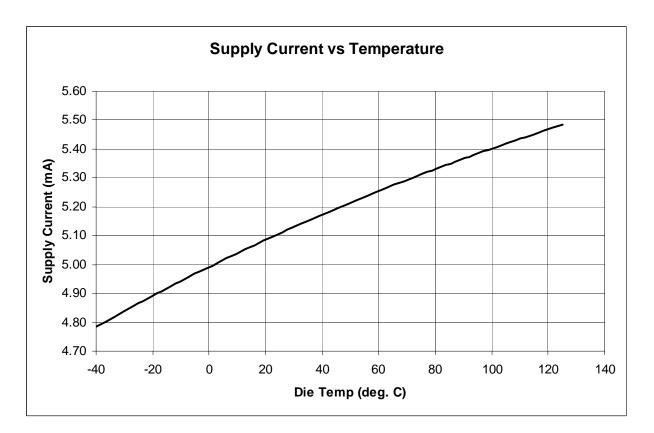


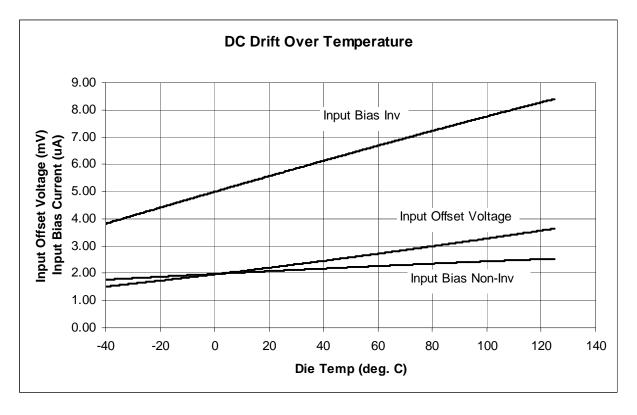


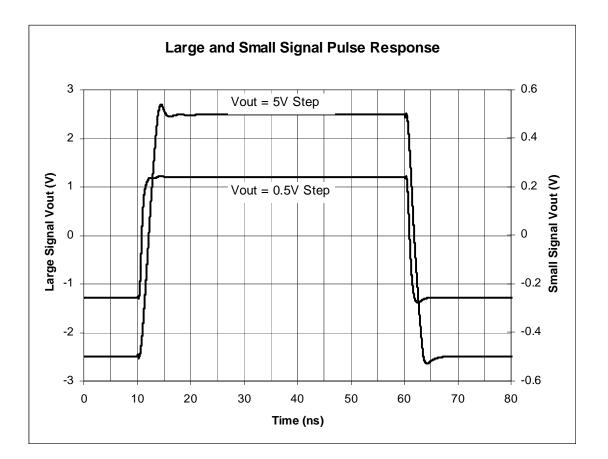


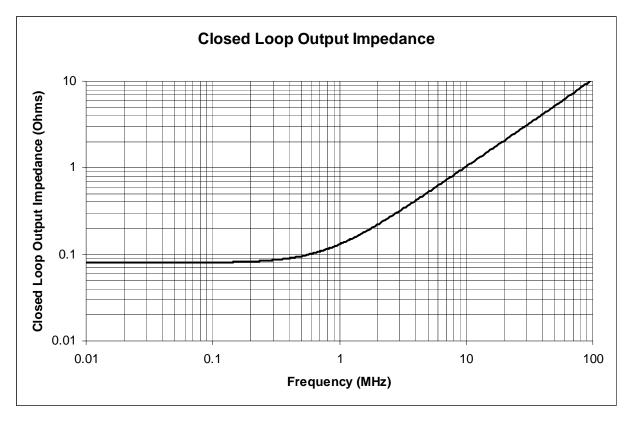


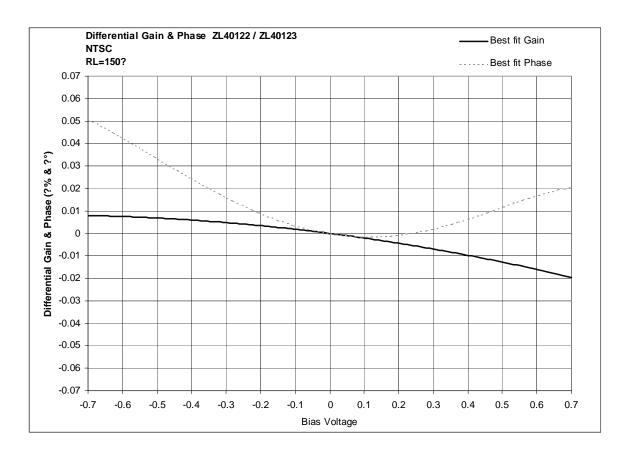


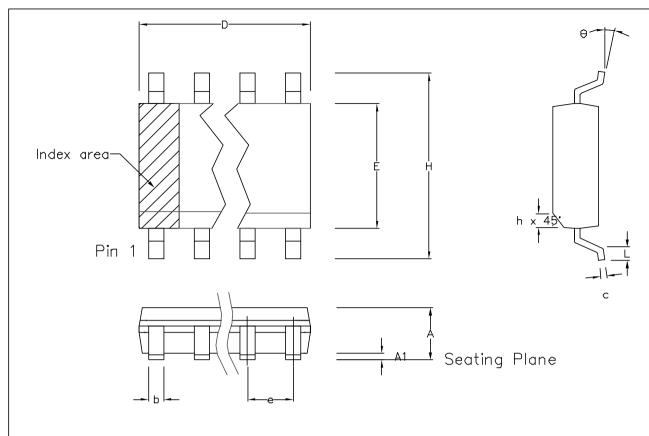












	Min	Max	Min	Max			
	mm	mm	inch	inch			
A	1.35	1.75	0.053	0.069			
A1	0.10	0.25	0.004	0.010			
D	8.55	8.75	0.337	0.344			
<u> </u>	5.80	6.20	0.228	0.244			
E	3.80	4.00	0.150	0.157			
L	0.40	1.27	0.016	0.050			
е	1.27	BSC	0.050 BSC				
b	0.33	0.51	0.013	0.020			
С	0.19	0.25	0.008	0.010			
0	٥°	රී	°()	8°			
h	0.25	0.50	0.010	0.020			
	Pin Features						
N	1	4					
Conforms to JEDEC MS-012AB Iss. C							

# Notes:

- 1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
- 2. Controlling dimensions are in inches.
- 3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
- 4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
- 5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ISSUE	6	2	3	4	5			Previous package codes	Package Outline for
ACN	214220	201937	202596	203707	212430		ZARLINK SEMICONDUCTOR	MP / S	14 lead SOIC (0.150" Body Width)
DATE	7Apr03	27Feb97	12Jun97	9Dec97	25Mar02				
APPRD.									GPD00011



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