20-Output PCIe Gen 1, 2, 3, 4 and 5 Buffer with Ultra-Low Additive Jitter

Features

- Fully Compliant with PCIe Gen 1, 2, 3 , 4, and 5.
- 20 Low-Power Push-Pull HCSL PCIe Outputs
- Ultra-low additive jitter: 10fs for PCIe 5.0
- Supports clock frequencies from 0 to 250MHz
- Supports 3.3V power supplies
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 50ps
- SMBus Interface
- Side-Band Interface (SBI)
- Eight OE pins
- Embedded series termination resistors for 100Ω differential transmission line
- Transparent for Spread Spectrum Clock

Ordering Information

ZL40295LDG6	80 pin GQFN	Trays
ZL40295LDF6	80 pin GQFN	Tape and Reel

Package size: 6 x 6 mm

-40°C to +85°C

Applications

- PCI Express generation 1/2/3/4/5 clock distribution
- Intel QPI
- Servers
- Storage and Data Centers
- Switches and Routers

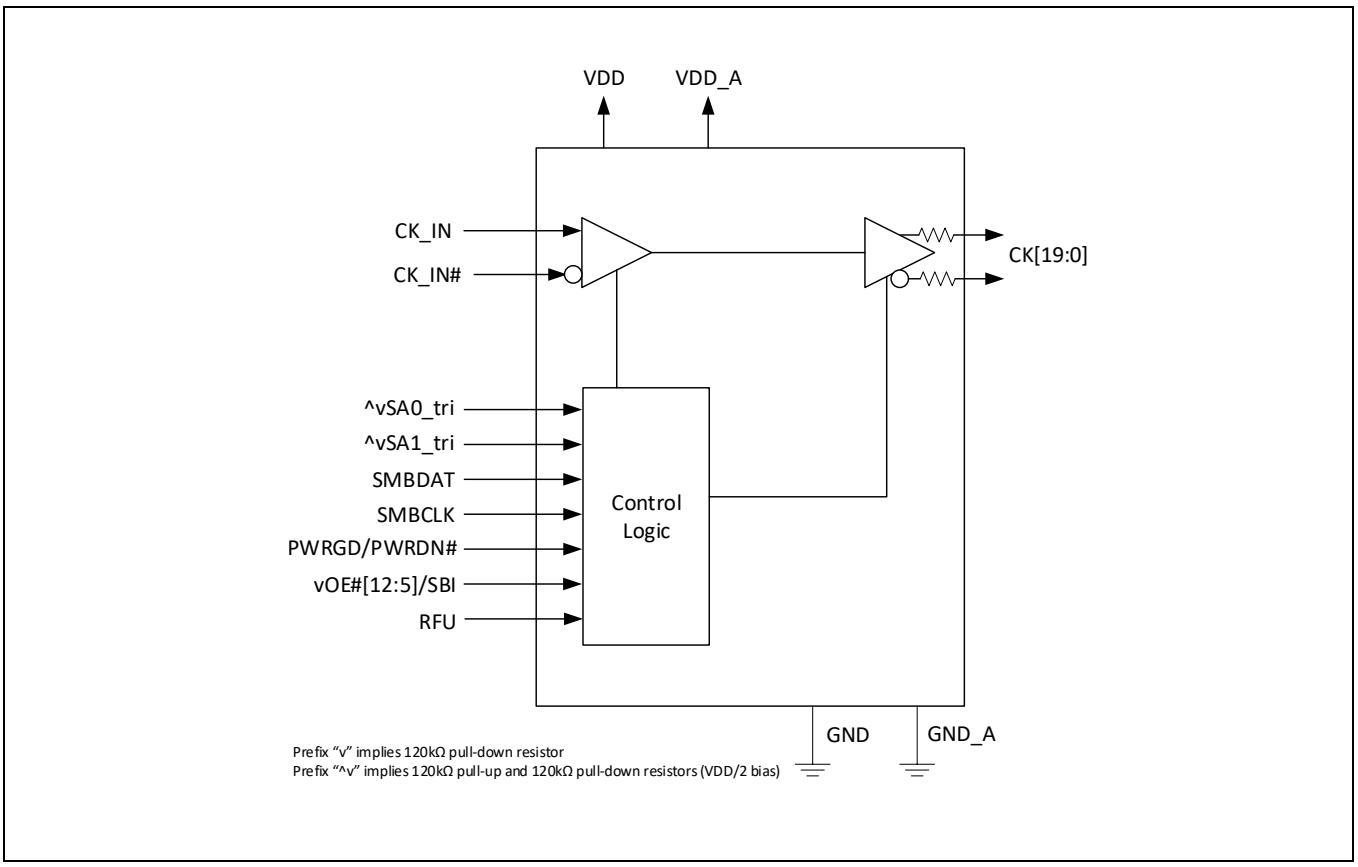

Figure 1. Functional Block Diagram

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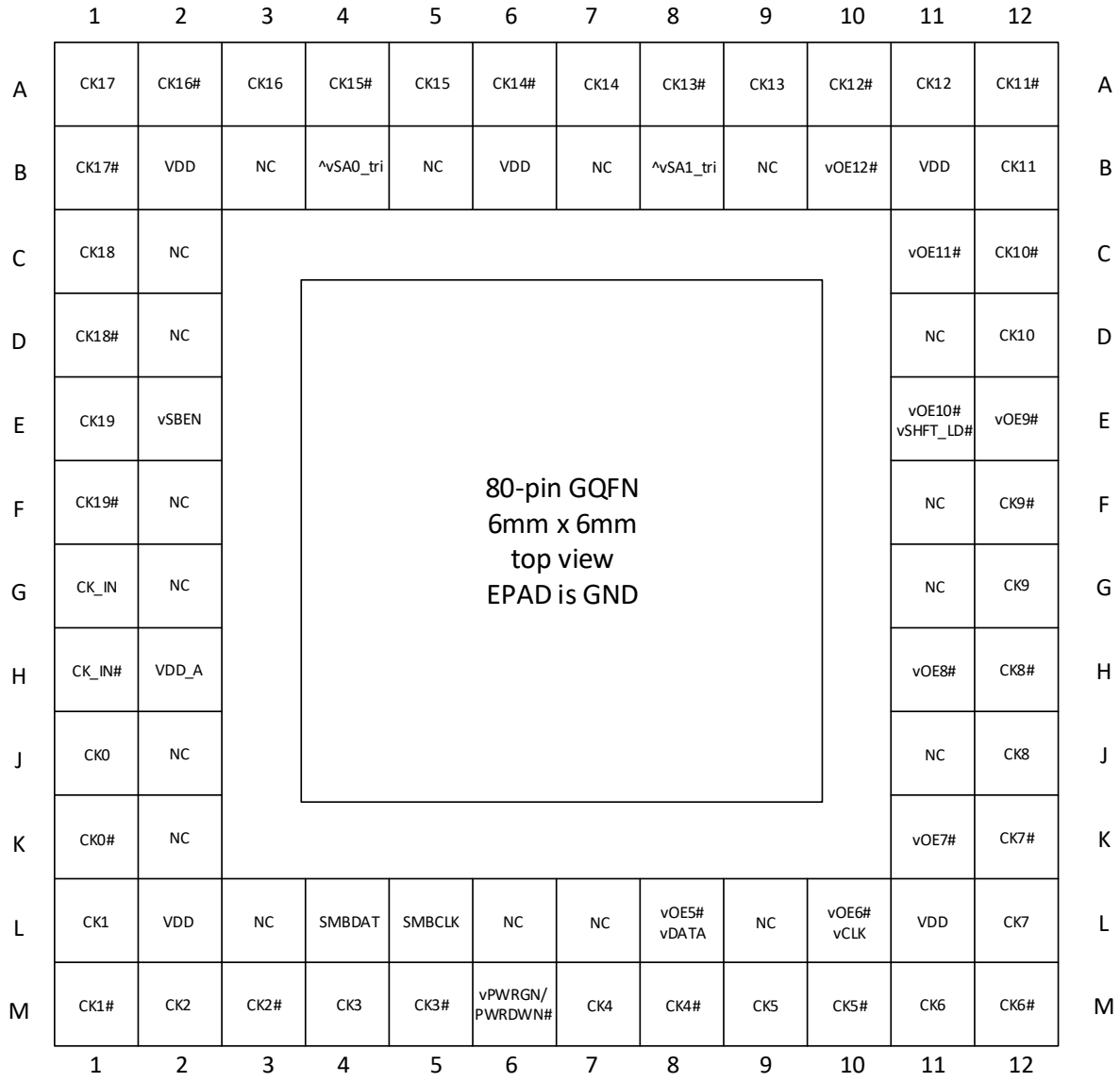
Pin Diagram

The device is packaged in a 6x6mm 80-pin GQFN.



Prefix “v” implies 120kΩ pull-down resistor
Prefix “^v” impies 120kΩ pull-up and 120kΩ pull-down resistors (VDD/2 bias)

Figure 2. Pin Diagram

Pin Descriptions

The I/O column uses the following symbols: I – input, I_{PU} – input with 120kΩ internal pull-up resistor, I_{PD} – input with 120kΩ internal pull-down resistor, O – output, I/O – Input/Output Drain pin, NC-No connect pin, P – power supply pin, . I_{TRI} – Tri-level input pin biased to VDD/2 by internal 120kΩ pull-up and 120kΩ pull-down resistors.

Table 1Pin Descriptions

#	Name	I/O	Description
Input Reference			
G1 H1	CK_IN CK_IN#	I	**Input Differential or Single Ended Reference** Input frequency range 0Hz to 250MHz.
Output Clocks			
J1 K1 L1 M1 M2 M3 M4 M5 M7 M8 M9 M10 M11 M12 L12 K12 J12 H12 G12 F12 D12 C12 B12 A12 A11 A10 A9 A8 A7 A6 A5 A4	CK0 CK0# CK1 CK1# CK2 CK2# CK3 CK3# CK4 CK4# CK5 CK5# CK6 CK6# CK7 CK7# CK8 CK8# CK9 CK9# CK10 CK10# CK11 CK11# CK12 CK12# CK13 CK13# CK14 CK14# CK15 CK15#	O	**Ultra-Low Additive Jitter Differential Outputs 0 to 19** Output frequency range 0 to 250MHz

A3 A2 A1 B1 C1 D1 E1 F1	CK16 CK16# CK17 CK17# CK18 CK18# CK19 CK19#		
Hardware Control			
K11 H11 E12 C11 B10	vOE7# vOE8# vOE9# vOE11# vOE12#	I_{PD}	**Output Enable.** Logic level on these pins enables/disables corresponding output. OE_n# = 0: CKn/n# Active OE_n# = 1: CKn/n# Low/Low both pulled low by 42.5 Ω
L8	vOE5#/vDATA	I_{PD}	**Output Enable/ Data input for Side Band Interface** When Side-Band interface is disabled (pin SBEN pulled low) this pin is Output Enable and the description is the same as for pin K11 above. When Side-Band interface is enabled (pin SBEN pulled high) this pin is Data Input for Side-Band interface.
L10	vOE6#/vCLK	I_{PD}	**Output Enable/ Clock input for Side Band Interface** When Side-Band interface is disabled (pin SBEN pulled low) this pin is Output Enable and the description is the same as for pin K11 above. When Side-Band interface is enabled (pin SBEN pulled high) this pin is Clock Input for Side-Band interface.
E11	vOE10#/ vSHFT_LD#	I_{PD}	**Output Enable/ Shift load for Side Band Interface** When Side-Band interface is disabled (pin SBEN pulled low) this pin is Output Enable and the description is the same as for pin K11 above. When Side-Band interface is enabled (pin SBEN pulled high) this pin is Shift Load Input for Side-Band interface. A falling edge on this pin transfers the sideband shift register content to the output register.
E2	vSBEN	I_{PD}	**Side-Band Interface Enable** When this pin is low, the Side-Band interface is disabled and OE pins and OE Register bits (via SMBus) can be used to enable/disable outputs. When this pin is high, the Side-Band interface can be used to enable/disable outputs, and OE pins and OE Register bits (via SMBus) are disabled.
M6	PWRGD/PWRDN#	I	**Power up / power down**
SMBus Control			
L5	SMBCLK	I	**SMBus slave clock input**

L4	SMBDAT	I/O	**Input/Open drain SMBus data**
B4 B8	^vSADR0_tri ^vSADR1_tri	I_{TRI}	**Tri level address selection inputs**
Power and Ground			
B2 B6 B11 L2 L11	VDD	P	**Positive Supply Voltage.** Connect to 3.3V supply.
H2	VDD_A	P	**Positive Analog Supply Voltage** Connect 3.3V power supply.
E-Pad	GND	P	**Ground.** Connect to ground
No Connect Pins			
B3 B5 B7 B9 C2 D2 D11 F2 F11 G2 G11 J2 J11 K2 L3 L6 L7 L9	N/C		**No Connect.** These pins are not connected to the die. Leave them open.

Functional Description

The ZL40295 is an ultra-low additive jitter, low power 1 to 20 fanout buffer which is fully compliant with PCIe Gen 1, 2, 3,4 and 5 Standards.

The device operates from 3.3V+/-5% supply and over the industrial temperature range -40°C to +85°C.

Clock Inputs

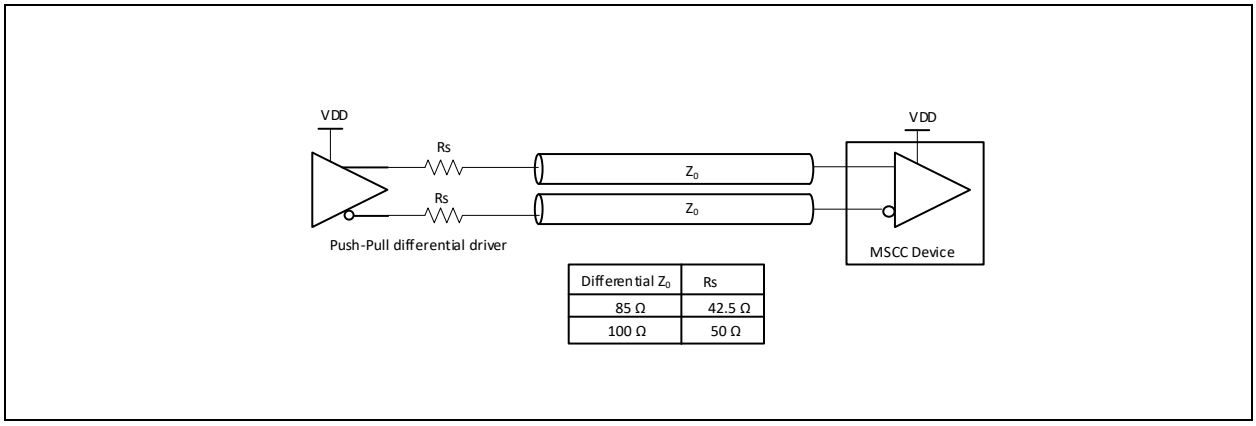
The following blocks diagram shows how to terminate different signals fed to the inputs of ZL40295 device.

The device input can be fed with transmission lines of any impedance. Examples below show only 50Ω single ended, 85 Ω differential and 100 Ω differential which are the most common ones in practice. Figure 3 and Figure 4 show how to terminate the input when driven from a push-pull and traditional HCSL drivers respectively.

Figure 5 shows how to terminate a single ended output such as LVCMOS. This example assumes 50 Ω transmission line which is the most common for single ended CMOS signaling. Ideally, resistors R1 and R2 should be 100Ω each and Ro + Rs should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing

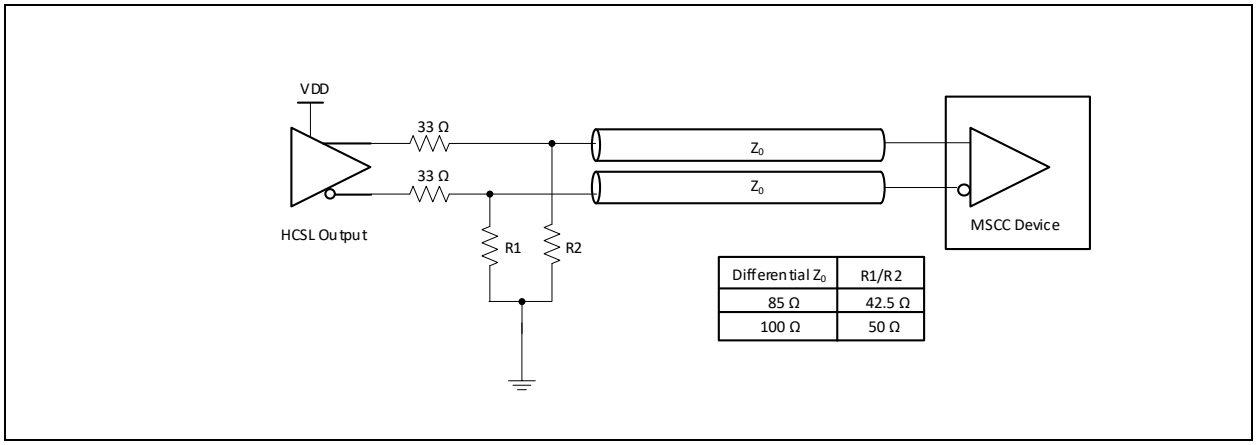
requirement is not violated (Figure 5). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.



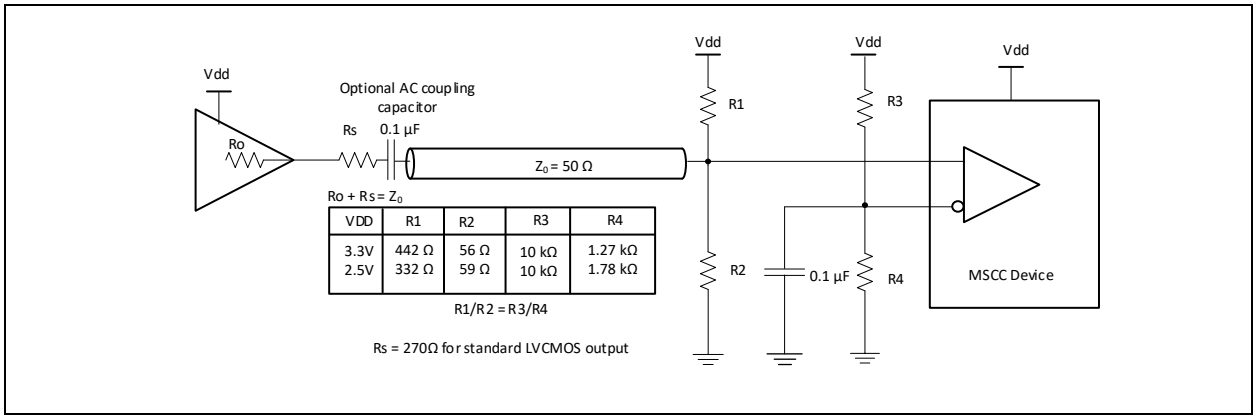
Differential Z_0	Rs
85 Ω	42.5 Ω
100 Ω	50 Ω

Figure 3. Input driven by a push-pull differential output



Differential Z_0	R1/R2
85 Ω	42.5 Ω
100 Ω	50 Ω

Figure 4. Input driven by an HCSL output



VDD	R1	R2	R3	R4
3.3V	442 Ω	56 Ω	10 kΩ	1.27 kΩ
2.5V	332 Ω	59 Ω	10 kΩ	1.78 kΩ

Figure 5. Input driven by a single ended output

Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 6. This provides significant saving relative to traditional current based HCSL outputs which require four resistors per differential pair (80 resistors for 20 outputs).

Embedded termination resistors in ZL40295 are matched for 100Ω differential transmission line.

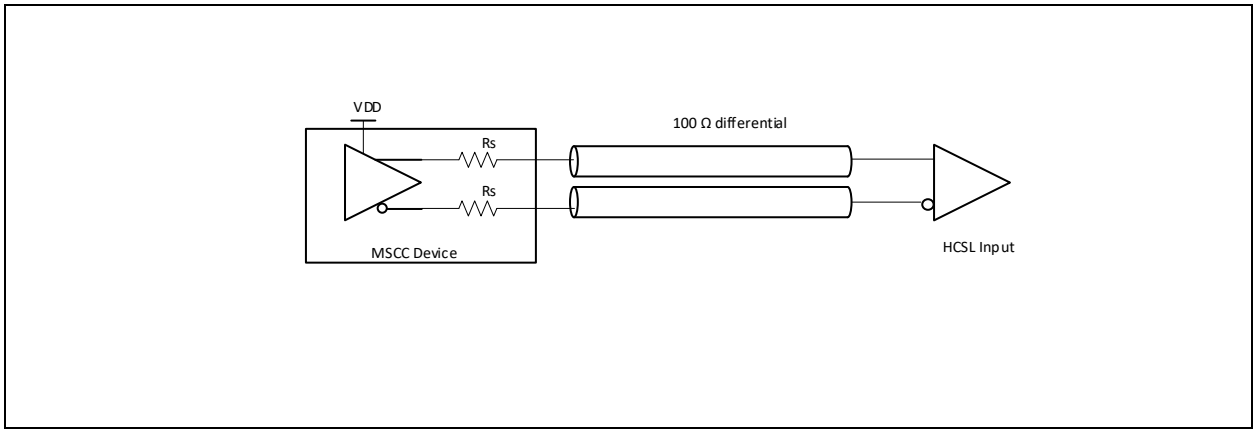


Figure 6. Terminating differential outputs.

Termination of unused outputs

Unused outputs should be left unconnected.

Power Supply Filtering

Each power pin (VDDA and VDD) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low DC resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling.

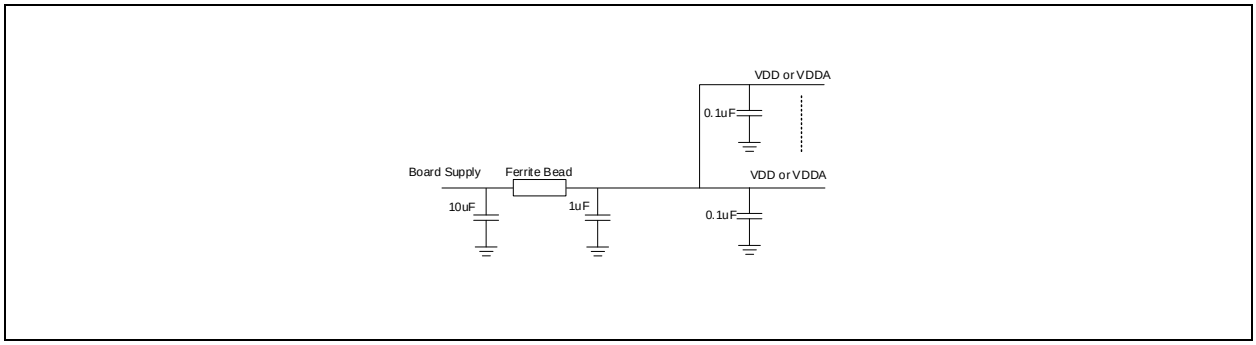


Figure 7. Power Supply Filtering

OE# and Output Enables (Control Register)

Each output can be individually enabled or disabled by SMBus control register bits or via OE# pin. The OE# pins are asynchronous asserted-low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

OE# pins are mapped to CK[12:5] outputs.

Note that the logic level for assertion or de-assertion is different in software than it is on hardware. This follows hardware default nomenclature for communication channels (e.g., output is enabled if OE# pin is pulled low) and still maintains software programming logic (e.g., output is enabled if OE register is true).

Refer to Table 2 for the truth table for enabling and disabling outputs via hardware and software. Note that both the control register bit must be a ‘1’ AND the OE# pin must be a ‘0’ for the output to be active.

Table 2 OE Functionality

Inputs		OE# Hardware Pins and Control Register Bits			
PWRGD/ PWRDN#	CK_IN/ CK_IN#	SMBUS Enable Bit	OE# Pin	CK/CK# [12:5]	CK/CK# [4:0] and [19:13]
0	X	X	X	0	0
1	Running	0	X	0	0
		1	0	Running	Running
		1	1	0	Running

OE# Assertion (Transition from ‘1’ to ‘0’)

All differential outputs that were disabled are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 0 - 10 CK clock periods.

OE# De-Assertion (Transition from '0' to '1')

The impact of de-asserting OE# is each corresponding output will transition from normal operation to disabled in a glitch free manner. A minimum of four valid clocks will be provided after the de-assertion of OE#. The maximum latency from the de-assertion to disabled outputs is 10 CK clock periods.

PWRGD / PWRDN#

PWRGD is asserted high and de-asserted low. De-assertion of PWRGD (pulling the signal low) is equivalent to indicating a powerdown condition. PWRGD (assertion) is used by the ZL40295 to sample initial configurations such as SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin which is used to disable (drive low/low) all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDN# is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

The assertion and de-assertion of PWRDN# is asynchronous.

Disabling of the CK_IN input clock prior to assertion of PWRDN# is an undefined mode and not recommended. Operation in this mode may result in glitches.

Table 3 PWRGD / PWRDN# Functionality

PWRGD / PWRDN#	CK	CK#
0	LOW	LOW
1	Normal	Normal

PWRDN# Assertion

When PWRDN# is sampled low by two consecutive rising edges of CK#, all differential outputs will be disabled on the next CK# high to low transition.

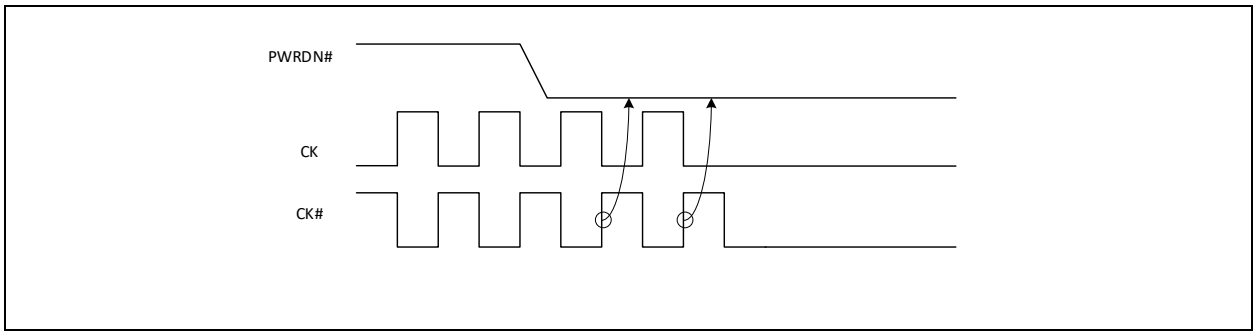


Figure 8. PWRDN# Assertion

PWRGD Assertion

PWRGD to the clock buffer should not be asserted before V_{DD} reaches V_{DDmin}. Prior to V_{DDmin} it is recommended to hold PWRGD low (less than 0.5 V)

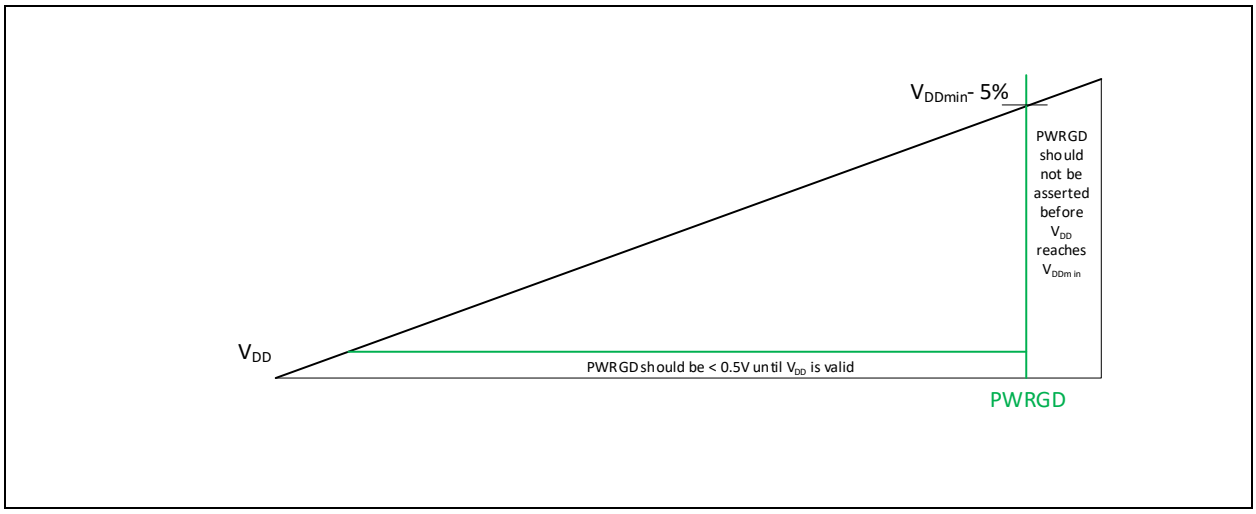


Figure 9. PWRGD and V_{DD} Relationship diagram

The power-up latency Tstable is to be less than 1.8 ms. This is the time from the valid CK_IN input clocks and the assertion of the PWRGD signal to the time that stable clocks are output from the buffer chip. All differential outputs stopped in a disabled condition resulting from power down must be driven high in less than 300 µs of PWRGD assertion to a voltage greater than 200 mV.

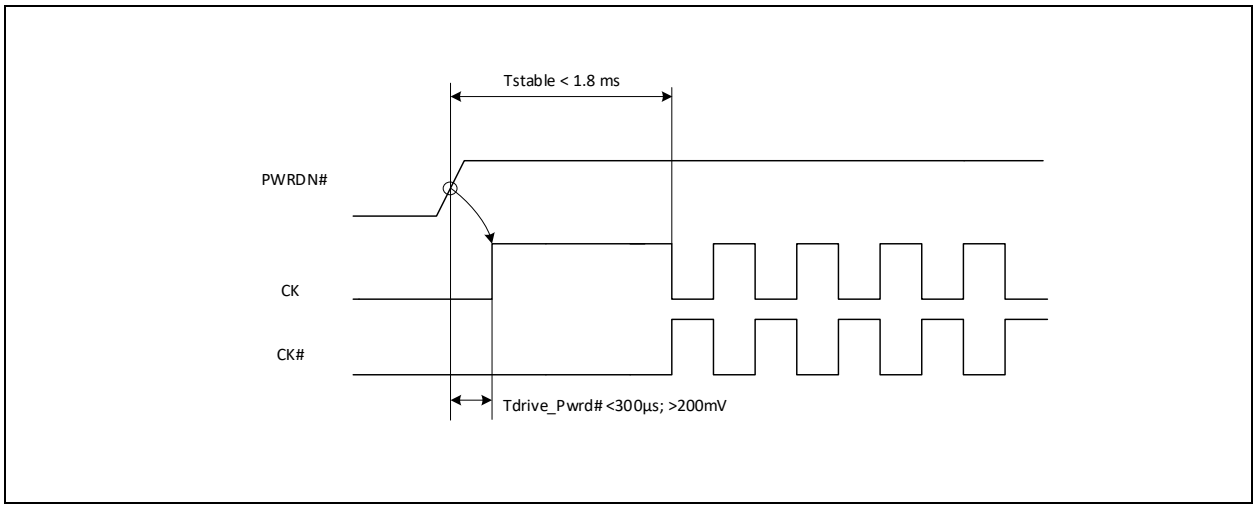


Figure 10. PWRGD Assertion

Programming via SMBus

The address selection is done via SA_0 and SA_1 tri-level hardware pins, which select the appropriate address for the device.

The two tri-level input pins that can configure the ZL40295 to nine different addresses (refer to Table 2 for VIL_Tri, VIM_Tri, VIH_Tri signal level).

Table 4 SMBus Address Table

SA_1	SA_0	SMBus Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

SMBus Byte Read/Write

Reading or writing a register in a SMBus slave device in byte mode always involves specifying the register number.

Read. The standard byte read is as shown in Figure 11. It is an extension of the byte write. The write start condition is repeated then the slave device starts sending data and the master acknowledges it until the last byte is sent. The master terminates the transfer with a NAK then a stop condition. For byte operation, the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

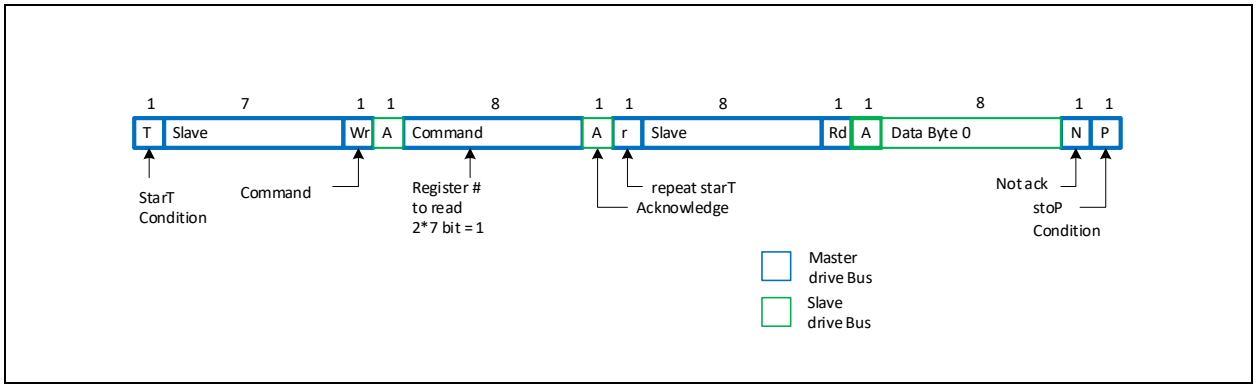


Figure 11. SMBus Byte Read

Write. Figure 12 illustrates a simple typical byte write. For byte operation the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set the next byte must be the byte transfer count. The count can be between 1 and 32. It cannot be zero or exceed 32.

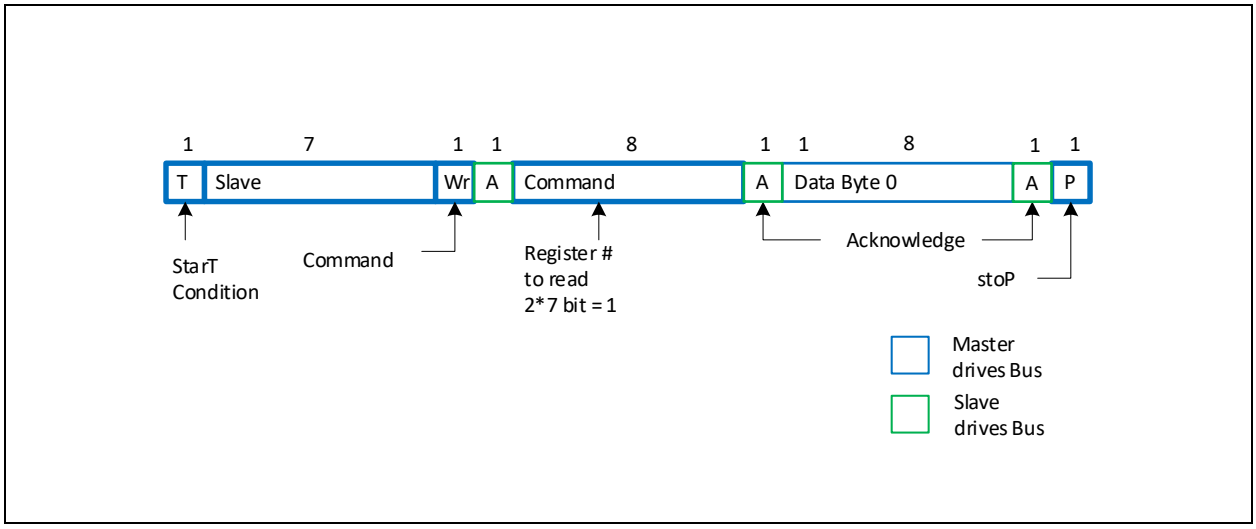


Figure 12. SMBus Byte Write

SMBus Block Read/Write

Read. After the slave address is sent with the r/w condition bit *set*, the command byte is sent with the MSB = 0. The slave Ack's the register index in the command byte. The master sends a repeat start function. After the slave Ack's this the slave sends the number of bytes it wants to transfer (>0 and <33). The master Ack's each byte except the last and sends a stop function.

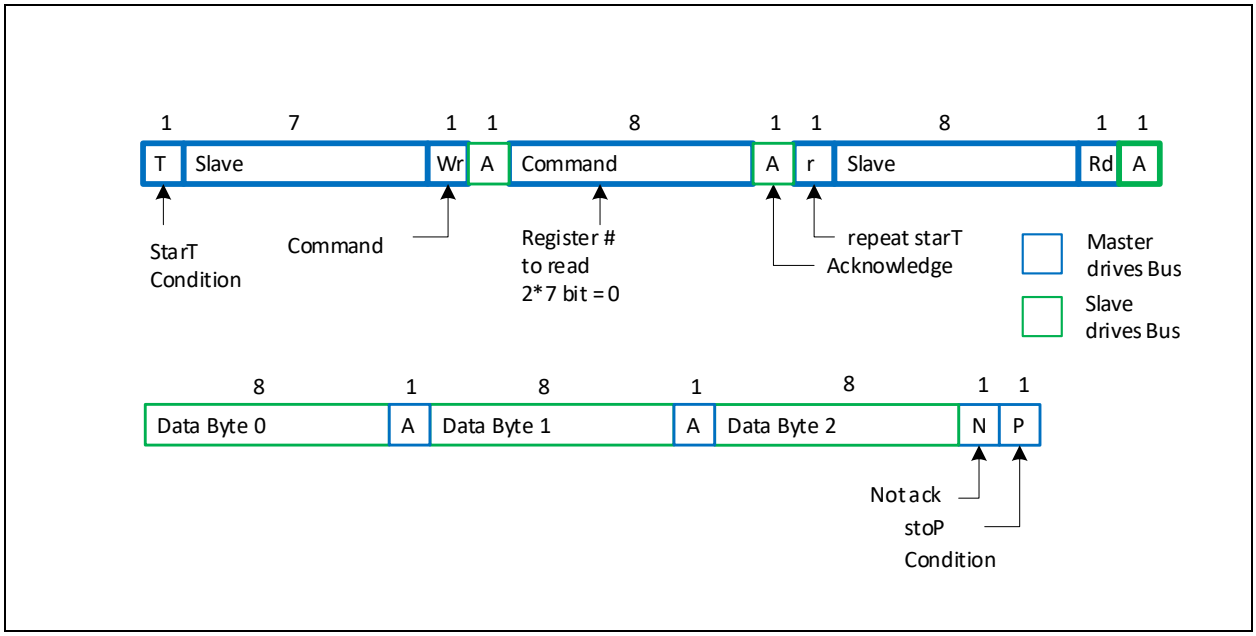


Figure 13. SMBus Block Read

Write. After the slave address is sent with the r/w condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate what register to start the transfer at. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

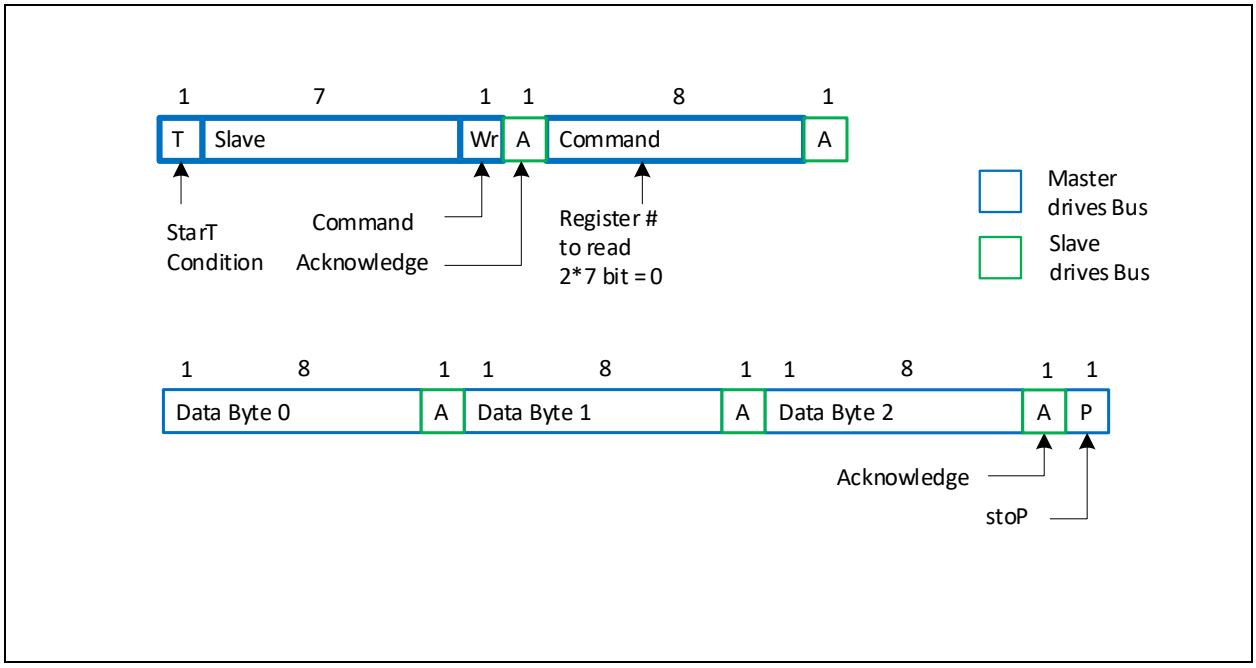


Figure 14. SMBus Block Write

Side-Band Interface

Besides OE pins and SMBUS interface the device outputs can be enabled/disabled via a simple 3-wire serial interface referred to as the Side-Band Interface (SBI).

This interface consists of the vDATA, vCLK and vSHFT_LD# pins. When the vSHFT_LD# pin is high, the rising edge of vCLK can shift vDATA into the shift register. After shifting data, the falling edge of vSHFT_LD# clocks the shift register contents to the Output register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable outputs, regardless of the method used.

Both interfaces are not active at the same time, and the SBEN pin selects which interface is active. Tying the SBEN high enables the SBI. Tying the SBEN pin low enables the traditional OE# pin/SMBus output-enable interface.

When the SBI is enabled, OE[7:9, 11,12]# are disabled and vDATA, vCLK and vSHFT_LD# are enabled on vOE5#, vOE6# and vOE10# respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active.

When set to 1, the mask register forces its respective output to ‘enabled’. This prevents accidentally disabling critical outputs when using the SBI.

A SMBus read-back bit in Byte 4 indicates which output-enable control interface is enabled.

When the SBI is enabled and power has been applied, the SBI is active, even if the PWRGD/PWRDN# pin indicates the part is in powerdown. This allows loading the shift register and transferring the contents to the output register before the assertion of PWRGD.

Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the PWRGD/PWRDN# is low. Figure 15 provides a functional description of the SBI.

The SBI and the traditional SMBus output-enable registers both default to the ‘output enabled’ state at power-up. The mask registers default to zero at power-up, allowing the shift register bits to disable their respective output.

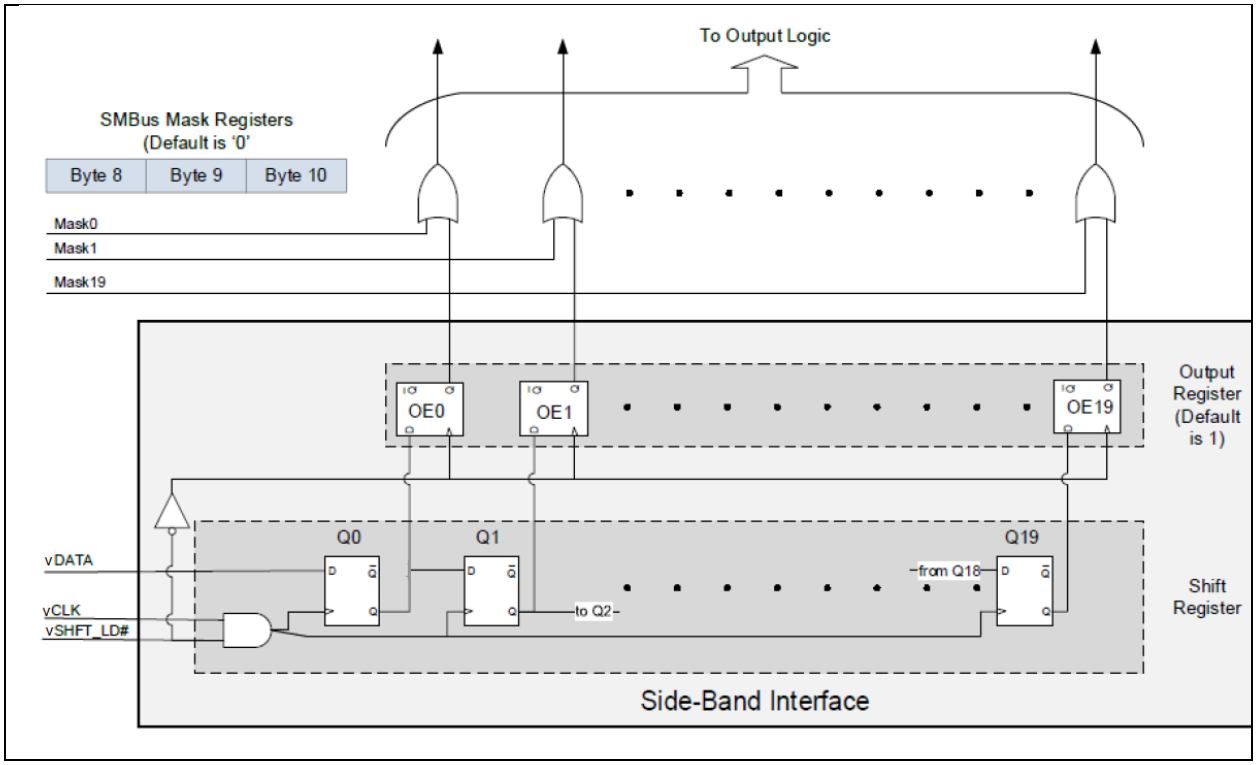


Figure 15. Side-Band Interface Control Logic – Functional Description

Figure 16 shows the basic timing of the side-band interface. The vSHFT_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable vDATA into the shift register. After the 20th clock cycle for output 19, it stops the clock low and drive the vSHFT_LD# pin low. The falling edge of vSHFT_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. It always shifts 20 bits of data into the shift register to control the outputs.

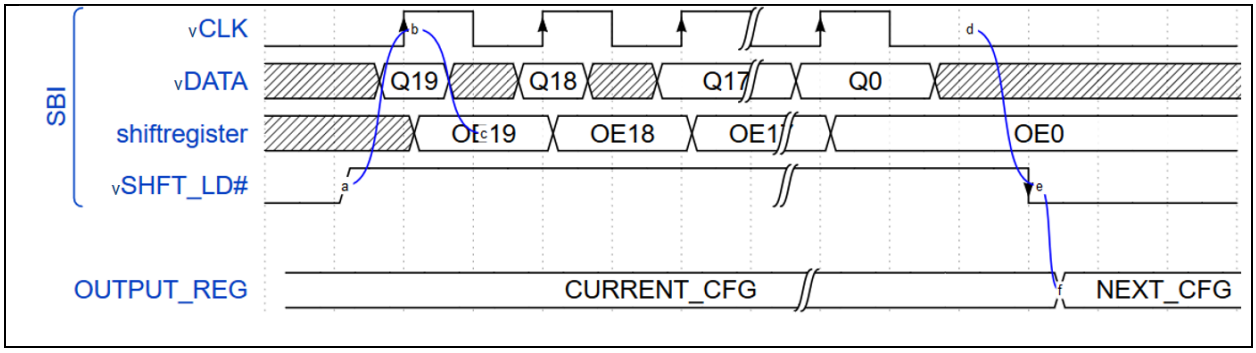


Figure 16. Side-Band Interface Functional Timing

The SBI supports clock rates up to 10 MHz. Multiple devices may share vCLK and vDATA pins. Dedicating a vSHFT_LD# pin to each device allows its use as a chip-select pin. When the vSHFT_LD# pin is low, the device ignores any activity on the vCLK and vDATA pins.

Typical Jitter Performance

Following figure shows a typical phase noise for 100MHz clock frequency. The light blue curve is the phase noise of the input clock fed to the device and the dark blue is the phase noise of the output clock. The plot shows phase noise floor of -163dBc/Hz and an absolute jitter in 12kHz to 20MHz of 76fs. The additive jitter is calculated as:

$J_{ADD} = \sqrt{(J_{OUT}^2 - J_{IN}^2)}$ where J_{OUT} and J_{IN} are respectively output and input jitter in the band of interest. The additive jitter for 12kHz to 20MHz band is 58fs.

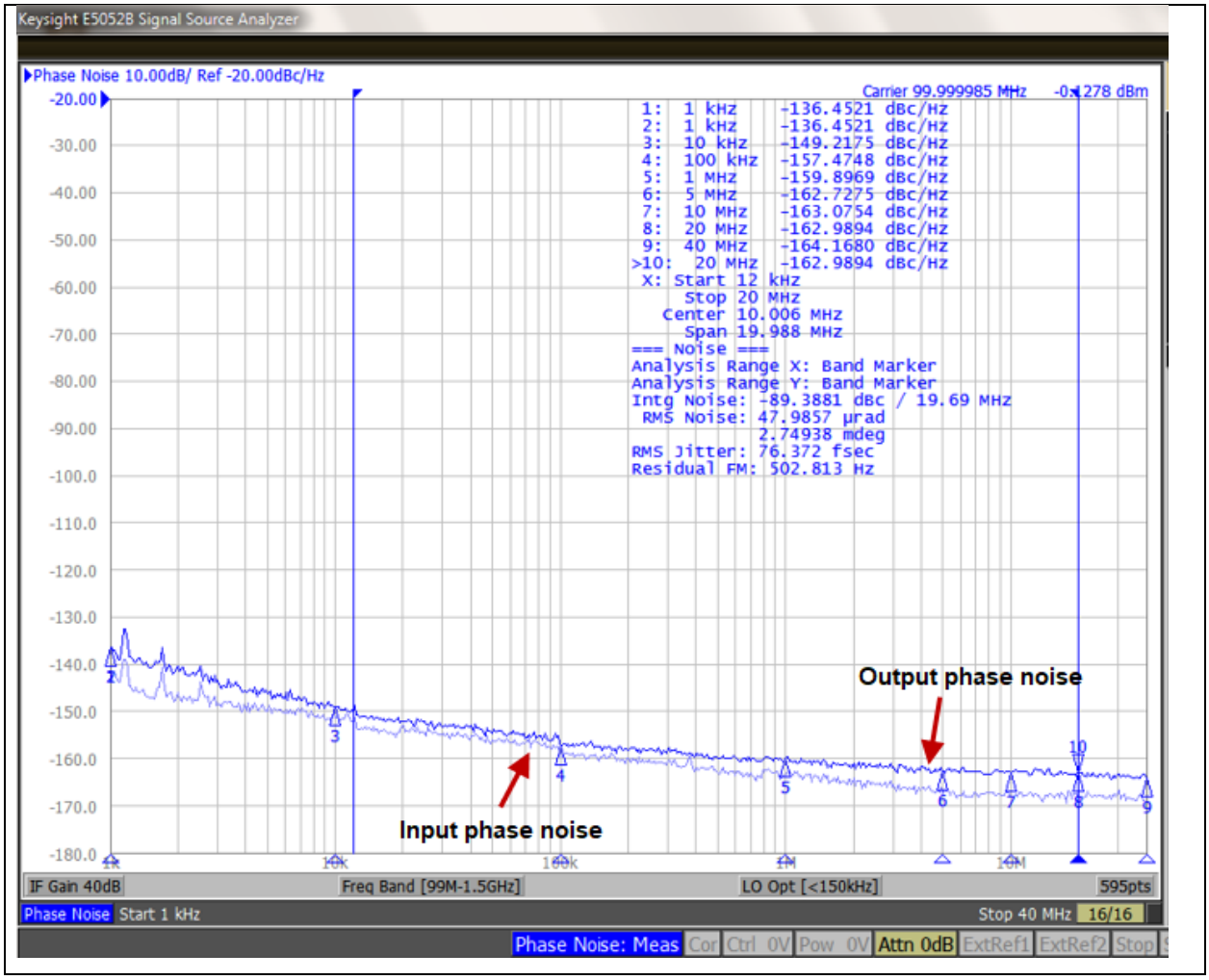


Figure 17. ZL40295 typical phase noise

Register Map

Table 5 Byte 0: Output Enable

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved				0	
1	Reserved				0	
2	Reserved				0	
3	Output Enable CK 16	LOW	Enable	RW	1	CK[16]
4	Output Enable CK 17	LOW	Enable	RW	1	CK[17]
5	Output Enable CK 18	LOW	Enable	RW	1	CK[18]
6	Output Enable CK 19	LOW	Enable	RW	1	CK[19]
7	Reserved				0	

Table 6 Byte 1: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK 0	LOW	Enabled	RW	1	CK[0]
1	Output Enable CK 1	LOW	Enabled	RW	1	CK[1]
2	Output Enable CK 2	LOW	Enabled	RW	1	CK[2]
3	Output Enable CK 3	LOW	Enabled	RW	1	CK[3]
4	Output Enable CK 4	LOW	Enabled	RW	1	CK[4]
5	Output Enable CK 5	LOW	Enabled	RW	1	CK[5]
6	Output Enable CK 6	LOW	Enabled	RW	1	CK[6]
7	Output Enable CK 7	LOW	Enabled	RW	1	CK[7]

Table 7 Byte 2: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK 8	LOW	Enabled	RW	1	CK[8]
1	Output Enable CK 9	LOW	Enabled	RW	1	CK[9]
2	Output Enable CK 10	LOW	Enabled	RW	1	CK[10]
3	Output Enable CK 11	LOW	Enabled	RW	1	CK[11]
4	Output Enable CK 12	LOW	Enabled	RW	1	CK[12]
5	Output Enable CK 13	LOW	Enabled	RW	1	CK[13]
6	Output Enable CK 14	LOW	Enabled	RW	1	CK[14]
7	Output Enable CK 15	LOW	Enabled	RW	1	CK[15]

Table 8 Byte 3: OE# Pin Realtime Readback Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Realtime Readback of OE_5#	OE_5# Low	OE_5# High	R	Realtime	CK[5]
1	Realtime Readback of OE_6#	OE_6# Low	OE_6# High	R	Realtime	CK[6]
2	Realtime Readback of OE_7#	OE_7# Low	OE_7# High	R	Realtime	CK[7]
3	Realtime Readback of OE_8#	OE_8# Low	OE_8# High	R	Realtime	CK[8]
4	Realtime Readback of OE_9#	OE_9# Low	OE_9# High	R	Realtime	CK[9]
5	Realtime Readback of OE_10#	OE_10# Low	OE_10# High	R	Realtime	CK[10]
6	Realtime Readback of OE_11#	OE_11# Low	OE_11# High	R	Realtime	CK[11]
7	Realtime Readback of OE_12#	OE_12# Low	OE_12# High	R	Realtime	CK[12]

Table 9 Byte 4: Reserved Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	RB_SBEN	Pin Low	Pin High	Input	Real time	
1	Reserved				0	
2	Reserved				0	
3	Reserved				0	
4	Reserved				0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

Table 10 Byte 5: Vendor/Revision Identification Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Vendor ID Bit 0			R	1	
1	Vendor ID Bit 1			R	1	
2	Vendor ID Bit 2			R	0	
3	Vendor ID Bit 3			R	0	
4	Revision Code Bit 0			R	1	
5	Revision Code Bit 1			R	1	
6	Revision Code Bit 2			R	0	
7	Revision Code Bit 3			R	0	

Table 11 Byte 6: Device ID Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Device ID 0			R	1	
1	Device ID 1			R	1	
2	Device ID 2			R	1	
3	Device ID 3			R	1	
4	Device ID 4			R	1	
5	Device ID 5			R	0	
6	Device ID 6			R	1	
7	Device ID 7 (MSB)			R	0	

Table 12 Byte 7: Byte Count Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	BC0 - Writing to this register configures how many bytes will be read back			RW	0	
1	BC1 - Writing to this register configures how many bytes will be read back			RW	0	
2	BC2 - Writing to this register configures how many bytes will be read back			RW	0	
3	BC2 - Writing to this register configures how many bytes will be read back			RW	1	
4	BC3 - Writing to this register configures how many bytes will be read back			RW	0	
5	BC4 - Writing to this register configures how many bytes will be read back			RW	0	
6	Reserved				0	
7	Reserved				0	

Table 13 Byte 8: SBI Mask – Functional only when SBEN=1

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Mask0 - Masks off Side Band Disable	Side Band shift register may disable the output	Forces output to always be enabled regardless of Side Band shift register value	RW	0	CK[0]
1	Mask1 - Masks off Side Band Disable			RW	0	CK[1]
2	Mask2 - Masks off Side Band Disable			RW	0	CK[2]
3	Mask3 - Masks off Side Band Disable			RW	0	CK[3]
4	Mask4 - Masks off Side Band Disable			RW	0	CK[4]
5	Mask5 - Masks off Side Band Disable			RW	0	CK[5]
6	Mask6 - Masks off Side Band Disable			RW	0	CK[6]
7	Mask7 - Masks off Side Band Disable			RW	0	CK[7]

Table 14 Byte 9: SBI Mask – Functional only when SBEN=1

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Mask8 - Masks off Side Band Disable	Side Band shift register may disable the output	Forces output to always be enabled regardless of Side Band shift register value	RW	0	CK[8]
1	Mask9 - Masks off Side Band Disable			RW	0	CK[9]
2	Mask10 - Masks off Side Band Disable			RW	0	CK[10]
3	Mask11 - Masks off Side Band Disable			RW	0	CK[11]
4	Mask12 - Masks off Side Band Disable			RW	0	CK[12]
5	Mask13 - Masks off Side Band Disable			RW	0	CK[13]
6	Mask14 - Masks off Side Band Disable			RW	0	CK[14]
7	Mask15 - Masks off Side Band Disable			RW	0	CK[15]

Table 15 Byte 10: SBI Mask – Functional only when SBEN=1

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Mask16 - Masks off Side Band Disable	Side Band shift register may disable the output	Forces output to always be enabled regardless of Side Band shift register value	RW	0	CK[16]
1	Mask17 - Masks off Side Band Disable			RW	0	CK[17]
2	Mask18 - Masks off Side Band Disable			RW	0	CK[18]
3	Mask19 - Masks off Side Band Disable			RW	0	CK[19]
4	Reserved			RW	0	
5	Reserved			RW	0	
6	Reserved			RW	0	
7	Reserved			RW	0	

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 16 Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Max.	Units	Notes
1	3.3 V Core Supply Voltage	V_{DD_A}	-	4.6	V	3
2	3.3 V I/O Supply Voltage	V_{DD}	-	4.6	V	3
5	3.3 V Input High Voltage	V_{IH}	-	4.6	V	1, 3
	3.3 V Input Low Voltage	V_{IL}	-0.5	-	V	3
	Storage Temperature	Ts	-65	150	°C	3
6	Input ESD protection	V_{DD-IN}	2000		V	2

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated

1. Maximum VIH is not to exceed maximum VDD.
2. Human body model.
3. Consult manufacturer regarding extended operation in excess of normal DC operating parameters.

Current consumption

Table 1 Current Consumption

	Parameter	Parameter Condition	Symbol	Min.	Typ.	Max	Units	Notes
1	Active Mode Supply Current	fIN = 100MHz All CKx/CKx# outputs enabled	I_{DDPG}		205	240	mA	1,2
2		fIN = 100MHz All CKx/CKx# outputs disabled			48	55		1,3
3		fIN = 133MHz All CKx/CKx# outputs enabled			257	308		1,2
4		fIN = 133MHz All CKx/CKx# outputs disabled			49	56		1,3
5	Power Down Mode Supply Current	fIN = 100MHz	I_{DDPD}		21	25	mA	1,4
6		fIN = 133MHz			22	26		1,4

1. VDD = 3.3V + 5%
2. Device operating in active mode (Pin PWRGD/PWRDN# = 1) with all 20 CKx/CKx# outputs enabled (all OE_xN pin = 0, all OCR1, OCR2, OCR3 register OEx bits = 1)
3. Device operating in active mode (Pin PWRGD/PWRDN# = 1) with all 20 CKx/CKx# outputs disabled (all OCR1, OCR2, OCR3 register OEx bits = 0)
4. Device operating in low power mode (Pin PWRGD/PWRDN# = 0)

DC Electrical Specification

Table 2 DC Operating Characteristics*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	3.3 V Core Supply Voltage	V_{DD_A}	3.135	3.3	3.465	V	
2	3.3 V I/O Supply Voltage	V_{DD}	3.135	3.3	3.465	V	
3	3.3 V Input High Voltage	V_{IH}	2.0		VDD+0.3	V	
4	3.3 V Input Low Voltage	V_{IL}	VSS-0.3		0.8	V	
5	Input Leakage Current	I_{IL}	-5		+5	µA	
6	Input Low Voltage, 3-level CMOS Input	V_{IL3}	VSS-0.3		0.9	V	
7	Input Midrange Voltage, 3-level CMOS Input	V_{IM3}	1.3		1.8	V	
8	Input High Voltage, 3-level CMOS Input	V_{IH3}	2.4		VDD	V	
9	Input Capacitance	C_{IN}			4.5	pF	1
10	Output Capacitance	C_{OUT}			4.5	pF	1
11	Ambient Temperature	T_A	-40		85	°C	

* Voltages are with respect to ground (GND) unless otherwise stated
1 For parasitic simulation use IBIS model.

Power Noise Tolerance

Table 1 Power Noise Tolerance*

	VDD Electrical Noise Range	Symbol	Min.	Typ.	Max	Units	Notes
1	f_{NOISE} = 12kHz to 20MHz	N_{VDD_MID}	100			mV,p-p	1,2,3
2	f_{NOISE} > 20MHz	N_{VDD_HIGH}	50			mV,p-p	1,2,3
3	f_{NOISE} = 12kHz to 20MHz	$N_{VDD\_A\_MID}$	40			mV,p-p	1,2,3
4	f_{NOISE} > 20MHz	$N_{VDD\_A\_HIGH}$	20			mV,p-p	1,2,3

* The device meets all specification in the presence of noise specified in this table
1 Jitter and electrical characteristics are met with specified AC noise present on any of the power pins.
2 Over the specified frequency range, a single sinusoid tone should be assumed swept as the worst case.
3 Maximum measured frequency for VDD was 650kHz and for VDD_A the maximum frequency was 900kHz due to limitation of the test setup

PCIe Electrical Characteristics

Table 2 PCIe Electrical Characteristics

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Rising edge rate	Rise_rate	1.4	1.6	2	V/ns	(2), (3)
2	Falling edge rate	Fall_rate	1.4	1.6	2	V/ns	(2), (3)
3	Differential High Voltage	V_{IH}	0.7			V	(2)
4	Differential Low Voltage	V_{IL}			-0.7	V	(2)
5	Single ended high voltage	V_{SIH}	0.7	0.76	0.82`	V	DC Measurement
6	Single ended low voltage	V_{SIL}	-0.05	0	0.05	V	DC Measurement
7	Absolute Crossing Voltage	V_{CROSS}	0.275		0.35	V	(1), (4), (5)
8	Variation of V_{CROSS} over all rising clock edges	ΔV_{CROSS}			0.08	V	(1), (4), (9)
9	Ring back voltage margin	V_{RB}	-0.3		0.3	V	(2), (11)
10	Time before V_{RB} is allowed	t_{STABLE}	500			ps	(2), (11)
11	Average Clock Period Accuracy	T_{PERIOD_AVG}	NA		NA	ppm	(10)
12	Absolute Period	T_{PERIOD_ABS}	NA		NA	ns	(6)
13	Cycle-to-cycle jitter	T_{JCC}		3.5	6	ps peak to peak	(2)
14	Absolute Maximum voltage	V_{MAX}			0.8	V	(1), (7)
15	Absolute Minimum voltage	V_{MIN}			-0.3	V	(1), (8)
16	Output Duty-Cycle (when input has 50% duty-cycle)	Duty_cycle	49	50	51	%	(2)
17	Rising to falling edge matching	r/f match			6	%	(1), (7)
18	Clock Source DC impedance (CK)	$Z_{C\text{-}DC\_CK}$	50 - 5%	50	50 + 5%	Ω	DC Measurement
19	Clock Source DC impedance (CK#)	$Z_{C\text{-}DC\_CK\#}$	50 – 5%	50	50 + 5%	Ω	DC Measurement
20	Output frequency	F_{MAX}	0		250	MHz	
21	Output to output skew	t_{OOSK}			50	ps	
22	Device to device output skew	t_{DOOSK}			0.5	ns	
23	Input to output delay	t_{IOD}	0.9		1.5	ns	
24	Output enable time	t_{EN}			10	cycles	
25	Output disable time	t_{DIS}			10	cycles	

* Values are over Recommended Operating Conditions

(0) Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets

(1) Measurement taken from single ended waveform

(2) Measurement taken from differential waveform.

(3) Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 21

(4) Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK# . See Figure 18

(5) Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 18.

(6) This requirement, from PCI Express Base Specification, Revision 4.0 is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

(7) Defined as the maximum instantaneous voltage including overshoot. See Figure 18.

(8) Defined as the minimum instantaneous voltage including undershoot. See Figure 18.

(9) Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in VCROSS for any particular system. See Figure 19.

(10) The PPM requirement from PCIe Express Base Specification, Revision 4.0 is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

(11) TSTABLE is the time the differential clock must maintain a minimum ±150 mV differential voltage after20 rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range. See Figure 22.

(12) Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cross point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 20.

Table 3 Skew and Jitter Performance

	Parameter	Symbol	Min.	Typ.	Max	Units	Notes
1	Input-to-Output Delay	I/O_{DELAY}	0.9		1.5	ns	1,3
2	Output-to-Output Skew	O/O_{DELAY}			50	ps	1,2
3	Peak-to-Peak Additive Jitter	$p\text{-}pAJ_{RMS}$			1	ps	1,2
4	Additive Jitter as per PCIe 1.0 (1.5MHz to 22MHz)	$T_{jPCIe\_1.0}$		0.73	0.90	ps RMS	1, 2
5	Additive Jitter as per PCIe 2.0 high band (1.5MHz to 50MHz)	$T_{jPCIe\_2.0\_high}$		82	100	fs RMS	1, 2
6	Additive Jitter as per PCIe 2.0 low band (10kHz to 1.5MHz)	$T_{jPCIe\_2.0\_low}$		20	30	fs RMS	1, 2
7	Additive Jitter as per PCIe 2.0 mid band (5MHz to 16MHz)	$T_{jPCIe\_2.0\_mid}$		64	79	fs RMS	1, 2
8	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe\_3.0}$		20	35	fs RMS	1, 2
9	Additive Jitter as per PCIe 4.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe\_4.0}$		20	35	fs RMS	1, 2
10	Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 to 1.8MHz, CDR for 32 GT/s CC)	$T_{jPCIe\_5.0}$		8	10	fs RMS	1, 2
11	Additive jitter as per Intel QPI 9.6Gbps	T_{jQPI}		29	36	fs RMS	1, 2
12	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		55	80	fs RMS	1, 2 (100MHz clock)
				42	60	fs RMS	1, 2 (133MHz clock)
13	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		58	83	fs RMS	1, 2 (100MHz clock)
				44	63	fs RMS	1, 2 (133MHz clock)
14	Noise floor	N_F		-163	-162	dBc/Hz	1, 2 (100MHz clock)
				-163	-162	dBc/Hz	1, 2 (133MHz clock)

1. Measured into AC test load as per Figure 23 .
2. Measured from differential crossing point to differential crossing point.
3. Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

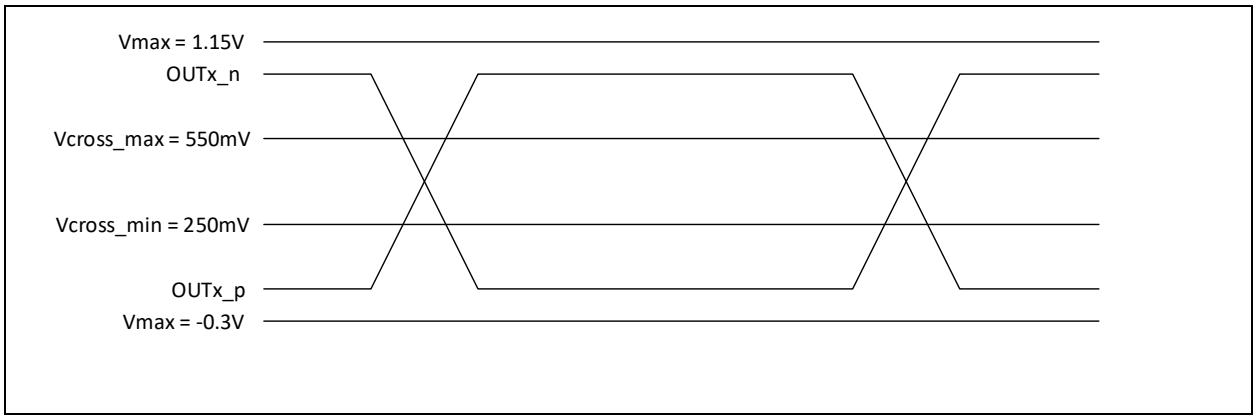


Figure 18. Single-Ended Measurement Points for Absolute Cross Point and Swing

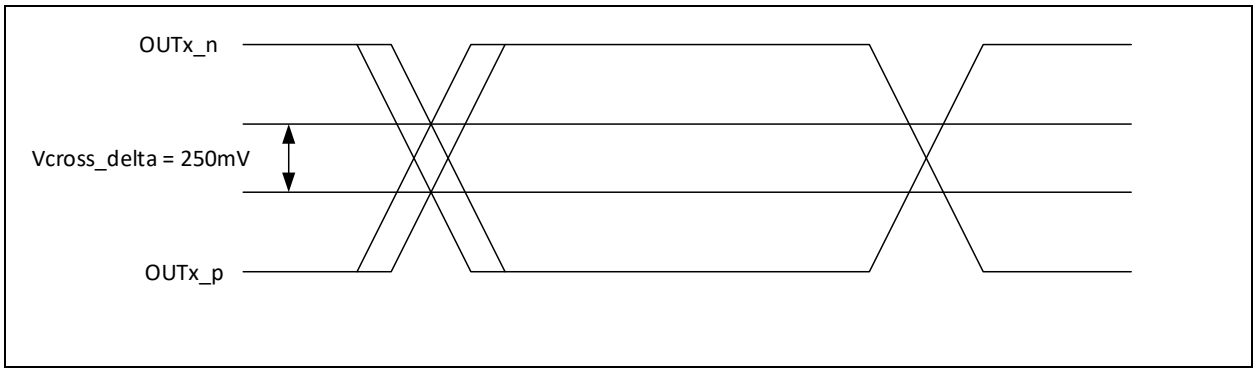


Figure 19. Single-Ended Measurement Points for Delta Cross Point

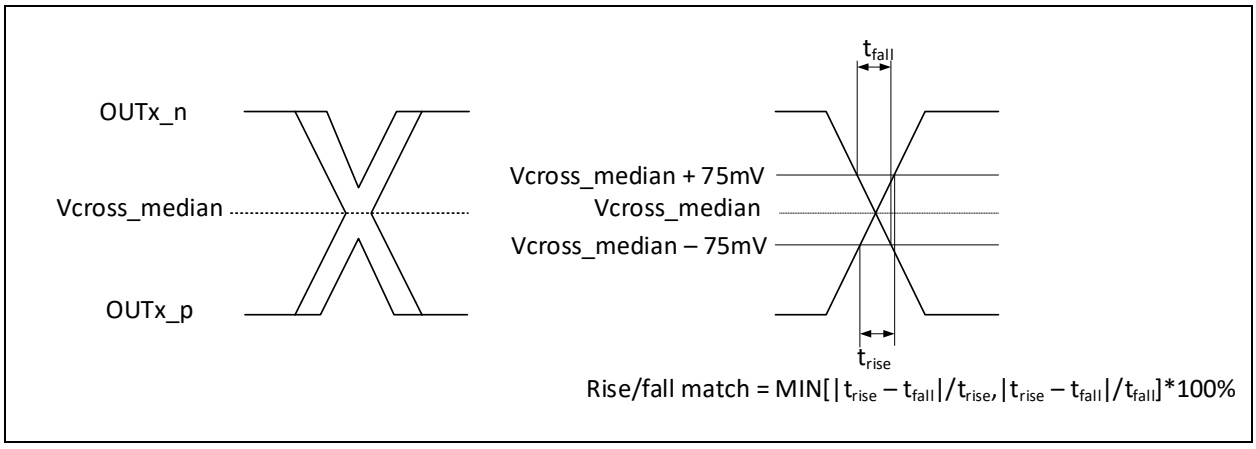


Figure 20. Single-Ended Measurement Points for Rise and Fall Time Matching

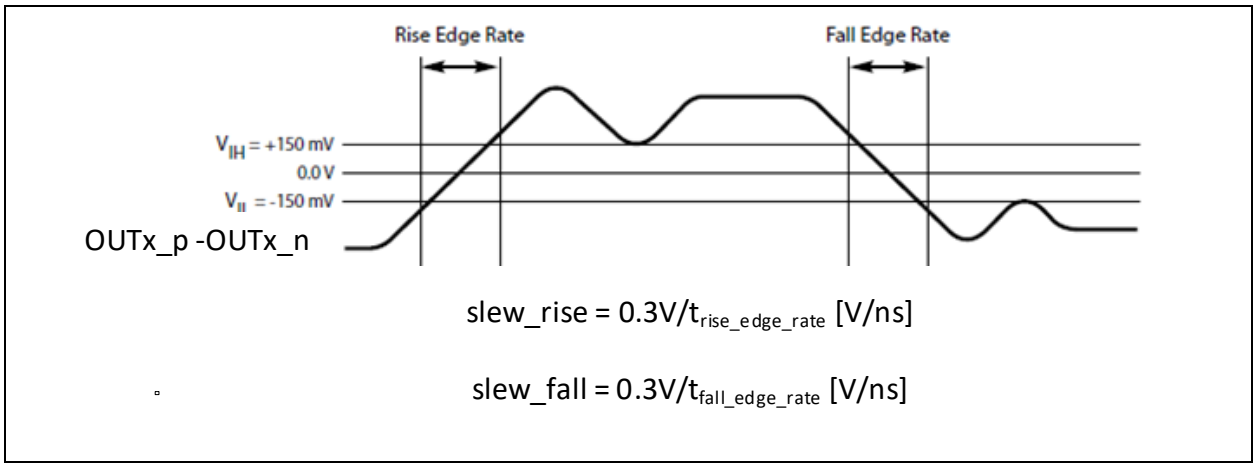


Figure 21. Differential Measurement Points for Rise and Fall Time

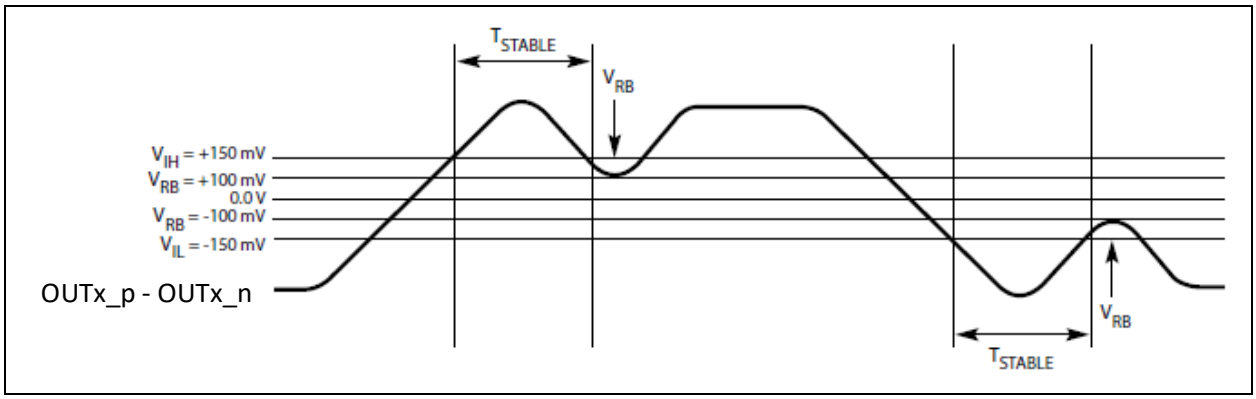


Figure 22. Differential Measurement Points for Ringback

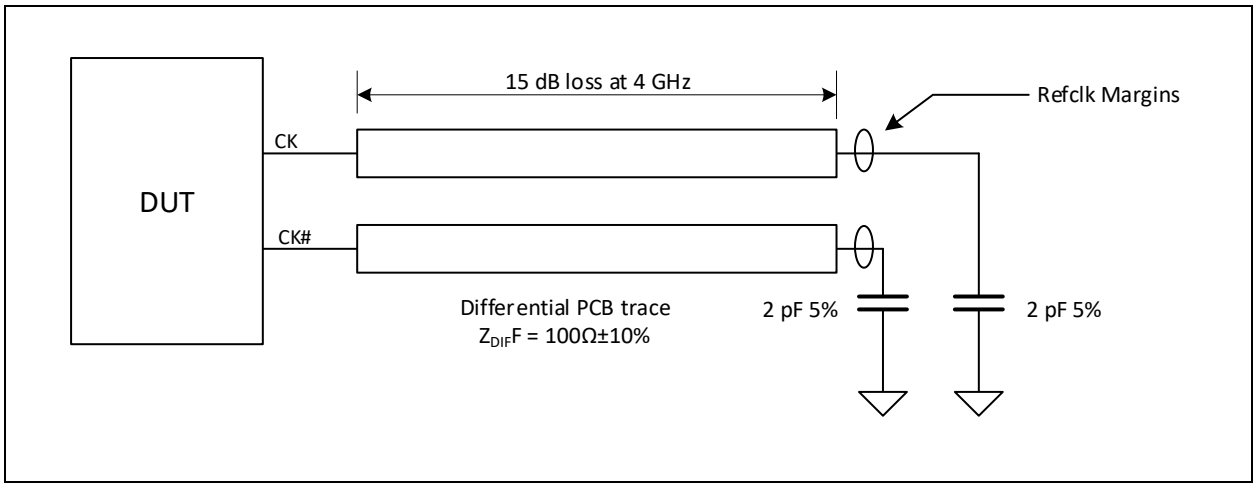


Figure 23. PCIe Test Circuit

Input Clock requirements

Table 4 Differential Input Clock AC Characteristics

	Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
1	Edge_rate	Input_Slew_Rate	0.7			V/ns	
2	Total Variation of Vcross Over All Edges	Total_Δ_Vcross			140	mV	
3	Input Voltage	Input_Voltage	200			mv diff	

SMBus Electrical Characteristics

Table 5 SMBus Electrical Characteristics

	Parameter	Symbol	Min.	Typ.	Max	Units	Notes
1	Nominal Bus Voltage	VDD_{SMB}	2.7		5.5	V	1
2	Input Low Voltage	V_{IL}			0.8	V	
3	Input High Voltage	V_{IH}	2.1		VDD_{SMB}	V	
4	Output Low Voltage	V_{OL}			0.4	V	At $I_{PULLUP,MAX}$
5	Input Leakage Current	I_{LEAK}			±10	µA	
6	Current sinking at $V_{OL,max}$	I_{PULLUP}	4			mA	
7	Pin capacitive load	C_I			10	pF	
8	Signal noise immunity from 10MHz to 100MHz	V_{NOISE}	300			mV_{p-p}	
9	Noise spike suppression time	T_{SPIKE}	0		50	ns	3
10	SMBus Operating Frequency	F_{SMB}	10		400	kHz	
11	Bus free time between Stop and Start Condition	T_{BUF}	4.7			µs	
12	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	$T_{HD:STA}$	4.0			µs	
13	Repeated Start Condition setup time	$T_{SU:STA}$	4.7			µs	
14	Stop Condition setup time	$T_{SU:STO}$	4.0			µs	
15	Data hold time	$T_{HD:DAT}$	300			ns	
16	Data setup time	$T_{SU:DAT}$	250			ns	
17	Clock low period	T_{LOW}	4.7			µs	
18	Clock high period	T_{HIGH}	4.0		50	µs	
19	Clock/Data Fall Time	T_F			300	ns	2
20	Clock/Data Rise Time	T_R			1000	ns	2

1. 3V to 5V ±10%
2. Rise and fall time is defined as follows:
TR = (VIL,MAX – 0.15) to (VIH,MIN + 0.15)
TF = (VIH,MIN + 0.15) to (VIL,MAX - 0.15)
3. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

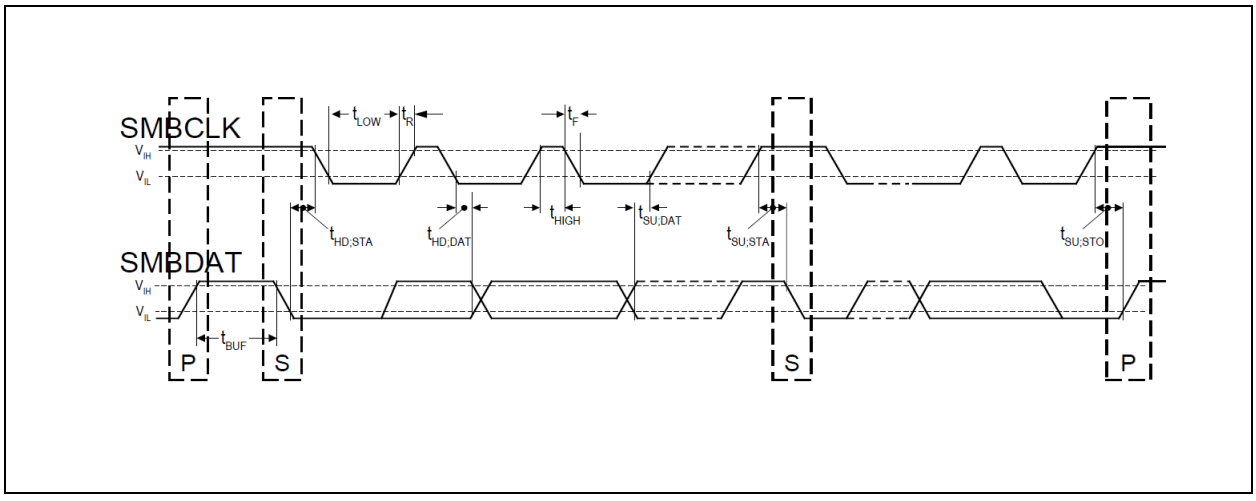


Figure 24. SMBus Timing

Side-Band Interface Characteristics

Table 6 Side-Band Interface

	Parameter	Symbol	Min.	Typ.	Max	Units	Notes
1	Clock Period	t_{PERIOD}	100			ns	
2	vSHFT_LD# setup to vCLK rising edge	t_{SETUP}	25			ns	
3	vDATA setup to vCLK rising edge	t_{DSU}	10			ns	
4	vDATA hold after vCLK rising edge	t_{DSHOLD}	5			ns	
5	Delay from vCLK rising edge to vSHFT_LD# falling edge	t_{DELAY}	25			ns	
6	Delay from vSHFT_LD# falling edge to next output configuration taking effect	t_{PD}	4		10	clocks	1
7	Slew Rate	t_{SLEW}			0	V/ns	

1. Refers to device differential input clock.

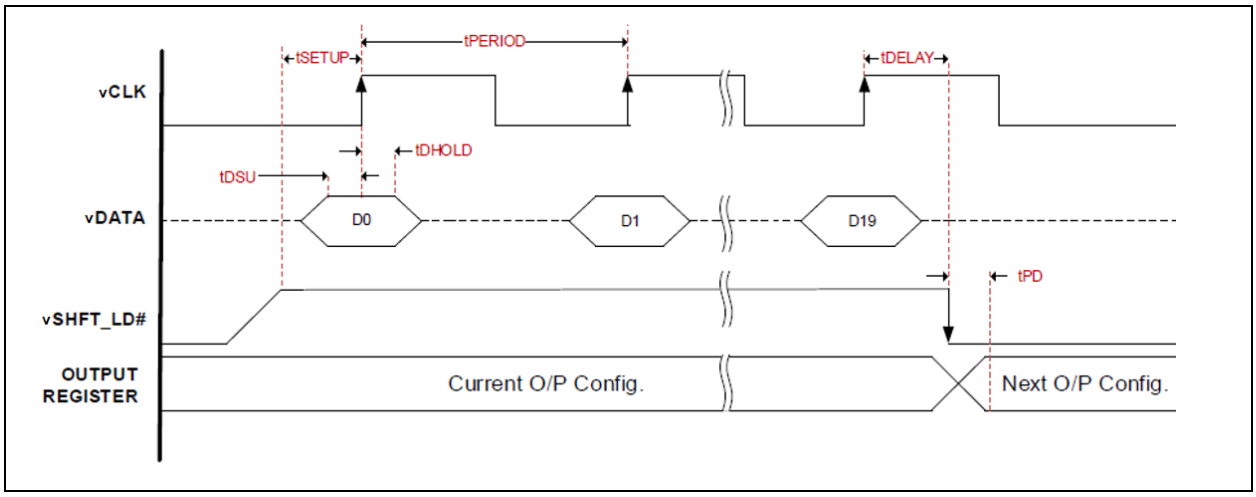


Figure 25. Side-Band Interface timing

Table 7 6x6mm GQFN Package Thermal Properties

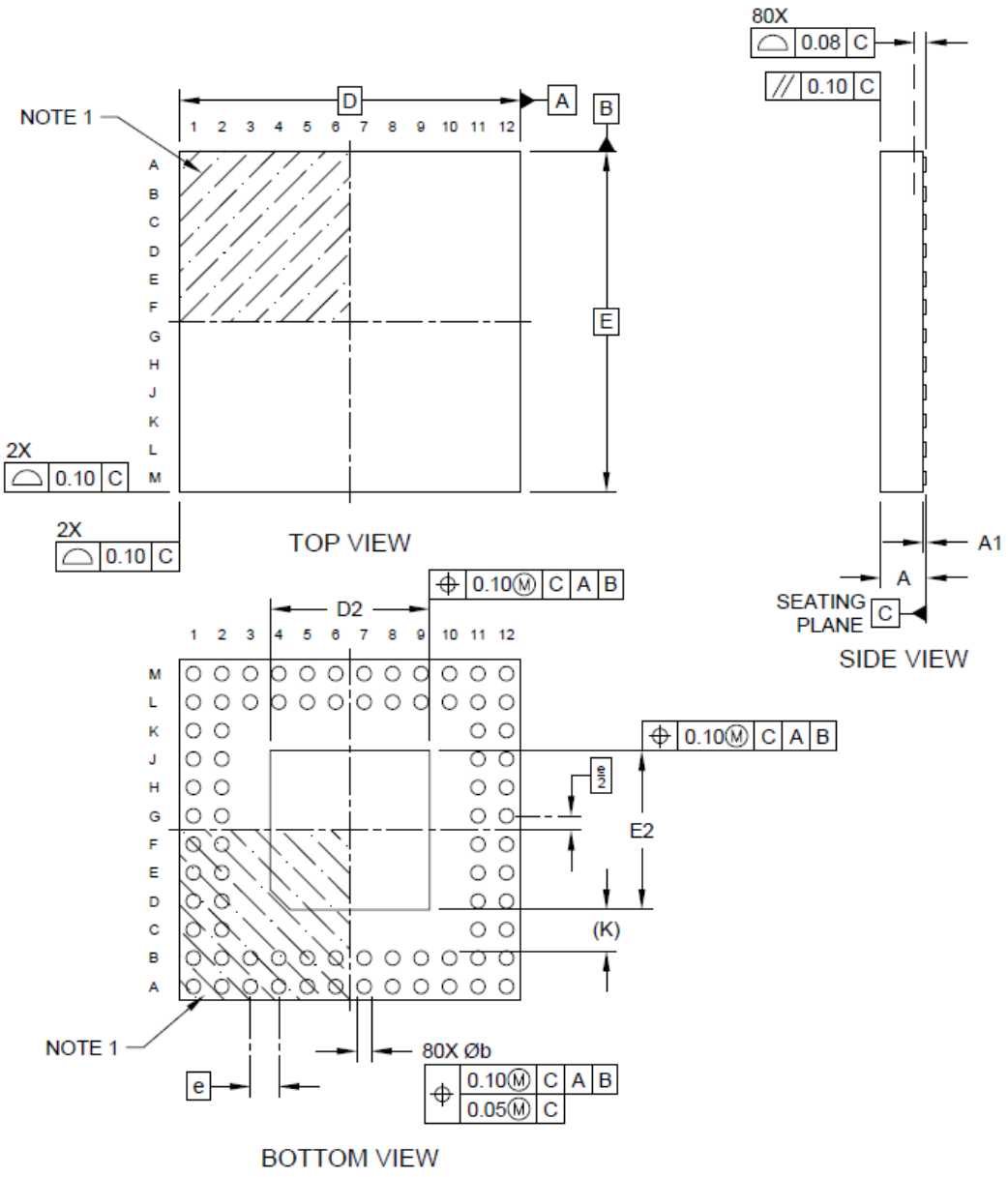
Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance(1) (Note 1)	θ_{JA}	still air	32.42	°C/W
		1m/s airflow	27.67	
		2.5m/s airflow	26.33	
Junction to Board Thermal Resistance	θ_{JB}		12.48	°C/W
Junction to Case Thermal Resistance	θ_{JC}		21.33	°C/W
Junction to Pad Thermal Resistance(2)	θ_{JP}	Still air	1.83	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.25	°C/W

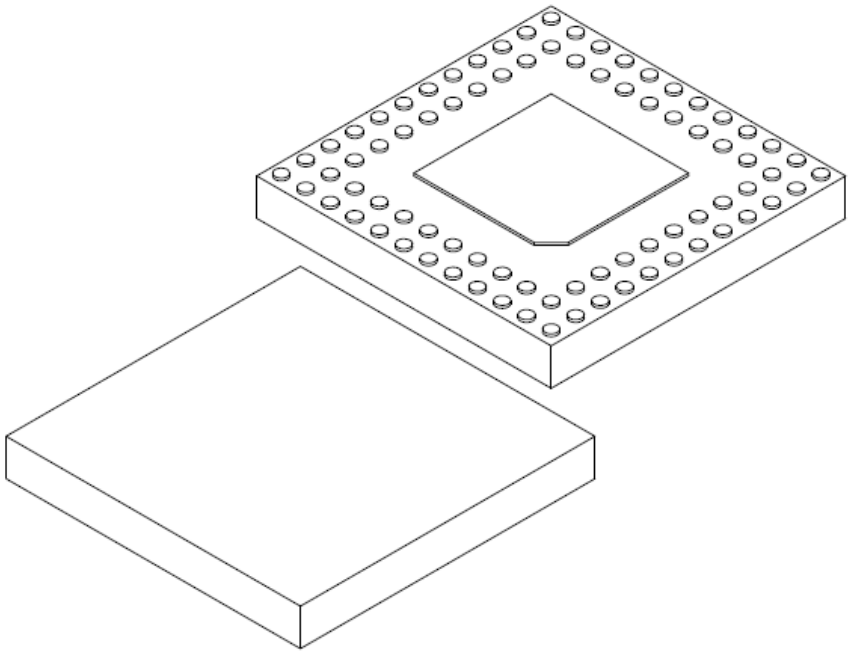
(1) Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power

(2) Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

Package Outline

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

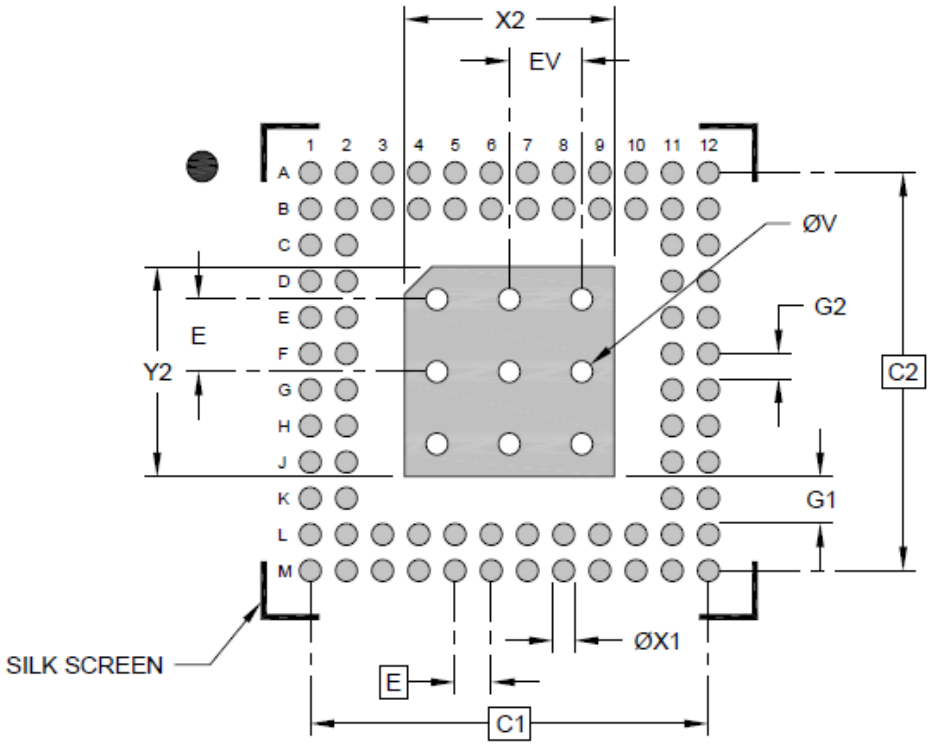




Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		80	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	2.70	2.80	2.90
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	2.70	2.80	2.90
Terminal Width	b	0.20	0.25	0.30
Terminal-to-Exposed-Pad	K		0.725 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Package Type WGQFN is not registered with JEDEC as of April, 2019
   Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.90
Optional Center Pad Length	Y2			2.90
Contact Pad Spacing	C1		5.50 BSC	
Contact Pad Spacing	C2		5.50 BSC	
Contact Pad Diameter (X80)	X1			0.30
Contact Pad to Center Pad (X32)	G1	0.65		
Contact Pad to Contact Pad	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Change History

- December 2019: Initial Release of ZL40295 Datasheet

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