ZL40812

10GHz Fixed Modulus ÷ 16

Data Sheet

July 2003

Features

- Very High Operating Speed
- Operation down to DC with Square Wave Input
- Low Phase Noise (Typically better than -152dBc/Hz at 10kHz)
- 5V Single Supply Operation
- Low Power Dissipation: 500mW (Typ)
- Surface Mount Plastic Package With Exposed Pad (See Application Notes

Applications

- DC to 10 GHz PLL applications
- HyperLan
- LMDS
- Instrumentation
- Satellite Communications
- Fibre Optic Communications; OC48, OC192
- Ultra Low Jitter Clock Systems

Ordering Information

ZL40812/DCE (tubes)	8 lead e-pad SOIC
ZL40812/DCF (tape and reel)	8 lead e-pad SOIC

-40°C to +85°C

Description

Description The ZL40812 is one of a range of 5V supply, very high speed low power prescalers for professional applications with a fixed modulus of divide by 16. The dividing elements are static D type flip flops and therefore allow operation down to DC if the drive signal is a pulse waveform with fast risetimes. The output stage has internal 50 ohm pull up giving a 1V p-p output. See application notes for more details.

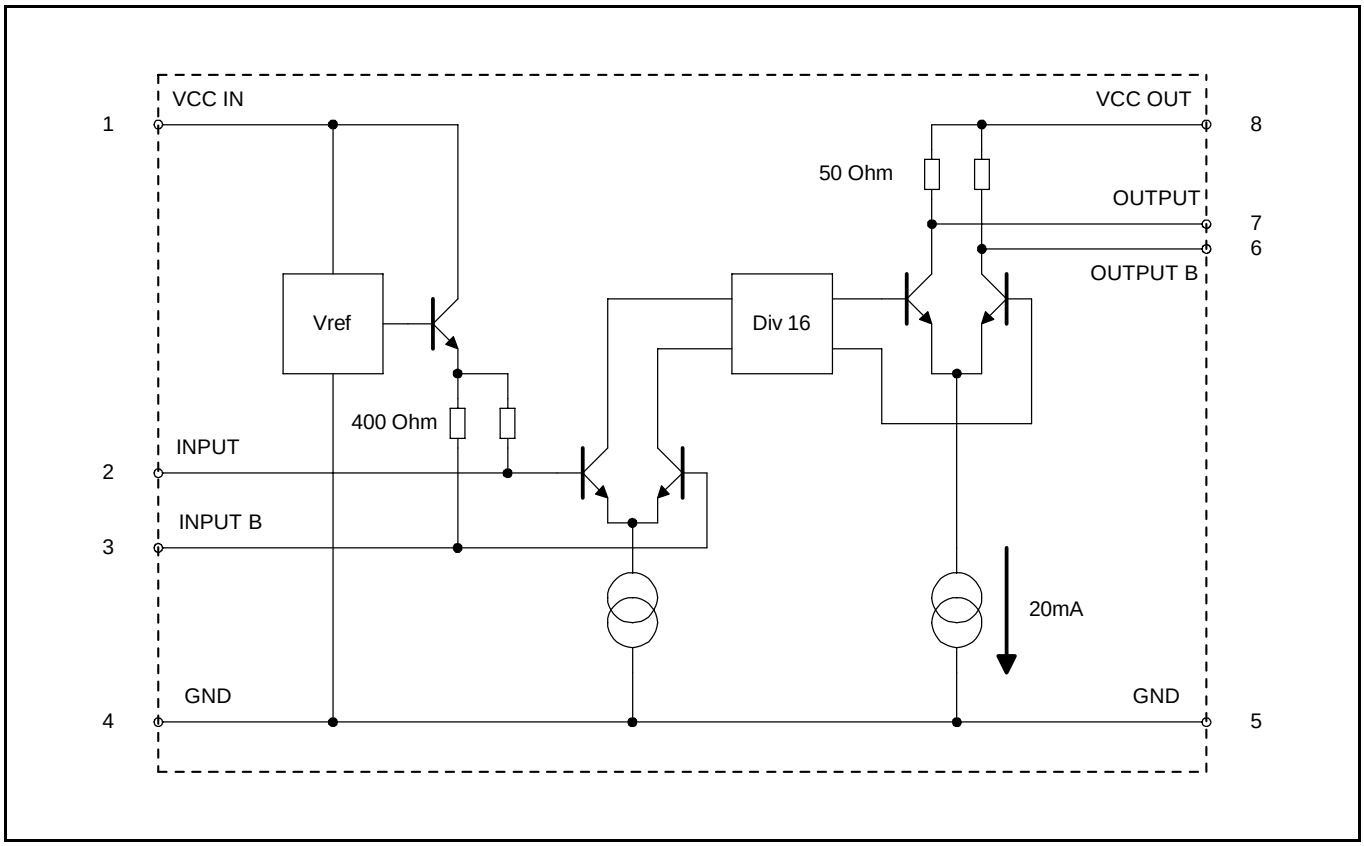
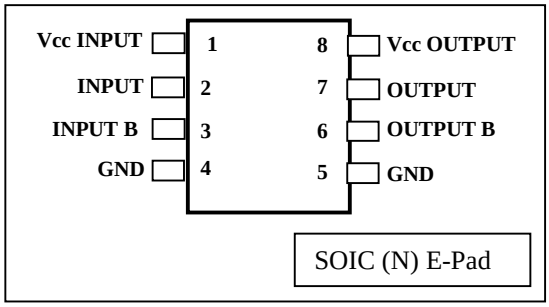


Figure 1 - Block Diagram

Pin Connection - Top View



Application Configuration

Figure 2 shows a recommended application configuration. This example shows the devices set up for single ended operation.

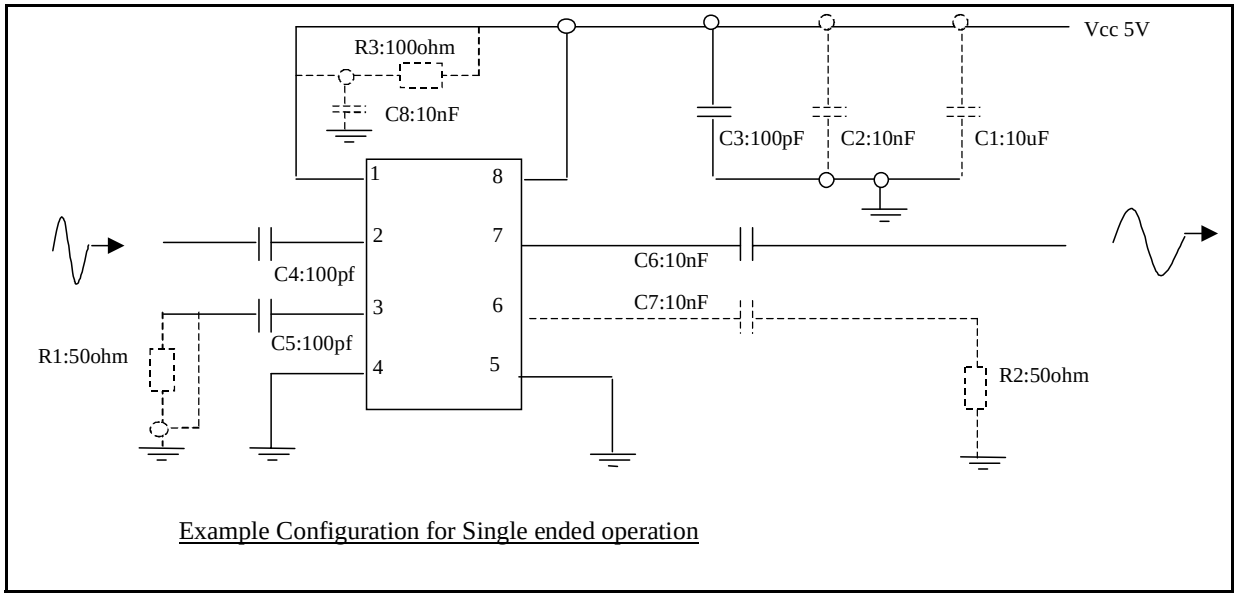


Figure 2 - Recommended Circuit Configuration

The above circuit diagram shows some components in dotted lines. These are optional in many applications.

1. C1 (10 µF) and C2 (10 nF) power supply decoupling capacitors may be available on the board already.
2. R3 (100 Ohm) and C8 (10 nF) can be included if further power supply decoupling is required for the first stage biasing circuit. This may optimise the noise and jitter performance. The values are suggestions and may have to be modified if the existing supplies are particularly noisy.
3. R1 (50 Ohm), in series with C5 (100 pF), may reduce feedthrough of the input signal to the output.
4. R2 (50 Ohm) and C7 (10 nF) will help to balance the current drawn from the power supply and may reduce voltage transients on the power supply line

Evaluation Boards From Zarlink Semiconductor

Zarlink Semiconductor provides prescaler evaluation boards. These are primarily for those interested in performing their own assessment of the operation of the prescalers.

The boards are supplied unpopulated and may be assembled for single ended or differential input and output operation, type No. ZLE40008. Fully populated evaluation boards are also available, type No. ZLE40810. Once assembled, all that is required is an RF source and a DC supply for operation. The inputs and outputs are connected via side launch SMA connectors.

Absolute Maximum Ratings

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	Vcc		6.5V	
2	Prescaler Input Voltage			2.5	Vp-p
3	ESD protection (Static Discharge)			2	kV
4	Storage temperature	T_{ST}	-65	150	ºC
5	Maximum Junction Temp			125	ºC
6	Thermal Characteristics	Thja		58.6	°C/W multi-layer PCB

AC/DC Electrical Characteristics

Electrical Characteristics (Tamb = 25C, Vcc = 5V)† ‡

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	1		0.35		mA	Input stage bias current
Supply current	8		100	130	mA	Divider and output stages
Input frequency	2,3	2		11	GHz	RMS sinewave (See Note 1)
Input sensitivity	2,3		-8		dBm	fin = 1GHz to 2GHz
Input sensitivity	2,3		-15	-10	dBm	fin = 2GHz to 9.5GHz
Input sensitivity	2,3		-10	0	dBm	fin = 11GHz
Input overload	2,3		8		dBm	fin = 1GHz to 4GHz
Input overload	2,3		11		dBm	fin = 5GHz to 11GHz
Input Edge Speed	2,3	900			V/ìs	For <2GHz operation.
Output voltage	6,7		1		Vp-p	Differential Into 50ohm pullup resistors
Output power	6,7	-3	-1	1.2	dBm	Single-ended output, fin = 2GHz to 10GHz, pwr ip= -10dBm
Phase Noise (10kHz offset)	6,7		-152		dBc/Hz	Fin = 5GHz, pwr ip = 0dBm See Figure 5 to Figure 8.
O/P Duty Cycle	6,7	45	50	55	%	

Note 1: The device characterisation test method incremented the amplitude over the entire range of frequency and ensures that there are no "holes" in the characteristic.

† Input sensitivity and output power values assume 50 Ohm source and load impedances.

‡ Characteristics are guaranteed by either production test or design.

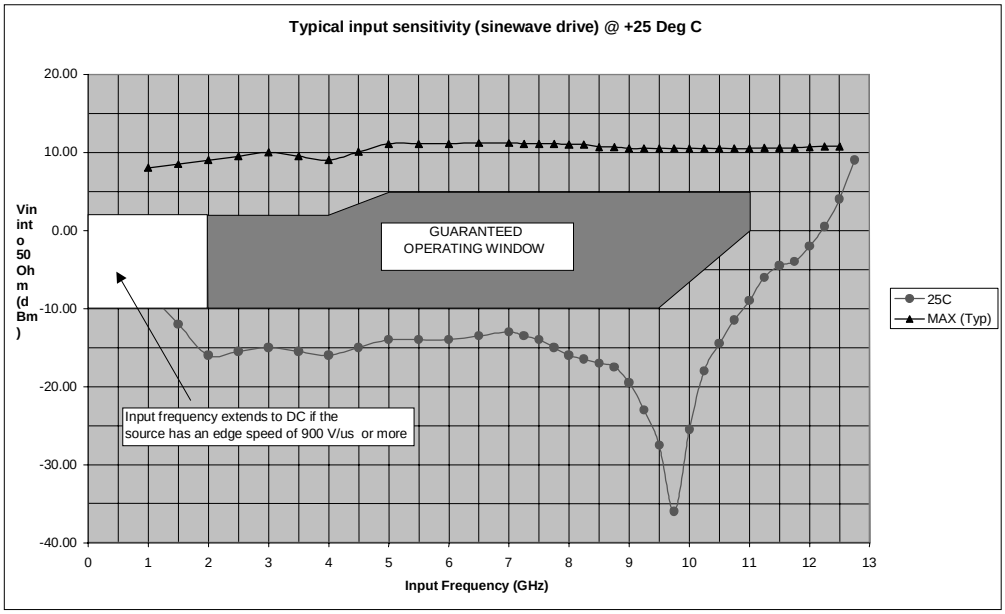


Figure 3 - Input Sensitivity @ +25 Deg C

Electrical Characteristics (Vcc = 5V ±5%, Tamb = -40 to +85C)† ‡

Characteristics	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	1		0.35		mA	Input stage bias current, see Note 1.
Supply current	8	70	99	127	mA	-40 degC 5.25V
Supply current	8	57	80	103	mA	-40 degC 4.75V
Supply current	8	78	109	140	mA	+25 degC 5.25V
Supply current	8	63	88	114	mA	+25 degC 4.75V
Supply current	8	84	119	153	mA	+85 degC 5.25V
Supply current	8	65	94	123	mA	+85 degC 4.75V

Note 1: Pin 1 is the Vcc pin for the 1st stage bias current. In some applications e.g. if the power supply is noisy, it may be advantageous to add further supply decoupling to this pin (i.e. an additional R, C filter, see diagram of the recommended circuit configuration, Figure 2).

† These characteristics are guaranteed by design and characterisation over the range of operating conditions unless otherwise stated.

‡ (Input Frequency range 1 to 10GHz rms Sinewave)

Input and Output Characteristics†

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Input sensitivity	2,3		-15	-10	dBm	Tamb = 85C, Fin = 2 to 8 GHz
Input overload	2,3	2	5		dBm	fin = 2 GHz
Input overload	2,3	2	8		dBm	fin = 4 GHz
Input overload	2,3	5	13		dBm	fin = 9 GHz
Input overload	2,3	5	11		dBm	fin = 10 GHz
Input Edge Speed	2,3	900			V/ìs	For <2GHz Operation, see Note 1
Output voltage	6,7		1		Vp-p	Differential Into 50ohm pullup resistors
Output power	6,7	-4	-1	2	dBm	Single-ended output, fin = 2GHz to 10GHz, pwr ip= -10dBm
O/P Duty Cycle	6,7	45	50	55	%	
Trise and Tfall	6,7		110		ps	

Note 1: for an input signal frequency of less than 2GHz, the slew rate of the sinewave signal becomes progressively too slow for the divider.

† Input sensitivity and output power values assume 50 Ohm source and load impedances

For details of the test set-up, refer to the Application Note for RF Prescalers.

The following graph summarizes the Input and Output Characteristics table:

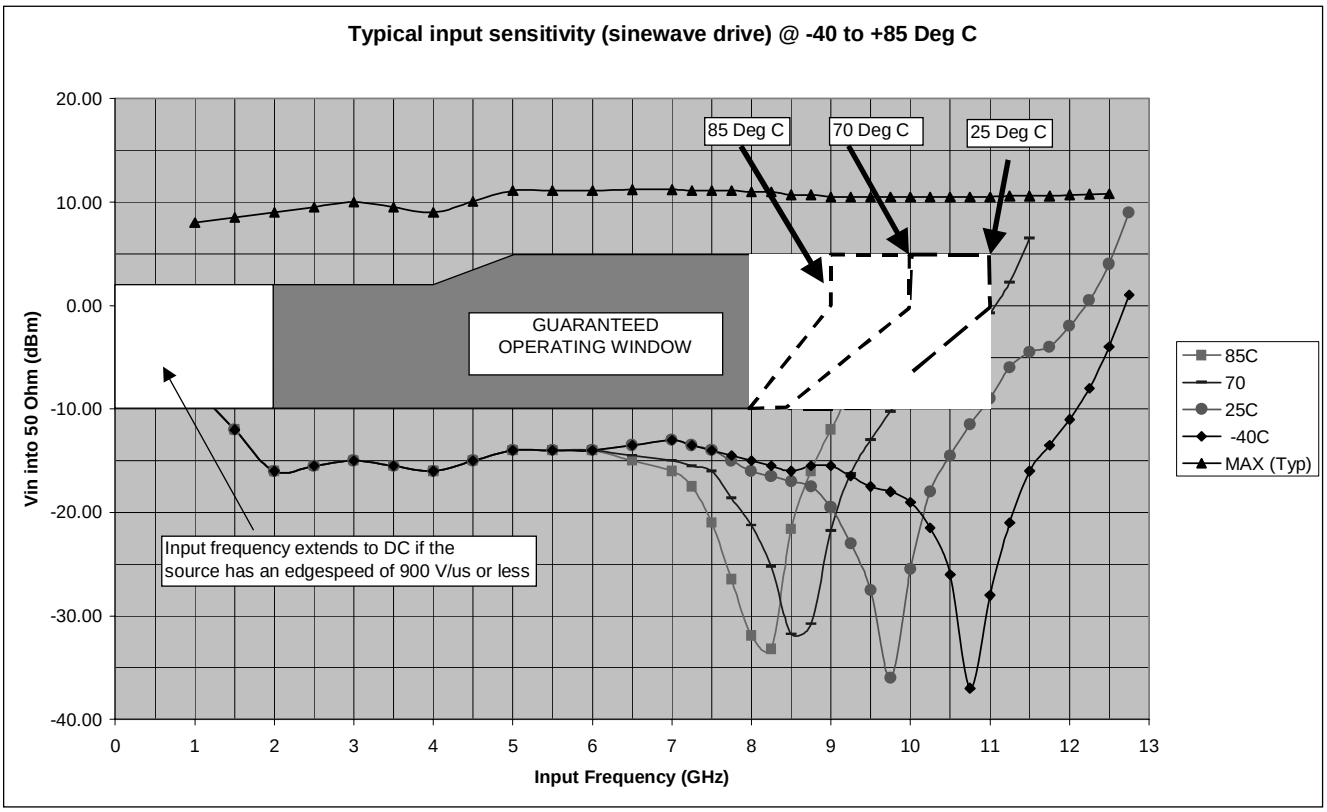


Figure 4 - Input Sensitivity @ -40, +25, +70 and +85 Deg C

Phase Noise Measurement Graphs

The following graph show how the phase noise of the divider output varies with frequency offset from the output (carrier) frequency.

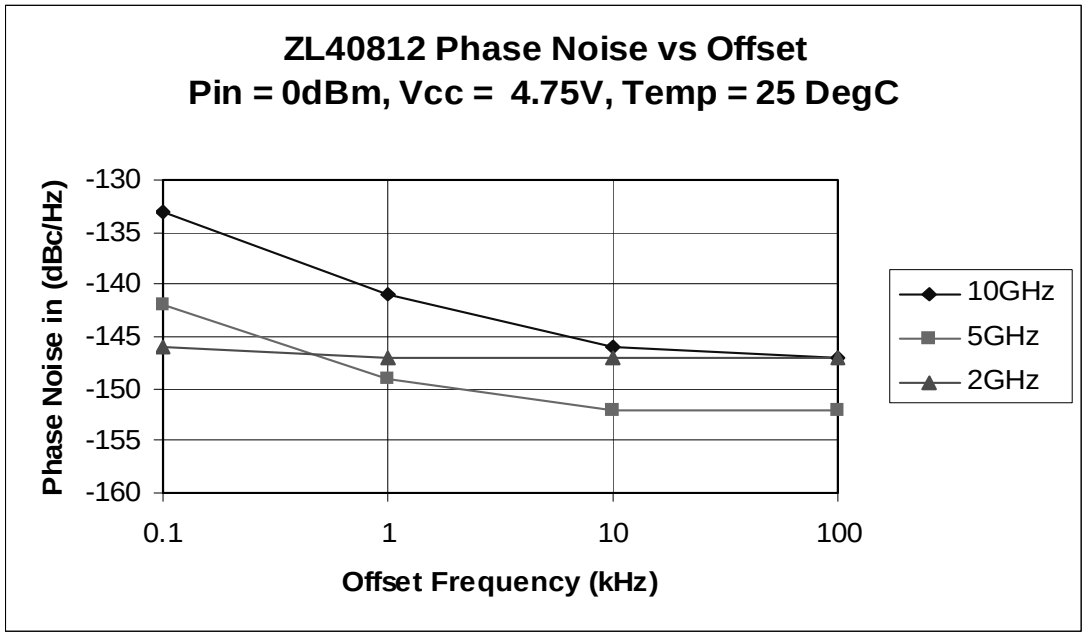


Figure 5 - ZL40812 Phase Noise vs Offset Frequency

The following graph show how the phase noise of the divider output varies with input frequency. The output frequency is the input divided by 16.

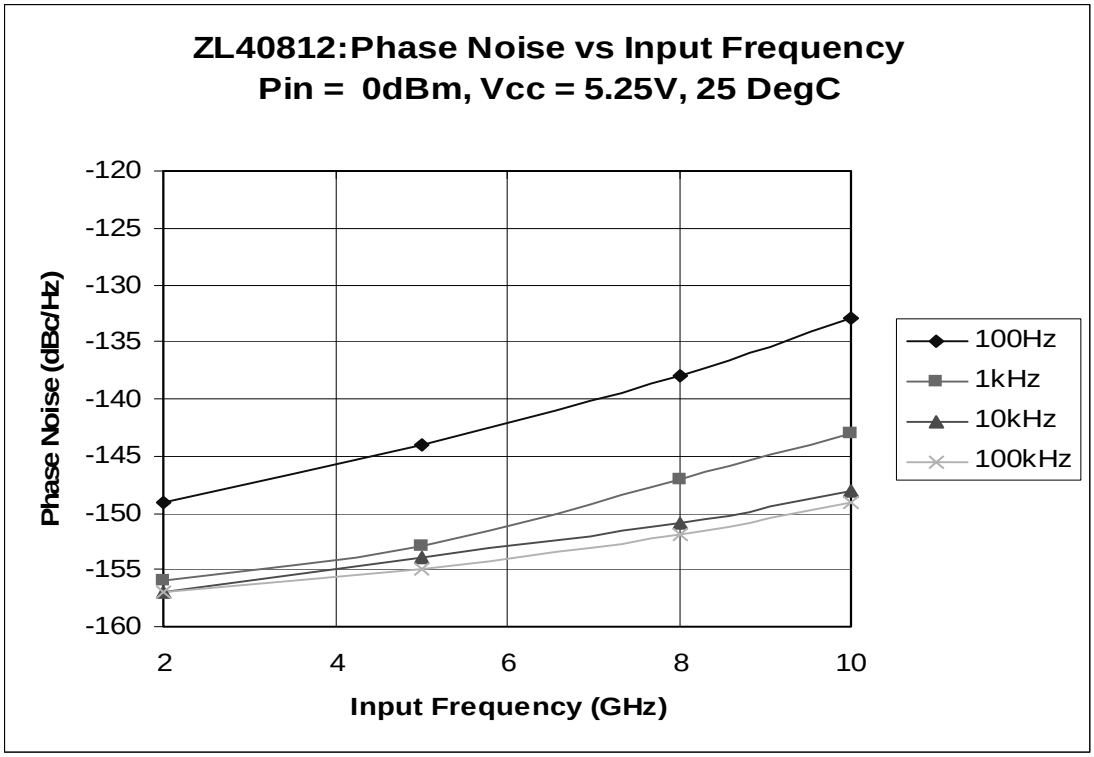


Figure 6 - ZL40812 Phase Noise vs Input Frequency

The following graph show how the phase noise of the divider output varies with input power.

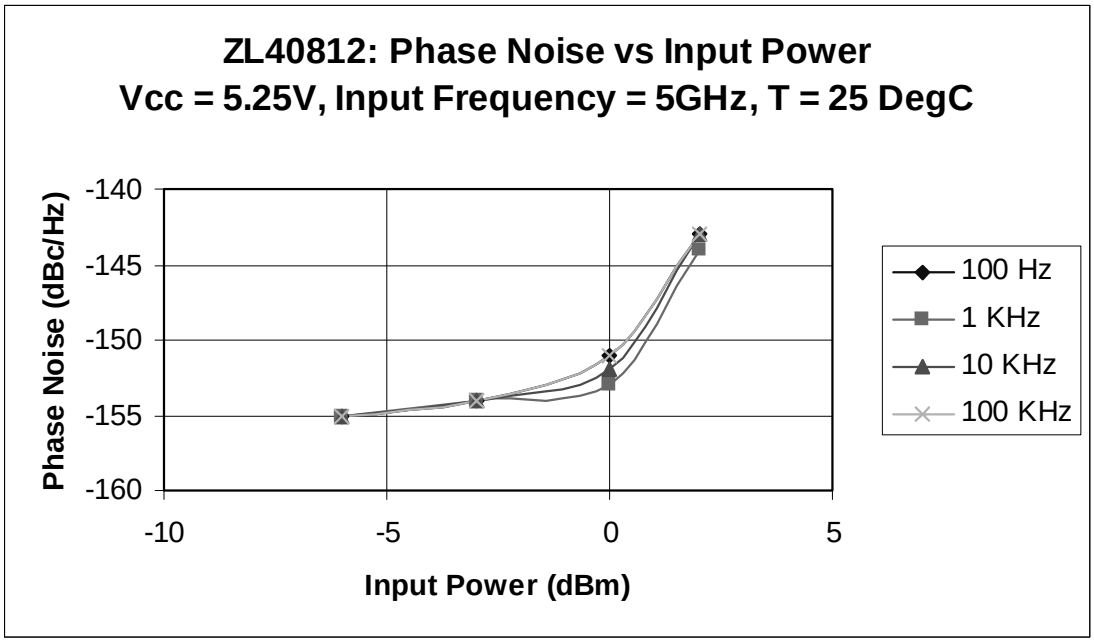


Figure 7 - ZL40812 Phase Noise vs Input Power

The following graph show how the phase noise of the divider output varies with power supply voltage Vcc.

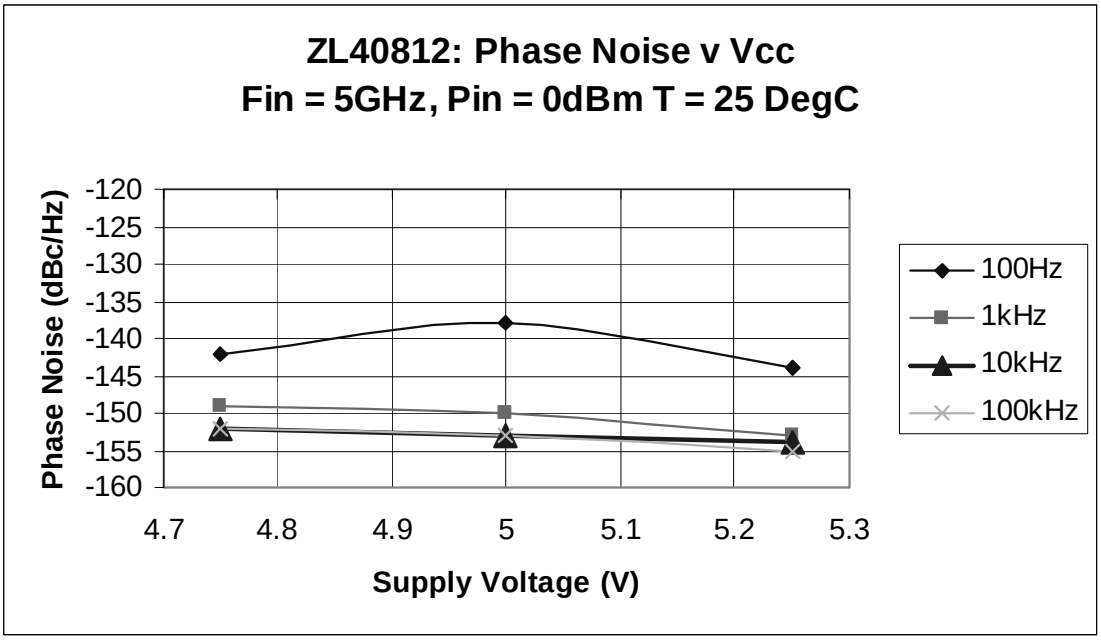


Figure 8 - ZL40812 Phase Noise vs Vcc

Single Ended Output Power

The following graphs show how the output power varies with supply.

Differential output power will be 3dB.

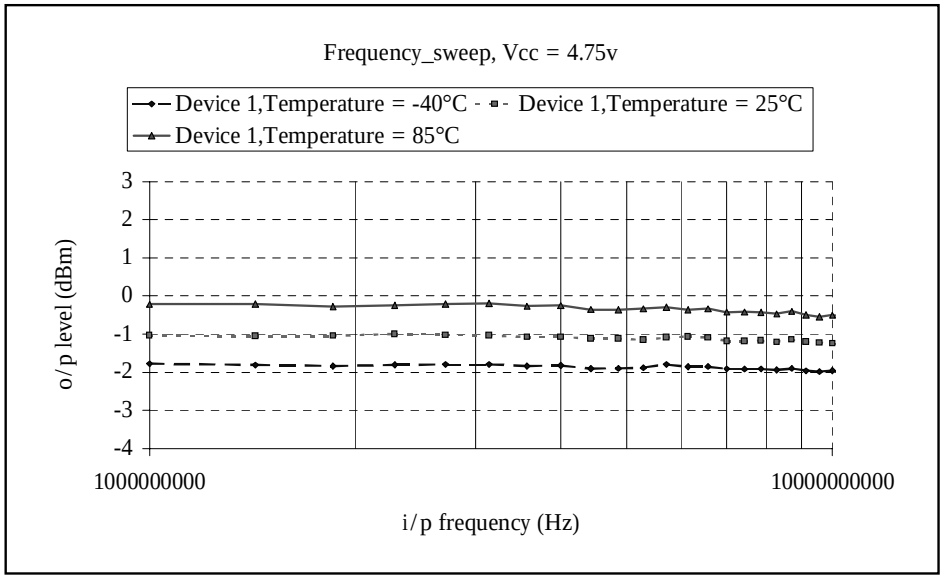


Figure 9 - Pout, Freq, Temp @ Vcc = 4.75V

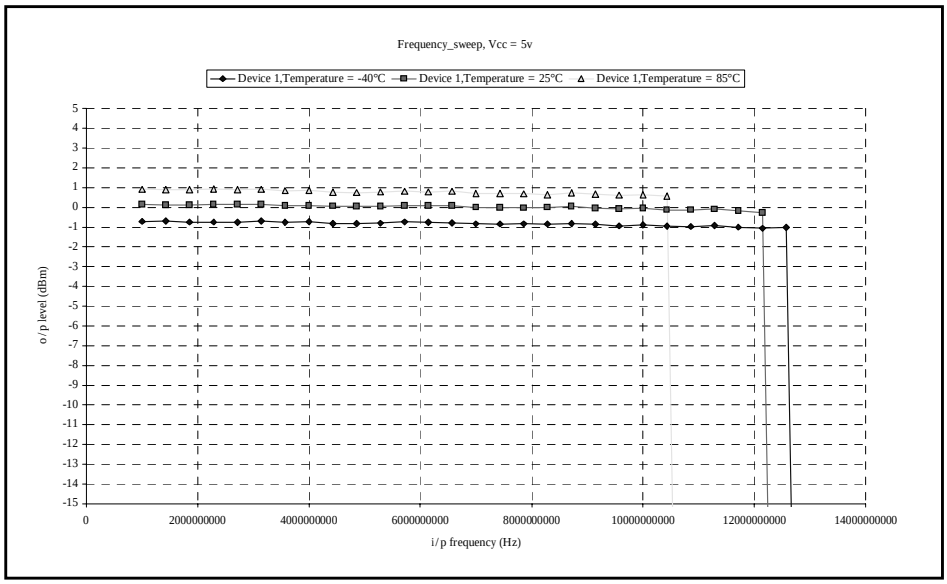


Figure 10 - Pout, Freq, Temp @ Vcc = 5V

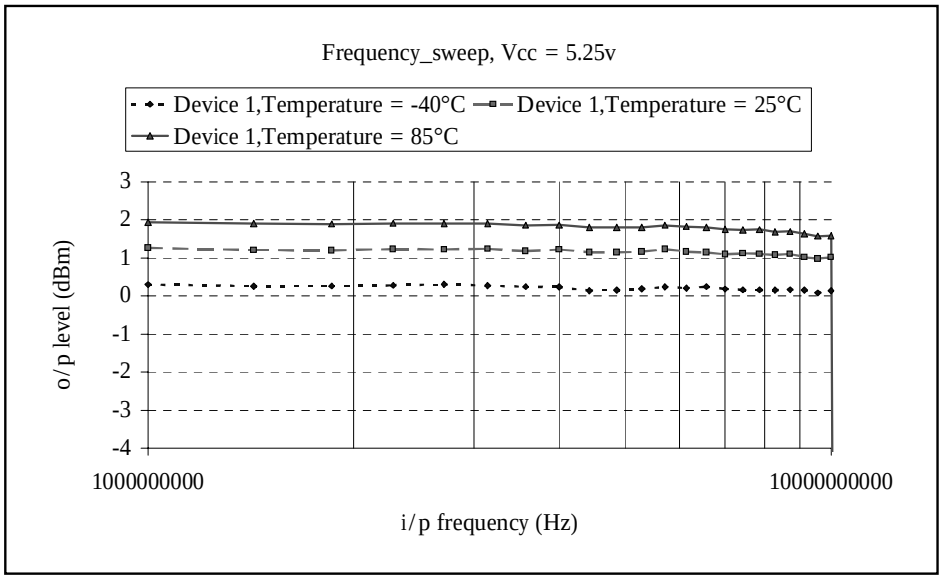


Figure 11 - Pout, Freq, Temp @ Vcc = 5.25V

Oscillographs of the Divider Output Waveforms

The following oscillographs show that the low-level feedthrough of the input waveform can be further reduced by summing the two output pins of the device differentially, refer to Figure 12 and Figure 13.

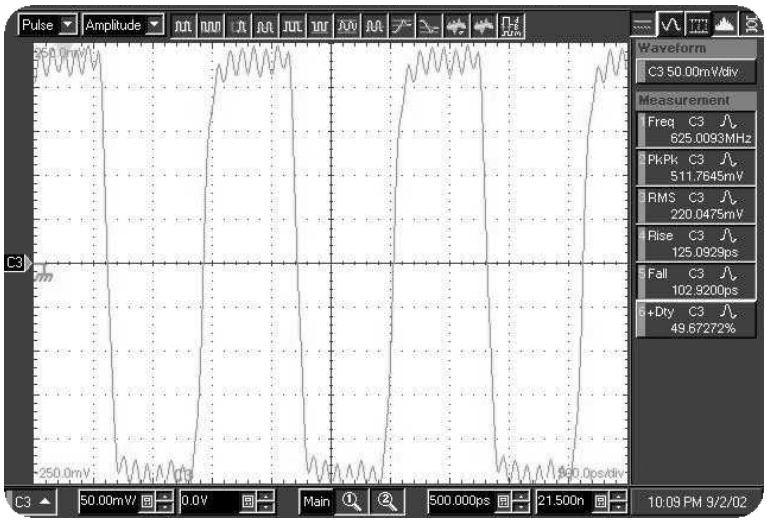


Figure 12 - Output waveform-single-ended VCC=5V, Vin=2dBm, Fin=10GHz

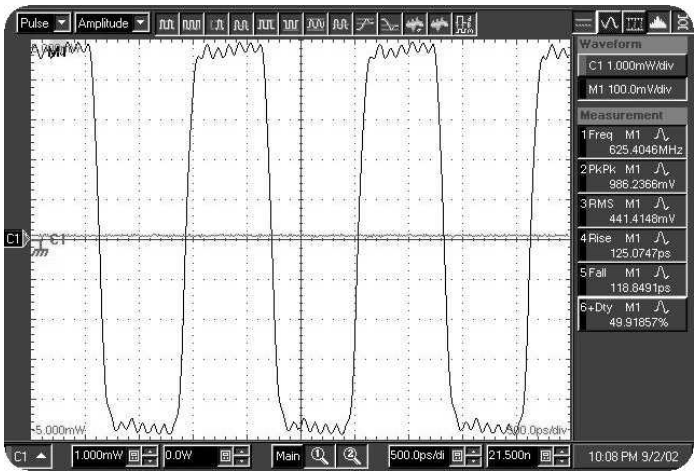


Figure 13 - Output waveform - differential VCC=5V, Vin=2dBm, Fin=10GHz

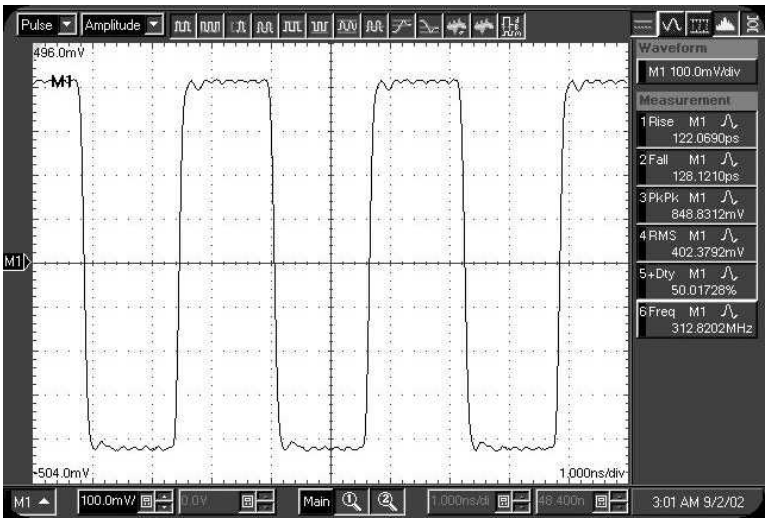


Figure 14 - Output waveform - differential
VCC=4.75V, Vin=-10dBm, Fin=5GHz

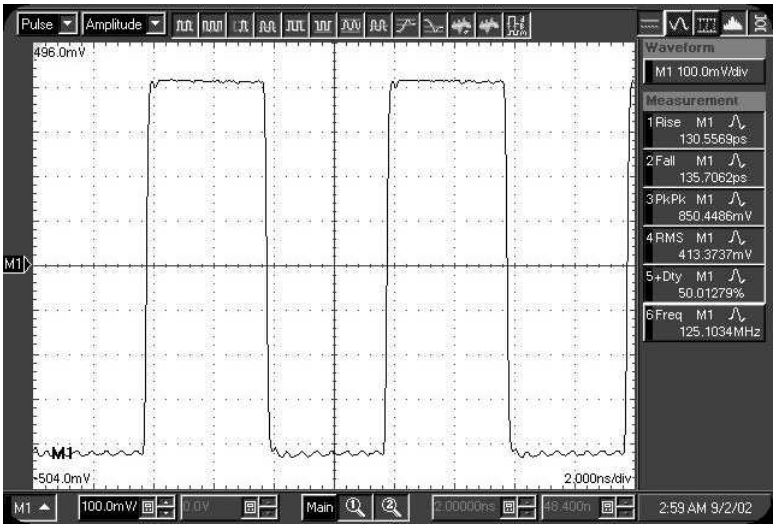
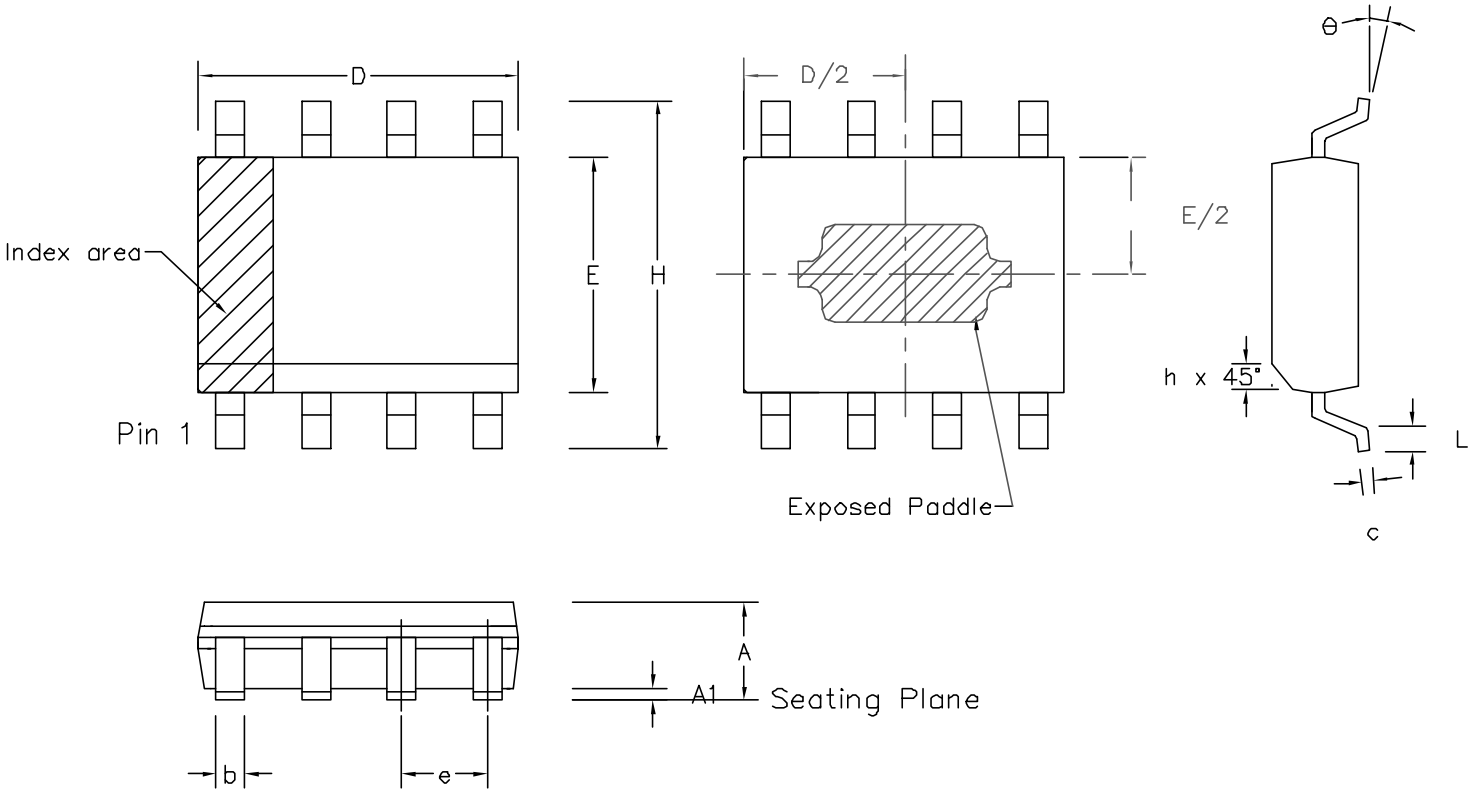


Figure 15 - Output waveform - differential
VCC=4.75V, Vin=-dBm, Fin=2GHz



	Min Inches	Max inches	Min mm	Max mm
A	0.056	0.066	1.43	1.68
A1	0.000	0.004	0.00	0.10
D	0.189	0.196	4.80	4.98
H	0.230	0.244	5.84	6.20
E	0.150	0.157	3.81	3.99
L	0.16	0.35	0.41	0.89
e	0.050 BSC		1.27 BSC	
b	0.0138	0.0192	0.35	0.49
c	0.0075	0.0098	0.19	0.25
Θ	0°	8°	0°	8°
h	0.010	0.016	0.25	0.41
	Pin Features		Pin Features	
N	8		8	

Notes:

1. Controlling dimensions are in inches.
2. Dimensions D & E do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
3. Exposed paddle not to scale on drawing
4. Extrusion of the exposed pad in bottom side is 0.20 mmTypical
5. Exposed Paddle dimension is 90x90mil Square max, and is governed by the leadframe paddle size.

ISSUE	1	2			
ACN	212933	214385			
DATE	14Jun02	13Jun03			
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MH / S

Package Code DC

Package Outline for 8 lead e-pad SOIC (0.150" Body width)

GPD00790

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE