ZL40815

10GHz Fixed Modulus ÷ 4

Data Sheet

March 2006

Features

- Very High Operating Speed
- Operation down to DC with Square Wave Input
- Low Phase Noise (Typically better than -146 dBc/Hz at 10 kHz)
- 5 V Single Supply Operation
- Low Power Dissipation: 510 mW (Typ)
- Surface Mount Plastic Package With Exposed Pad (See Application Notes)

Applications

- DC to 10 GHz PLL applications
- HyperLan
- LMDS
- Instrumentation
- Satellite Communications
- Fibre Optic Communications; OC48, OC192
- Ultra Low Jitter Clock Systems

Ordering Information

ZL40815DCE	8 Pin SOP/SOIC	Tubes, Bake & Drypack
ZL40815DCF	8 Pin SOP/SOIC	Tape & Reel, Bake & Drypack
ZL40815DCF1	8 Pin SOP/SOIC*	Tape & Reel, Bake & Drypack
ZL40815DCE1	8 Pin SOP/SOIC*	Tubes, Bake & Drypack

*Pb Free Matte Tin

-40°C to +85°C

Description

The ZL40815 is one of a range of 5 V supply, very high speed, low power prescalers for professional applications with a fixed modulus of divide by 4. The dividing elements are static D type flip flops, and therefore, allow operation down to DC if the drive signal is a pulse waveform with fast risetimes. The output stage has internal 50 ohm pull up giving a 1 V p-p output. See application notes for more details

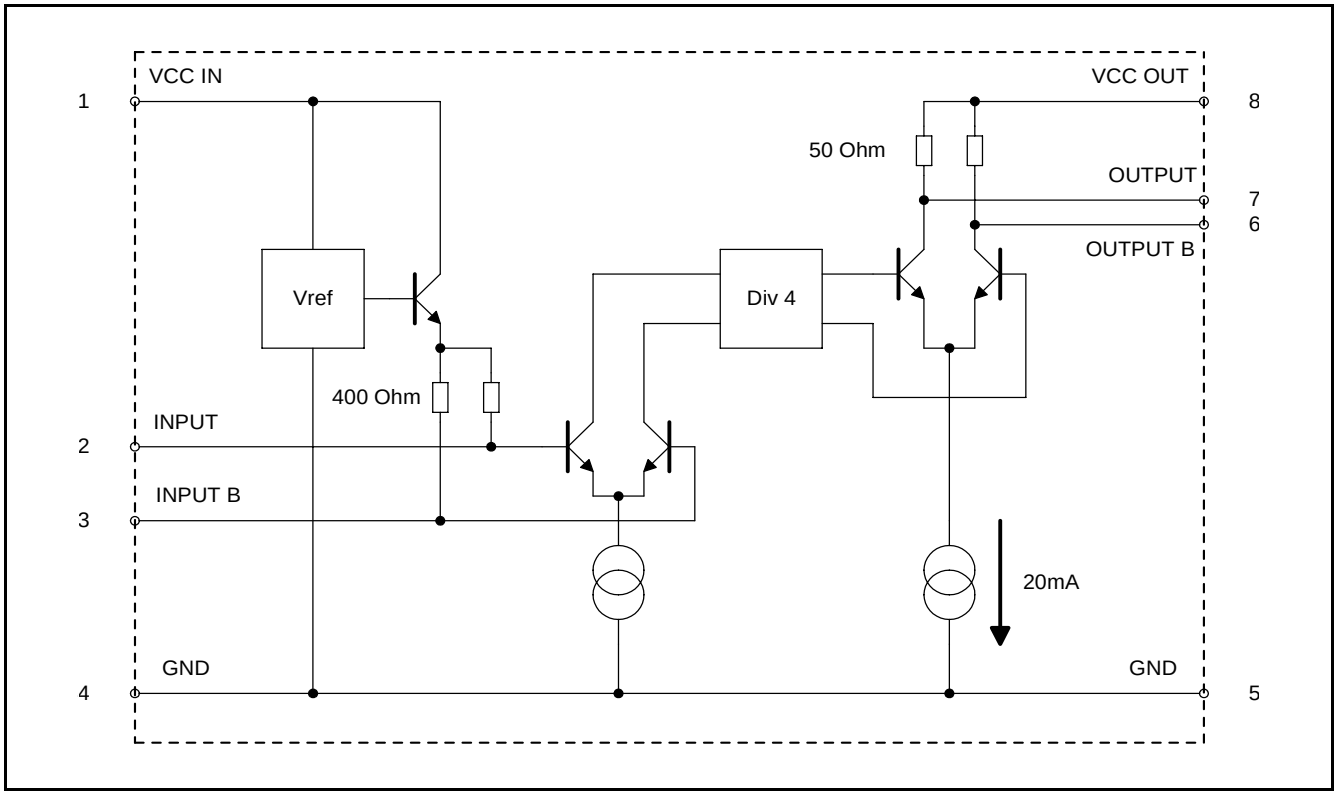
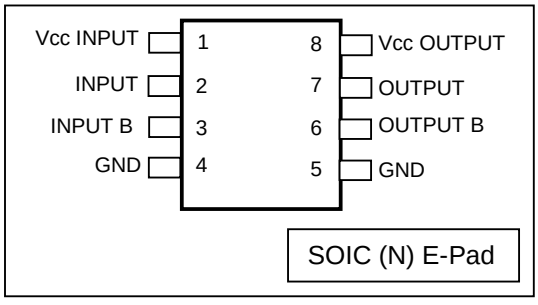


Figure 1 - Block Diagram

Pin Connections - Top View



Applications Configuration

Figure 2 shows a recommended application configuration. This example shows the devices set up for single ended operation.

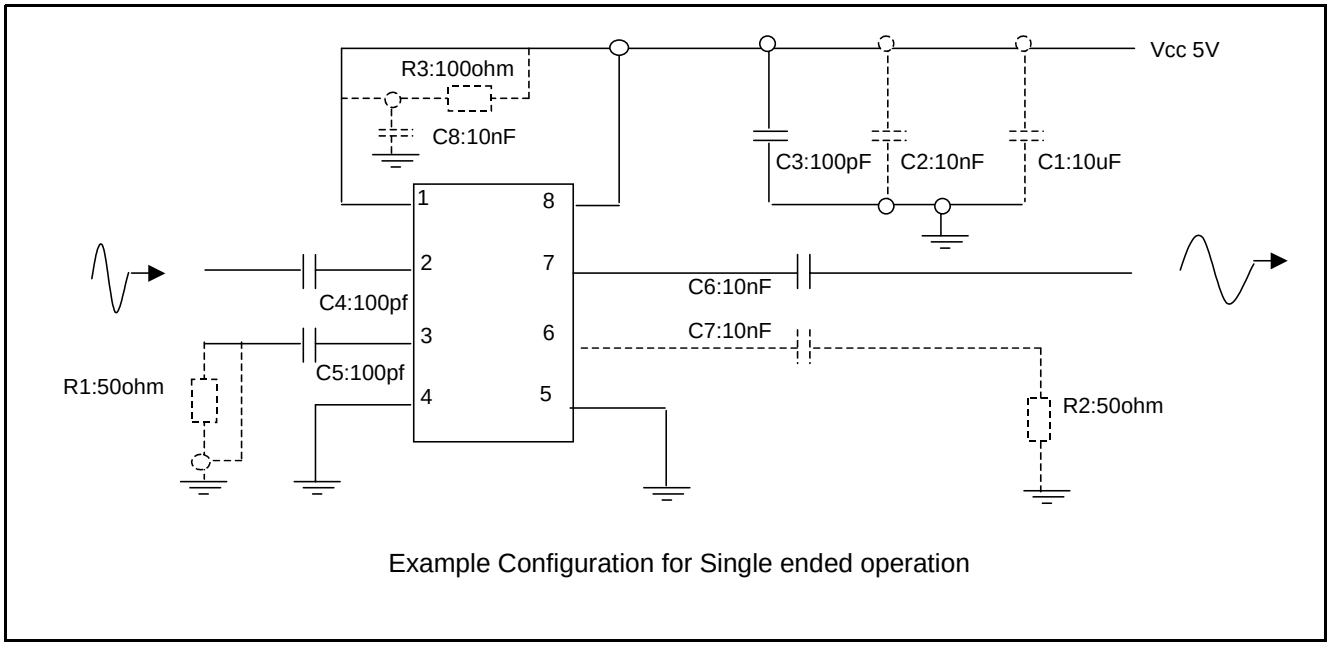


Figure 2 - Recommended circuit configuration

The above circuit diagram shows some components in dotted lines. These are optional in many applications.

1. C1 (10 µF) and C2 (10 nF) power supply decoupling capacitors may be available on the board already.
2. R3 (100 Ohm) and C8 (10 nF) can be included if further power supply decoupling is required for the first stage biasing circuit. This may optimize the noise and jitter performance. The values are suggestions and may have to be modified if the existing supplies are particularly noisy.
3. R1 (50 Ohm), in series with C5 (100 pF), may reduce feedthrough of the input signal to the output.
4. R2 (50 Ohm) and C7 (10 nF) will help to balance the current drawn from the power supply and may reduce voltage transients on the power supply line.

Evaluation Boards From Zarlink Semiconductor

Zarlink Semiconductor provides prescaler evaluation boards. These are primarily for those interested in performing their own assessment of the operation of the prescalers.The boards are supplied unpopulated and may be assembled for single ended or differential input and output operation, type No. ZLE40008. Fully populated evaluation boards are also available, type No. ZLE40810. Once assembled, all that is required is an RF source and a DC supply for operation. The inputs and outputs are connected via side launch SMA connectors.

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	Vcc		6.5	V
2	Prescaler Input Voltage		2.5	(Vdd_IO+5%)	Vp-p
3	ESD protection (Static Discharge)		2k		V
4	Storage temperature	T_{ST}	-65	+150	°C
5	Maximum Junction Temp	$T_J$max		+125	°C
6	Thermal characteristics	TH_{ja}	58.6		°C/W multi-layer PCB

AC/DC Electrical Characteristics

Electrical Characteristics (Tamb = 25C, Vcc = 5V)†

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	1		0.35		mA	Input stage bias current
Supply current	8		102	130	mA	Divider and output stages
Input frequency	2,3	2		11	GHz	RMS sinewave (see Note 1)
Input sensitivity	2,3		-8		dBm	fin = 1 GHz to 2 GHz
Input sensitivity	2,3		-15	-10	dBm	fin = 2 GHz to 9.5 GHz
Input sensitivity	2,3		-10	0	dBm	fin = 11 GHz
Input overload	2,3		8		dBm	fin = 1 GHz to 4 GHz
Input overload	2,3		11		dBm	fin = 5 GHz to 11 GHz
Input Edge Speed	2,3	900			V/ìs	For <2 GHz operation.
Output voltage	6,7		1		Vp-p	Differential Into 50 ohm pullup resistors
Output power	6,7	-3	-1	1.2	dBm	Single-ended output, fin = 2 GHz to 10 GHz, pwr ip= -10 dBm
Phase Noise (10kHz offset)	6,7		-146		dBc/Hz	Fin = 5 GHz, pwr ip = 0 dBm See Figure 7 and Figure 8.
O/P Duty Cycle	6,7	45	50	55	%	

Note 1: Input sensitivity and output power values assume 50 Ohm source and load impedances.

† The following characterization test method incremented the amplitude over the entire range of frequency and ensures that there are no "holes" in the characteristic.

† The following characteristics are guaranteed by either production test or design.

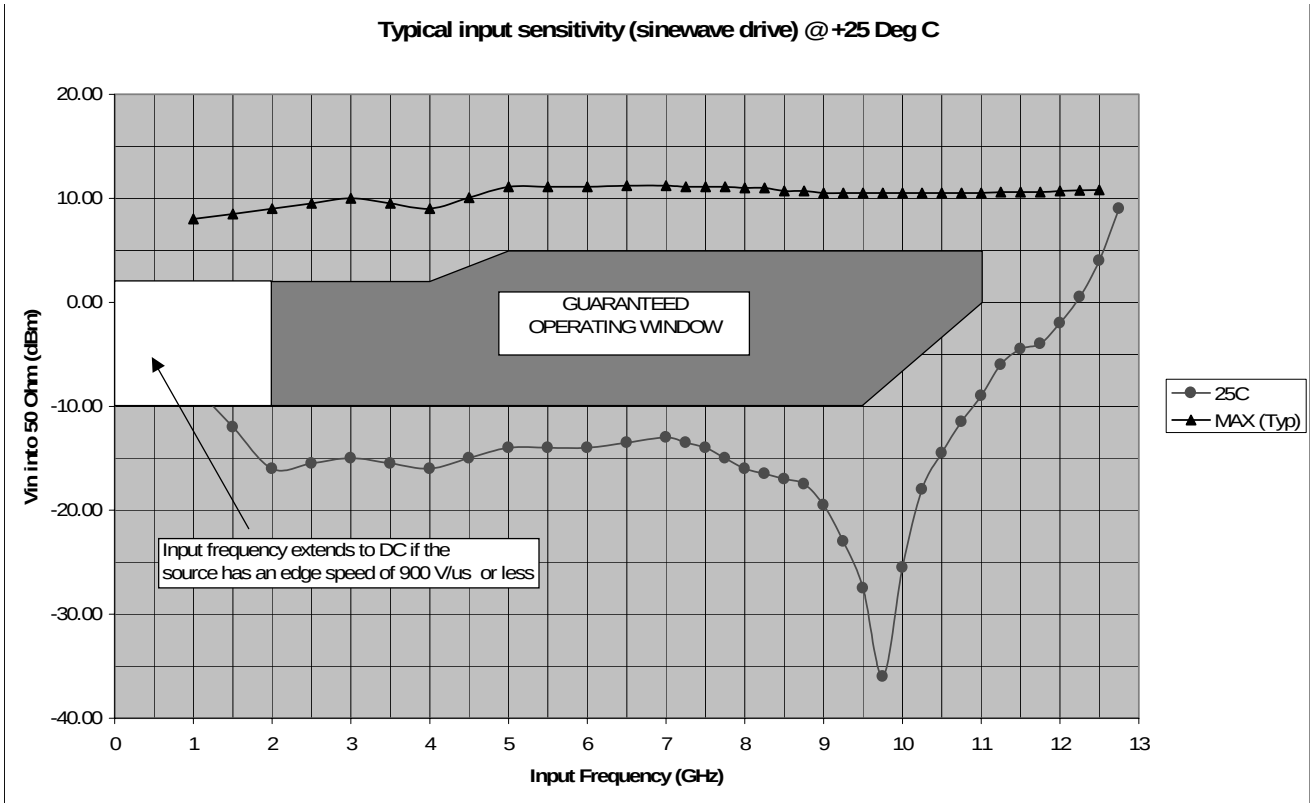


Figure 3 - Input Sensitivity @ +25°C

Electrical Characteristics (Vcc = 5V ±5%, Tamb = -40 to +85C)†

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	1		0.35		mA	Input stage bias current (see Note 1)
Supply current	8	73	102	131	mA	-40°C 5.25 V
Supply current	8	59	83	106	mA	-40°C 4.75 V
Supply current	8	81	112	142	mA	+25°C 5.25 V
Supply current	8	65	91	116	mA	+25°C 4.75 V
Supply current	8	87	121	156	mA	+85°C 5.25 V
Supply current	8	67	96	125	mA	+85°C 4.75 V

Note 1: Pin 1 is the Vcc pin for the 1st stage bias current. In some applications e.g., if the power supply is noisy, it may be advantageous to add further supply decoupling to this pin (i.e., an additional R, C filter, see diagram of the recommended circuit configuration, figure 9).

† The characteristics are guaranteed by design and characterisation over the range of operating conditions unless otherwise stated:

‡ (Input Frequency range 1 to 10 GHz rms Sinewave)

Input and Output Characteristics†

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Input sensitivity	2,3		-15	-10	dBm	Tamb = 85C, Fin = 2 to 8 GHz
Input overload	2,3	2	5		dBm	fin = 2 GHz
Input overload	2,3	2	8		dBm	fin = 4 GHz
Input overload	2,3	5	13		dBm	fin = 9 GHz
Input overload	2,3	5	11		dBm	fin = 10 GHz
Input Edge Speed	2,3	900			V/ìs	For <2GHz Operation, see Note 1
Output voltage	6,7		1		Vp-p	Differential Into 50 ohm pullup resistors
Output power	6,7	-4	-1	2	dBm	Single-ended output, fin = 2 GHz to 10GHz, pwr ip= -10dBm
O/P Duty Cycle	6,7	45	50	55	%	
Trise and Tfall	6,7		110		ps	

Note 1: Input sensitivity and output power values assume 50 Ohm source and load impedances.
† Input sensitivity and output power values assume 50 Ohm source and load impedances.

For details of the test set-up, refer to the Application Note for RF Prescalers.

The following graph summarizes the Input and Output Characteristics table.

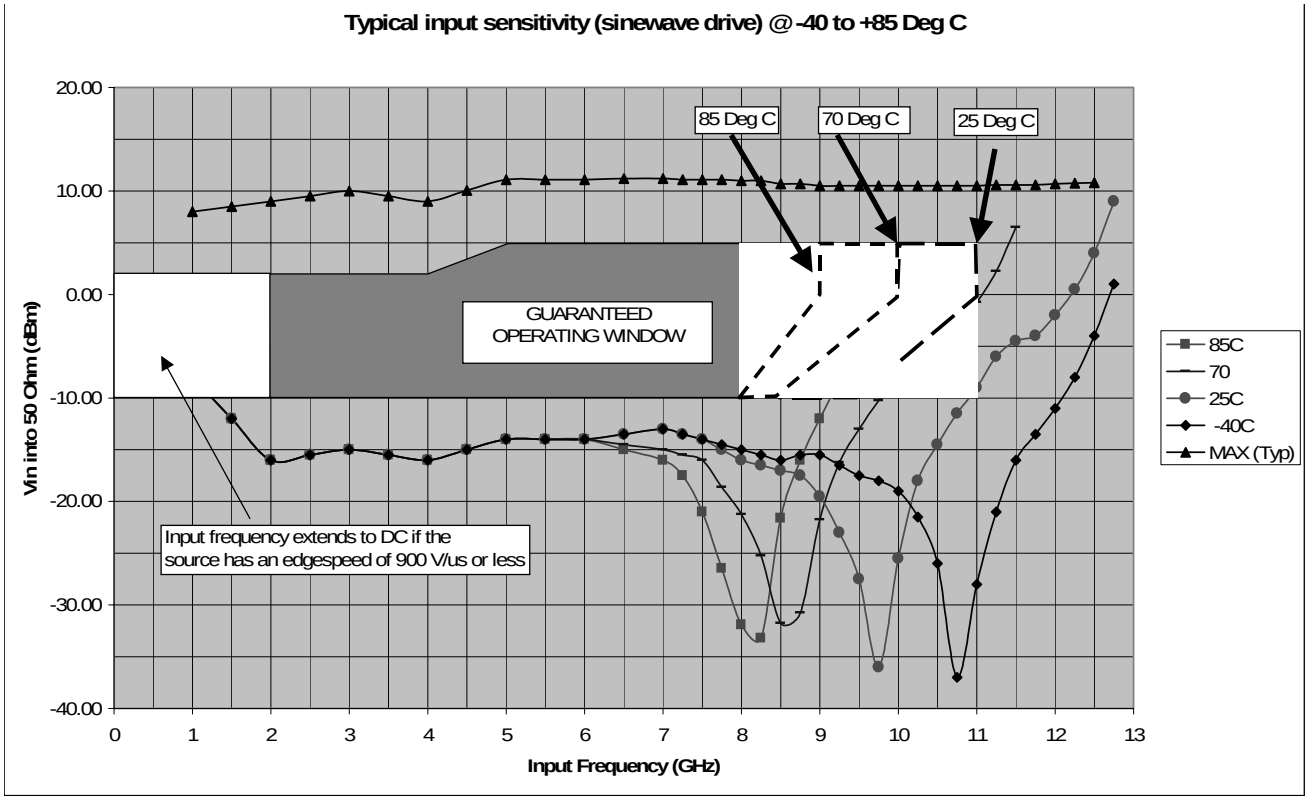


Figure 4 - Input Sensitivity @ -40, +25, +70 and +85°C

Phase Noise Measurement Graphs

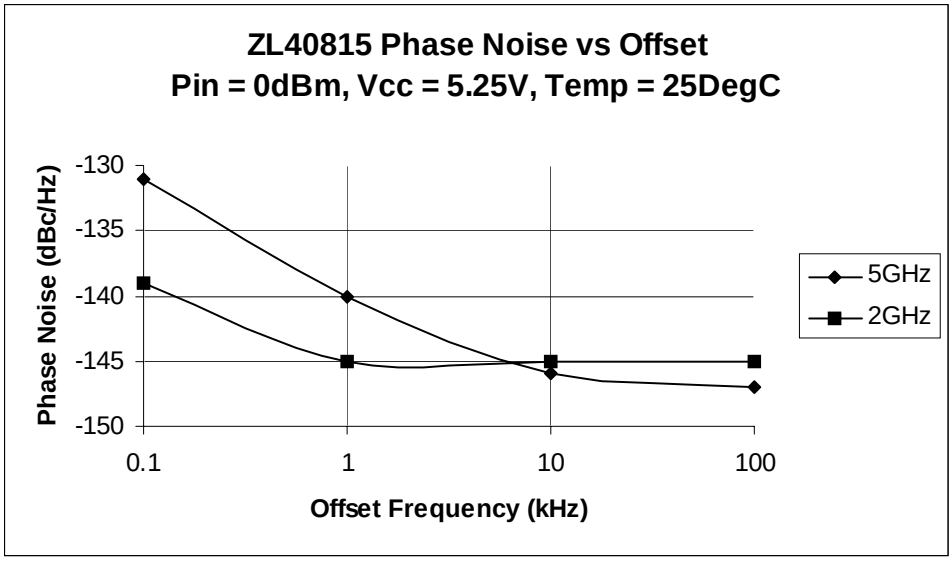


Figure 5 - ZL40815 Phase Noise vs Offset Frequency

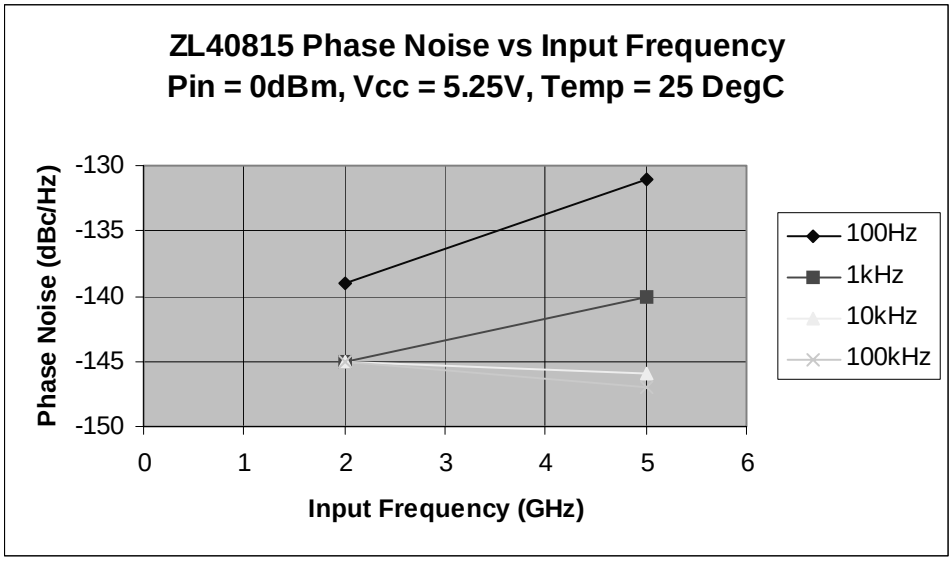


Figure 6 - ZL40815 Phase Noise vs Input Frequency

Single Ended Output Power

The following graphs show how the output power varies with supply.

Differential output power will be 3 dB.

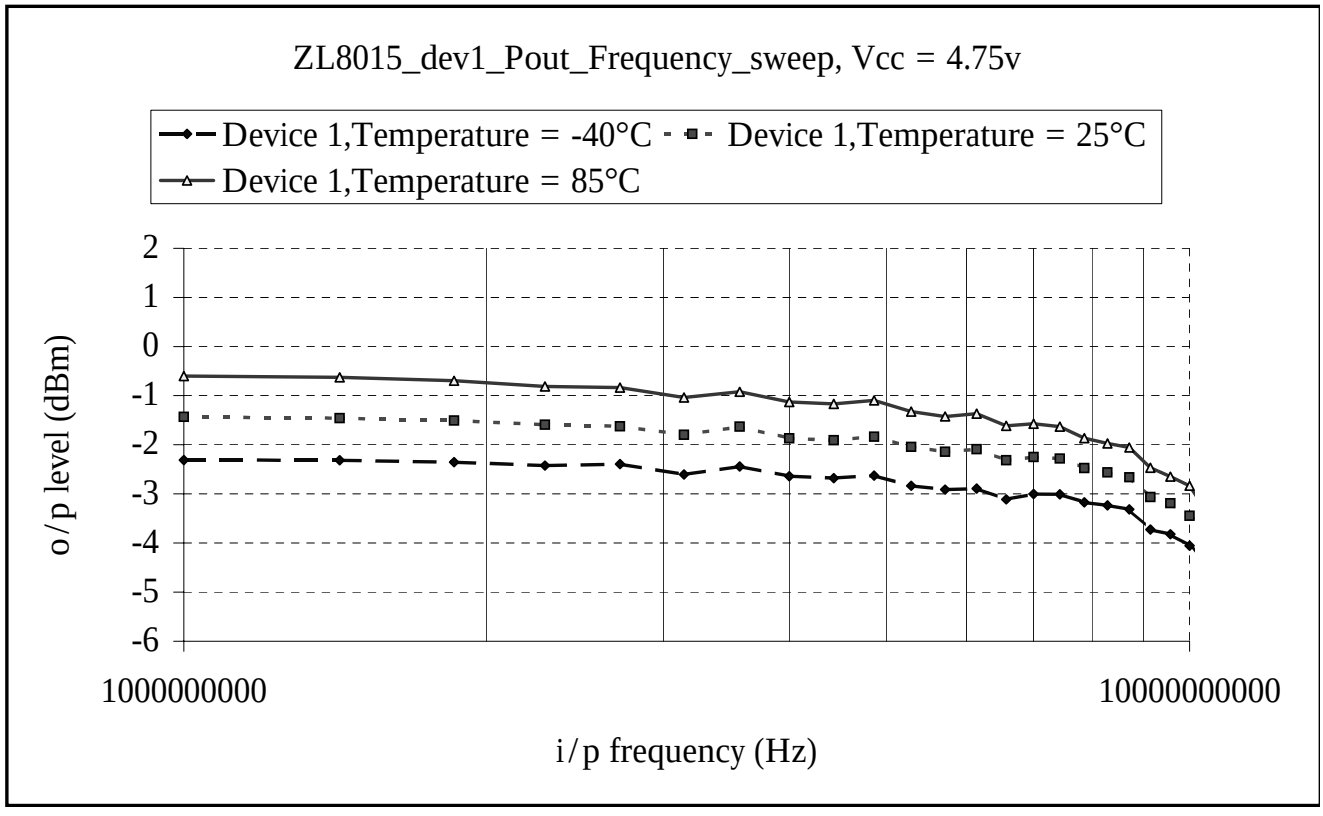


Figure 7 - Pout, Freq, Temp @ Vcc = 4.75 V

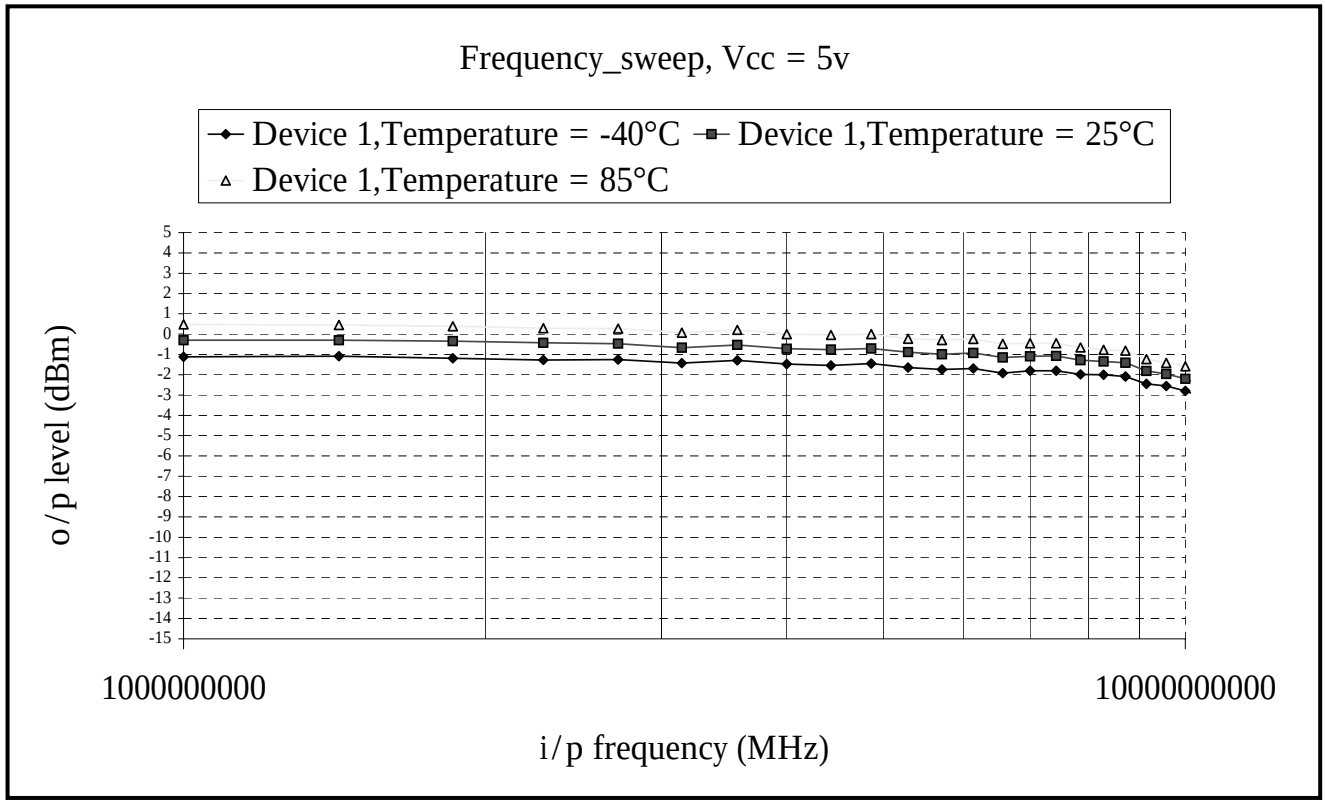


Figure 8 - Pout, Freq, Temp @ Vcc = 5 V

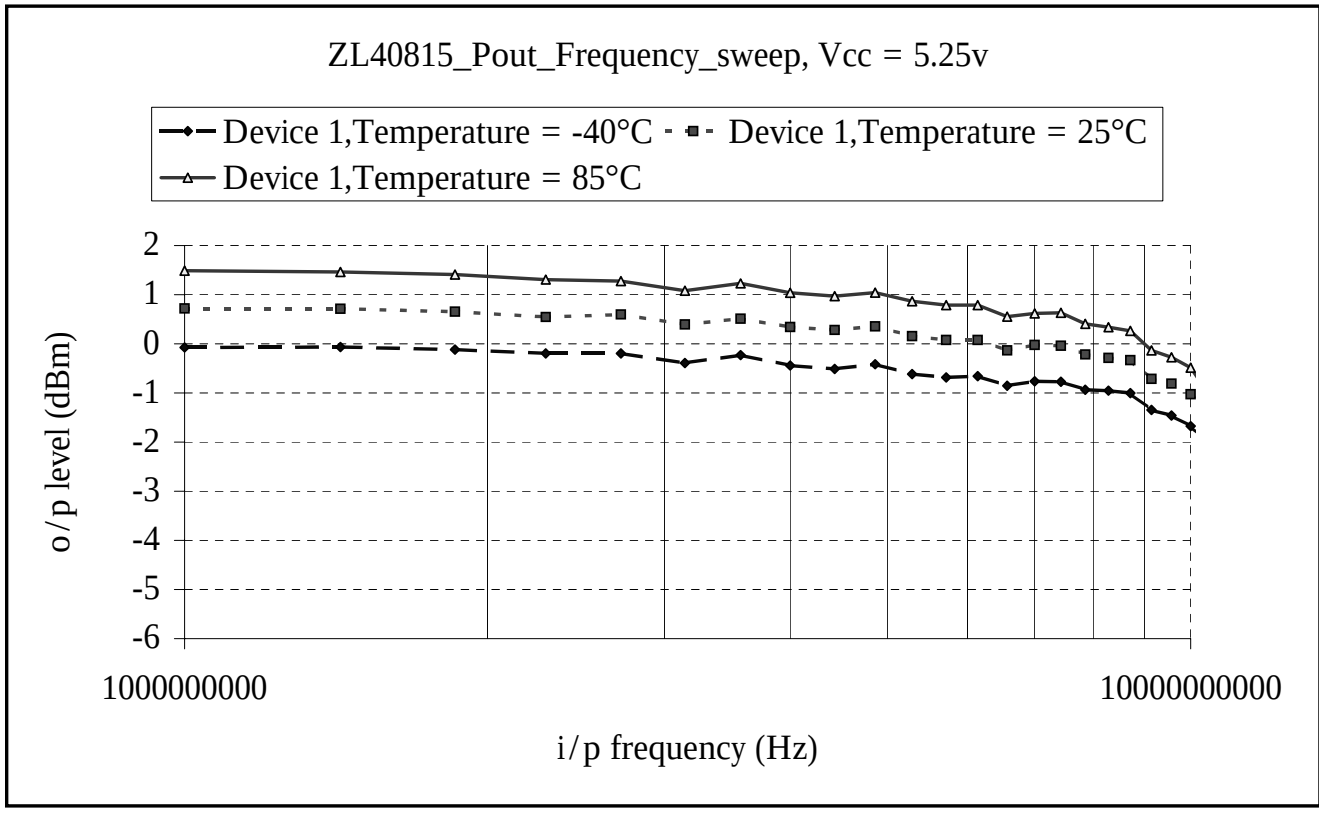


Figure 9 - Pout, Freq, Temp @ Vcc = 5.25 V

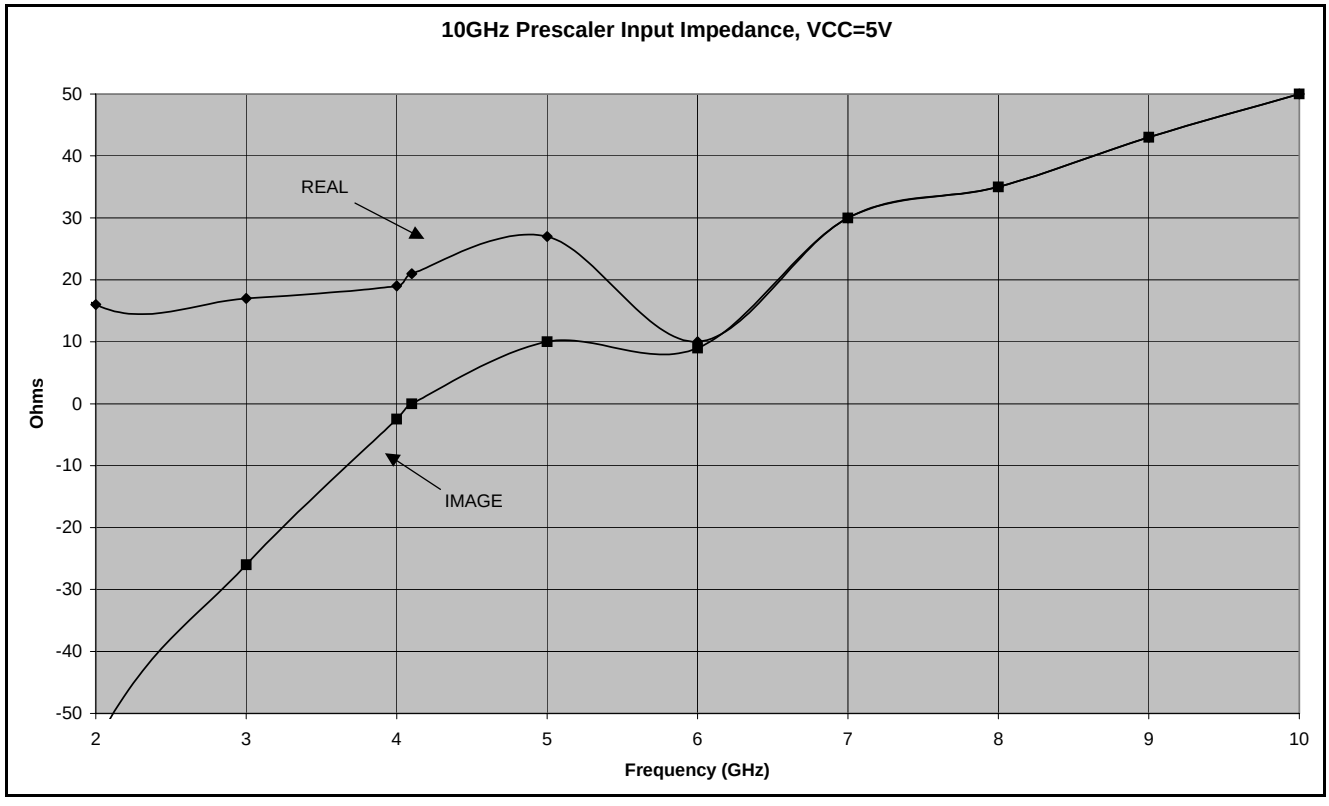


Figure 10 - Input Impedance of 10 GHz Prescalers

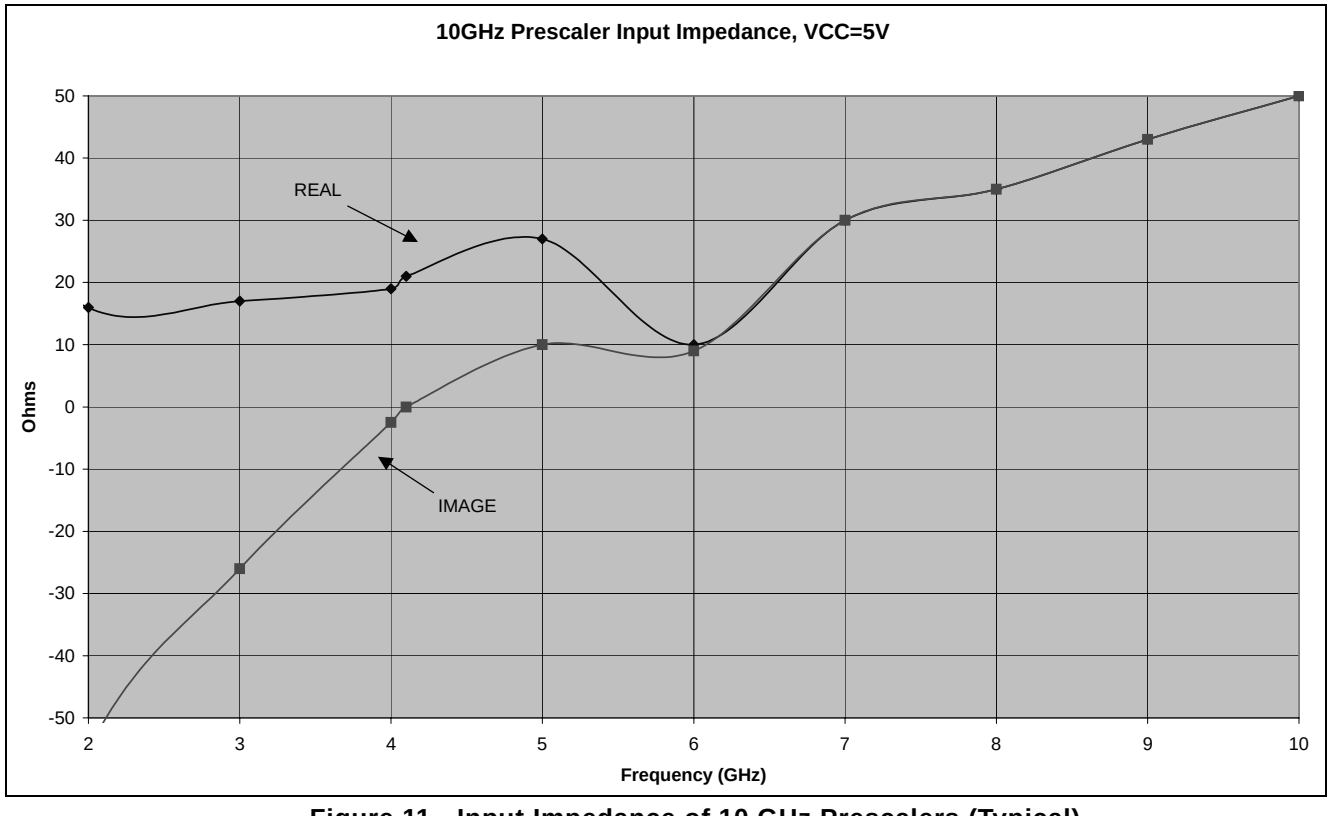


Figure 11 - Input Impedance of 10 GHz Prescalers (Typical)

Oscillographs of the Divider Output Waveforms

The following oscillographs show that the low-level feedthrough of the input waveform can be further reduced by summing the two output pins of the device differentially, refer to Figure 12 and Figure 13.

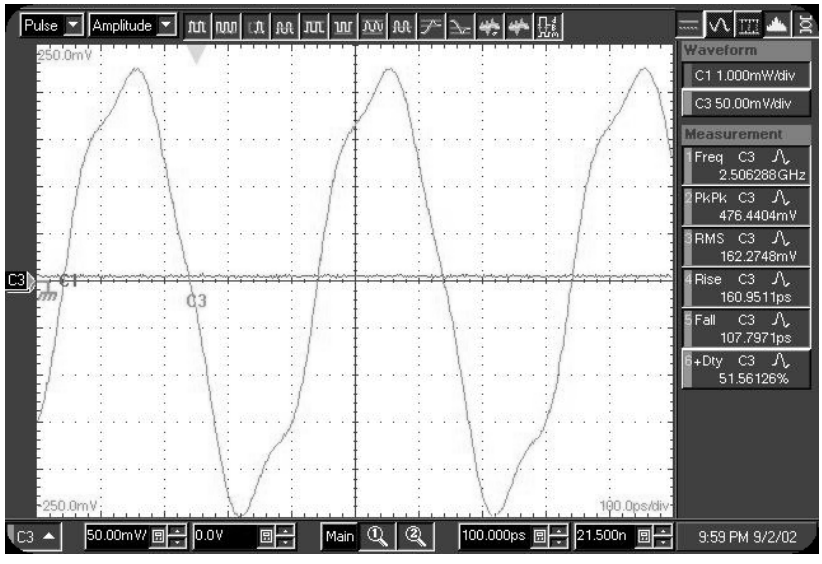


Figure 12 - Feedthrough of the input single-ended-output configuration VCC = 5 V, Vin = 2 dBm, Fin = 10 GHz

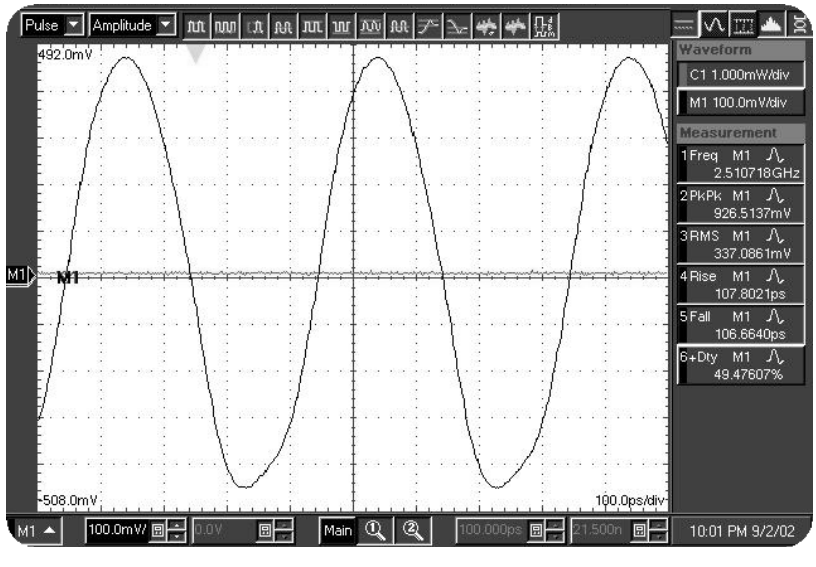


Figure 13 - Feedthrough of the input using differential output configuration VCC = 5 V, Vin = 2 dBm, Fin = 10 GHz

Figure 14 and Figure 15 show the output waveforms with a lower input frequency.

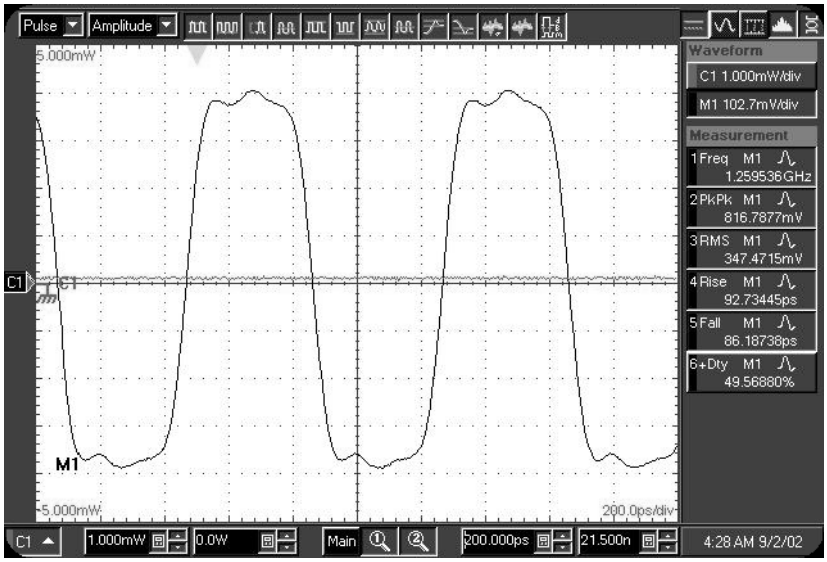


Figure 14 - Differential output with small input amplitude waveform VCC = 4.75 V, Vin = 10 dBm, Fin = 5 GHz

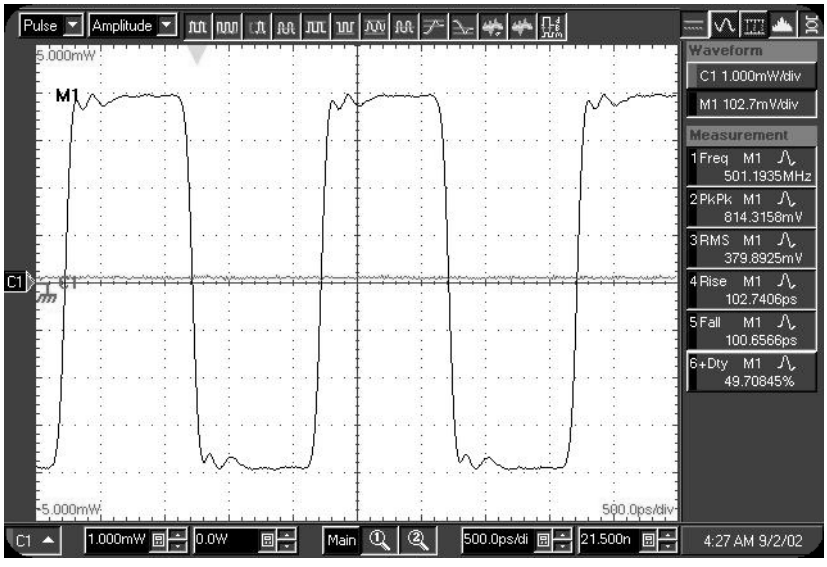
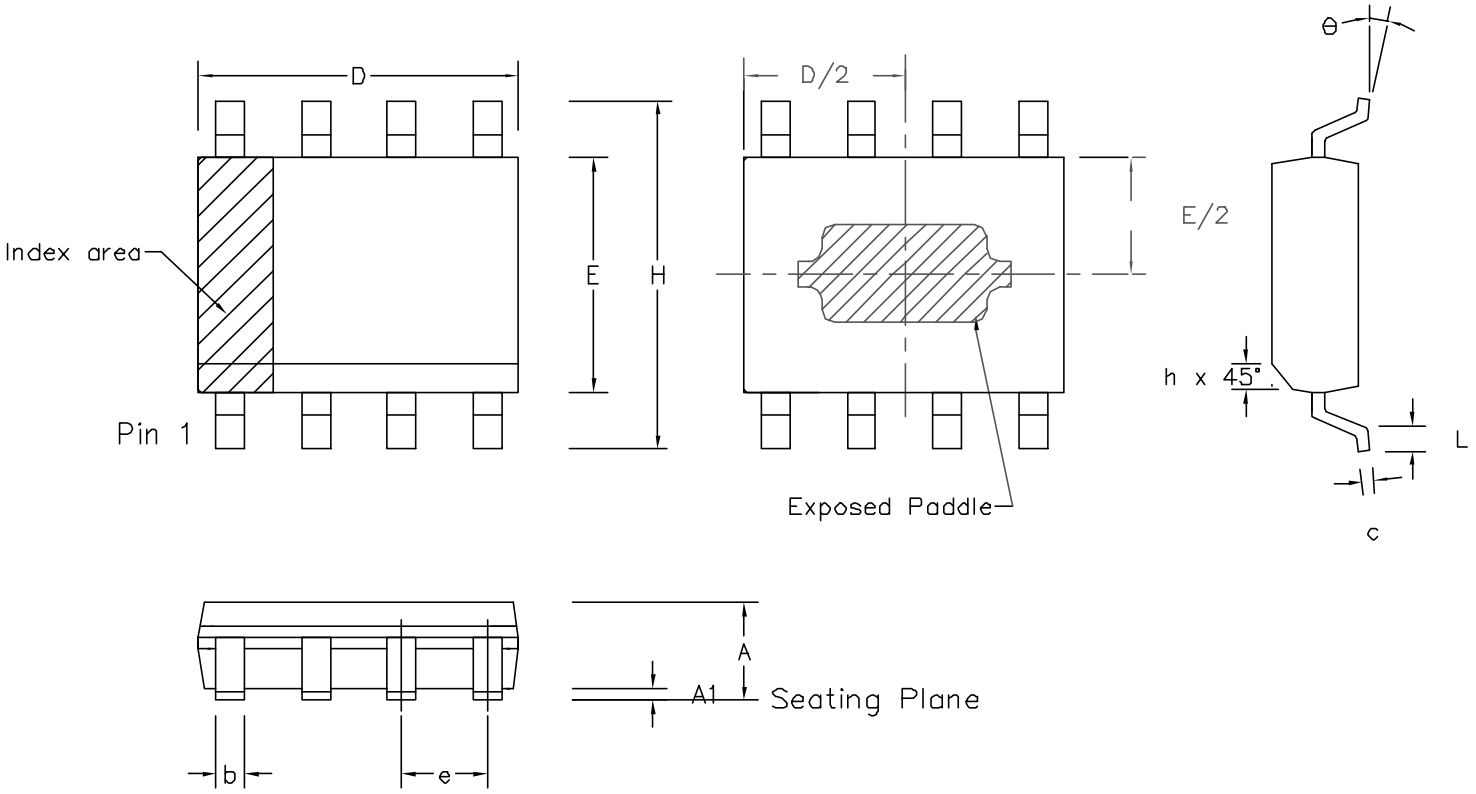


Figure 15 - Differential output with lower frequency input VCC = 4.75 V, Vin = 10 dBm, Fin = 2 GHz



	Min Inches	Max inches	Min mm	Max mm
A	0.056	0.066	1.43	1.68
A1	0.000	0.004	0.00	0.10
D	0.189	0.196	4.80	4.98
H	0.230	0.244	5.84	6.20
E	0.150	0.157	3.81	3.99
L	0.16	0.35	0.41	0.89
e	0.050 BSC		1.27 BSC	
b	0.0138	0.0192	0.35	0.49
c	0.0075	0.0098	0.19	0.25
Θ	0°	8°	0°	8°
h	0.010	0.016	0.25	0.41
	Pin Features		Pin Features	
N	8		8	

Notes:

1. Controlling dimensions are in inches.
2. Dimensions D & E do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
3. Exposed paddle not to scale on drawing
4. Extrusion of the exposed pad in bottom side is 0.20 mmTypical
5. Exposed Paddle dimension is 90x90mil Square max, and is governed by the leadframe paddle size.

ISSUE	1	2			
ACN	212933	214385			
DATE	14Jun02	13Jun03			
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MH / S

Package Code DC

Package Outline for 8 lead e-pad SOIC (0.150" Body width)

GPD00790

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE