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Features

- Single +3.3 V supply dissipating 70 mW per channel

- 4-channel VCSEL driver operates from DC to 6.25 Gb/s

- Individual channel control for enable, drive currents, and VCSEL fault control

- Adjustable temperature compensation for threshold and modulation drive currents

- Selectable analog multiplexer provides junction temperature, supply voltage and VCSEL bias current for each channel

- Programmable VCSEL fault detection with autonomous fault handling and interrupt

- Squelch automatically disables channel when input amplitude falls below programmable threshold

- Adjustable VCSEL peaking control

- 2-wire interface provides access to internal registers

- IC dimensions 2245 x 3870 um

- 250-micron channel pitch matches optical ribbon fiber and VCSEL arrays

- Differential CML compatible inputs with on-chip termination

Applications

- Single data rate (SDR) and double data rate (DDR) XAUI

- Single data rate (SDR) and double data rate (DDR) Infiniband®

- 1x, 2x, 4x Fiber Channel

- Gigabit Ethernet

- PCI Express 1.1 and 2.0

- QSFP and POP4 optical modules

- Proprietary and CWDM parallel optical modules

Description

The growing use of the Internet has created increasingly higher demand for multi-Gb/s I/O performance. The demand for 40 Gb/s bandwidth and beyond fuels the growth of short-reach 10 Gb/s infrastructures within high-end telco and datacom routers, switches, servers and other proprietary chassis-to-chassis links.

The Zarlink ZL63034 4x6.25Gb/s VCSEL Driver is a 4-channel VCSEL driver designed for various parallel optics and CWDM PMD applications. It consists of a DC-coupled amplifier with selectable threshold and modulation currents optimized for driving commercially available, common cathode VCSELs from a single +3.3 V supply.

Individual channel settings are used to control the threshold and modulation drive current and their temperature coefficients, allowing the optical output power and extinction ratio to be optimized. A selectable analog multiplexer provides junction temperature, supply voltage, and VCSEL bias current for each channel to enable optical module diagnostic features.

Data controlling the Zarlink ZL63034 VCSEL driver settings is loaded by a simple 2-wire serial serial interface reducing the number of pins required of a microcontroller.
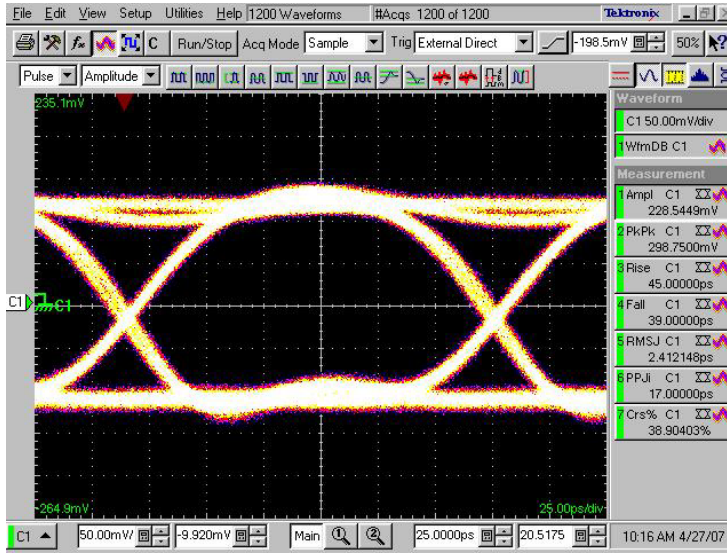
Figure 1: Representative Optical Data Pattern at 6.25 Gb/s with a Bessel-Thomson Filter
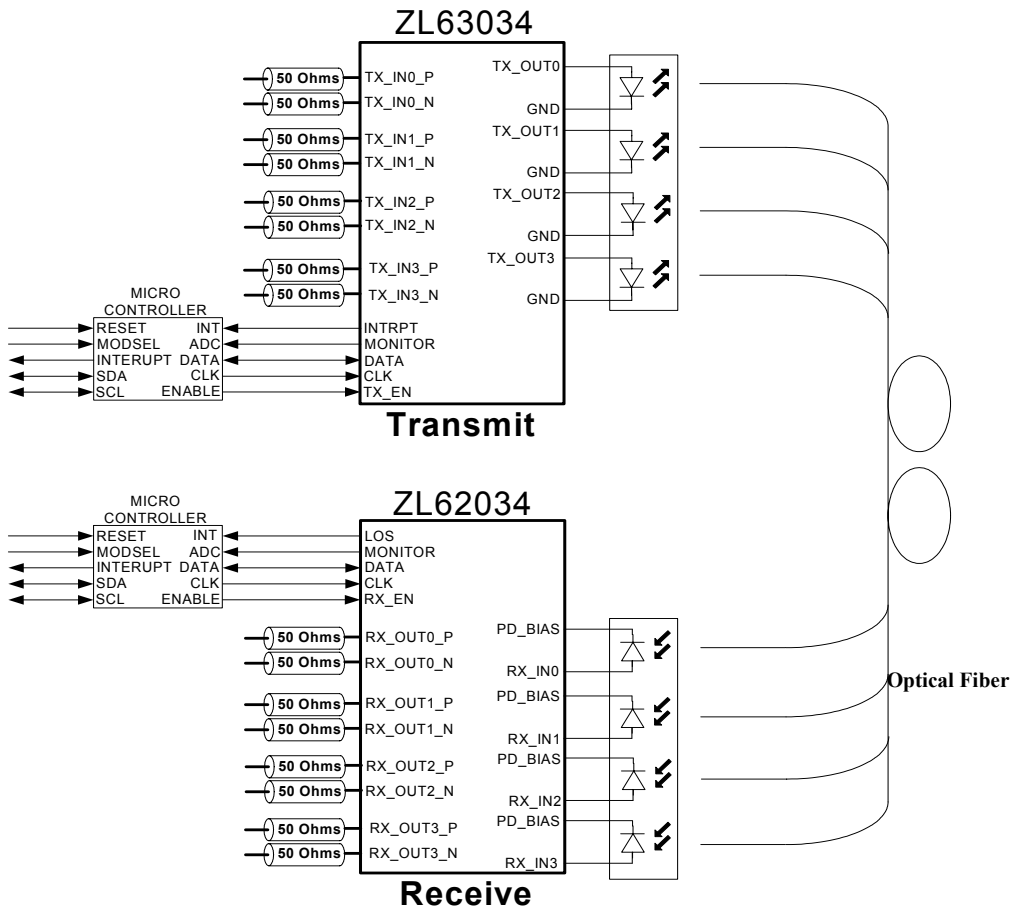

Figure 2: Application Block Diagram Utilizing the ZL63034 VCSEL Driver and the ZL62034 Optical Receiver

Functional Description

The Zarlink ZL63034 VCSEL driver is a 4-channel, monolithic SiGe BiCMOS integrated circuit that provides all the functionally needed to digitally modulate commercially available common cathode VCSEL arrays. Features include buffered, fully differential CML and LVDS compatible inputs that are DC-coupled to VCSEL drivers. Independent control of VCSEL drive currents and temperature coefficients enable the design of cost-effective, 4-channel optical data communication transmitters.

The differential inputs (TX_IN) are internally terminated and drive single-ended, ground-referenced, output current drivers as seen in Figure 3. Loading of on-chip CMOS control registers through a 2-wire interface sets the VCSEL current levels for digital modulation. An internal bandgap voltage reference enables precise, separately adjustable logic-high current (I_{max}) and logic-low current (I_{min}) levels for each channel, allowing each VCSEL output's optical power and extinction ratio to be optimized. Separately adjustable temperature coefficients for I_{max} and I_{min} allow each VCSEL output to be maintained through ambient temperature variations. A multiplexed analog output provides a proportional signal for VCSEL bias, junction temperature, and power supply voltage for analog diagnostics.
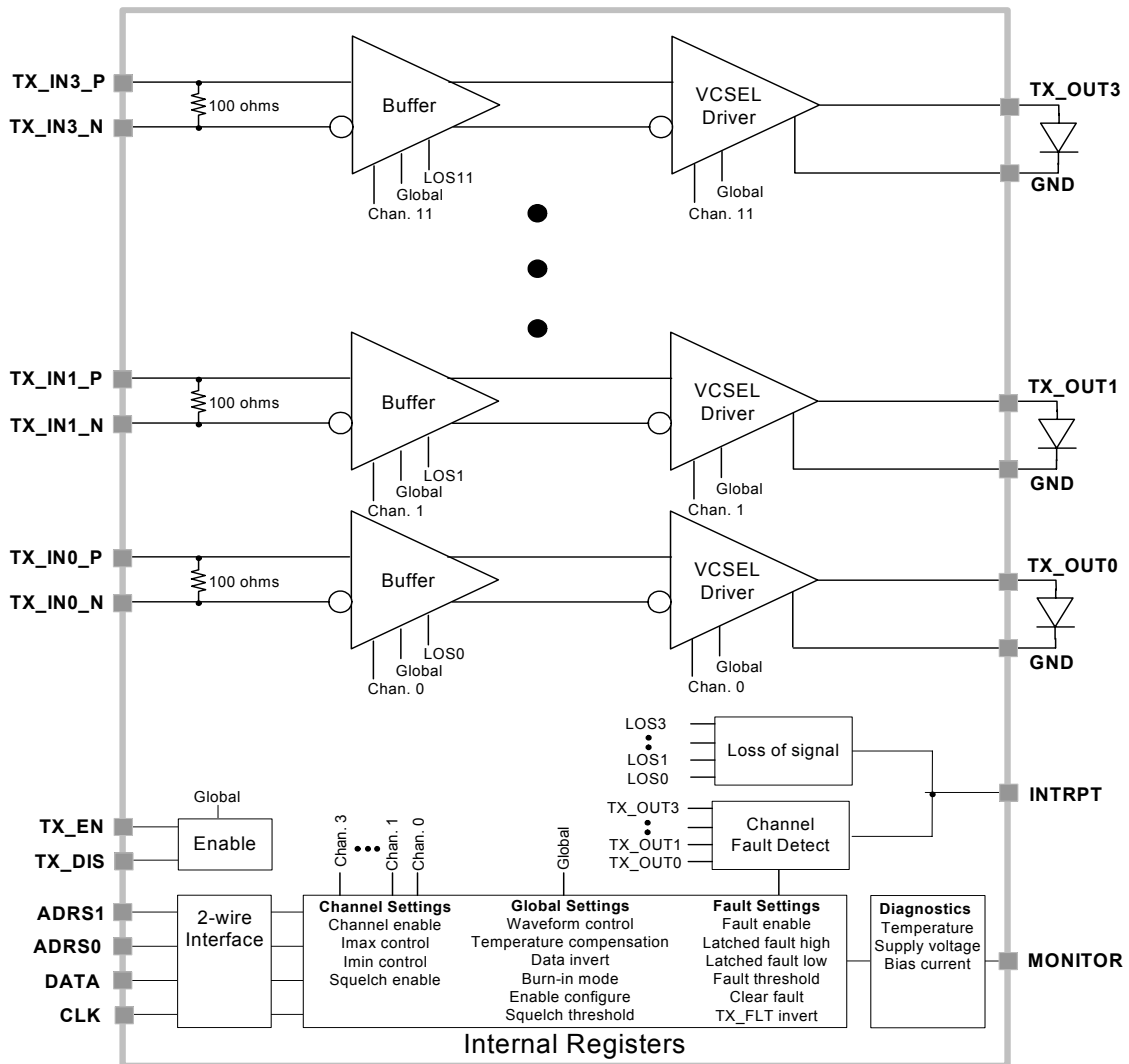

Figure 3: Block Diagram

VCSEL Current Waveform Control

The waveshaping feature of the ZL63034 provides variable peaking control to optimize the optical output. Three global control (IWF[2:0]) register bits provide waveshaping disable and 7 adjustable edge peaking settings. Note that this feature will affect the drive current modulation amplitude.

Interrupt Output

The interrupt output (INTRPT) indicates that a fault condition or a loss of signal condition has occurred on one or more channels. The interrupt is intended to alert the microcontroller. The internal registers of the IC may then be queried to determine the details of the error.

The polarity of the INTRPT output may be toggled by setting the INTRPT_INVERT global register bit. The output may be configured as either a CMOS output or an open-drain output using the INTRPT_CONFIG global register bit.

VCSEL Output Fault

The ZL63034 fault detection circuit senses over-current and under-current fault conditions. When the circuit detects a fault condition it disables the individual channel and asserts the interrupt output pad (INTRPT). The ZL63034 also asserts the corresponding FLT_HIGH or FLT_LOW channel register bit.

The fault interrupt is cleared when the clear interrupt instruction sequence is followed. This will reset the FLT_HIGH and FLT_LOW register bits and also de-assert the output interrupt.

The over-current threshold may be adjusted by setting the IFAULT[2:0] register bits. The fault high and fault low detection circuits may be independently enabled with FLT_EN_HIGH and FLT_EN_LOW global register bits. The INTRPT output has several different configurations. See the Interrupt Output section for details.

Bias and Modulation Currents

The output logic-high drive currents (I_{max}) and logic-low currents (I_{min}) are determined by the equations in Table 1. Both equations are a function of the channel register bits IMAX[5:0] and IMIN[5:0]. Equations use the decimal equivalent of the binary input words.

Current Equation	Units
I_{max} (IMAX) = IMAX * 0.33	mA
I_{min} (IMIN) = (IMIN * 0.1) + 0.3	mA

Table 1: Logic-high current and logic-low current equations when TC_MAX[1:0]=[00] and TC_MIN[1:0]=[00]
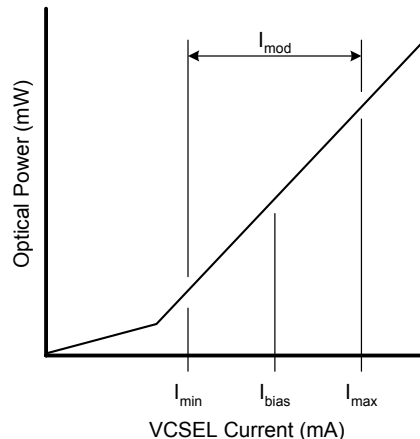

Figure 4: Optical output power vs. VCSEL current shows the relationship between bias, modulation, logic-low (I_{min}) and logic-high (I_{max}) drive currents

Temperature Compensation

The temperature compensation circuits for I_{max} and I_{min} each have four operating modes as shown in Table 2. The circuits independently compensate the drive currents depending on the IC temperature above 25 ºC and the TC_MAX[1:0] and TC_MIN[1:0] setting as seen in Figures 5 and 6.

TC_MAX[1:0], TC_MIN[1:0] Input	I_{max} Current Increase	I_{min} Current Increase	Unit
00	0	0	% / °C
01	0.18	0.2	% / °C
10	0.36	0.4	% / °C
11	0.54	0.6	% / °C

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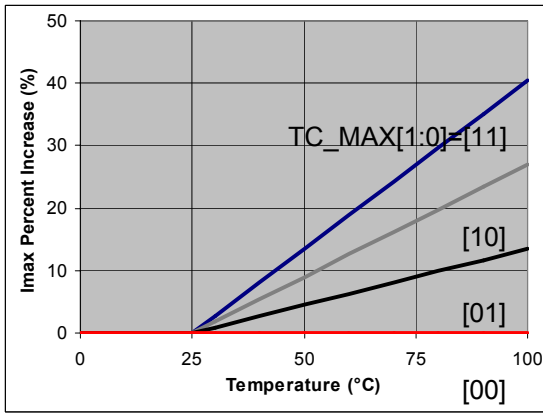**Table 2**: **Temperature Compensation Settings**

Figure 5: Drive current (I_{max}) temperature compensation vs temperature for each setting
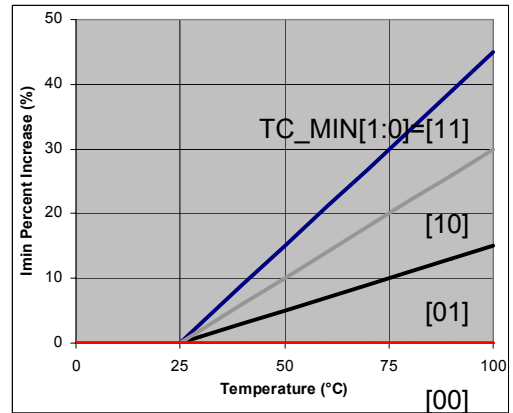

Figure 6: Drive current (I_{min}) temperature compensation vs temperature for each setting

Enable

The high-speed channels of the ZL63034 are controlled globally with the TX_EN and TX_DIS input. The ENMODE[1:0] register bits allow the user to connect or disconnect pull-up and pull-down resistors on the TX_EN and TX_DIS inputs. The four modes of ENMODE are shown in Table 3. Note that ENMODE[1:0]=00 is the default setting.

Individual channels may be enabled or disabled with the 2-wire interface through the CHANNEL register.

ENMODE[1:0]	TX_EN	TX_DIS
00 (POR)	Pull-down	Pull-up
01	Open	Pull-down
10	Open	Open
11	Pull-up	Pull-down

Table 3: TX_EN and TX_DIS Resistor Configurations using ENMODE[1:0]

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MONITOR Diagnostics

The MONITOR[7:0] register bits control the output of the analog multiplexer (MONITOR). The MONITOR output provides a voltage that is proportional to the selected diagnostic parameter. Parameters include VCSEL bias current, junction temperature, and power supply voltage as defined in Table 4. Equations for the proportional MONITOR voltage may be seen in Table 5.

MONITOR[7:0]	Description
0	Channel 0 VCSEL bias current
1	Channel 1 VCSEL bias current
2	Channel 2 VCSEL bias current
3	Channel 3 VCSEL bias current
4-23	Reserved
24	Junction temperature (POR state)
25	Power supply voltage monitor (Vcc/2)
26	Factory test 1
27	Factory test 2
28-30	Reserved
31	Open circuit state (high impedance)

Table 4: MONITOR Diagnostic Parameters

Description	Equation	Unit
VCSEL bias current	$Ibias = Vmonitor * 12.5$	mA
Junction temperature	$Tjunc = (Vmonitor - 1.456 \text{ V}) / (0.005 \text{ V/C})$	°C
Power supply voltage	$VCC = Vmonitor * 2$	V

Table 5: MONITOR Equations

IC Identification

The ZL63034 provides revision control with the addressable IDCODE register. The 8 bit register provides a unique value for each Zarlink product and IC revision.

Loss of Signal and Squelch

Each channel of the ZL63034 has a loss of signal indicator. When the differential input amplitude falls below a programmable threshold, the circuit asserts the INTRPT output pad and sets the corresponding channel register bit (CH_LOS). The circuit will also disable the channel if the (SQ_EN) CHANNEL register bit is set. The amplitude threshold may be adjusted with the SD_TH[2:0] GLOBAL register bits.

Data Invert

The DATA_INVERT global register bit inverts the data polarity of all high-speed channels.

Differential Inputs

Each of the high-speed differential inputs are terminated with a differential 100 impedance. The differential inputs are self biased for AC-coupled connections and may also be DC-coupled to appropriate signals.

A small offset voltage is provided on the differential inputs to ensure that a logic-low will be generated on the driver output for no connect or non-driven AC-coupled inputs. The DATA_INVERT register bit may be used to generate a logic-high on the driver output.

The TX_OUT_HIGH register bit will introduce a stronger offset voltage on the differential inputs to force a logic-high on the driver output for no connected or non-driven AC-coupled inputs. Desired burn in drive currents may be programmed with the IMAX register bits.

Digital Control

The Zarlink ZL63034 VCSEL driver provides a serial digital interface that allows internal registers to be programmed and monitored as seen in Figure 7. The simple 2-wire interface allows commonly available microcontrollers to access registers for device optimization and analog diagnostics.

The 2-wire interface is intended for use in a master-slave bus configuration. A microcontroller is the master and the Zarlink IC is the slave. The 2-wire bus consists of a unidirectional clock that is driven by the master and a bidirectional data port that may be driven by either the master or the slave. The data port (DATA) consists of a CMOS input and an open-drain output with an internal pull-up resistor and the clock input (CLK) is CMOS. The bus configuration supports multiple addressable slave devices.
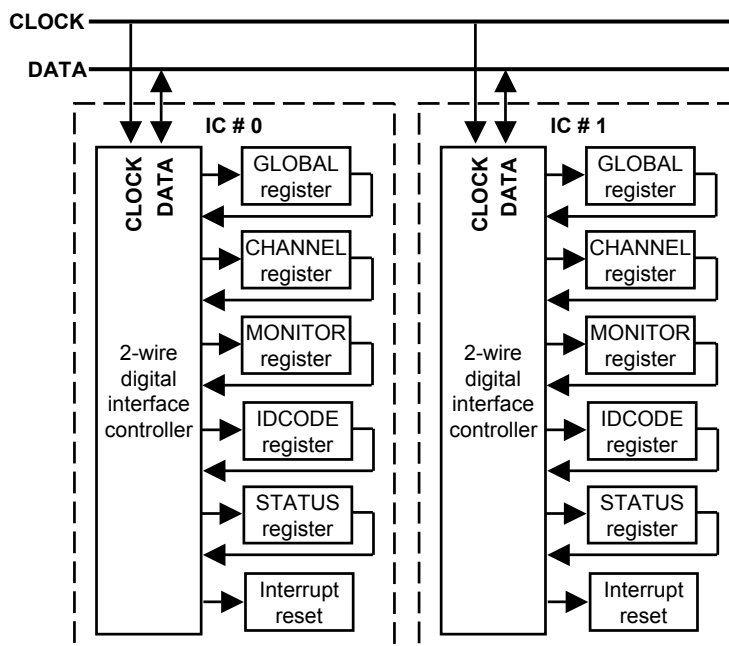

Figure 7: Block Diagram of 2-wire Bus

The ZL63034 has two address inputs (ADRS0 and ADRS1) that may be used to set the physical address of the IC (ADDRESS[3:0]). There are 8 unique addresses available for the ZL63034 and 8 unique addresses for the ZL62034 for up to 16 ICs on a single 2-wire bus. The ADRS0 and ADRS1 tri-level inputs maybe connected to VCC, ground, or no connected (NC). The physical IC addresses are shown in Table 6.

ADRS1	ADRS0	ADDRESS[3:0]
NC	NC	0000
NC	GND	0001
NC	VCC	0010
GND	NC	0011
GND	GND	0100
GND	VCC	0101
VCC	NC	0110
VCC	GND	0111
VCC	VCC	0000

Table 6: Physical IC Address Settings

The ZL63034 has five addressable registers as defined in Table 7. Each register can be accessed independently by its specific register address (REGISTER[2:0]). It is necessary for the master to initiate and terminate write or read operations with the exact register length.

Register	Type	Number of bits	Address REGISTER[2:0]
GLOBAL	Read/Write	24	000
MONITOR	Read/Write	8	001
CHANNEL	Read/Write	72	010
IDCODE	Read only	8	011
STATUS	Read only	16	100

Table 7: Register Definitions

Write Sequence

A register write transaction is initiated by the master with a start sequence followed by a physical IC address (ADRESS[3:0]), a register address (REGISTER[2:0]), write indicator (WR[0]=0) and register payload data. The write transaction is completed by the master with a stop sequence as show in Tables 8 and 9.

START	ADDRESS[3:0]	REGISTER[2:0]	WR[0]=0	Register data (8-72 bits)	STOP

Table 8: Register Write Sequence

Field	Description
START	Start condition, initialed by the master, and consists of a falling edge on DATA while CLOCK is high
ADDRESS[3:0]	Physical address of slave. Determined by ADRS1 and ADRS0 connections (VCC, NC, or GND)
REGSITER[2:0]	Address for internal registers (GLOBAL, MONITOR, CHANNEL, IDCODE, and STATUS)
WR[0]	Read/write indicator. WR[0]=0 for the write operation
Register data	Register data. Payload must equal to the length of the register (8-72 bits)
STOP	Stop condition, a rising edge on DATA with CLOCK high terminates the 2-wire transaction and resets the digital interface controller

Table 9: Description of Fields in Write Sequence

Figure 8 shows a timing diagram for a register write operation. The binary input is clocked into DATA on the rising edge of CLOCK. It is important to have glitch-free DATA signal while CLK is high to avoid faulty start or stop conditions. The stop condition also serves as the digital reset for the digital interface controller.
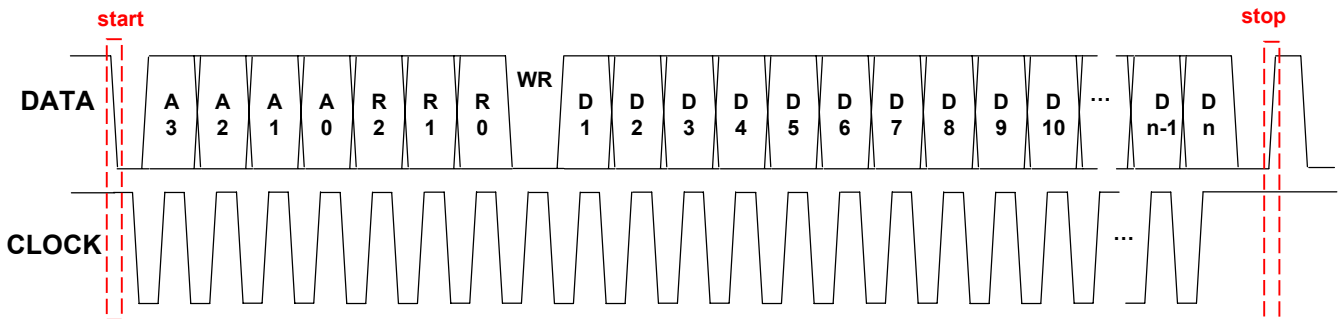

Figure 8: Register Write Timing Diagram

Read Sequence

A register read transaction is initiated by the master with a start sequence followed by a physical IC address (ADRESS[3:0]), a register address (REGISTER[2:0]), and a write indicator (WR[0]=1) as seen in Table 10. The data payload that follows is always in single byte units. After reading each byte, the master must send an ACK bit to continue reading the contents of a register or a NACK after the complete register has been read. A stop sequence following the NACK will terminate the transaction.

START	ADDRESS[3:0]	REGISTER[2:0]	WR[0]=1	Data (8 bits)	ACK	Data (8 bits)	ACK	…	NACK	STOP

Table 10: Register Read Sequence

A timing diagram for a read transaction is shown in Figure 9. The blue-highlighted (byte_1 and byte_n) sections in the DATA waveform indicate that the bidirectional DATA port of the IC is in output mode. The remainder of the time, both CLOCK and DATA of the IC are in input mode.

All registers are set to default values after the IC is powered on. These values are known as power on reset (POR) values and may be seen the the register definition Tables 13-17. The POR register values may be observed by reading a register after a power cycle. Registers may be read repeatably without disturbing the contents of the register.
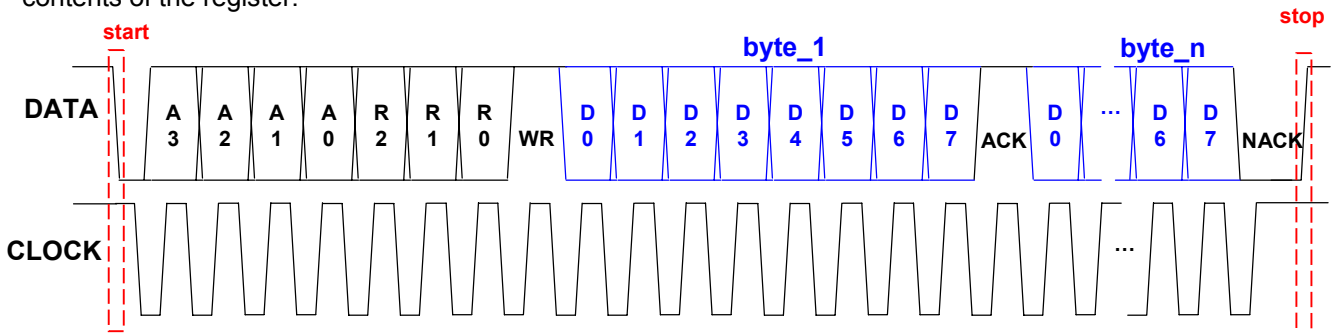

Figure 9: Register Read Timing Diagram

Clear Interrupt Sequence

In addition to register access, a special 2-wire sequence allows the user to clear the interrupt output (INTRPT). The clear interrupt instruction sequence is shown in Table 11 and the timing diagram is shown in Figure 10.

START	ADDRESS[3:0]	REGISTER[2:0]	WR[0]=0	STOP

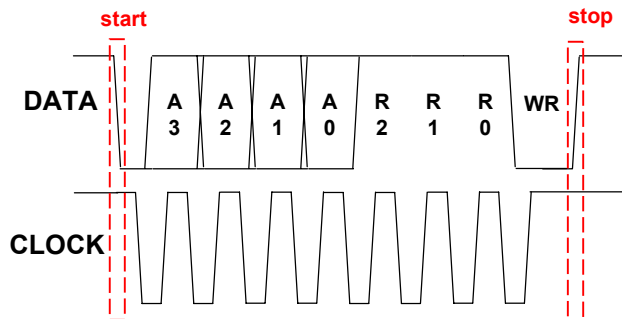**Table 11: Clear Interrupt Sequence**

Figure 10: Clear Interrupt Timing Diagram

Critical Timing

The register read, register write, and clear interrupt 2-wire transactions share the same timing requirements. Figures 11 and 12 show critical timing relationships and Table 12 provides worst case timing.
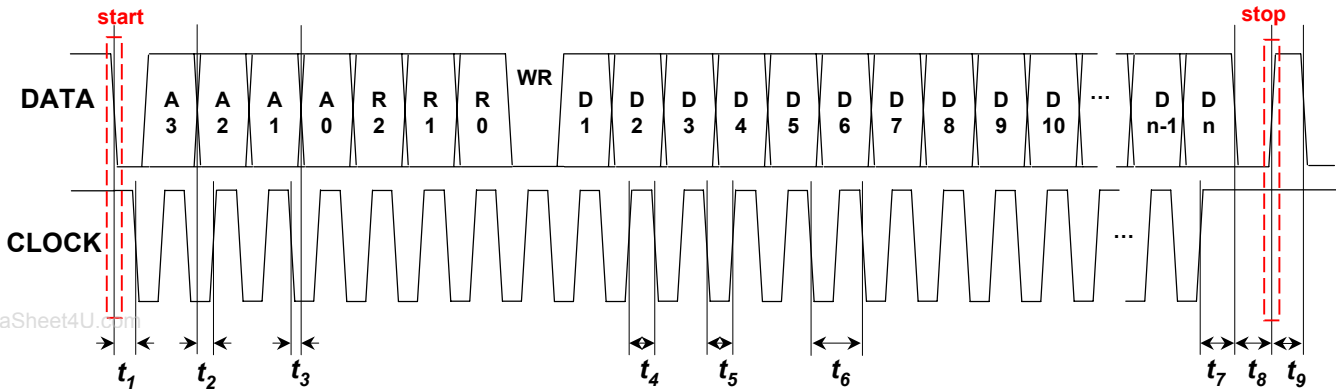

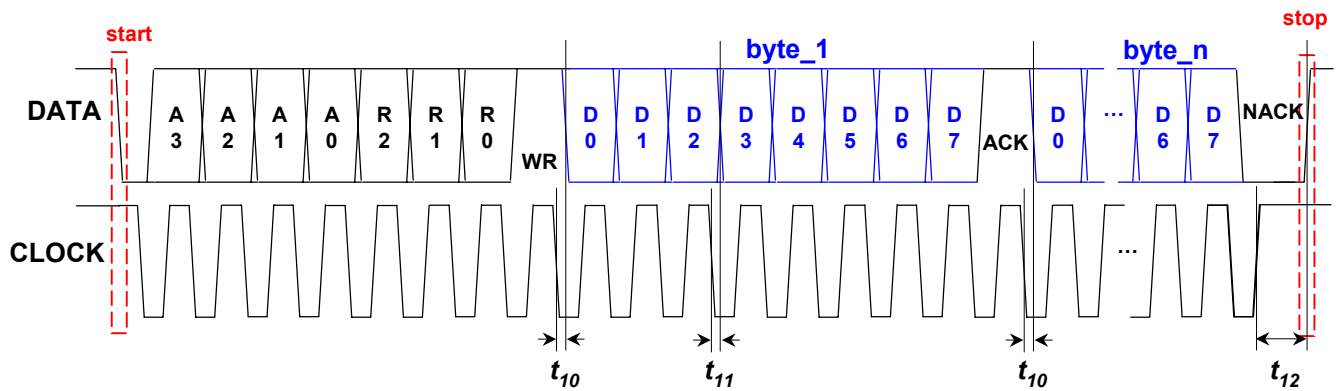**Figure 11: Register Write Sequence with Timing Relationships**

Figure 12: Register Read Sequence with Timing Relationships

Symbol	Description	Worst Case Timing (ns)
t_1	Start condition to first clock transition	0.2
t_2	Write data to clock set time	1.2
t_3	Write data to clock hold time	0.5
t_4	Clock high	17.0
t_5	Clock low	7.0
t_6	Clock period	34.0
t_7	Last clock to last write data transition	6.0
t_8	Data=low before stop condition	0.1
t_9	Between control sequences	22.0
t_{10}	Read data available to clock edge	2.6
t_{11}	Read data delay from clock	2.1
t_{12}	Last clock to stop in read sequence	0.5

Table 12: Worst Case Timing for 2-wire Transactions

Bit	Name	Power on reset	Description, see Note 1
0	TC_IMAX[1]	1	Imax temperature compensation – MSB
1	TC_IMAX[0]	0	Imax temperature compensation
2	TC_IMIN[1]	1	Imin temperature compensation – MSB
3	TC_IMIN[0]	0	Imin temperature compensation
4	IWF[2]	0	Waveform control for VCSEL driver output – MSB
5	IWF[1]	0	Waveform control for VCSEL driver output
6	IWF[0]	0	Waveform control for VCSEL driver output
7	FLT_EN_HIGH	0	Enable over-current fault detection for all channels
8	FLT_EN_LOW	0	Enable under-current fault detection for all channels
9	IFAULT[2]	1	Over-current fault detection threshold – MSB
10	IFAULT[1]	1	Over-current fault detection threshold
11	IFAULT[0]	1	Over-current fault detection threshold
12	INTRPT_INVERT	0	Invert INTRPT output polarity
13	INTRPT_CONFIG	1	Selects I/O style for INTRPT pad; 1 = CMOS, 0 = open-drain
14	DATA_INVERT	0	Invert data polarity on all differential inputs
15	TX_OUT_HIGH	0	Mode for burn-in forces outputs to a logic high with open circuit inputs
16	EF_LO	1	Reserved for future use, see Note 2
17	LOAD_BAL	1	Reserved for future use, see Note 2
18	EN_MODE[1]	0	TX_EN and TX_DIS pull-up/down configure – MSB
19	EN_MODE[0]	0	TX_EN and TX_DIS pull-up/down configure
20	SD_TH[2]	0	Input signal detect threshold – MSB
21	SD_TH[1]	1	Input signal detect threshold
22	SD_TH[0]	1	Input signal detect threshold
23	Reserved	0	Reserved for future use, see Note 2
Note 1: All register bits are asserted by a logic level "1" unless otherwise specified			
Note 2: Reserved bits should always be programmed with POR values during write operations			

Table 13: GLOBAL Register Definition. Register type = Read/Write, address REGISTER[2:0] = 000

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Bit	Name	Chan	Power on reset	Description, see Note 1
0	IMAX[5]	0	1	VCSEL logic-high current setting – MSB
1	IMAX[4]	0	0	VCSEL logic-high current setting
2	IMAX[3]	0	0	VCSEL logic-high current setting
3	IMAX[2]	0	0	VCSEL logic-high current setting
4	IMAX[1]	0	0	VCSEL logic-high current setting
5	IMAX[0]	0	1	VCSEL logic-high current setting
6	IMIN[5]	0	0	VCSEL logic-low current setting – MSB
7	IMIN[4]	0	1	VCSEL logic-low current setting
8	IMIN[3]	0	0	VCSEL logic-low current setting
9	IMIN[2]	0	0	VCSEL logic-low current setting
10	IMIN[1]	0	0	VCSEL logic-low current setting
11	IMIN[0]	0	1	VCSEL logic-low current setting
12	CH_EN	0	1	Channel enable
13	SQ_EN	0	0	Channel input squelch enable
14	Reserved	0	0	Reserved for future use, see Note 2
15	Reserved	0	0	Reserved for future use, see Note 2
16	Reserved	0	1	Reserved for future use, see Note 2
17	Reserved	0	1	Reserved for future use, see Note 2
18-35	See bits 0 -17	1	-	See bits 0 -17
36-53	See bits 0 -17	2	-	See bits 0 -17
54-71	See bits 0 -17	3	-	See bits 0 -17
Note 1: All register bits are asserted by a logic level "1" unless otherwise specified				
Note 2: Reserved bits should always be programmed with POR values during write operations				

Table 14: CHANNEL Register Definition. Register type = Read/Write, address REGISTER[2:0] = 010

Bit	Name	Power on reset	Description
0	Reserved	0	Reserved for future use, see Note 1
1	Reserved	0	Reserved for future use, see Note 1
2	Reserved	0	Reserved for future use, see Note 1
3	MONITOR[4]	1	Monitor output control – MSB
4	MONITOR[3]	1	Monitor output control
5	MONITOR[2]	0	Monitor output control
6	MONITOR[1]	0	Monitor output control
7	MONITOR[0]	0	Monitor output control
Note 1: Reserved bits should always be programmed with POR values during write operations			

Table 15: MONITOR Register Definition. Register type = Read/Write, address REGISTER[2:0] = 001

Bit	Name	Chan	Power on reset	Description, see Note 1
0	FLT_HIGH	0	0	VCSEL over-current fault
1	FLT_LOW	0	0	VCSEL under-current fault
2	CH_LOS	0	0	Channel loss of input signal
3	Reserved	0	0	Reserved for future use
4-7	See bits 0-3	1	-	See bits 0-3
8-11	See bits 0-3	2	-	See bits 0-3
12-15	See bits 0-3	3	-	See bits 0-3
Note 1: All register bits are asserted as logic level "1" unless otherwise specified				

Table 16: STATUS Register Definition. Register type = Read Only, address REGISTER[2:0] = 100

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Bit	Name	POR	Description
0	IDCODE[7]	0	IC identification code – MSB
1	IDCODE[6]	0	IC identification code
2	IDCODE[5]	0	IC identification code
3	IDCODE[4]	0	IC identification code
4	IDCODE[3]	0	IC identification code
5	IDCODE[2]	1	IC identification code
6	IDCODE[1]	1	IC identification code
7	IDCODE[0]	1	IC identification code

Table 17: IDCODE Register Definition. Register type = Read Only, address REGISTER[2:0] = 011

Absolute Maximum Ratings

The IC should be used within the limits specified in Table 18. Exceeding the specified limits may impair the useful life of the component and the device may no longer perform to the specifications within this data sheet. Functionality at or above the values listed is not implied.

Symbol	Description	Min.	Typical	Max	Units	Remarks
VCC	IC supply voltage	-0.5		+3.63	V	
V_{DIFF_PP}	TX_IN Input amplitude			2.6	V	See Note 1
V_{In}	TX_IN DC input voltage	-0.5		VCC + 0.5	V	
V_{ESD}	ESD tolerance, human body model	2			kV	ESD on all pads
T_{JUNC}	Junction temperature			125	°C	
T_{STG}	Storage temperature	-65			°C	

Table 18: Absolute Maximum Rating

Note 1: $V_{DIFF\_PP} = 2 * V_{SE\_PP}$

Recommended Operating Conditions

Symbol	Description	Min.	Typical	Max.	Units	Remarks
VCC	Positive supply voltage	+2.97	+3.3	+3.63	V	
ICC	Positive supply current		5		mA	All channels disabled
			97		mA	All channels enabled, see Note 1
PD	Power dissipation		17		mW	All channels disabled
			280		mW	All channels enabled, see Notes 1 and 2

Table 19: Recommended Operating Conditions

Note 1: TC_MAX[1:0]=[00], TC_MIN[1:0]=[00], all other registers set to POR values
Note 2: Excludes power dissipated in VCSEL array

DC Characteristics

(VCC=3.3 V +/- 10%, T_{JUNC}=0-100 °C)

Symbol	Description	Min.	Typical	Max.	Units	Remarks
V_{DIFF_PP}	Differential input voltage	200		2000	mVpp	
V_{SING_PP}	Single-ended input voltage	100		1000	mVpp	
V_{CM}	Common mode input voltage	850		VCC	mV	
			2.6		V	AC-coupled input
R_{TERM}	Differential termination resistance		100		ohms	

Table 20: High-Speed Inputs

Symbol	Description	Min.	Typical	Max	Units	Remarks
I_{max}	Logic-high drive current range		17		mA	IMAX[5:0]=11111, See Note 1
			0		mA	IMAX[5:0]=00000, See Note 1
I_{min}	Logic-low drive current range		6		mA	IMIN[5:0]=11111, See Note 2
			0		mA	IMIN[5:0]=00000, See Note 2
V_{OUT}	Output voltage	1		VCC-0.5	V	

Table 21: High-Speed Outputs

Note 1: TX_OUT = logic high, IWF[3:0]=[000], $I_{max} > I_{min}$
Note 2: TX_OUT = logic low, IWF[3:0]=[000], $I_{max} > I_{min}$

Symbol	Description	Min.	Typical	Max	Units	Remarks
V_{IH}	High-level input voltage	2		VCC+0.3	V	VOUT>=VOU (min) or
V_{IL}	Low-level input voltage	-0.3		0.8	V	VOUT <= VOL (max)
V_{OH}	High-level output voltage	VCC-0.2			V	IOH=-100 uA
V_{OL}	Low-level output voltage			0.2	V	IOH=100uA

Table 22: Low-Speed Inputs and Outputs

AC Characteristics

(VCC=3.3 V +/- 10%, T_{JUNC}=0-100 °C)

Symbol	Description	Min.	Typical	Max	Units	Remarks
T_{RISE}	Electrical rise time		50		Ps	See Notes 1 and 2
T_{FALL}	Electrical fall time		50		Ps	See Notes 1 and 2
T_{SKEW}	Channel to channel skew		20		Ps	
DJ	Deterministic jitter			0.08	UI_{PP}	
RJ	Random jitter			0.02	UI_{PP}	
DRATE	Data rate	6.25			Gb/s	

Table 23: High-Speed Output Timing

Note 1: Rise and fall times measured 20% to 80%
Note 2: Output AC-coupled (using bias-t) 50 ohms to ground with default POR register values

Pad Name	Number	I/O	Style	Description
NC	1	N/A	N/A	No connect
GND	2	-	Ground	Ground
TX_IN3_N	3	Input	Digital	Data channel 3, differential input, negative
TX_IN3_P	4	Input	Digital	Data channel 3, differential input, positive
TX_IN2_N	5	Input	Digital	Data channel 2, differential input, negative
TX_IN2_P	6	Input	Digital	Data channel 2, differential input, positive
TX_IN1_N	7	Input	Digital	Data channel 1, differential input, negative
TX_IN1_P	8	Input	Digital	Data channel 1, differential input, positive
TX_IN0_N	9	Input	Digital	Data channel 0, differential input, negative
TX_IN0_P	10	Input	Digital	Data channel 0, differential input, positive
GND	11	-	Ground	Ground
MONITOR	12	Output	Analog	Programmable output provides proportional analog signal
GND	13	-	Ground	Ground
GND	14	-	Ground	Ground
GND	15	-	Ground	Ground
GND	16	-	Ground	Ground
INTRPT	17	Output	Digital	Indicates either a output fault condition or a loss of signal condition
TX_EN	18	Input	Digital	Enables all high-speed channels. See Note 1
CLK	19	Input	Digital	Clock input for 2-wire interface. See Note 2
ADRS0	20	Input	Tri-level	Sets the physical IC address for 2-wire interface. Connect to VCC, NC, or GND.
DATA	21	Input/Output	Digital	Bi-directional data port for the 2-wire interface. See Note 2
TX_DIS	22	Input	Digital	Disables all high-speed channels. See Note 1
VCC	23	-	Supply	+3.3V power supply
VCC	24	-	Supply	+3.3V power supply
VCC	25	-	Supply	+3.3V power supply
VCC	26	-	Supply	+3.3V power supply
VCC	27	-	Supply	+3.3V power supply
MONITOR	28	Output	Analog	Programmable output provides proportional analog signal
GND	29	-	Ground	Ground
GND	30	-	Ground	Ground, VCSEL cathode connection
TX_OUT0	31	Output	Analog	VCSEL anode connection
GND	32	-	Ground	Ground, VCSEL cathode connection
TX_OUT1	33	Output	Analog	VCSEL anode connection
GND	34	-	Ground	Ground, VCSEL cathode connection
TX_OUT2	35	Output	Analog	VCSEL anode connection
GND	36	-	Ground	Ground, VCSEL cathode connection
TX_OUT3	37	Output	Analog	VCSEL anode connection
GND	38	-	Ground	Ground, VCSEL cathode connection
GND	39	-	Ground	Ground, VCSEL cathode connection
VCC	40	-	Supply	+3.3V power supply
VCC	41	-	Supply	+3.3V power supply
VCC	42	-	Supply	+3.3V power supply
VCC	43	-	Supply	+3.3V power supply
VCC	44	-	Supply	+3.3V power supply

Table 24: Pad Description

Pad Name	Number	I/O	Style	Description
TX_DIS	45	Input	Digital	Disables all high-speed channels. See Note 1
DATA	46	Input/Output	Digital	Bi-directional data port for the 2-wire interface. See Note 2
ADRS1	47	Input	Tri-level	Sets the physical IC address for 2-wire interface. Connect to VCC, NC, or GND.
CLK	48	Input	Digital	Clock input for 2-wire interface. See Note 2
TX_EN	49	Input	Digital	Enables all high-speed channels. See Note 1
INTRPT	50	Output	Digital	Indicates either a output fault condition or a loss of signal condition
GND	51	-	Ground	Ground
GND	52	-	Ground	Ground
GND	53	-	Ground	Ground
GND	54	-	Ground	Ground

Table 24: Pad Description - cont.

Note 1: Selectable 40 k ohm pull-up or pull-down resistor
Note 2: Internal 40 k ohm pull-up to VCC
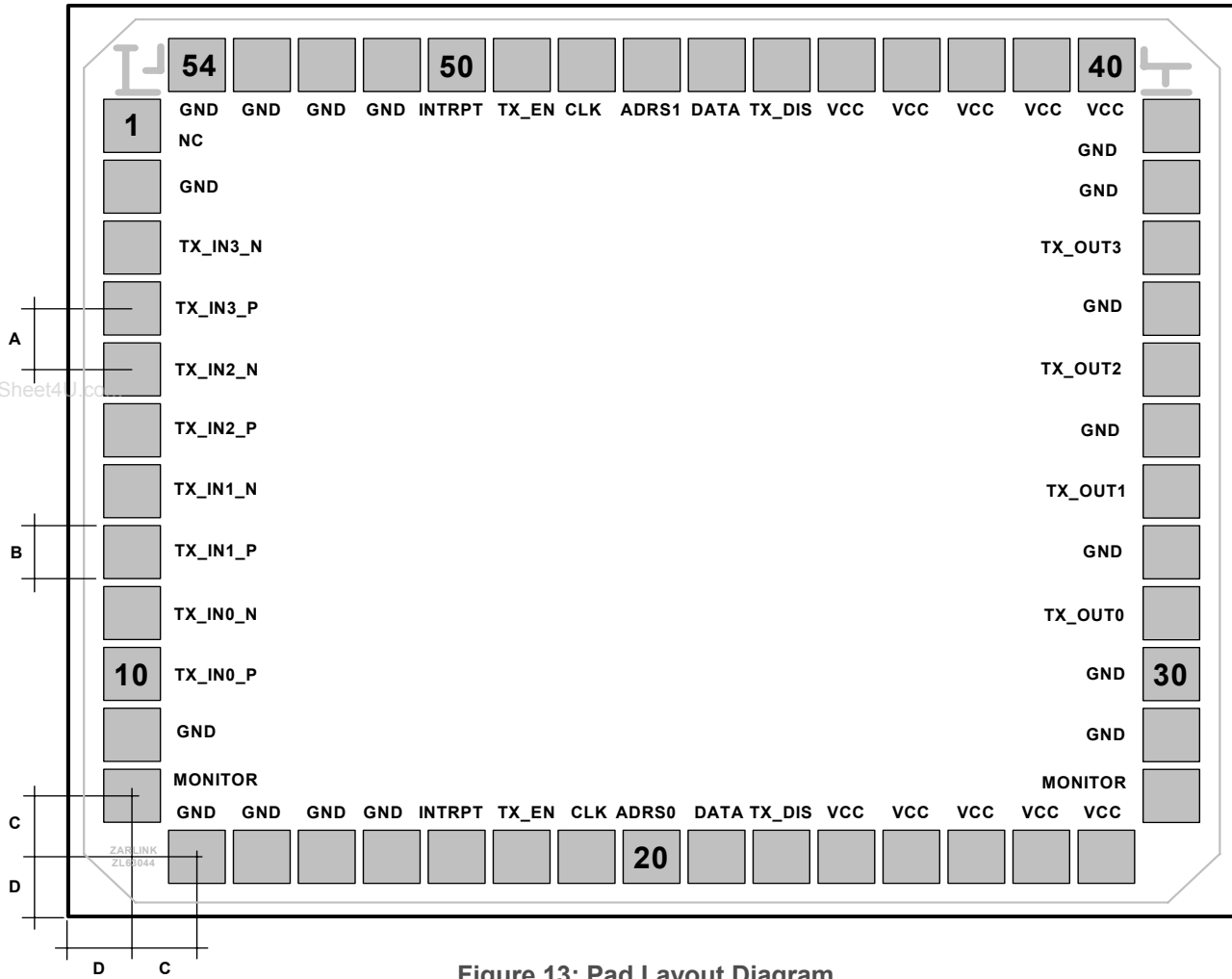
Figure 13: Pad Layout Diagram

Symbol	Description	Length	Unit
A	Pad to pad pitch	125	um
B	Bond pad length/width	114	um
C	Corner pad to corner pad pitch	125	um
D	Pad center to edge of die	122.5	um
X	Overall IC dimensions	2245 +/-25	um
Y	Overall IC dimensions	1870 +/-25	um
Z	Standard die thickness	17	mils

Table 25: Critical Dimensions

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visit our Web Site at**

www.zarlink.com

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