ZN427E8 / ZN427J8

MICROPROCESSOR COMPATIBLE 8-BIT SUCCESSIVE APPROXIMATION A-D CONVERTER

The ZN427 is an 8-bit successive approximation converter with three-state outputs to permit easy interfacing to a common data bus. The IC contains a voltage switching DAC, a fast comparator, successive approximation logic and a 2.56V precision bandgap reference, the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted, thus allowing ratiometic operation

Only passive external components are required for operation of the converter.

FEATURES

- Easy Interfacing to Microprocessor, or Operates as a 'Stand-Alone' Converter
- Fast: 10 microseconds Conversion time Guaranteed
- No Missing Codes over Operating Temperature Range
- Data Outputs Three-State TTL Compatible, other Logic Inputs and Output TTL and CMOS Compatible
- Choice of On-Chip or External Reference Voltage
- Ratiometric Operation
- Unipolar or Bipolar Input Ranges
- Complementary to ZN428 DAC
- Commercial or Military Temperature Range

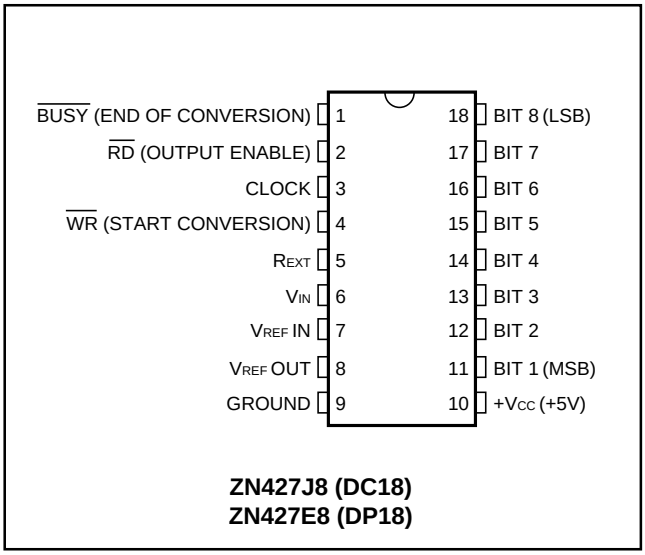

Fig.1 Pin connection - top view

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN427E8	0°C to +70°C	DP18
ZN427J8	-55°C to +125°C	DC18

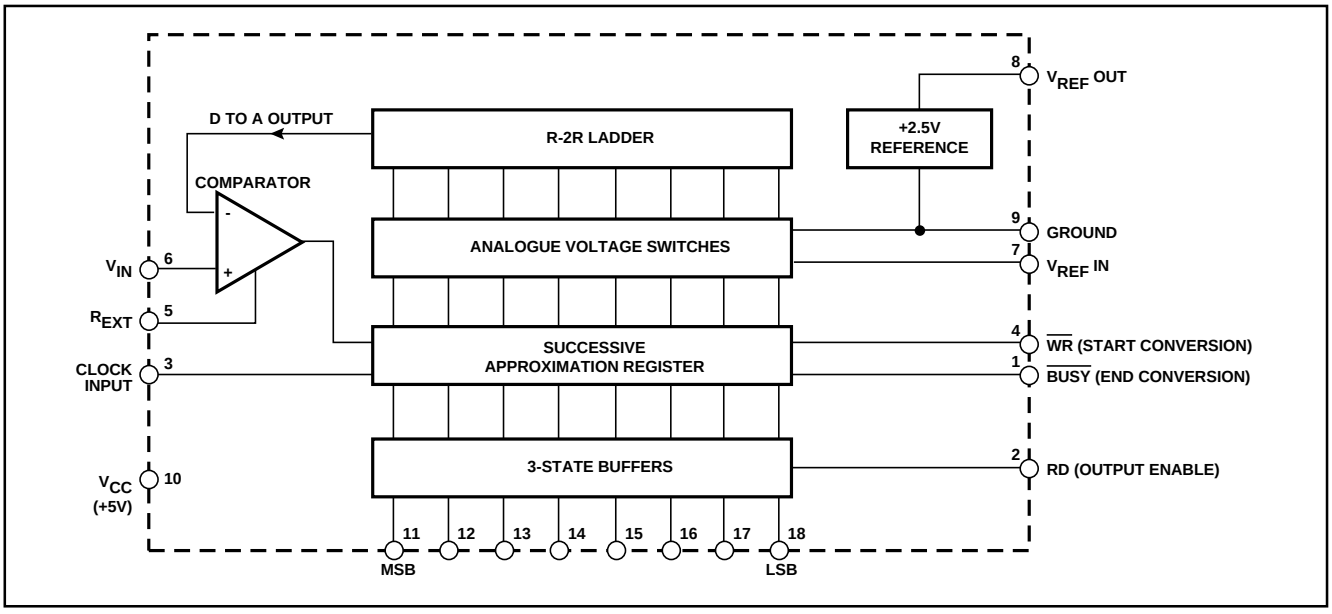

Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max. voltage, logic and V_{REF} input	+V_{CC}
Operating temperature range	0°C to +70°C (ZN427E8)
	-55°C to +125°C (ZN427J8)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C unless otherwise specified).

Parameter		Min.	Typ.	Max.	Units	Conditions
Converter						
Resolution		8	-	-	Bits	
Linearity error		-	-	±0.5	LSB	
Differential non-linearity		-	±0.5	-	LSB	
Linearity error T.C.		-	±3	-	ppm/°C	
Differential non-linearity T.C.		-	±6	-	ppm/°C	
Full-scale (gain) T.C.		-	±2.5	-	ppm/°C	External Ref. 2.5V
Zero T.C.		-	±8	-	µV/°C	
Zero transition	00000000	12	15	18	mV	DC Package
	to 00000001	10	13	16	mV	DP Package
F.S. transition	11111110	2.545	2.550	2.555	V	$V_{REF\ IN}$ = 2.560V
	to 11111111					
Conversion time		-	-	10	µs	See note 1
External reference voltage		1.5	-	3.0	V	
Supply voltage (V_{CC})		4.5	-	5.5	V	
Supply current		-	25	40	mA	
Power consumption		-	125	-	mW	
Comparator						
Input current		-	1	-	µA	V_{IN} = +3V, R_{EXT} = 82kΩ
Input resistance		-	100	-	kΩ	V - = -5V
Tail current, I_{EXT}		25	-	15	µA	
Negative supply, V–		-3.0	-	-30.0	V	See comparator (page x-xx)
Input voltage		-0.5	-	3.5	V	
Internal voltagee reference						
Output voltage		2.475	2.560	2.625	V	R_{REF} = 390Ω, C_{REF} = 4µ7
Slope resistance		-	0.5	2	Ω	
V_{REF} temperature coefficient		-	50	-	ppm/°C	
Reference current		4	-	15	mA	See reference (page x-xx)
Logic (over operating temperature range)						
High level input voltage V_{IH}		2.0	-	-	V	
Low level input voltage V_{IL}		-	-	0.8	V	
High level input current,		-	-	50	µA	V_{IN} = 5.5V, V_{CC} = max.
WR and RD inputs I_{IH}		-	-	15	µA	V_{IN} = 2.4V, V_{CC} = max.
High level input current,		-	-	100	µA	V_{IN} = 5.5V, V_{CC} = max.
Clock input I_{IH}		-	-	30	µA	V_{IN} = 2.4V, V_{CC} = max.
Low level input current I_{IL}		-	-	-5	µA	V_{IN} = 0.4V, V_{CC} = max.
High level output current I_{OH}		-	-	-100	µA	
Low level output current I_{OL}		-	-	1.6	mA	
High level output voltage V_{OH}		2.4	-	-	V	I_{OH} = max., V_{CC} = min.
Low level output voltage V_{OL}		-	-	0.4	V	I_{OL} = max., V_{CC} = min.
Disable output leakage		-	-	2	µA	V_O = 2.4V
Input clamp diode voltage		-	-	-1.5	V	
Read input to data output		-	-	250	ns	See Fig.9
Enable/disable delay time t_{RD}		-	180	250	ns	
Start pulse width tWR		250	160	-	ns	See Fig.9
WR to BUSY propagation delay t_{BD}		-	-	250	ns	
Clock pulse width		500	-	-	ns	
Maximum clock frequency		900	1000	-	kHz	See note 1

Note 1: A 900kHz clock gives a conversion time of 10µs (9 clock periods).

GENERAL CIRCUIT OPERATION

The ZN427 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the WR input the BUSY output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the

MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$.

Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the ninth negative clock edge BUSY goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held high to keep the three-state buffers in their high impedance state. Data can be read out by taking RD high, thus enabling the three-state output. Readout is non-destructive. The BUSY output may be tied to the RD input to automatically enable the outputs when the data is valid.

For reliable operation of the converter the start pulse applied to the WR input must meet certain timing criteria with respect to the converter clock. These are detailed in the timing diagram of Fig.3.

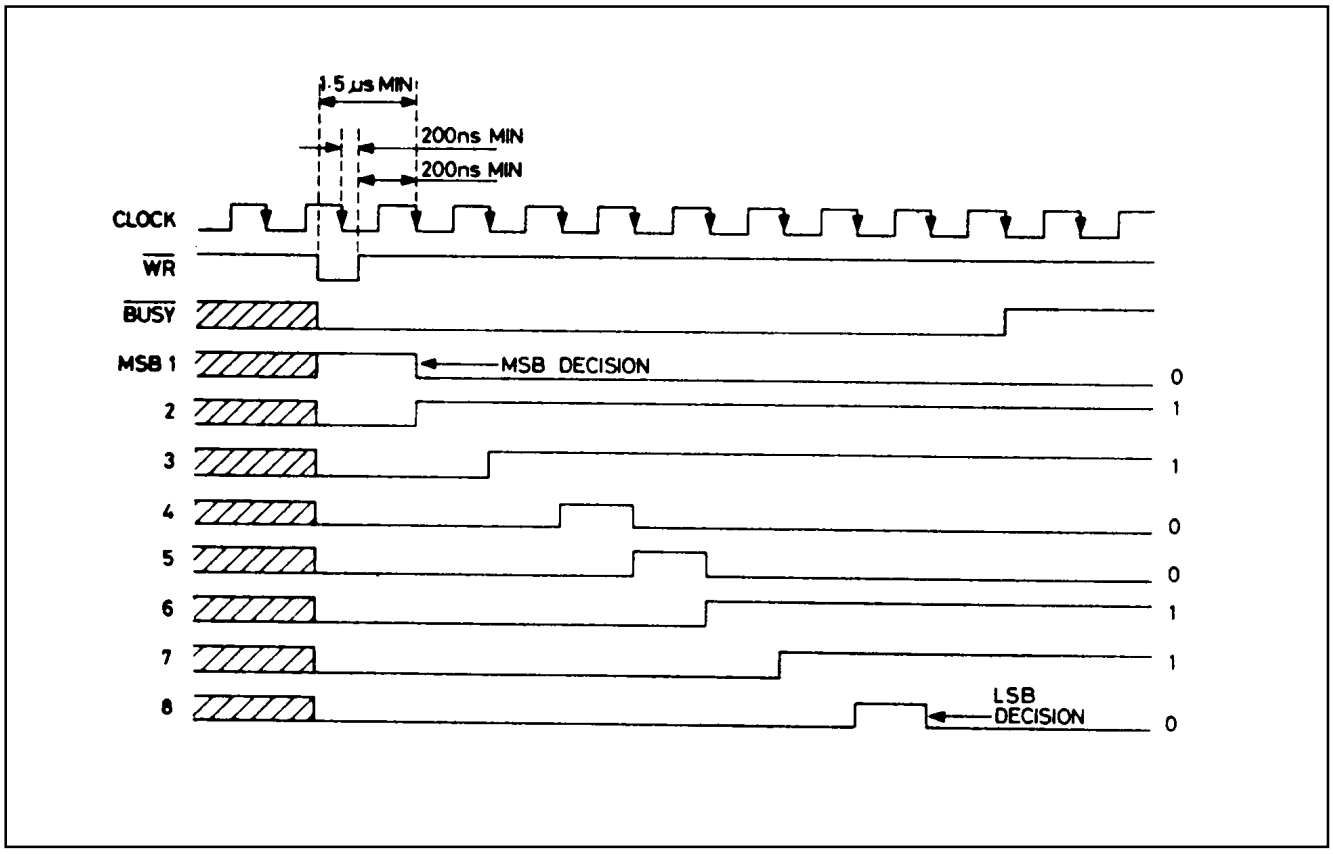

Fig.3 Timing diagram

NOTES ON TIMING DIAGRAM

1. A conversion sequence is shown for the digital word 01100110. For clarity the three-state outputs are shown as being enabled during the conversion, but normal practice would be to disable them until the conversion was complete.

2. The BUSY output goes low during a conversion. When BUSY goes high at the end of a conversion the output data is valid. In a microprocessor system the BUSY output can be used to generate an interrupt request when the conversion is complete.

3. In the timing diagram cross hatching indicates a 'don't care' condition.

4. The start pulse operates as an asynchronous (independent of clock) reset that sets the MSB output to 1 and sets all other outputs and the end of conversion flag to 0. This resetting occurs on the low-going edge of the start pulse and as long as WR is low the converter is inhibited. Conversion commences on the first active (negative going) clock edge after the WR input has gone high again, when the MSB decision is made. A number of timing constraints thus supply to the start pulse.

(a) The minimum duration of the start pulse is 250ns, to allow reliable resetting of the converter logic circuits.

(b) There is no limit to the maximum duration of the start pulse.

(c) To allow the MSB to settle at least 1.5µs must elapse between the negative going edge of the start pulse and the first active clock edge that indicates the MSB desicion.

(d) To ensure relaible clocking the positive-going edge of the start pulse should not occur within 200ns of an active (negative-going) clock edge. The ideal place for the positive-going edge of the start pulse is coincident with a positive-going clock edge. As a special case of the above conditions that start pulse may be synchronous with a negative-going clock pulse.

PRACTICAL CLOCK AND SYNCHRONISING CIRCUITS

The actual method of generating the clock signal and synchronising it to the start conversion system in which the ZN427 is incorporated.

When used with a microprocessor the ZN427 can be treated as RAM and can be assigned a memory address using an address decoder. If the µP clock is used to drive the ZN427 and the µP write pulse meets the ZN427 timing criteria with respect to the µP clock then generating the start pulse is simply a matter of gating the decoded address with the microprocessor write pulse. Whilst the conversion is being performed the microprocesor can perform other instructions or No operation (NOP). when the conversion is complete the outputs can be enabled onto the bus by gating the decoded address with the read pulse. A timing diagram for this sequence of operation is given in Fig.4.

An advantage of using the microprocessor clock is that the conversion time is known precisely in terms of machine cycles. the data outputs may therefore be read after a fixed delay of at least nine clock cycles after the end of the WR pulse, when the conversion will be complete.

Alternatively the read operation may be initiated by using the BUSY output to generate interrupt request.

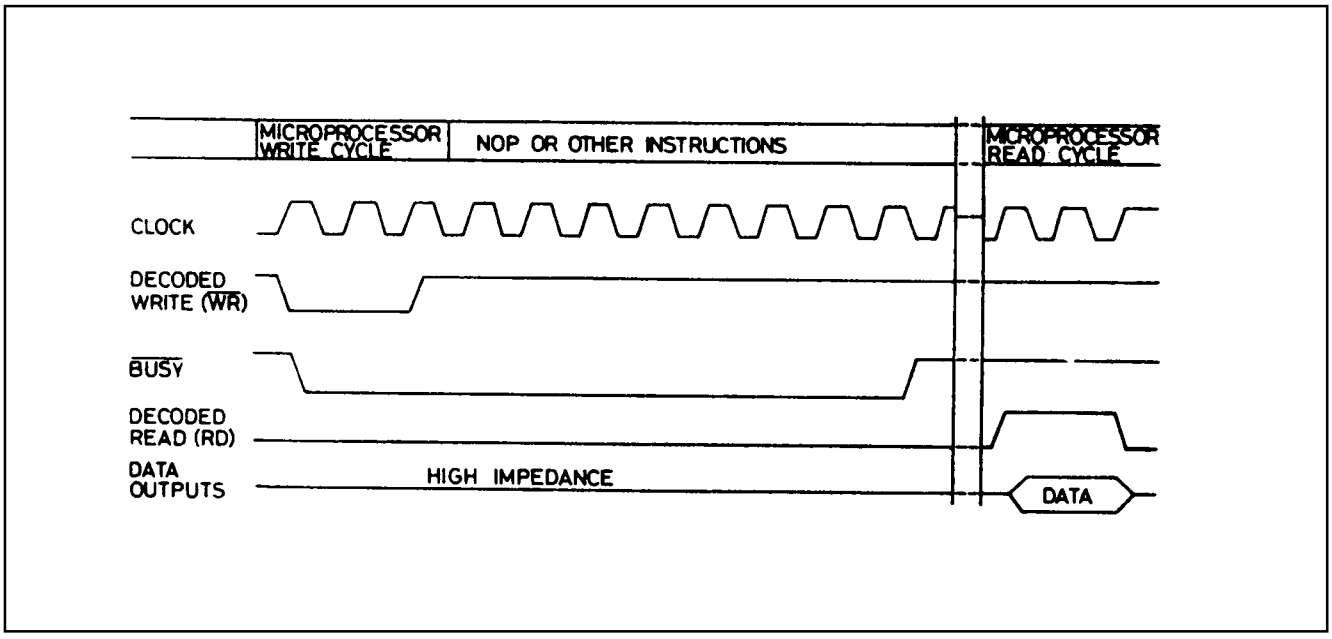

Fig.4 Typical timing diagram using µP clock and write pulse

In some systems, for example single-chip microcomputers such as the 8048, this simple method may not be feasible for one or more of the following reasons:

(a) The MPU clock is not available externally.

(b) The clock frequency is too high.

(c) The write pulse timing criteria make it unsuitable for direct use as a start conversion pulse.

If any of these conditions apply then the self-synchronising clock circuit of Fig.5a is recommended.

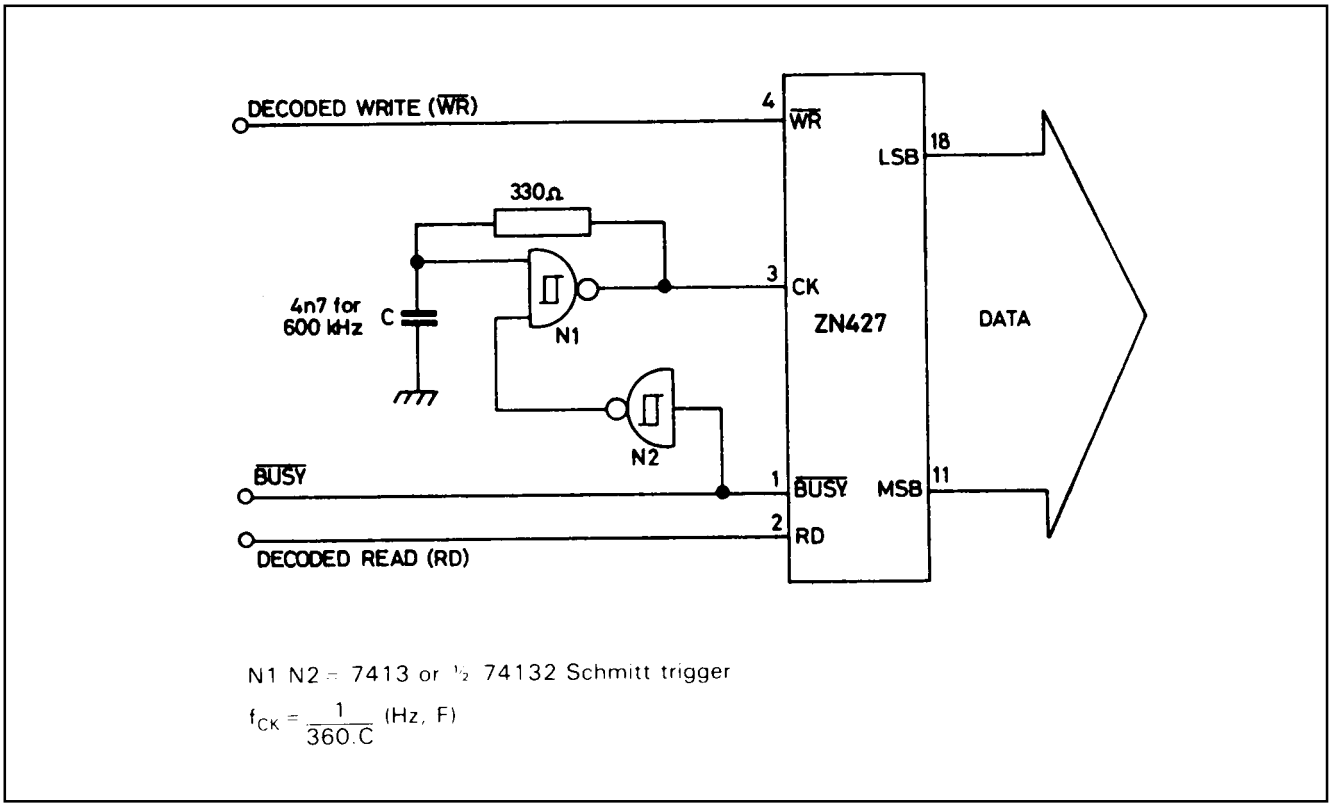

Fig.5a Self-synchronising clock circuit

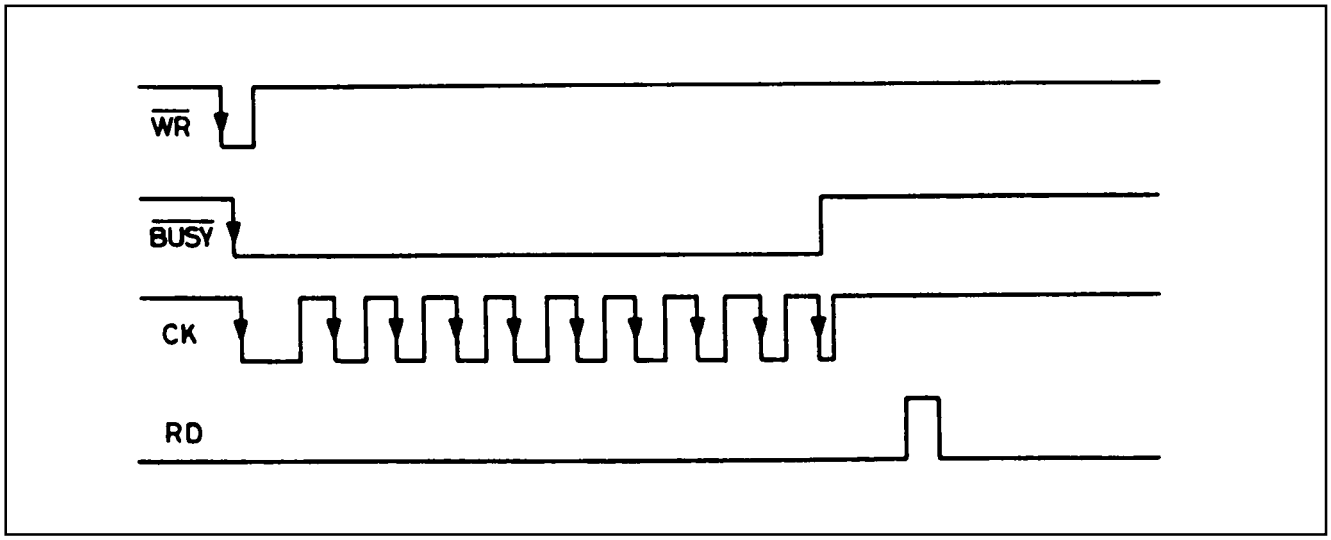

Fig.5b Timing diagram for circuit of Fig.5a

N1 is connected as an astable multivibrator which, when the BUSY output is high, is inhibited by the output of N2 holding one of its inputs low. The start conversion pulse resets the BUSY flag and N1 begins to oscillate. When the conversion is complete BUSY goes high and the clock is inhibited.

Since the start pulse starts the clock it may occur at any time. The only constraints on the start pulse are that it must be longer than 250ns but at least 200ns shorter than the first clock pulse. The first clock pulse is in fact longer than the rest since C1 starts from a fully charged condition whereas on subsequent cycles it changes between the upper and lower threshold (V_{T+} and V_{T-}) of the Schmitt trigger.

LOGIC INPUTS AND OUTPUTS

The logic inputs of the ZN427 utilise the emitter-follower configuration shown in Fig.6. This gives extremely low input currents for CMOS as well as TTL compatibility.

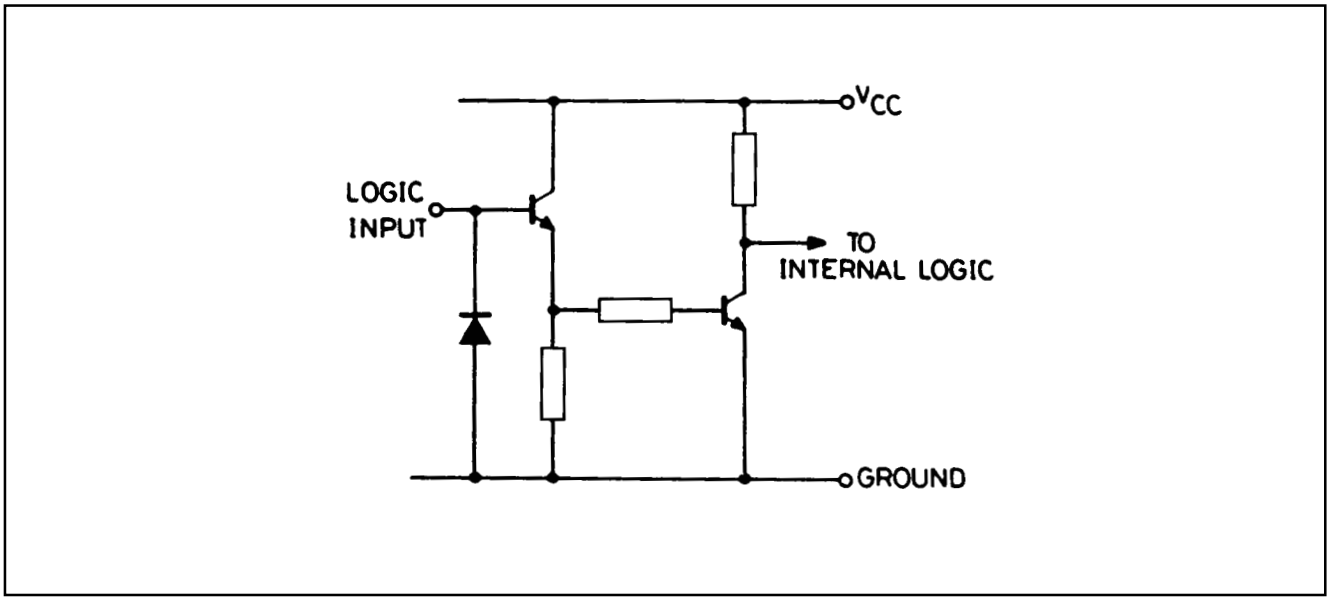

Fig.6 Equivalent circuit of all inputs

The BUSY output, shown in Fig.7, utilises a passive pullup for CMOS/TTL compatibility.

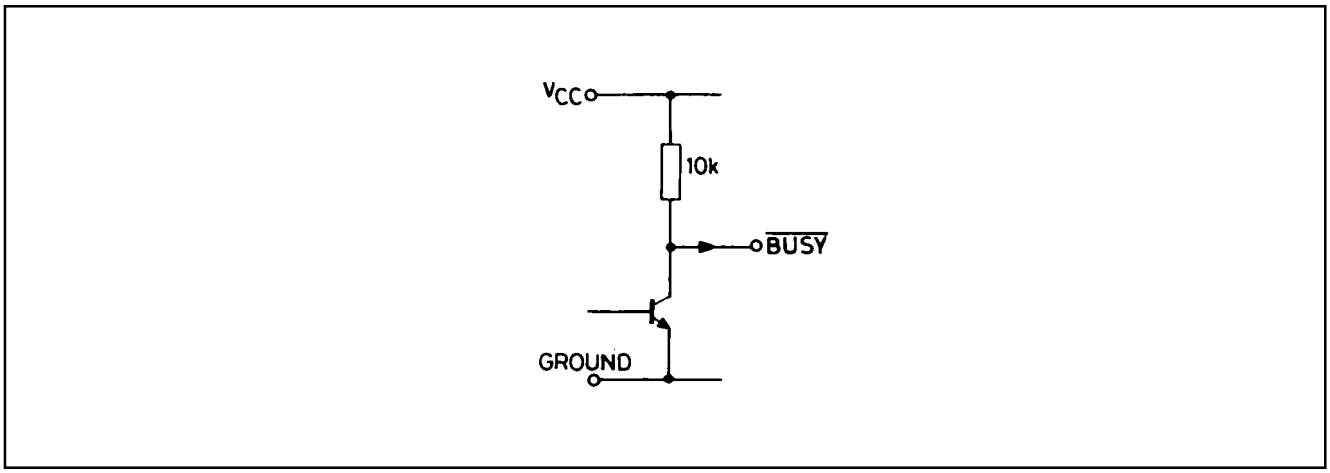

Fig.7

The data outputs have three-state buffers, an equivalent circuit of which is shown in Fig.8. Whilst the RD input is low both output transistors are turned off and the output is in a high impedance state. When RD is high the data output will assume the appropriate logic state (0 or 1).

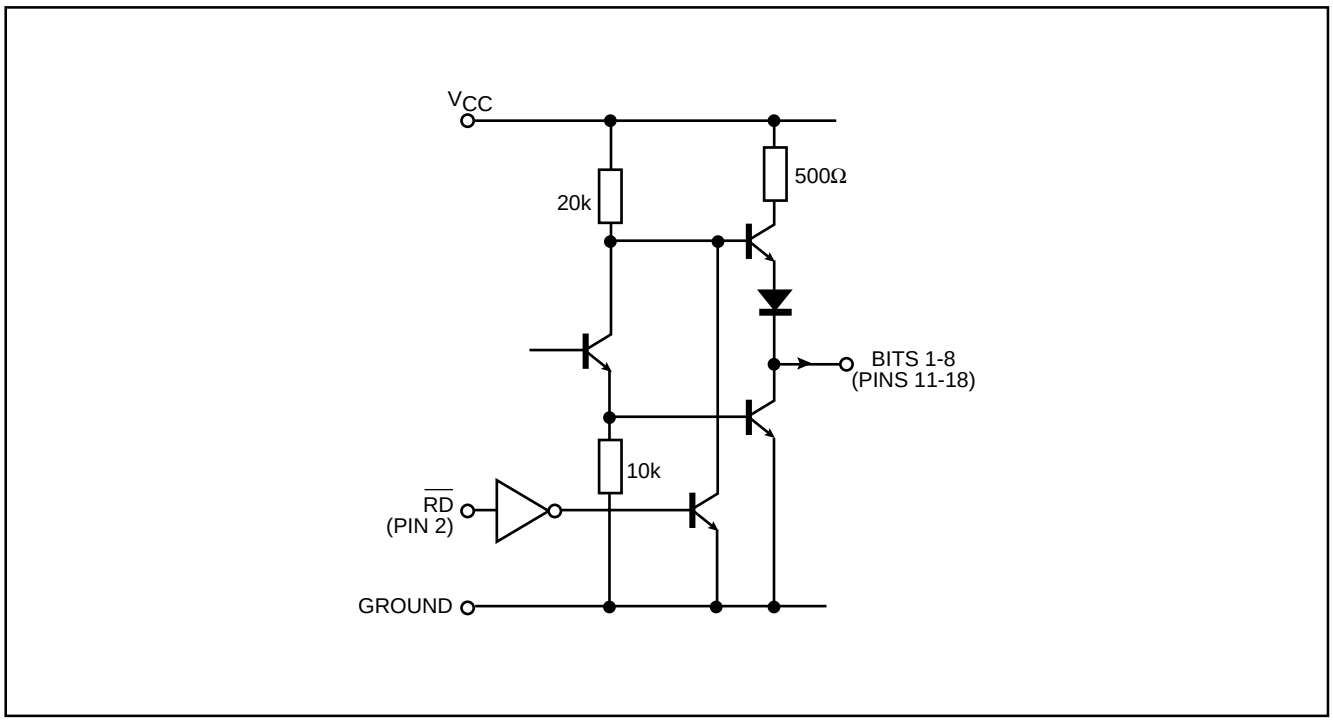

Fig.8 Equivalent circuit of data outputs

A test circuit and timing diagram for the output enable/disable delays are given in Fig.9.

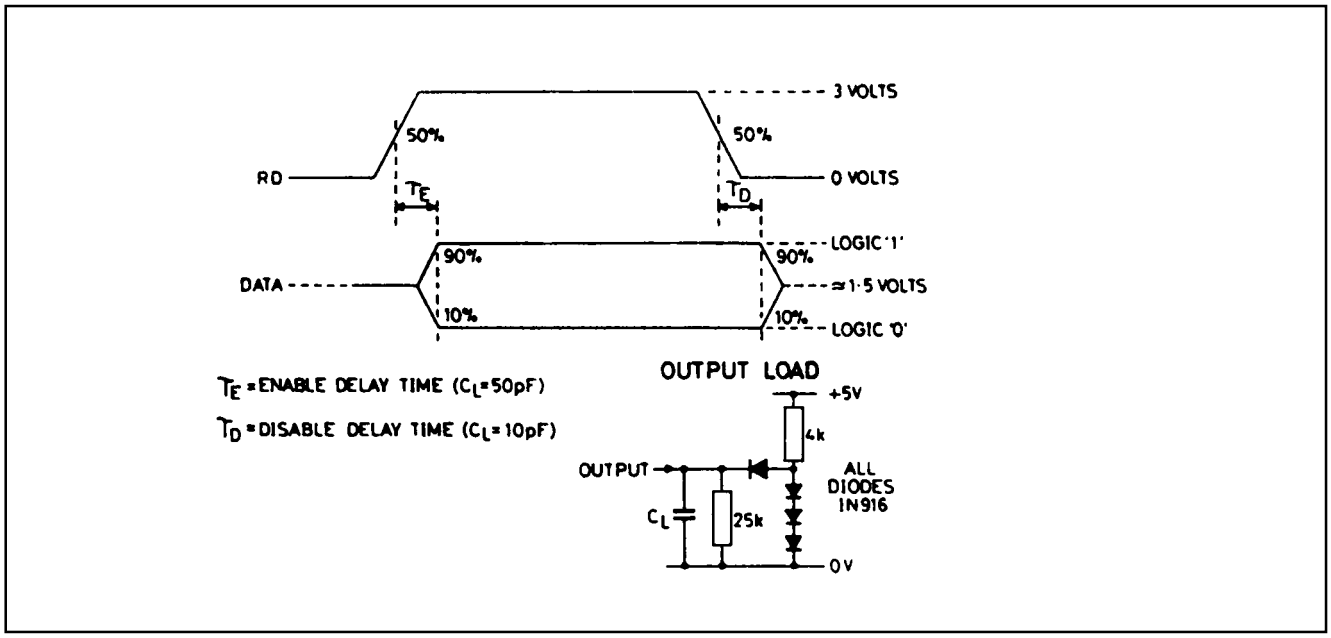

Fig.9 Output enable/disable waveforms

ANALOG CIRCUITS

D-A converter

IThe converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.10. Each element is connected to either 0V or V_{REF} IN by transistor voltage switches specially designed for low offset voltage (<1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

D to A output = $\frac{n}{256}$ (V_{REF} IN -V_{OS}) + V_{OS}

where n is the digital input to the D-A from successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 2mV for the ZN427E8 and 4mV for the ZN427J8.

This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8µV/°C), the effect on accuaracy will be negligible.

The D-A output range can be considered to be 0 - $V_{REF\ IN}$ through an output resistance R (4k).

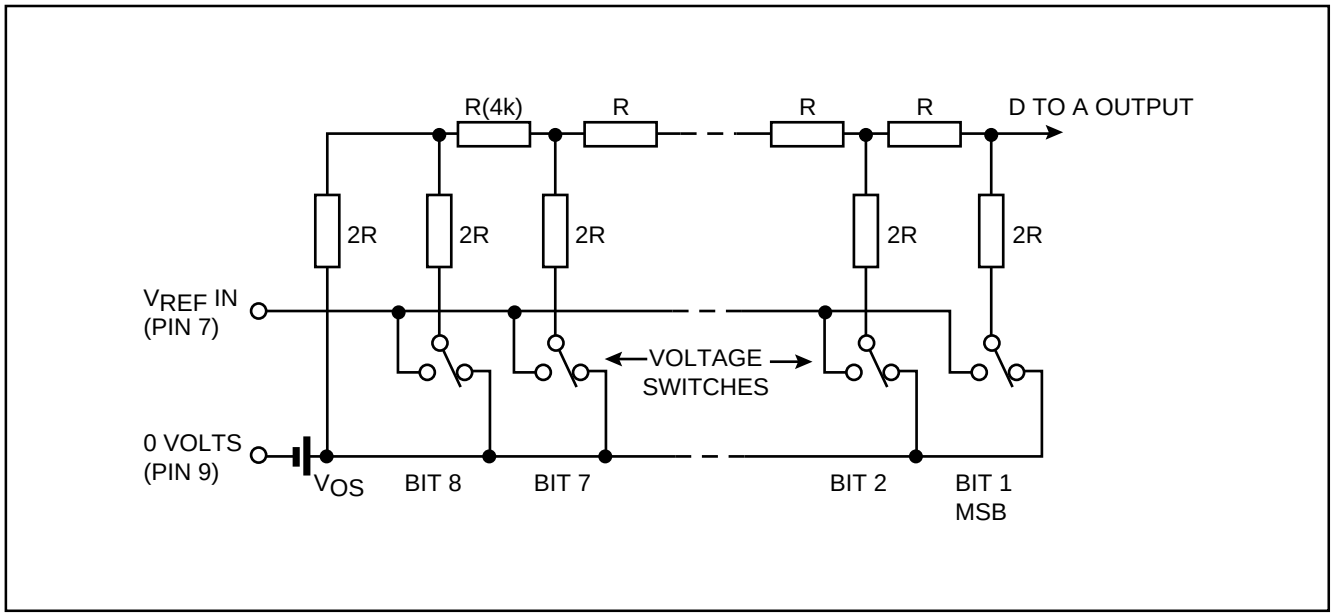

Fig.10 R-2R ladder network

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.11). A Resistor (R_{REF}) should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0 - 2.5)/0.39=6.4mA. A stabilising/decoupling capacitor, C_{REF} (4µ7), is required between pins 8 and 9. For internal reference operation V_{REF} OUT (pin 8) is connected to V_{REF} IN (pin 7).

UP to five ZN427's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

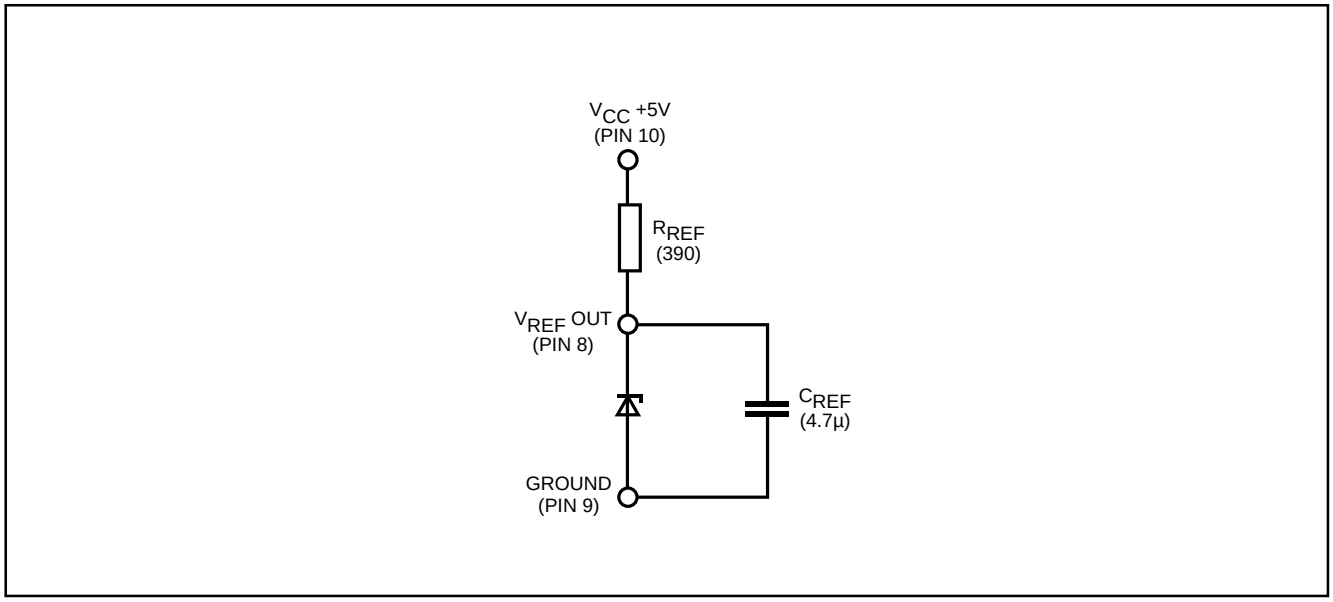

Fig.11 Internal voltage reference

(b) External reference

If required an external reference in the range +1.5 to +3.0V may be connected to V_{REF} IN. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN448/9 will operate if V_{REF} IN is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in Fig.12.

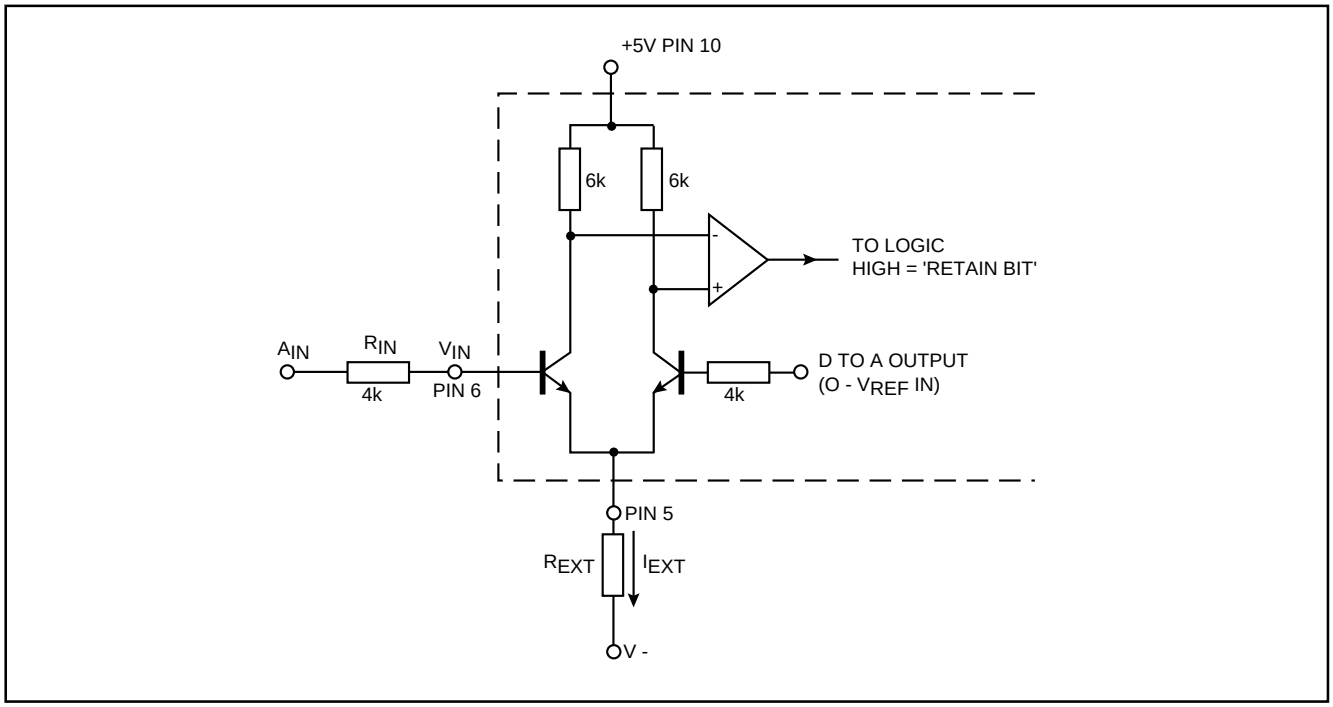

Fig.12 Comparator equivalent circuit

The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V–.

This arrangement allows the ZN427 to work with any negative supply in the range -3 to -30 volts. the ZN427 is designed to be insensitive to changes in I_{EXT} from 25µA to 150µA. The suggested nominal value of I_{EXT} is 65µA and a suitable value for R_{EXT} is given by R_{EXT} = |V_|15kΩ.

V_ (volts)	R_{EXT} (±10%)
-3	47kΩ
-5	82kΩ
-10	150kΩ
-12	180kΩ
-15	220kΩ
-20	330kΩ
-25	390kΩ
-30	470kΩ

The output from the D-A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analog input to be converted could be connected directly to the other comparator input (V_{IN}, pin 6) but for optimum stability with temperature the analog input should be applied through a source resistance (R_{IN} = 4kΩ) to match the ladder resistance).

ANALOG INPUT RANGES

The basic connection of the ZN427 shown in Fig.13 has an analog input range 0 to V_{REF} IN which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analog input input range so that the comparator always sees a positive input voltage.

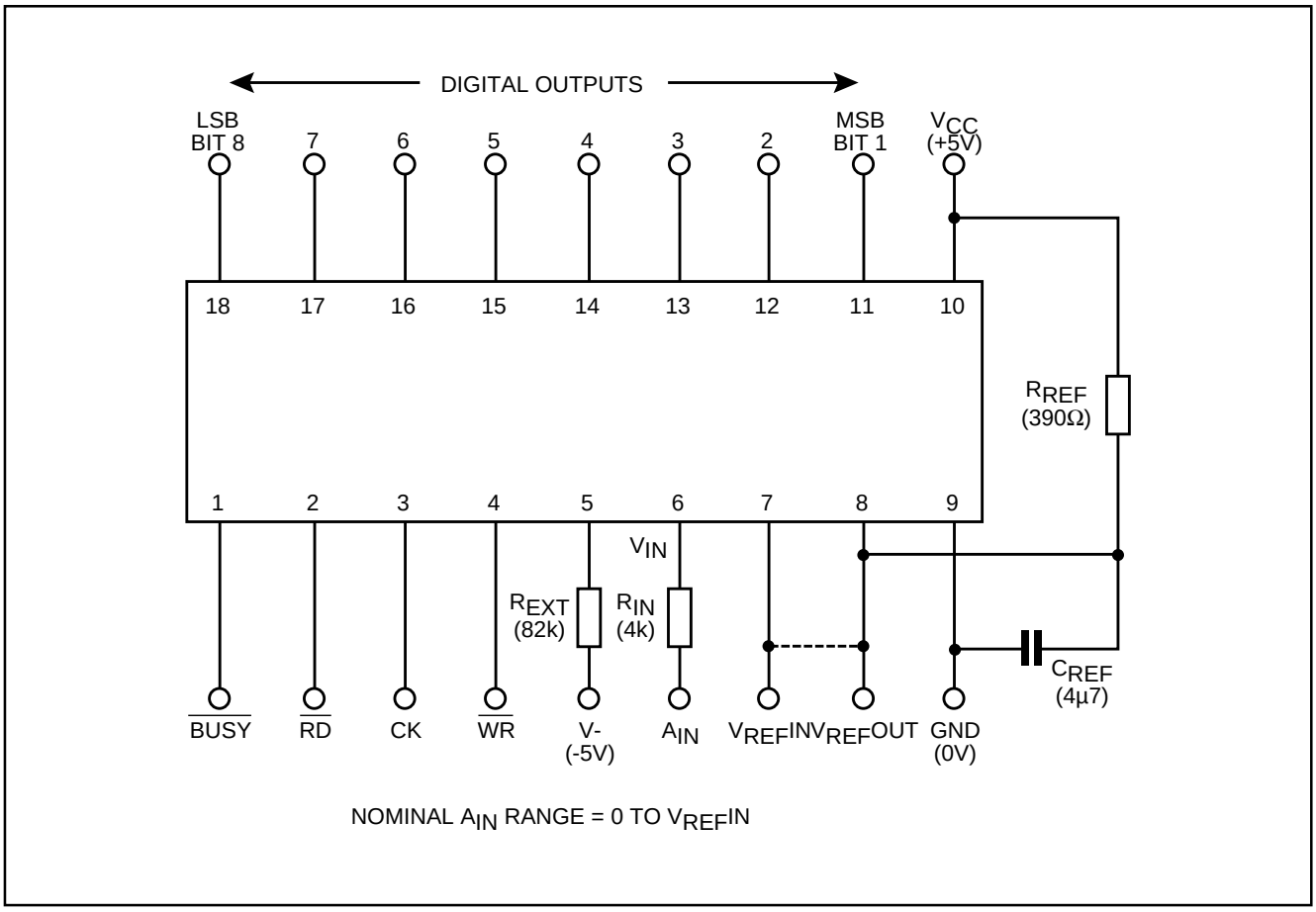

Fig.13 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig.14.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF}IN$ when the analogue input (A_{IN}) is at full-scale.

The resulting full-scale range is given by:

$$A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right), V_{REF}IN = G.V_{REF}IN.$$

To match the ladder resistance R_1/R_2 (R_{IN}) = 4kΩ.

The required nominal values of R_1 and R_2 are given by $R_1 = 4Gk$, $R_2 = \frac{4G}{G-1}$ kΩ

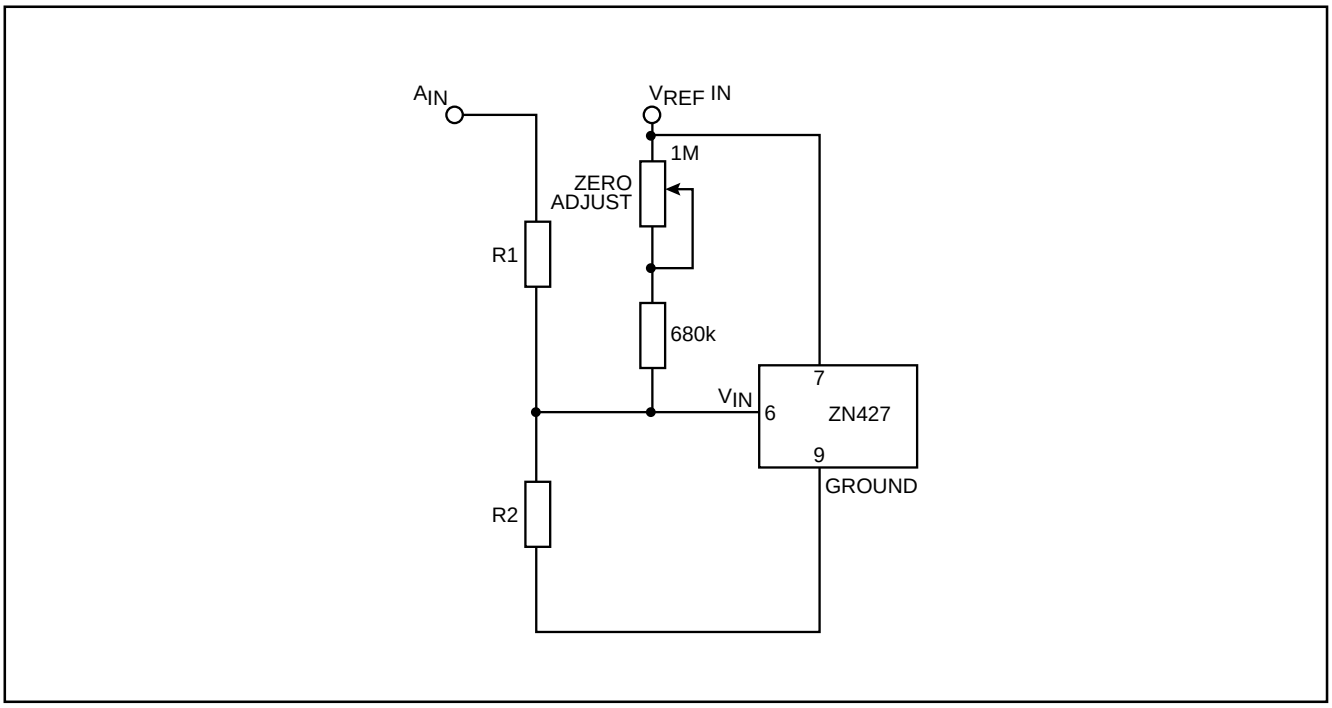

Fig.14 Unipolar operation - general connection

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for V_{REF} IN = 2.5V.

Input range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

Gain adjustment

Due to tolerance in R_1 and R_2, tolerance in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

Zero adjustment

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which correpsonds to 1.5LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of +0.5LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1.5 times V_{REF} IN.

Practical circuit values for +5 and +10V input ranges are given in Fig.15, which incorporates both zero and gain adjustments.

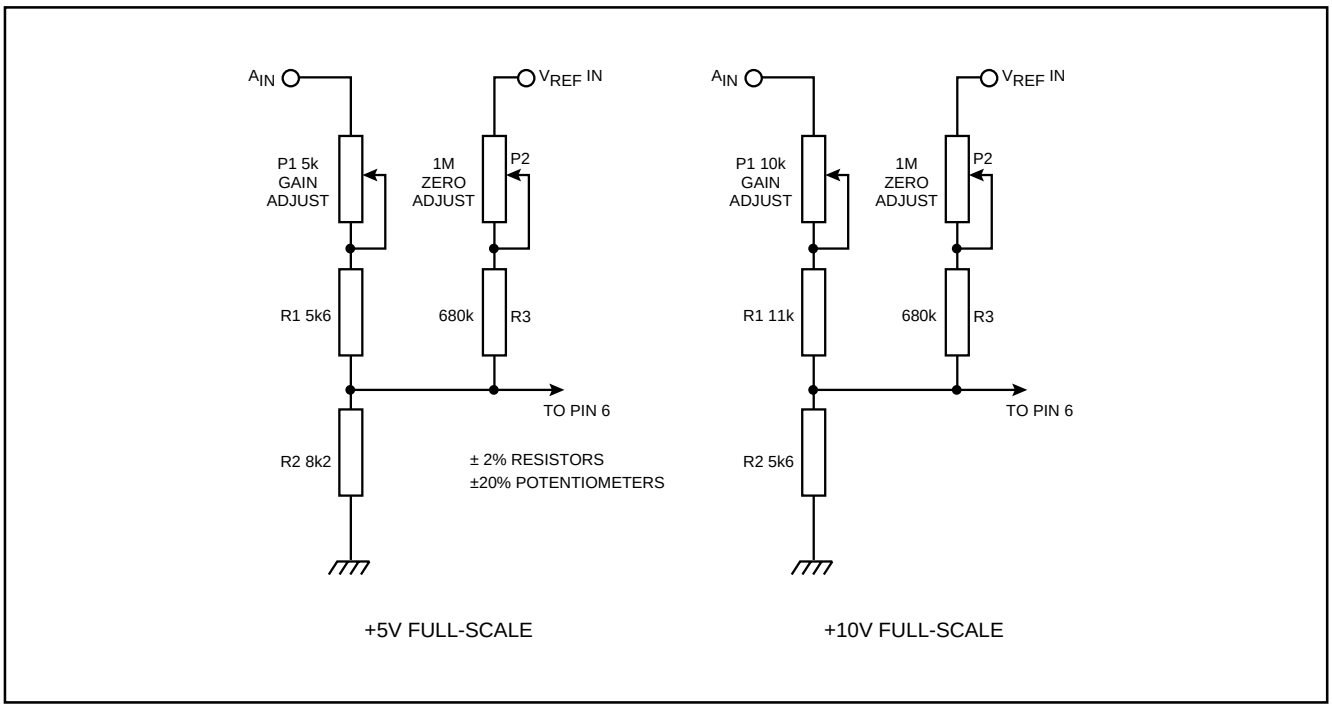

Fig.15 Unipolar operation - component values

Unipolar adjustment prodedure

(i) Apply continuous convert pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1.5LSB to A_{IN} and adjust off-set until the 8 bit (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply 0.5LSB) to A_{IN} and adjust zero until 8 bit just flickers between 0 and 1 with all other bits at 1.

Unipolar setting up points

Input range, +FS	0.5LSB	FS - 1.5LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

Unipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
0.75FS	11000000
0.5FS + 1LSB	10000001
0.5FS	10000000
0.5FS - 1LSB	01111111
0.25FS	01000000
1LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN427 is offset by half full-scale by connecting a resistor R_3 between V_{REF} IN and V_{IN} (Fig.16).

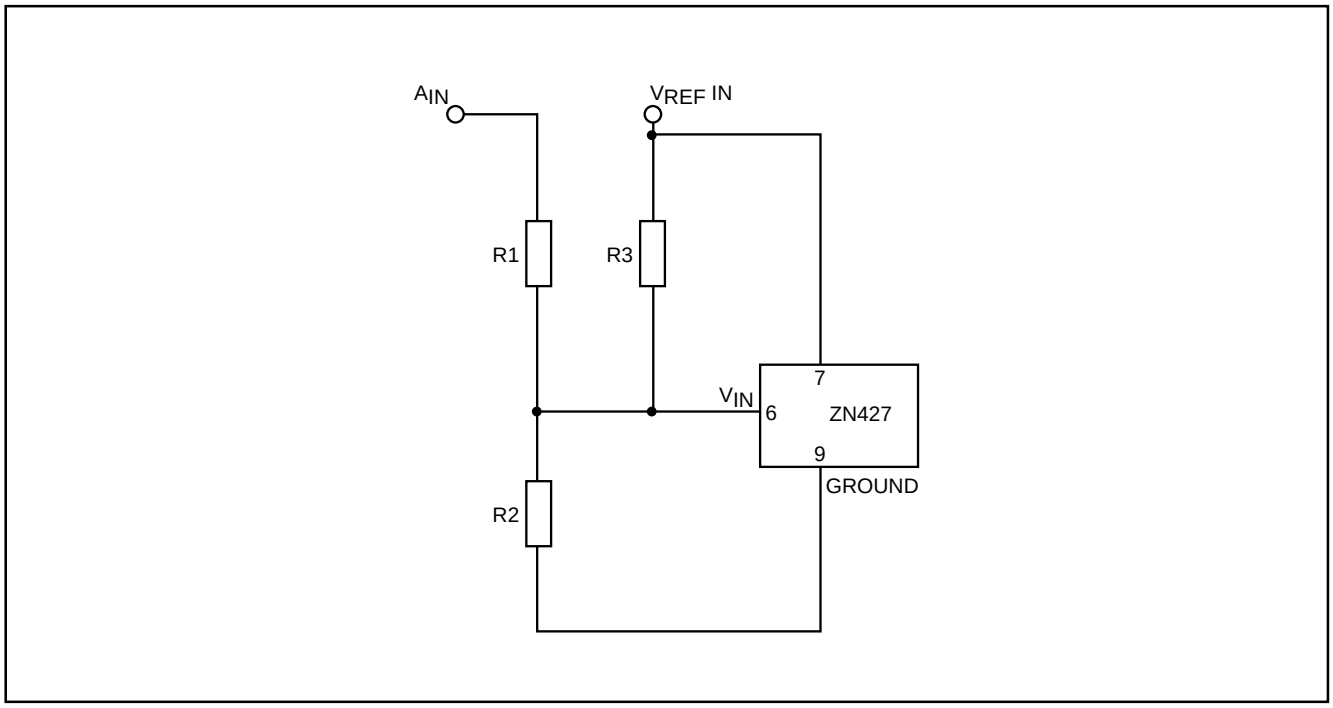

Fig.16 Bipolar operation - general connection

When A_{IN} = -FS, V_{IN} needs to be equal to zero.

When A_{IN} = +FS, V_{IN} needs to be equal to V_{REF} IN.

If the full-scale range is $\pm$ G. V_{REF} IN then R_1 = (G - 1). R_2 and R_1 = G. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ (=R_{IN}) = 4k.

Thus the nominal values of R_1, R_2, R_3 are given by R_1 = 8 GkΩ, R_2 = 8G/(G - 1)k, R_3 = 8kΩ.

A bipolar range of $\pm V_{REF}$ IN (which corresponds to the basic unipolar range 0 to $+V_{REF}$ IN) results if $R_1 = R_3$ = 8kΩ and R_2 = ∞.

Assuming the $V_{REF\,IN}$ = 2.5V the nominal values of resistors for ±5 and ±10V input ranges are given in the following table.

Input range	G	R_1	R_2	R_3
+5V	2	16kΩ	16kΩ	8kΩ
+10V	4	32kΩ	10.66kΩ	8kΩ

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig.17.

Note that in the ±5V case R_3 has been chosen as 7.5k (instead of 8.2k) to obtain a more symmetrical range of adjustment using standard potentiometers.

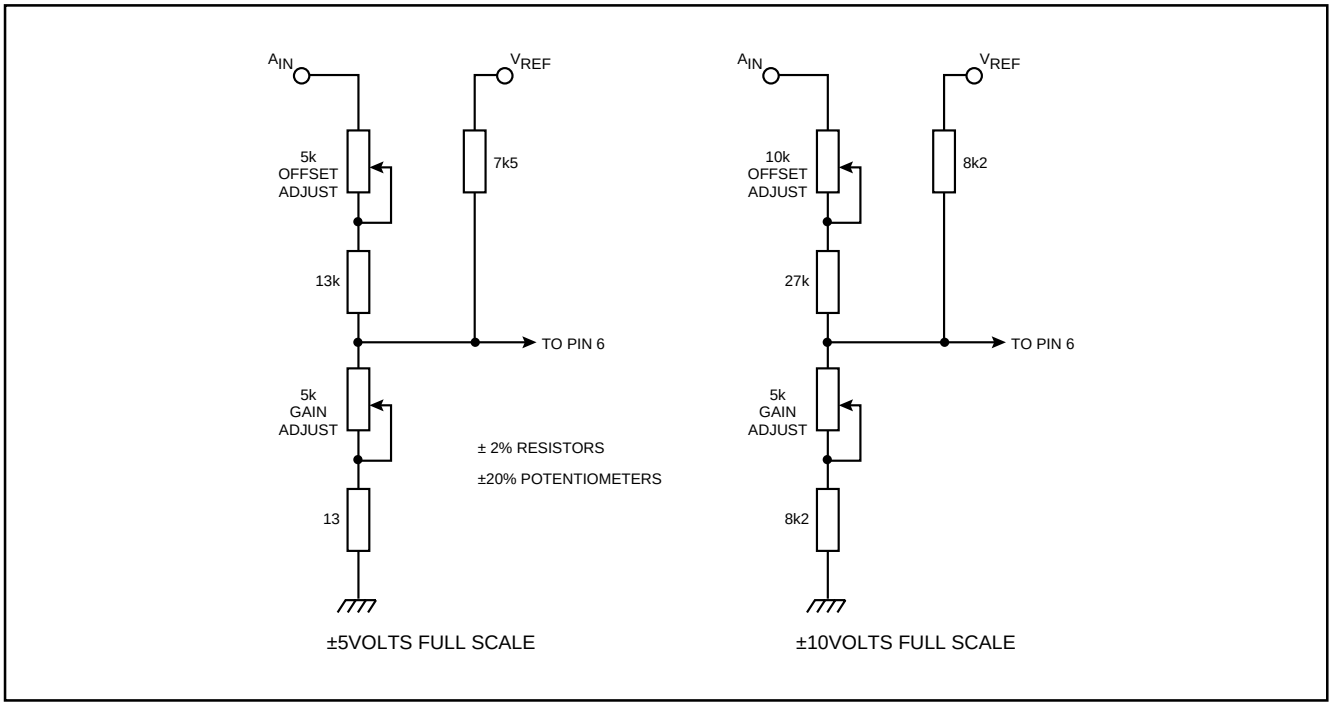

Fig.17 Bipolar operation - component values

Bipolar adjustment prodedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply -(FS -0.5LSB) to A_{IN} and adjust off-set until the 8 bit (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS -1.5LSB) to A_{IN} and adjust gain until the 8 bit just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

Bipolar setting up points

Input range, ±FS	-(FS -0.5LSB)	+(FS -1.5LSB)
+5V	-4.9805V	+4.9414V
+10V	-9.9609V	+9.8828V

$$1LSB = \frac{2FS}{265}$$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
+0.5FS	11000000
+1LSB	10000001
0	10000000
-1LSB	01111111
-0.5FS	01000000
-(FS - 1LSB)	00000001
-FS	00000000

SINGLE 5 V SUPPLY RAIL OPERATION

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig.18 works with any clock frequency from 10kHz to 1MHz and can supply up to five ZN427's.

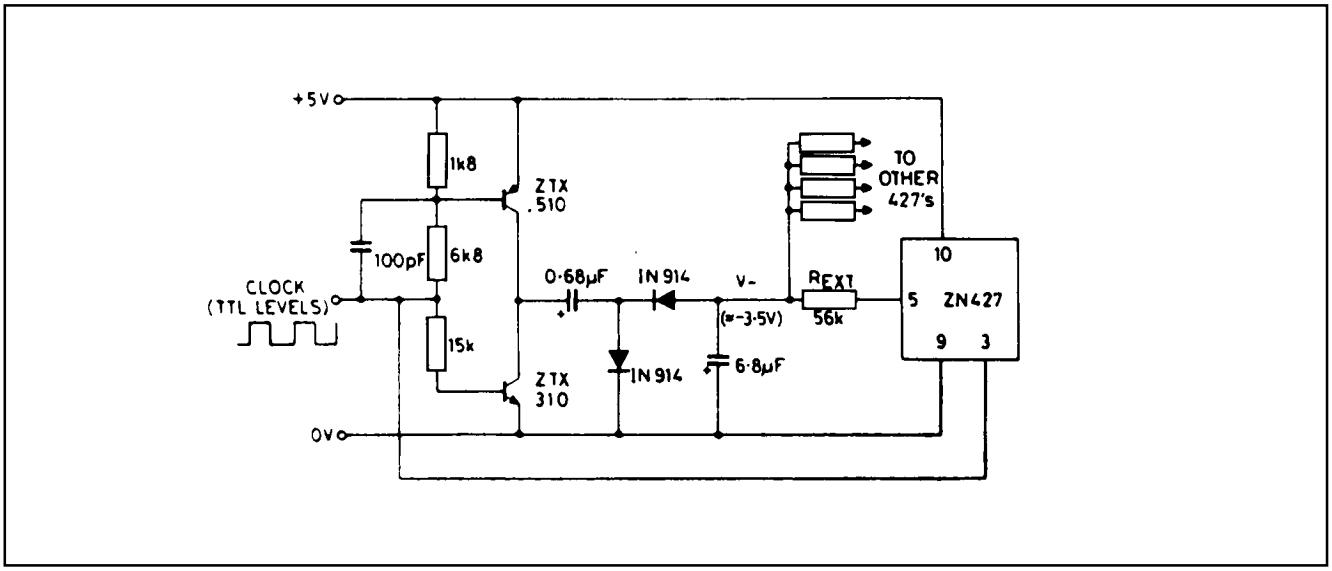

Fig.18 single 5V supply operation

HEADQUARTERS OPERATIONS
GEC PLESSEY SEMICONDUCTORS
Cheney Manor, Swindon,
Wiltshire SN2 2QW, United Kingdom.
Tel: (0793) 518000
Fax: (0793) 518411

GEC PLESSEY SEMICONDUCTORS
P.O. Box 660017
1500 Green Hills Road,
Scotts Valley, California 95067-0017,
United States of America.
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