8-bit multifunction data converter

ZN435E
ZN435J

FEATURES

- Multimode device operates as:
  - DAC
  - ADC
  - Tracking ADC
  - Voltage to frequency converter
  - Ramp and sawtooth generator
  - Nonlinear waveform generator
  - Voltage-controlled oscillator
  - Track-and-hold circuit
- 8-bit accuracy
- 800ns D-A converter settling time
- On-chip up/down counter
- On-chip clock
- On-chip voltage reference
- Single +5V supply
- Commercial or military temperature range

DESCRIPTION

The ZN435 is a versatile, multifunction 8-bit data conversion system. A voltage-output DAC, 8-bit up/down counter, stable 2.5V bandgap reference and clock generator are contained on a single chip.

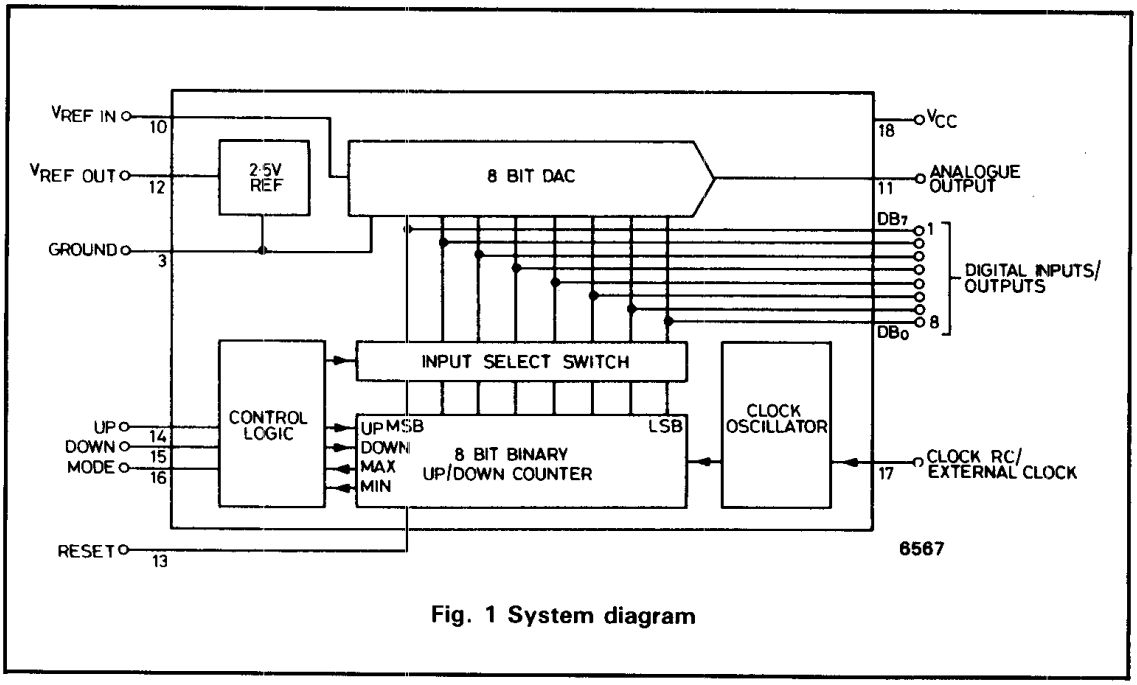


Fig. 1 System diagram

ZN435E ZN435J

ABSOLUTE MAXIMUM RATINGS

		Min.	Max.
Supply voltage			+7.0V
Max. voltage, logic and V_{REF} inputs			V_{CC}
Operating temperature range	ZN435E	0°C	+70°C
	ZN435J	−55°C	+125°C
Storage temperature range		−55°C	+125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{REF} = 1.5-3.0V, T_{amb} = +25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
D-A converter					
Resolution	8	–	–	Bits	
Linearity error	–	±0.25	±0.5	LSB	T_{min} T_{amb} T_{max}
Differential linearity error	±0.25		±1	LSB	
Zero error	–	5.0	10.0	mV	ZN435E All bits OFF
	–	5.0	10.0	mV	ZN435J
Settling time to 0.5LSB	–	500	–	ns	All bits OFF to ON
	–	800	–	ns	or vice versa
Full-scale output	2.545	2.550	2.555	V	All bits ON V_{REF} = 2.56V
Output resistance	–	4	–	kΩ	
Full-scale temperature coefficient	–	4	–	ppm/°C	Ext. V_{REF} = 2.56V
Reference voltage	0	–	3	V	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
On-chip voltage reference					
Output voltage	2.4	2.59	2.7	V	$R_{REF} = 390\Omega$
Slope resistance	–	2	4	Ω	$C_{REF} = 220nF$
Temperature coefficient of V_{REF}	–	50	–	ppm/°C	
Reference current	4	–	15	mA	
Counter (with external clock)					
High level threshold voltage V_{T+}	–	–	2.3	V	
Low level threshold voltage V_{T-}	1.7	–	–	V	
Maximum clock frequency	1	–	–	MHz	Note 1
On-chip clock					
Maximum frequency	500	–	–	kHz	
Clock frequency T.C.	–	100	–	ppm/°C	
Clock resistor	3.3	–	100	kΩ	
Clock capacitor	100	–	–	pF	
High level threshold voltage V_{T+}	–	4.6	–	V	
Low level threshold voltage V_{T-}	–	1.5	–	V	
Supply rejection	–	0.8	–	%/V	
Logic circuits					
BIT INPUTS					
High level input voltage V_{IH}	2.0	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	–	−100	μA	$V_{IN} = 2.4V$
Low level input current I_{IL}	–	–	−220	μA	$V_{IN} = 0.4V$
BIT OUTPUTS					
High level output voltage V_{OH}	–	5.0	–		No load
Low level output voltage V_{OL}	–	0.1	–		
High level output voltage V_{OH}	2.4	–	–	V	$I_{IH} = -40\mu A$
Low level output voltage V_{OL}	–	–	0.4	V	$I_{IL} = 2.5mA$

Note 1: Speeds of up to 1.7MHz may be obtained by reducing the mark space ratio of the clock.

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
CONTROL INPUTS					
High level input voltage V_{IH}	2	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	–	−25	μA	V_{IN} = 2.4V
Low level input current I_{IL}	–	–	−95	μA	V_{IN} = 0.4V
Reset pulse width	200	–	–	ns	
Power supply					
Supply voltage	4.5	5	5.5	V	
Supply current	–	35	45	mA	V_{CC} = 5.5V

GENERAL CIRCUIT OPERATION

The ZN435 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN435 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

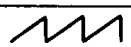
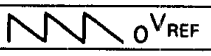
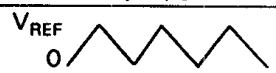
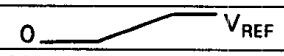
An on-chip oscillator is provided to drive the clock input of the up/down counter. The on-chip clock may be overridden by an external clock signal.

UP/DOWN COUNTER AND CONTROL LOGIC

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory, the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN435. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continuously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs accessible from the I/O port.

A truth table for the control inputs is given in Table 1.

Reset	Mode	Down	Up	Digital function	Analogue waveform
1	1	1	1	Counter stopped.	
1	1	1	0	Count up continuously.	
1	1	0	1	Count down continuously.	
1	1	0	0	Count up, reverse at F.S., count down, reverse at zero.	
1	0	1	1	Counter stopped.	
1	0	1	0	Count up, stop at F.S.	
1	0	0	1	Count down, stop at zero.	
X	0	0	0	DAC mode, counter output disabled. Counter can still be reset by taking reset input low.	
0	X	X	X	Counter reset. Does not affect analogue output in DAC mode.	

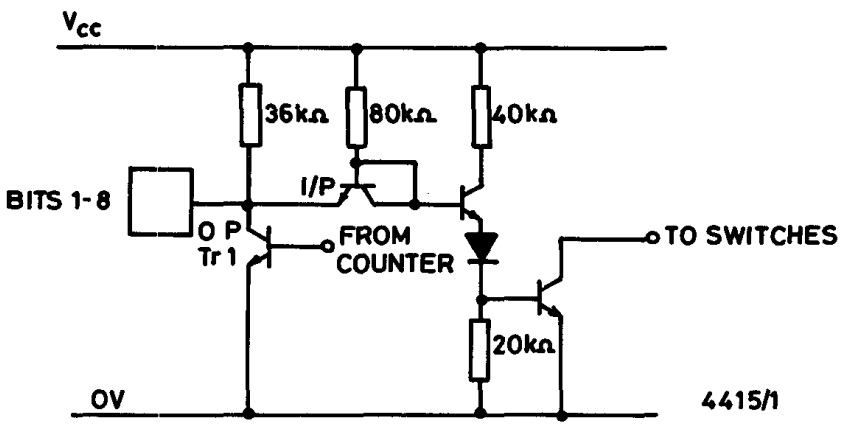


Fig. 2 Bit inputs/outputs

DATA PORT

One bit of the data port is shown in Fig. 2. The input/output pin is the junction of the counter output buffer and the DAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families.

CLOCK CIRCUIT

The on-chip clock circuit of the ZN435 is shown in Fig. 3.

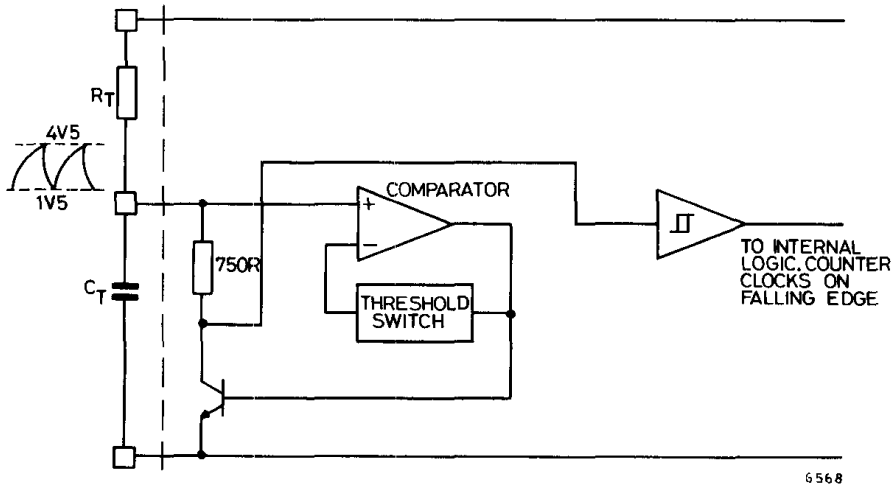


Fig. 3

The frequency of the clock is given by $f_{CLK} \simeq \frac{1}{2R_TC_C}$ (Hz, Ω,F)

Typical graphs of oscillator frequency versus resistor and capacitor values are given in Fig. 4.

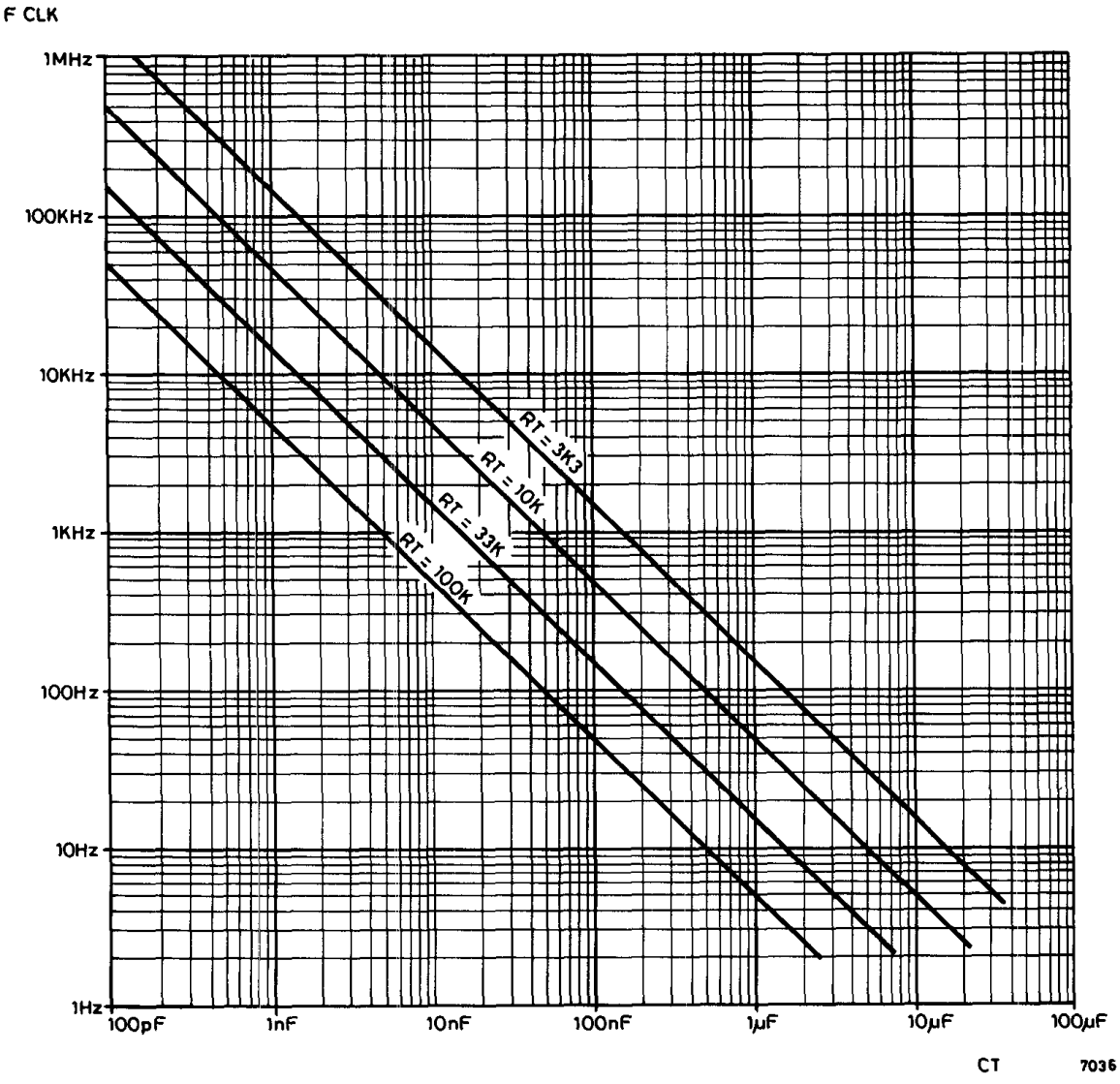


Fig. 4

The external capacitor C_T is charged via the external resistor R_T to the upper threshold of the comparator (about +4.5V with V_{CC} = +5V). The comparator turns on the discharge transistor to discharge C_T and switches its threshold to the lower value of about 1.5V. When the voltage on C_T has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven from either a TTL totem-pole output (Fig. 5a), an open collector output (Fig. 5b), or a CMOS gate (Fig. 5c). In all three cases the V_{OH} of the driving gate must be attenuated to below 4.5V so that the internal discharge transistor is not turned on.

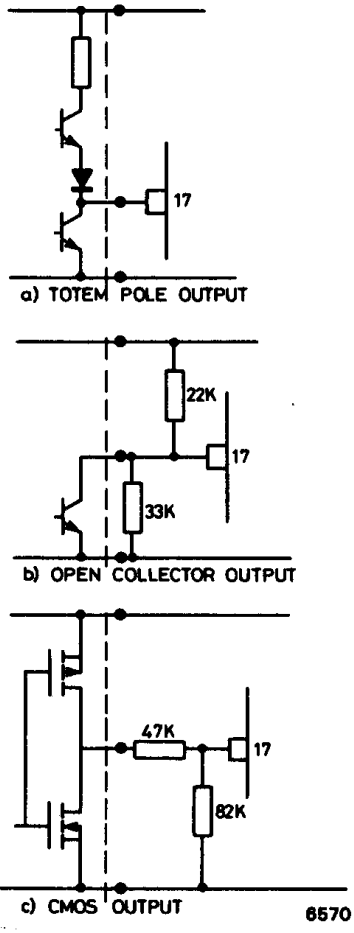


Fig. 5 Overdriving the clock input

ANALOGUE CIRCUITS

D-A converters

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 6.

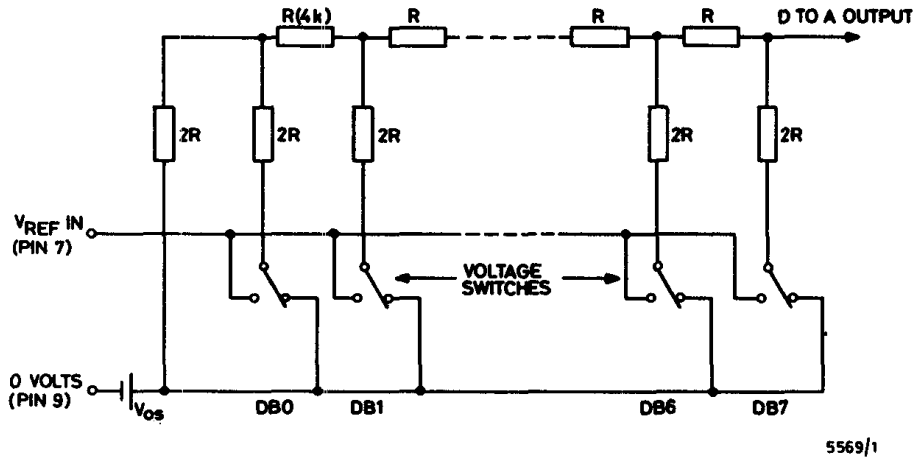


Fig. 6 R-2R ladder network

Each 2R element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256} (V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 5mV for both the ZN435E and ZN435J. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0V to $V_{REF\ IN}$ with an output resistance R (4kΩ).

REFERENCE

On-chip reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig. 7).

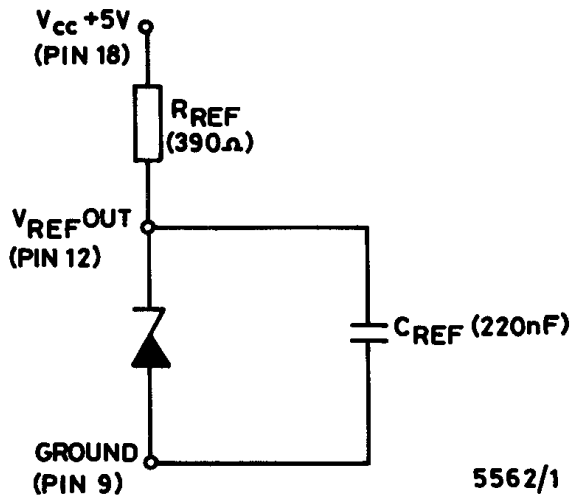


Fig. 7 Internal voltage reference

An external resistor (R_{REF}) should be connected between pins 12 and 18 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor (C_{REF}) is required between pins 12 and 9.

To use the internal reference $V_{REF\ OUT}$ (pin 12) is connected to $V_{REF\ IN}$ (pin 10).

The recommended reference resistor of 390Ω will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN435's. Where several ZN435's are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

APPLICATIONS

The applications of the ZN435 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated. It should be noted that there is a danger of obtaining incorrect codes if the up/down control lines change at the same time as the active negative edge of the clock. Therefore if these control lines are changing asynchronously then extra circuitry should be used to prevent them changing at the negative edge of the clock. This is best achieved by latching these signals using positive edge triggered D-type flip-flops as is demonstrated in the circuit diagrams of Figs. 9 and 10.

WAVEFORM GENERATOR

The circuit of a low frequency waveform generator is illustrated in Fig. 8.

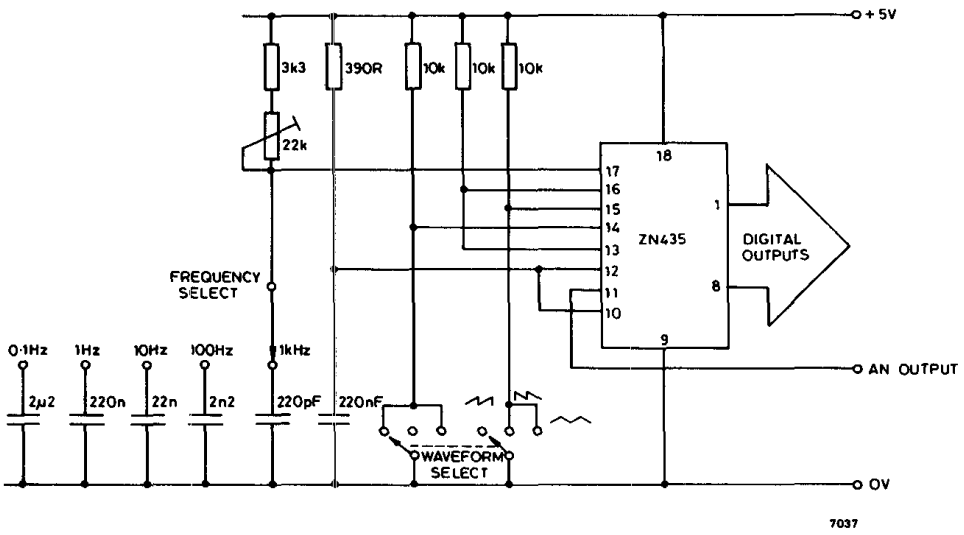


Fig. 8 Waveform generator

Note: The frequencies given above apply to the sawtooth waveforms. For the triangular waveforms divide the frequencies above by two.

This will produce stable, linear, sawtooth and triangle waveforms.

RAMP AND COMPARE A-D CONVERTER

A simple ramp and compare A-D converter can be constructed using the ZN435 as shown below.

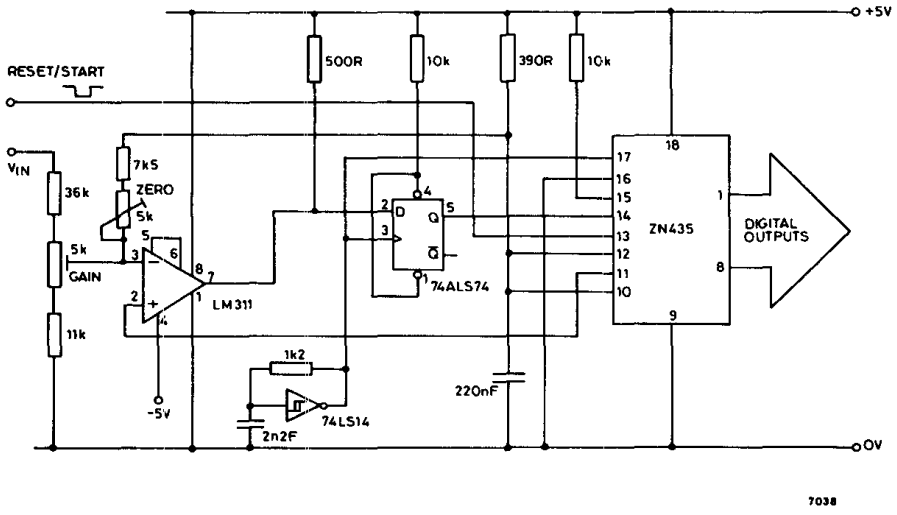


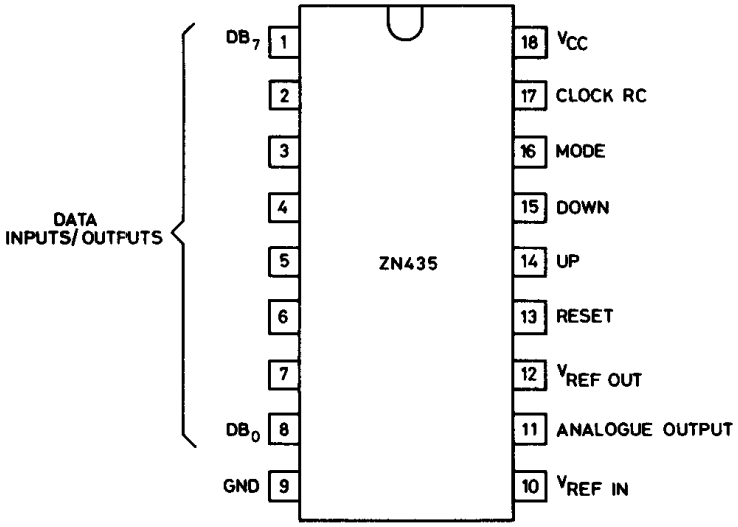
Fig. 9 Ramp and compare ADC

In this circuit two LM311 op-amps are used to make a window comparator. This has a dead-band equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2. This is easily achieved by applying a stable voltage at the input. Then with the ZN435 removed, applying a variable voltage to pin 11 on the ZN435 socket. By varying this voltage and monitoring the op-amp outputs the window can be adjusted so that the threshold of A1 is 10mV above that of A2.

Whenever the analogue voltage is above the threshold of A2 the counter will count up so that the DAC output increases to follow the analogue voltage. Whenever the analogue voltage is below the threshold of A1 the counter will count down so that the DAC output decreases to follow the analogue voltage. When the analogue voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped. Again the input voltage range is $\pm$ 10V, other ranges being possible by suitable choice of input resistors.

ZN435E ZN435J

PIN CONNECTIONS



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