T-51-10-08

8-bit μP compatible A-D converter

ADVANCE PRODUCT INFORMATION

ZN439 Series

FEATURES

- Choice of linearity: ¼LSB-ZN439-9, ½LSB-ZN439-8, 1LSB-ZN439-7
- 5μs conversion time
- μP, TTL and CMOS compatible
- On-chip clock
- Trimmable bandgap reference
- Versatile microprocessor interfacing with double buffered output latch
- Equally suitable for stand alone applications
- ROM type operation
- Commercial or military temperature ranges
- 22 lead DIL package

DESCRIPTION

The ZN439 is an 8-bit successive approximation A-D converter designed to be easily interfaced to microprocessors. All active circuitry is contained on-chip including clock generator, trimmable 2.5V bandgap reference, control logic and double buffered latches with three-state outputs.

These features give extra flexibility in use, with just three inputs to control all ADC operations and double buffered output latches which will allow data to be read at any time irrespective of the status of the converter.

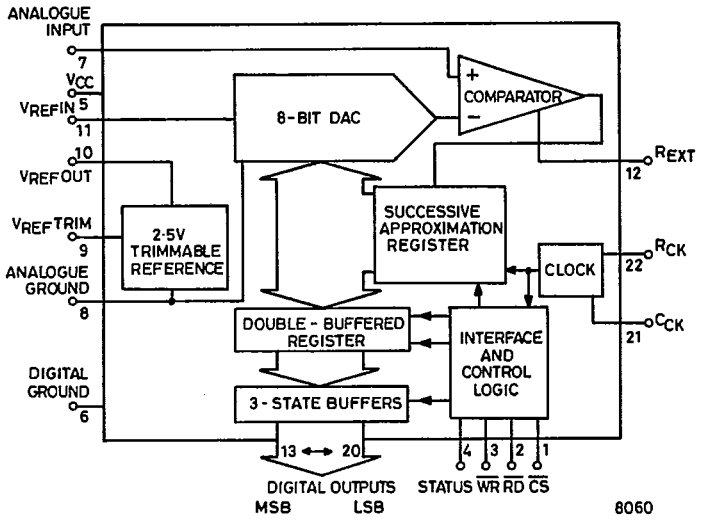

Fig. 1 System diagram

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ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} . . . . . +7.0V
Maximum voltage, logic and V_{REF} inputs, A_{IN} . . . . . V_{CC}, −0.5V
Operating temperature range . . . . . 0 to +70°C (E package)
−55 to +125°C (J package)
Storage temperature range . . . . . −55 to +125°C

ELECTRICAL CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C and f_{CLK} = 1.6MHz unless otherwise specified).

Parameter	T_{amb} = +25°C			Over specified Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
ZN439-9							
Linearity error	–	–	±0.25	–	±0.25	LSB	
Differential linearity error	–	–	±0.5	–	±0.5	LSB	
ZN439-8							
Linearity error	–	–	±0.5	–	±0.5	LSB	
Differential linearity error	–	–	±0.75	–	±0.75	LSB	
ZN439-7							
Linearity error	–	–	±1	–	±1	LSB	
Differential linearity error	–	–	±1	–	±1	LSB	
ALL TYPES							
Zero transition	–	7	–	–	–	mV	Moulded "E"
(00000000→00000001)	–	7	–	–	–	mV	Ceramic "J"
Full-scale transition	–	2.550	–	–	–	V	Moulded "E"
(11111110→11111111)	–	2.550	–	–	–	V	Ceramic "J"
Linearity temperature coefficient		±3 typ.				ppm/°C	Ext. Ref.
Differential linearity temperature coefficient		±6 typ.				ppm/°C	
Gain temperature coefficient		±10 typ.				ppm/°C	
Offset temperature coefficient		±7 typ.				ppm/°C	
Resolution	8	–	–	–	–	Bits	
Conversion time	5	–	–	–	–	µs	
Supply rejection	–	0.2	–	–	–	%/V	
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current	–	30	45	–	–	mA	Outputs in high impedance state
Power consumption	–	150	225	–	–	mW	
Reference input range	1.5	–	3.0	–	–	V	
Ladder output impedance	–	2.7	–	–	–	kΩ	
COMPARATOR							
Input current	–	1.0	–	–	–	µA	V_{in} = +3V, R_{ext} = 82K
Input resistance	–	100	–	–	–	kΩ	
Tail current	25	–	150	25	150	µA	R_{ext} = 82K, V_{-} = −5V
Negative supply	−3	−5	−30	−3	−30	V	
Input voltage	−0.5	–	+3.5	−0.5	+3.5	V	

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ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	$T_{amb} = +25°C$			Over specified Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
INTERNAL VOLTAGE REFERENCE							
Output voltage	–	2.588	–	–	–	V	PIN 9 NC $R_{REF} = 1.6K$ $C_{REF} = 0.47\mu F$
Output voltage tolerance	–	–	±3	–	–	%	
Slope impedance	–	0.75	–	–	–	Ω	
Reference current	0.25	–	5.2	0.25	5.2	mA	
Trim range	±5	–	–	±5	–	%	$R_{TRIM} = 10K$
Output voltage temperature coefficient	–	70	–	–	–	ppm/°C	At 5mA operating current (worst case) 25ppm at 2.0mA
CLOCK							
Maximum on-chip clock frequency	–	1.6	–	–	–	MHz	$R_{ck} = 1.5K\Omega$ $C_{ck} = 100pF$ (See Fig. 13)
Clock frequency tempco	–	−0.1	–	–	–	%/°C	
Clock capacitor	100	–	–	–	–	pF	
Clock resistor	1.0	–	–	–	–	kΩ	
Maximum external clock frequency	2	–	–	2	–	MHz	
Clock pulse width	250	–	–	–	–	ns	
High level I/P voltage V_{IH}	3.5	–	–	3.5	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	1	–	–	–	μA	$V_{CC} = 5.5V$ $V_{IN} = 4V$
Low level I/P current I_{IL}	–	10	–	–	–	nA	$V_{CC} = 5.5V$ $V_{IN} = 0.8V$
Supply rejection	–	3.5	–	–	–	%/V	Int. clock Freq.
LOGIC $\overline{WR}$ + $\overline{CS}$ INPUTS							
High level I/P voltage V_{IH}	2	–	–	2	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	40	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$
High level I/P current I_{IH}	–	20	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	−50	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
LOGIC $\overline{RD}$ INPUT							
High level I/P voltage V_{IH}	2	–	–	2	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	220	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$

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ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	$T_{amb} = +25°C$			Over specified Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
High level I/P current I_{IH}	–	120	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	−370	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
DATA AND STATUS OUTPUTS							
High level output voltage V_{OH}	2.4	–	–	2.4	–	V	$I_{OH\ MAX}$
Low level output voltage V_{OL}	–	–	0.4	–	0.4	V	$I_{OL\ MAX}$
High level output current I_{OH}	–	–	−800	–	–	μA	
Low level output current I_{OL}	–	–	2	–	–	mA	
Three-state disable output leakage current	–	–	2.0	–	–	μA	$V_{OUT} = 0.4V$
	–	–	2.0	–	–	μA	$V_{OUT} = 2.4V$
Enable/disable Delay times T_{E1}	90	120	160	–	–	ns	
T_{E0}	60	100	120	–	–	ns	
T_{D1}	80	120	160	–	–	ns	
T_{D0}	60	80	110	–	–	ns	
Write pulse width	150	–	–	–	–	ns	
$\overline{WR}$ input to status O/P high	–	280	350	–	–	ns	
Read pulse width	160	–	–	–	–	ns	
Read input high to status output high	–	240	400	–	–	ns	

GENERAL CIRCUIT OPERATION

The ZN439 utilises the successive approximation technique to produce an 8-bit parallel digital output. Upon receipt of a negative going pulse on the $\overline{WR}$ input the status output goes high, and the DAC input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. If the analogue input is larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 8 bits have been compared. On the 8th negative clock edge status goes low indicating that the conversion is complete.

The double-buffered register means the outputs can be enabled at any time, irrespective of the conversion status, and valid data will always be presented to the data bus. **Therefore the $\overline{RD}$ signal can be completely asynchronous with respect to the status.** Data can be read by taking $\overline{RD}$ low, thus enabling the three-state outputs. $\overline{RD}$ cannot be tied low as this will prevent the converter from updating it's outputs at the end of a conversion.

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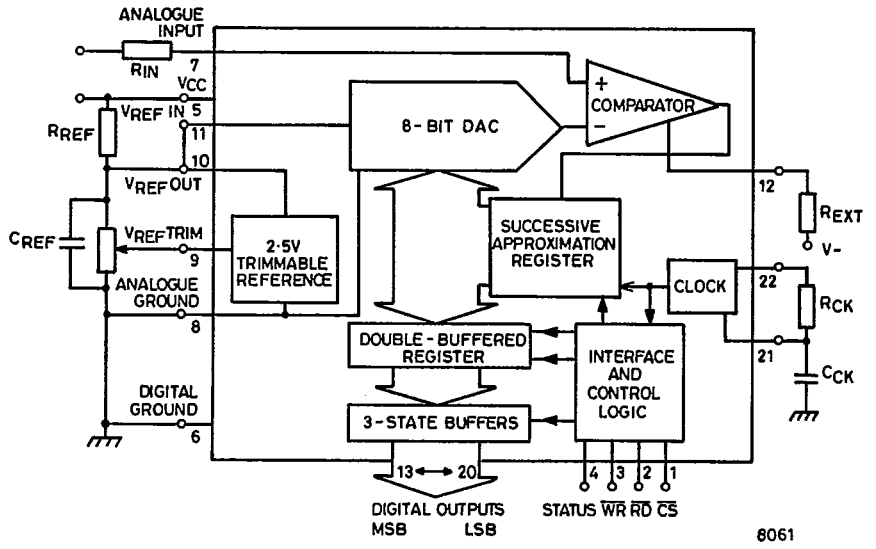

Fig. 2 Typical external components

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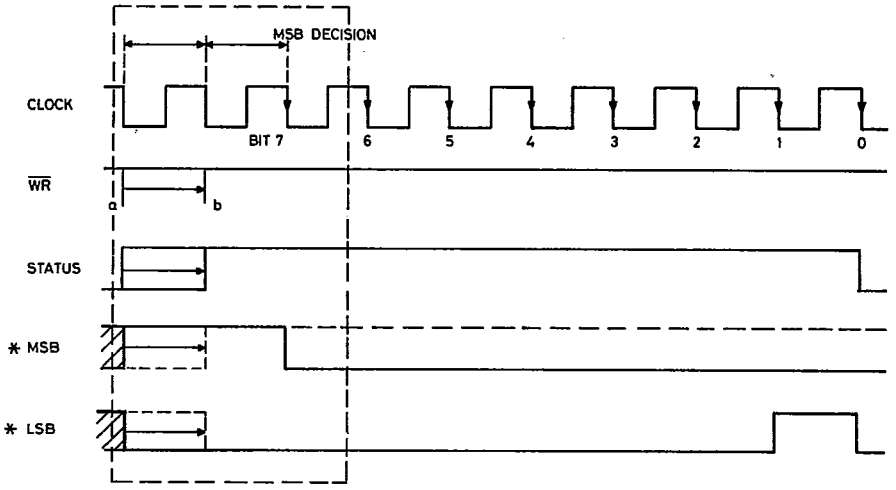
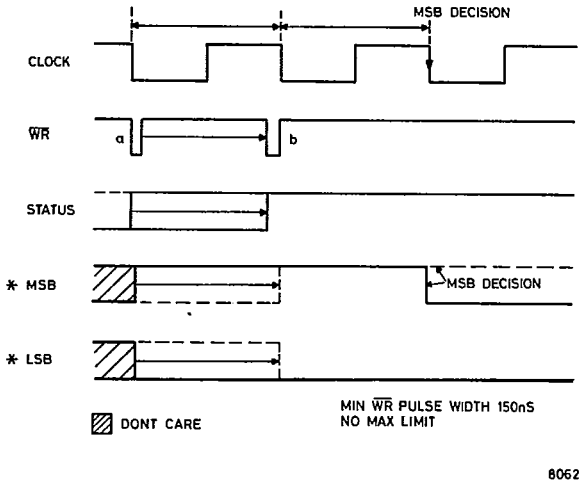


Fig. 3a



*Note: These signals are the internal MSB and LSB of the successive approximation register.

Fig. 3b (expanded inset)

Fig. 3 Timing diagram

CONVERSION TIMING

The ZN439 will accept a low going convert ($\overline{WR}$) pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 8 and up to 9 clock pulses later depending on the relative timing of the clock and convert signals. Timing diagrams for a conversion are shown in Fig. 3.

The ZN439 is first selected by taking $\overline{CS}$ (chip select) low. The converter is cleared by a low going convert ($\overline{WR}$) pulse, which sets the most significant bit and the status while resetting all other bits. Holding the $\overline{WR}$ input low will not inhibit the operation of the device.

The convert ($\overline{WR}$) pulse can be as short as 150ns; however the MSB must be allowed to settle for at least 625ns before the MSB decision is made. To ensure that this criterion is met even with short write pulses the converter waits for a falling clock edge before commencing with the conversion. This ensures that the MSB is allowed to settle for at least a full clock period or 625ns at maximum clock frequency. If the $\overline{WR}$ input is pulsed low at any time the conversion will restart. The input signals can be locked out during a conversion by removing the $\overline{CS}$ signal. This will isolate the converter from the external signals around it.

The status output goes low at the end of a conversion indicating that new data is now available. Internal logic monitors the $\overline{WR}$ input and if at the end of a conversion the $\overline{WR}$ input is high the clock signal will be locked out of the converter leaving it set up (i.e. the code 10000000 will appear on the input to the DAC) and waiting for its next convert ($\overline{WR}$) pulse. If the $\overline{WR}$ input is low the clock signal will not be inhibited allowing the converter to procede with another conversion. The double buffering on the three-state data outputs gives extra flexibility allowing the $\overline{RD}$ input to operate completely asynchronously with respect to the status and always produce valid data. Note that the $\overline{RD}$ input cannot be tied low as this will prevent the converter from updating at the end of a conversion.

CONTINUOUS CONVERSION

The ZN439 can be made to cycle by simply tying the $\overline{CS}$ and $\overline{WR}$ inputs low. It should be noted that after power up, valid data will only be available after the internal reference has stabilised. This time will depend upon the values of the reference decoupling capacitor and load resistor, but will be approximately 2mS for a 1K6 resistor and a 0.47μF capacitor.

A timing diagram for the continuous conversion mode is shown in Fig. 5 (overleaf).

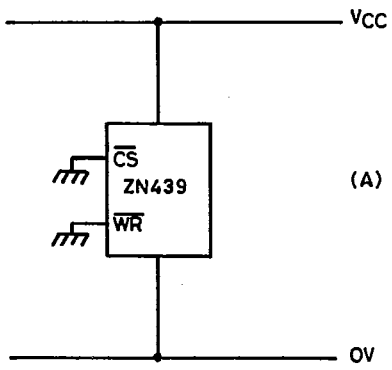


Fig. 4 Circuit for continuous conversion

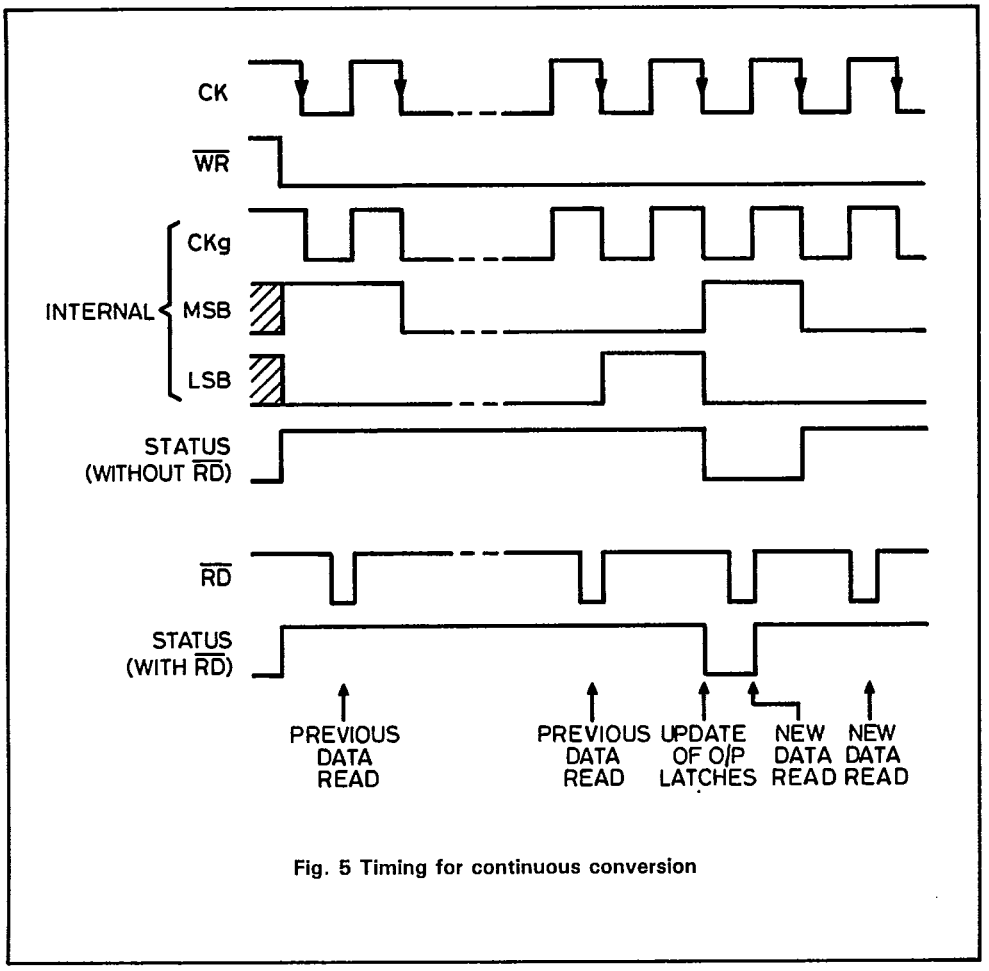


Fig. 5 Timing for continuous conversion

INTERRUPT DRIVEN

The ZN439 can also be used in an interrupt driven mode by using the status output. A $\overline{WR}$ pulse initiates a conversion sending the status high. The high to low transition of the STATUS output, indicating the end of a conversion, can be used as an interrupt signal by the microprocessor i.e. informing the microprocessor that a conversion has been completed. On receiving the interrupt the microprocessor sends out an $\overline{RD}$ pulse to take in the new data. On the rising edge of the $\overline{RD}$ pulse data is latched into the microprocessor and internal control logic forces the status output high hence removing the interrupt signal.

A timing diagram for the interrupt driven mode is shown in Fig. 6.

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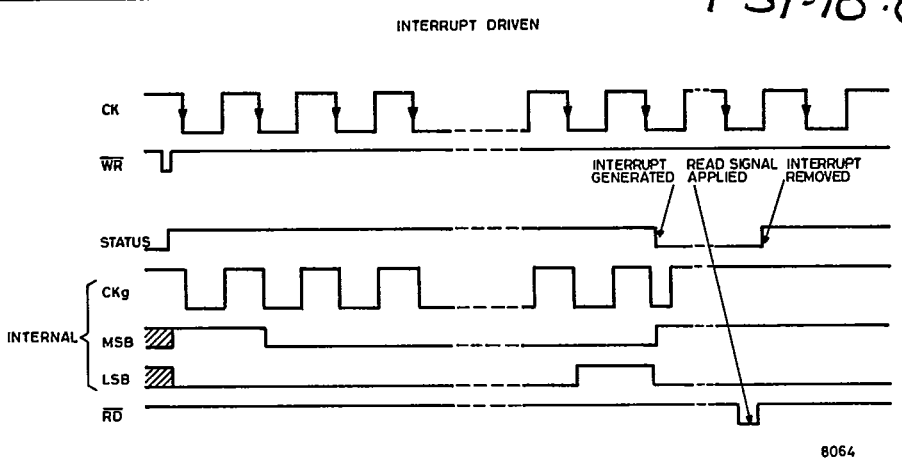

Fig. 6 Timing for interrupt driven mode

'STAND ALONE' OPERATION

The ZN439 is equally suitable for stand alone applications containing an on-chip clock and a 2.5V trimmable bandgap reference.

A typical circuit for unipolar operation is shown in Fig. 7a.

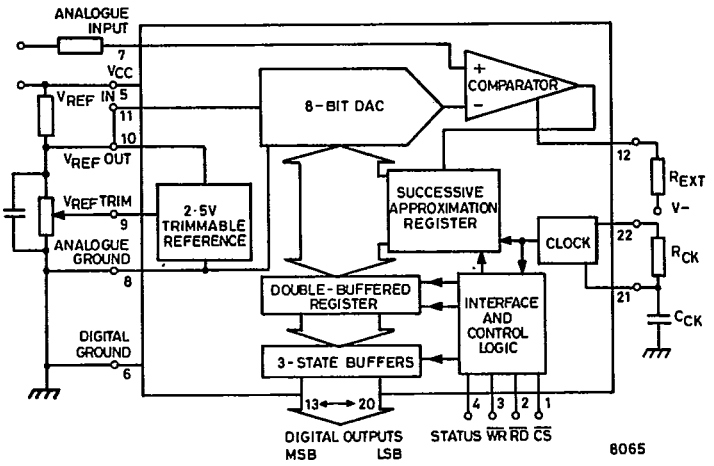

Fig. 7a Unipolar operation

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By tying the $\overline{WR}$ and $\overline{CS}$ inputs low the device can be made to cycle. Also if the status output is connected via an inverter to the $\overline{RD}$ input the device can be updated at the end of each conversion and the output buffers enabled without the need for extra external control signals.

A timing diagram for stand alone operation is shown in Fig. 8.

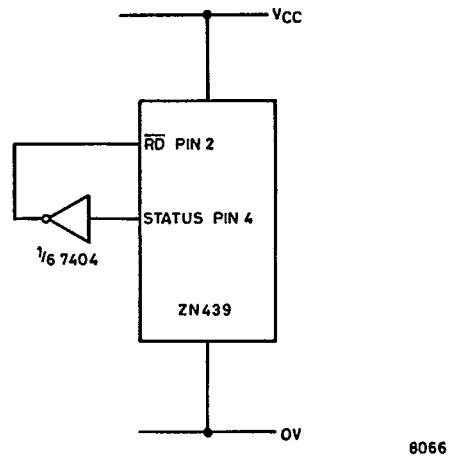
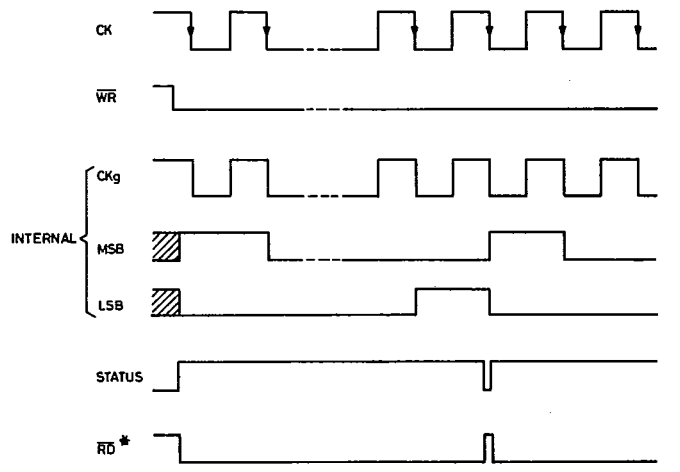


Fig. 7b Circuit for updating 'stand alone' converter



*Data valid while read is low subject to three-state delays

Fig. 8 Timing for 'stand alone' operation

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DATA OUTPUTS

The data outputs are provided with three-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 9. Whilst the $\overline{RD}$ input is high both output transistors are off and the device presents only a high impedance load to the bus. When $\overline{RD}$ is low the data outputs will assume the logic states present on the outputs of the double buffered register.

A test circuit and timing diagram for the output enable/disable delays are given in Fig. 10 (overleaf).

The status output utilises the same active pull-up as the data outputs for CMOS/TTL compatibility.

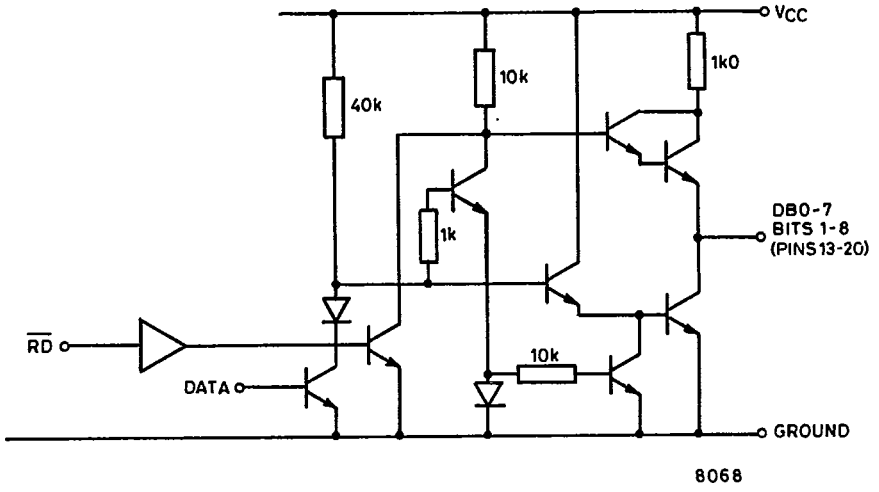

Fig. 9 Data outputs

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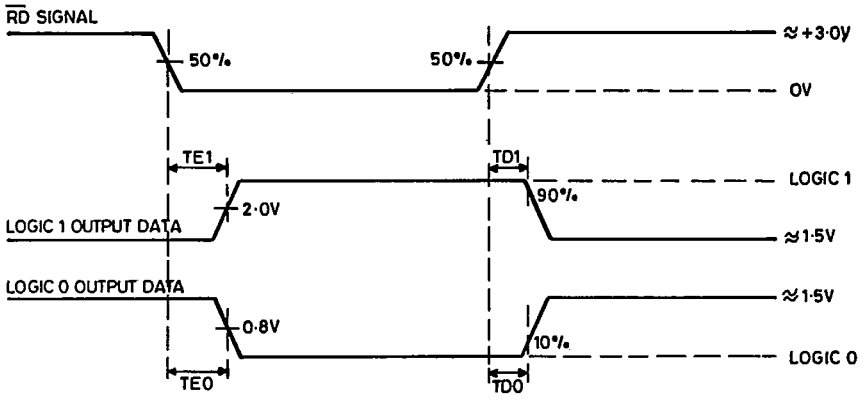

TE = RD ENABLE DELAY TIME
TD = RD DISABLE DELAY TIME

Fig. 10a Output enable/disable delays

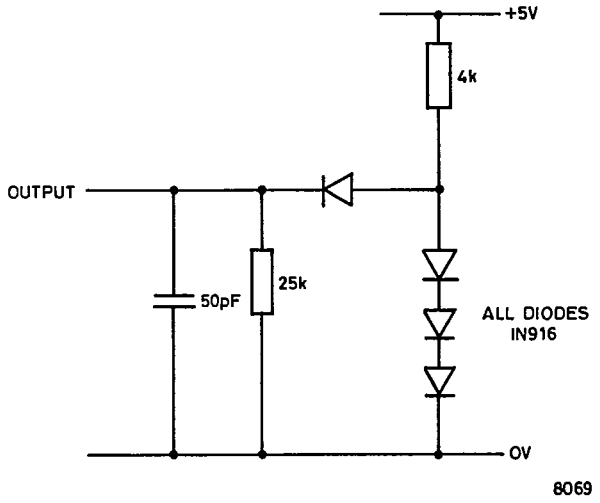

Fig. 10b Output load circuit

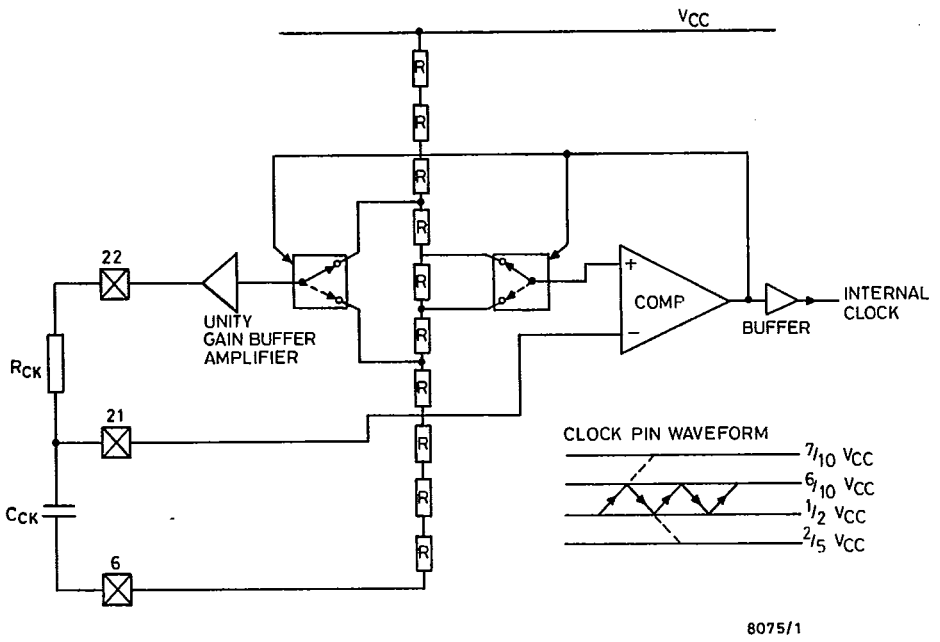

Fig. 11 Clock oscillator circuit

ON-CHIP CLOCK

The ZN439 on-chip clock oscillator operates with only two external components; a resistor connected between pin 21 and pin 22 and a capacitor between pin 21 and pin 6. The clock oscillator circuit and the external component connections are shown in Fig. 11.

The oscillator frequency may be varied with the aid of a potentiometer or variable capacitor as shown in Fig. 12a and Fig. 12b. Alternatively it is possible to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate as shown in Fig. 12c.

A graph of oscillator frequency against capacitor and resistor values is given in Fig. 13.

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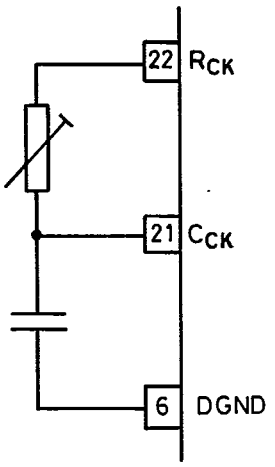

Fig. 12a Fixed capacitor + fixed/variable resistor

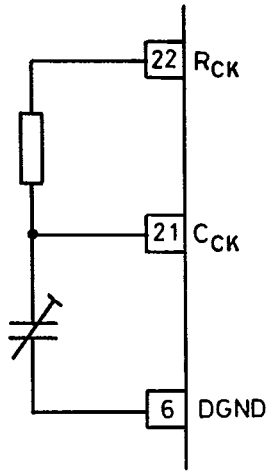

Fig. 12b Fixed resistor + fixed/variable capacitor

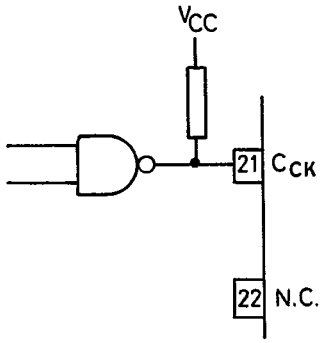

Fig. 12c External TTL or CMOS drive

Fig. 12 Clock circuit external components

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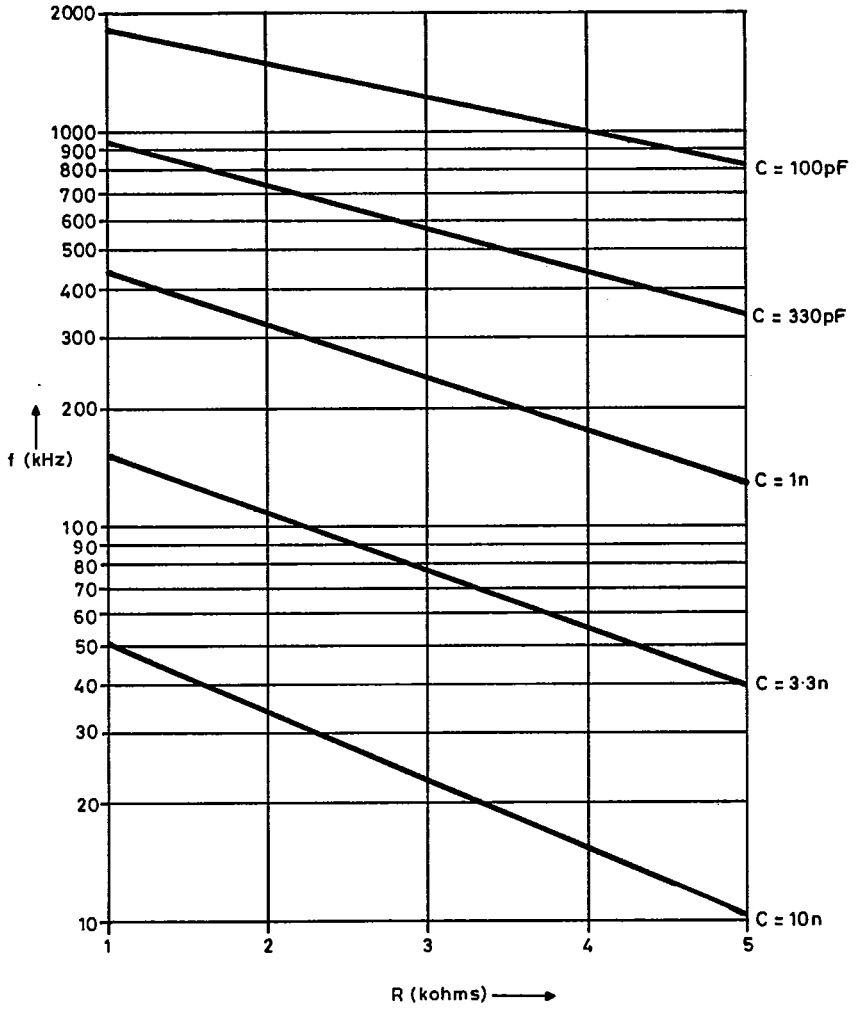

Fig. 13 Typical clock frequency v R. and C. values

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ANALOGUE CIRCUITS

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5 Zener diode with a very low slope impedance (Fig. 14). A resistor (R_{REF}) should be connected between V_{CC} and $V_{REF\ OUT}$, and a decoupling capacitor, C_{REF} (0.47μF), is required between $V_{REF\ OUT}$ and AGND. For internal reference operation $V_{REF\ OUT}$ is connected to $V_{REF\ IN}$.

A suitable current to drive one ZN439 is nominally 1.5mA and will be supplied by an R_{REF} of 1K6 [(5 – 2.56)/1K6 = 1.5mA].

If the reference is required to drive more than one ZN439 then the reference current can be increased e.g. an $R_{REF} = 470\Omega$ will supply a nominal reference current of (5 – 2.56)/0.47 = 5.2mA and this may be used to drive up to four ZN439's from just one internal reference. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively with $R_{REF} = 680\Omega$, the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

(b) External reference

If required an external reference in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN439 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN439 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

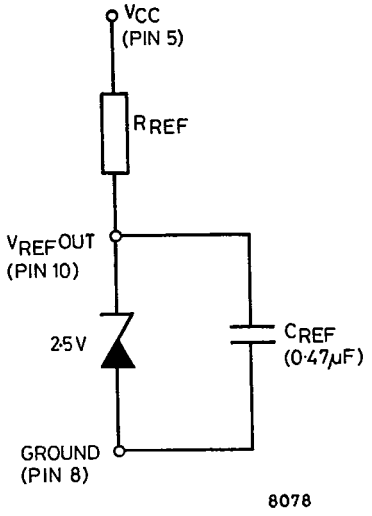

Fig. 14 Internal voltage reference

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COMPARATOR

The ZN439 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 15. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150μA and need not be well stablised it can be supplied by a simple diode pump circuit driven from the R_{CK} pin (pin 22).

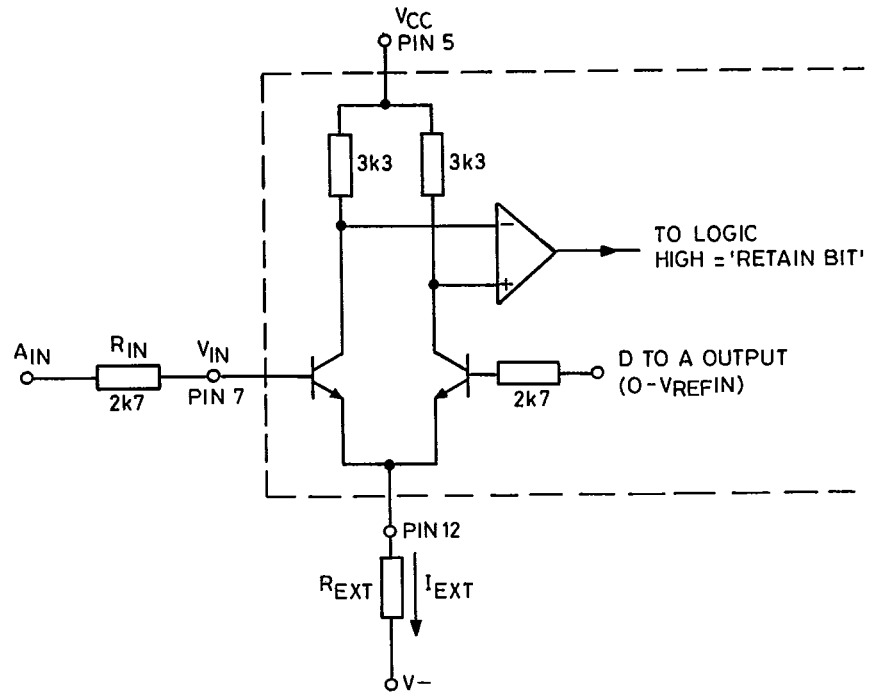

Fig. 15 Comparator equivalent circuit

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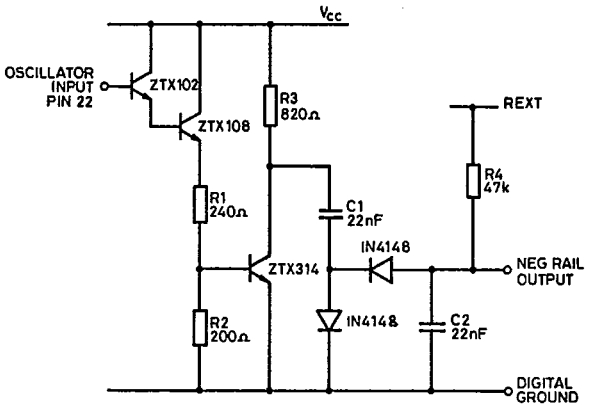

Fig. 16 Diode pump circuit

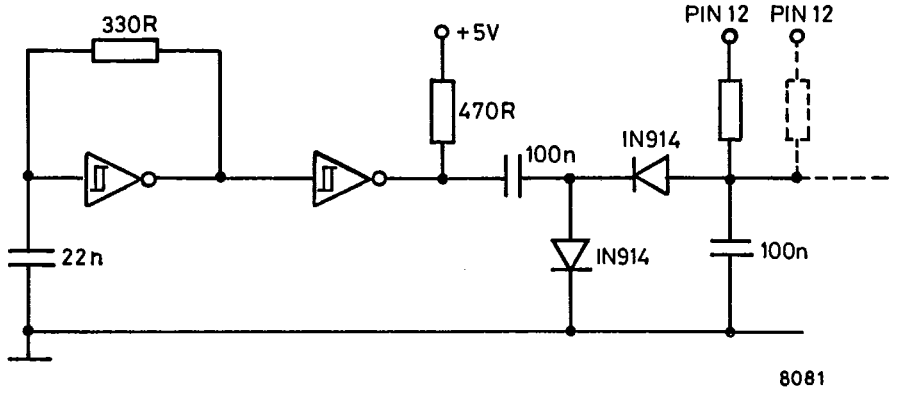

Fig. 17 Diode pump circuit to supply comparator tail current for up to five ZN439's

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A suitable circuit is shown in Fig. 16. This circuit can be used in any converter operation mode. The diode pump circuit shown in Fig. 16 is driven by the on-chip clock (pin 22) and applies a voltage of about −3V to R4, thus providing the tail current for the comparator.

Where several ZN439's are used in a system the self-oscillating diode pump circuit of Fig. 17 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistors for different supply voltages is given in Table 1.

Table 1

V_- (volts)	R_{EXT} (kΩ)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 18. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally by removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

The D-A output range can be considered to be $0 - V_{REF\ IN}$ through an output resistance R(2k7).

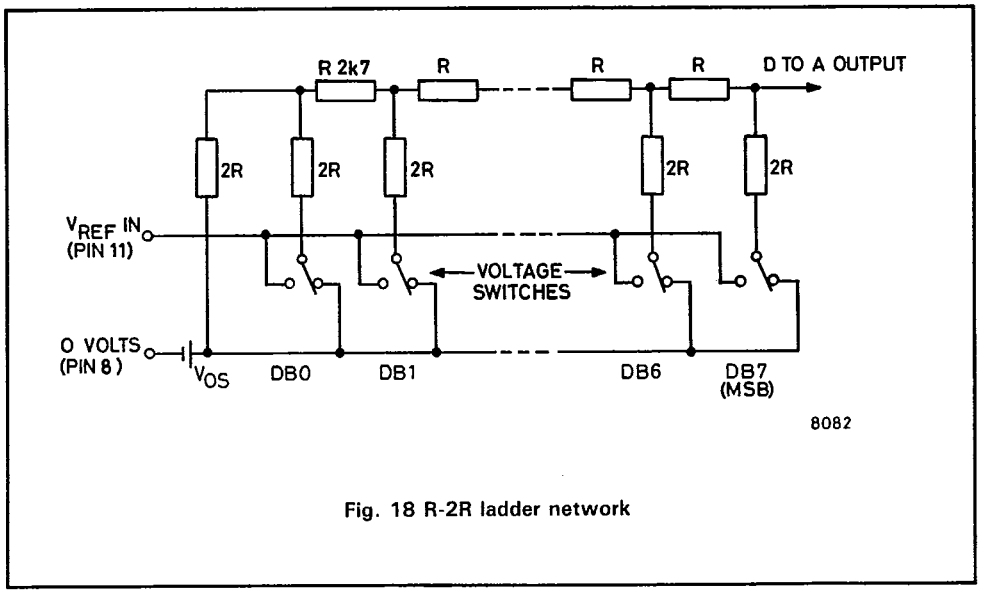

Fig. 18 R-2R ladder network

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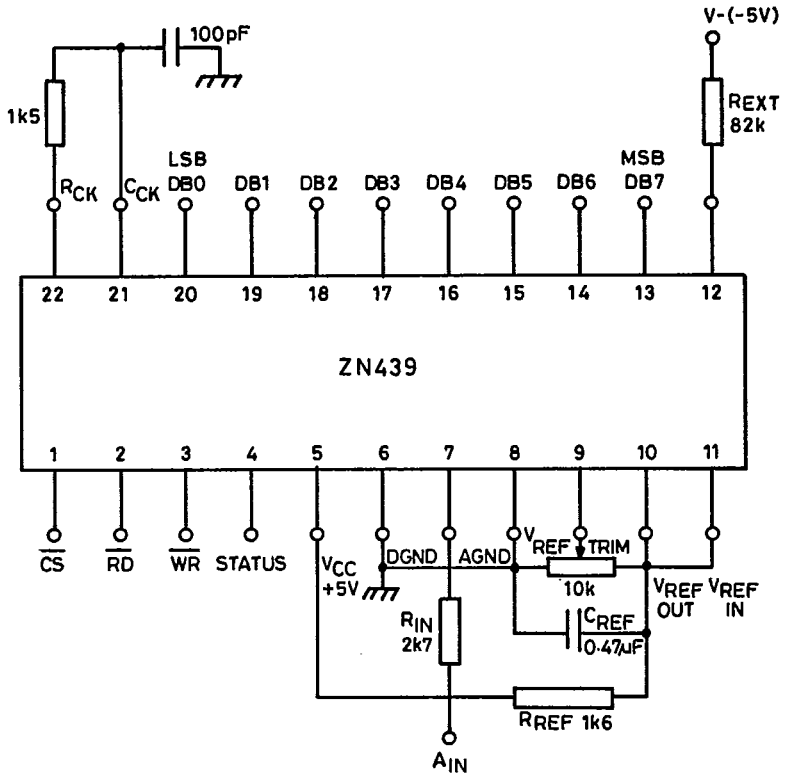
ANALOGUE INPUT RANGES

The basic connection of the ZN439 shown in Fig. 19 has an analogue input range 0 to $V_{REF\,IN}$ which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input ranges so that the comparator always sees a positive input voltage.



Nominal A_{IN} range = 0 to $V_{REF\,IN}$

Fig. 19 External components for basic operation

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UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 20.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the analogue input (A_{IN}) is at full-scale.

The resulting full-scale range is given by: $A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right)$, $V_{REF\ IN} = G.V_{REF\ IN}$.

To match the ladder resistance R_1/R_2 (R_{IN}) = 2.7k.

The required nominal values of R_1 and R_2 are given by $R_1 = 2.7Gk$, $R_2 = \frac{2.7G}{G-1}$ k

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Input range	G	R_1	R_2
+5V	2	5.4k	5.4k
+10V	4	10.8k	3.6k

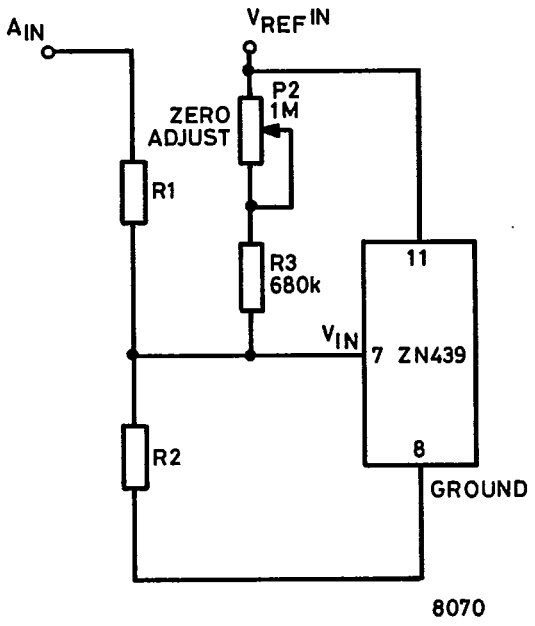

Fig. 20 General unipolar input connections

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GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

ZERO ADJUSTMENT

Zero adjustment must be provided to set the zero transition to the value of +½LSB. This is achieved by applying an adjustable positive offset to tie the comparator input via P2 and R_3. The values shown are suitable for all input ranges greater than 1½ times $V_{REF\ IN}$.

Practical circuits values for +5 and +10V input ranges are given in Fig. 21 which incorporates both zero and gain adjustments.

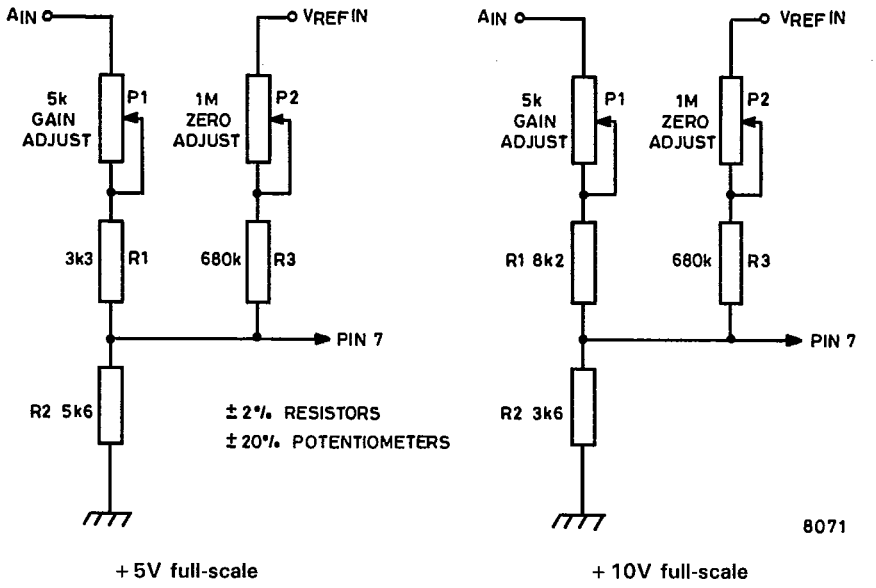

Fig. 21 Unipolar operation component values

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UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{WR}$ pulses at intervals long enough to allow a complete conversion or hold $\overline{WR}$ low and monitor the digital outputs.

OFFSET SETTING

(ii) Apply ½LSB to A_{IN} and adjust zero until DB0 (LSB) just flickers between 0 and 1 with all other bits at 0.

i.e. for transition 00000000 to 00000001.

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GAIN SETTING

(iii) Apply full-scale minus 1.½LSB to A_{IN} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. for transition 11111111 to 11111110.

UNIPOLAR SETTING-UP POINTS

Input range, +FS	½LSB	FS - 1½LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
¾FS	11000000
½ FS + 1LSB	10000001
½FS	10000000
½FS - 1LSB	01111111
¼FS	01000000
1LSB	00000001
0	00000000

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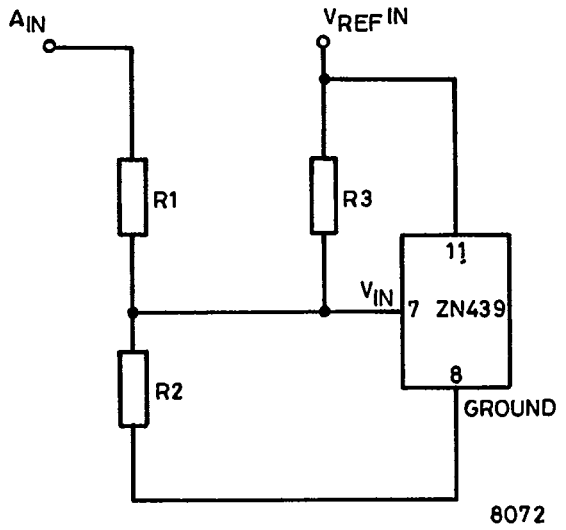

Fig. 22 Basic bipolar input connection

BIPOLAR OPERATION

For bipolar operation the input to the ZN439 is offset by half full-scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 22).

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full-scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ $(= R_{IN}) = 2.7k$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 5.4Gk$, $R_2 = 5.4G/(G - 1)k$, $R_3 = 5.4k$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 5.4k$ and $R_2 = \infty$.

Assuming the $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ± 5 and $\pm 10V$ input ranges are given in the following table.

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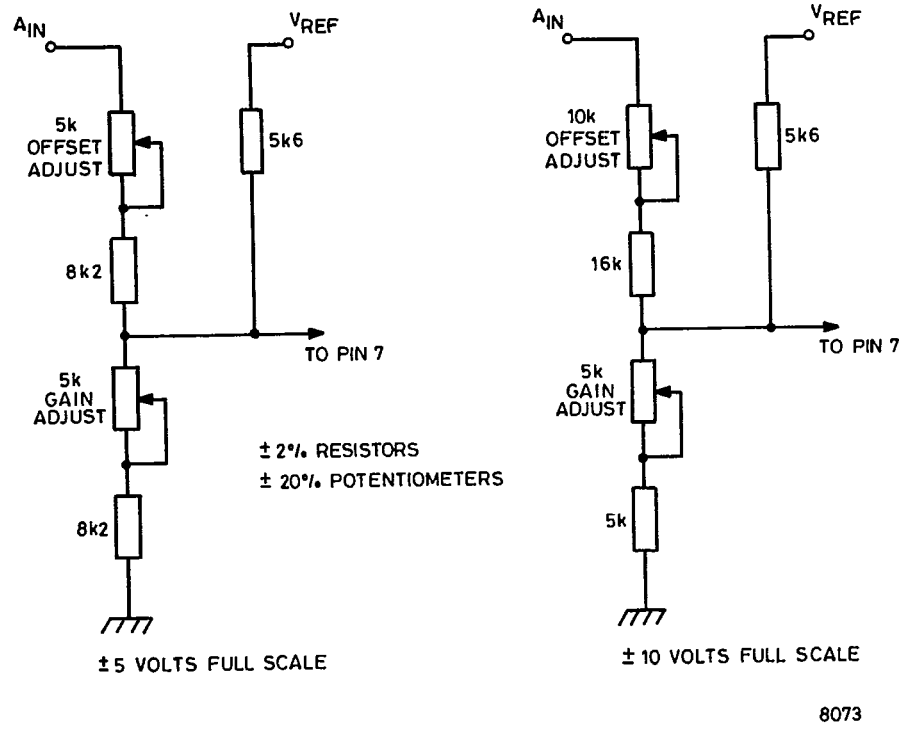

Fig. 23 Bipolar operation - component values

Input range	G	R_1	R_2	R_3
±5V	2	10.8k	10.8k	5.4k
±10V	4	21.6k	7.2k	5.4k

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1. Practical circuit realisations are given in Fig. 23.

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BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{WR}$ pulses at intervals long enough to allow a complete conversion or hold $\overline{WR}$ low and monitor the digital outputs.

OFFSET SETTING

(ii) Apply −(FS - ½LSB) to A_{IN} and adjust offset until the DB0 (LSB) output just flickers between 0 and 1 with all other bits at 0.

i.e. for transition 00000000 to 00000001.

GAIN SETTING

(iii) Apply +(FS - 1½LSB) to A_{IN} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. for transition 11111111 to 11111110.

BIPOLAR SETTING-UP POINTS

Input range, ±FS	−(FS − ½LSB)	+(FS − 1½LSB)
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

$$1LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Digital output code MSB LSB
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
+½FS	11000000
+1LSB	10000001
0	10000000
−1LSB	01111111
−½FS	01000000
−(FS - 1LSB)	00000001
−FS	00000000

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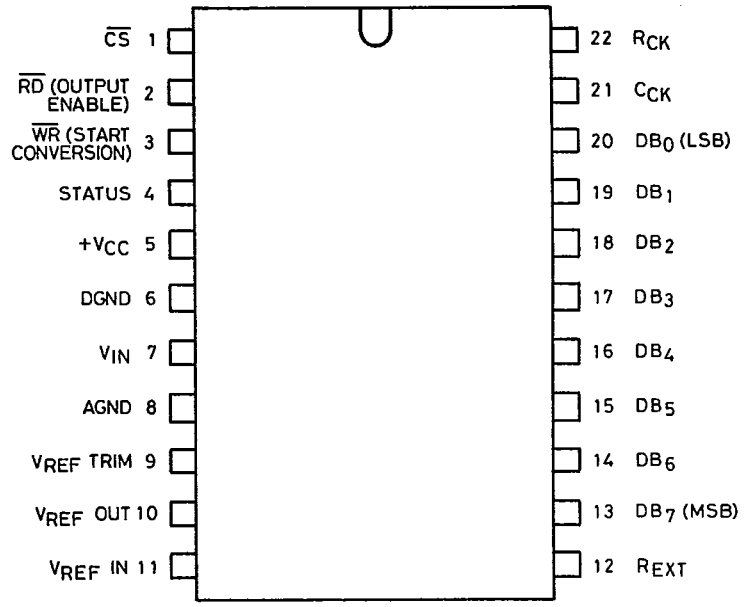
PIN CONNECTIONS



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ORDERING INFORMATION

Type	Linearity error (LSB)	Operating temperature range	Package
ZN439E-9	¼	0°C to +70°C	Moulded
ZN439J-9	¼	−55°C to +125°C	Ceramic
ZN439E-8	½	0°C to +70°C	Moulded
ZN439J-8	½	−55°C to +125°C	Ceramic
ZN439E-7	1	0°C to +70°C	Moulded
ZN439J-7	1	−55°C to +125°C	Ceramic