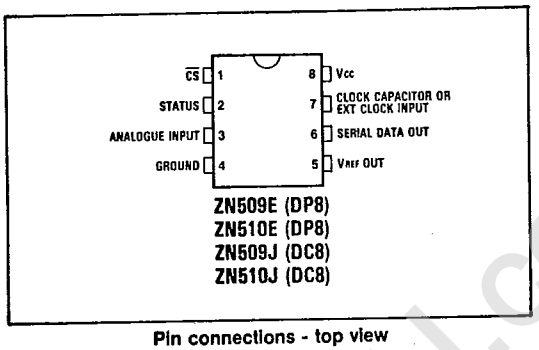
PLESSEY
Semiconductors

T-51-10-08

ZN509/ZN510

8-BIT SERIAL A-D CONVERTER

The ZN509 and ZN510 are 8-bit serial output, successive approximation, A-D converters. Included on-chip is a clock generator which can be overdriven by an external clock, a 2.5V bandgap reference and 3-state output buffers. The devices operate from a single +5V supply and are economically packaged in an 8-pin DIL. Chip select determines the start of conversion, the conversion mode - either 'continuous' or 'single-shot' - and the 3-state control.



ZN509E (DP8)
ZN510E (DP8)
ZN509J (DC8)
ZN510J (DC8)

Pin connections - top view

FEATURES

- ½ or 1 LSB Linearity
- 8 microseconds Conversion Time
- Serial Data Output - Suitable for Remote Operation
- Easy Microprocessor Interfacing
- Equally suitable for 'Stand-Alone' Applications
- Operates from a Single +5V Supply
- On-Chip Bandgap Reference
- TTL and CMOS Compatible
- Commercial or Military Temperature Ranges

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs, A_{IN}	V_{CC}, −0.5V
Operating temperature range	
ZN509E, ZN510E	0°C to +70°C
ZN509J, ZN510J	−55°C to +125°C
Storage temperature range	−55°C to +125°C

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN509E	½	0°C to +70°C	DP8
ZN509J	½	−55°C to +125°C	DC8
ZN510E	1	0°C to +70°C	DP8
ZN510J	1	−55°C to +125°C	DC8

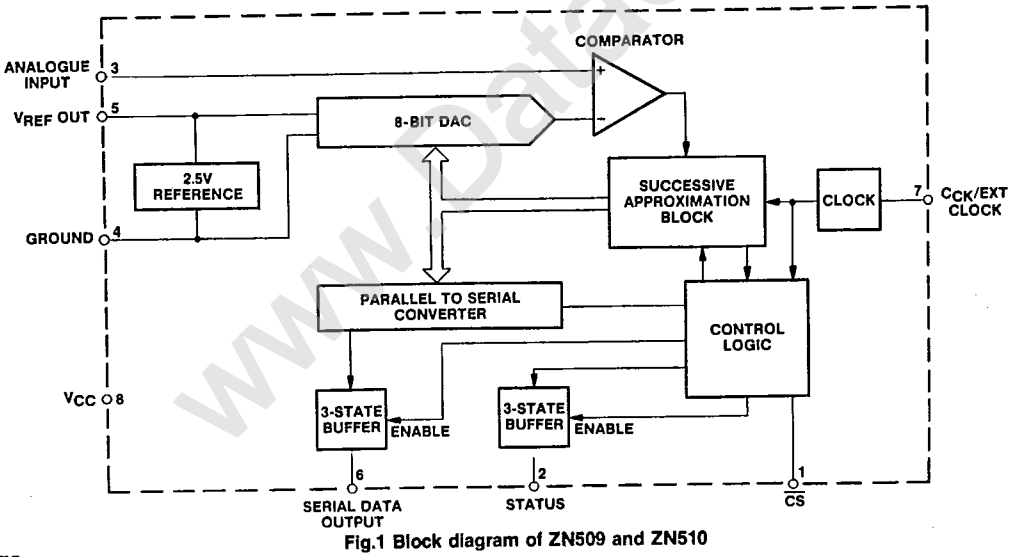


Fig.1 Block diagram of ZN509 and ZN510

ELECTRICAL CHARACTERISTICS (at $V_{CC} = 5V$, $T_{amb} = 25°C$ and $f_{CLK} = 1.0MHz$ unless otherwise specified).

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Parameter	$T_{amb} = +25°C$			Over specified temp. range		Unit	Conditions
	Min.	Typ.	Max.	Min.	Max.		
ZN509							
Linearity error	–	–	±0.5	–	±0.5	LSB	
Differential linearity error	–	–	±0.75	–	±0.75	LSB	
ZN510							
Linearity error	–	–	±1	–	±1	LSB	
Differential linearity error	–	–	±1	–	±1	LSB	
ALL TYPES							
Zero transition	–	15	–	–	–	mV	ZN509/10E
(00000000→00000001)	–	15	–	–	–	mV	ZN509/10J
Full-scale transition	–	2.540	–	–	–	V	ZN509/10E
(11111110→11111111)	–	2.540	–	–	–	V	ZN509/10J
Linearity temperature coefficient		±3 typ.				ppm/°C	
Differential linearity temperature coefficient		±6typ.				ppm/°C	
Gain temperature coefficient		±10 typ.				ppm/°C	
Offset temperature coefficient		±7 typ.				ppm/°C	
Resolution	8	–	–	–	–	Bits	
Conversion time	8	–	–	–	–	μs	
Supply rejection	–	0.2	–	–	–	%/V	
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current	–	29	40	–	–	mA	
Power consumption	–	145	200	–	–	mW	
Ladder output impedance	–	3	–	–	–	kΩ	
COMPARATOR							
Analogue input current	–	230	–	–	–	μA	
Analogue input resistance	–	13	–	–	–	kΩ	
Analogue input voltage	−0.5	–	+3.5	−0.5	+3.5	V	

ELECTRICAL CHARACTERISTICS Cont.

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Parameter	$T_{amb} = +25°C$			Over specified temp. range		Unit	Conditions
	Min.	Typ.	Max.	Min.	Max.		
INTERNAL VOLTAGE REFERENCE							
Output voltage	–	2.535	–	–	–	V	
Output voltage tolerance	–	–	±3	–	–	%	
Slope impedance	–	0.75	2	–	–	Ω	
Reference current	0.75	–	5.2	0.75	5.2	mA	
Output voltage temperature coefficient	–	70	–	–	–	ppm/°C	
CLOCK							
Maximum on-chip clock frequency	–	1.0	–	–	–	MHz	$C_{ck} = 220pF$
Clock frequency tempco	–	–0.125	–	–	–	%/°C	
Clock capacitor	220	–	–	–	–	pF	
Maximum external clock frequency	1.0	–	–	1.0	–	MHz	
Clock pulse width	250	–	–	–	–	ns	
High level I/P voltage V_{IH}	3.5	–	–	3.5	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	850	–	–	–	μA	$V_{CC} = 5.5V$ $V_{IN} = 4V$
Low level I/P current I_{IL}	–	–880	–	–	–		$V_{CC} = 5.5V$ $V_{IN} = 0.8V$
Supply rejection	–	3.0	–	–	–	%/V	
LOGIC $\overline{CS}$ INPUT							
High level I/P voltage V_{IH}	2.4	–	–	2.4	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	250	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$
High level I/P current I_{IH}	–	120	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	–350	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
DATA AND STATUS OUTPUTS							
High level output voltage V_{OH}	2.4	–	–	2.4	–	V	$I_{OH\ MAX}$
Low level output voltage V_{OL}	–	–	0.4	–	0.4	V	$I_{OL\ MAX}$
High level output current I_{OH}	–	–	–800	–	–	μA	
Low level output current I_{OL}	–	–	2	–	–	mA	
Three-state disable output leakage current			2		10	μA	

ELECTRICAL CHARACTERISTICS Cont.

Parameter	T_{amb} = +25°C			Over specified temp. range		Unit	Conditions
	Min.	Typ.	Max.	Min.	Max.		
CONTINUOUS CONVERSION							
Data output							
Delay times T_{EO}	–	100	125	–	150	ns	
T_{CD}	–	265	310	–	390	ns	
Status output							
Delay times T_{E1}	–	250	300	–	430	ns	
T_{SO}	–	165	210	–	260	ns	
T_{SI}	–	220	270	–	370	ns	
SINGLE SHOT OPERATION							
Data output							
Delay times T_{EO}	–	100	125	–	150	ns	
T_{DO}	–	200	260	–	310	ns	
T_{DI}	–	200	260	–	310	ns	
T_{CD}	–	265	310	–	390	ns	
Status output							
Delay times T_{E1}	–	250	300	–	430	ns	
T_{SO}	–	220	270	–	300	ns	
T_{SI}	–	230	280	–	320	ns	
T_{DSI}	–	250	300	–	360	ns	

GENERAL CIRCUIT OPERATION

The ZN509/10 uses the successive approximation technique to produce an 8-bit serial digital output. At the beginning of the conversion sequence the DAC input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. If the analogue input is larger the MSB is left in circuit, if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all 8-bits have been compared.

CONVERSION TIMING

The ZN509/10 will accept a low going chip select ($\overline{CS}$) pulse, which can be completely asynchronous with respect to the clock; this pulse enables the 3-state output buffers and starts the conversion. Valid serial data will be produced between one and two clock periods later depending on the relative timing of the clock and $\overline{CS}$ signals (see Fig. 3 & 4).

Upon receipt of a low going $\overline{CS}$ pulse the ZN509/10 is cleared i.e. the MSB and STATUS are set to one and all other bits reset to zero. The $\overline{CS}$ pulse can be as short as 150ns and if pulsed low during a conversion the device will be cleared and the conversion will restart. Holding the $\overline{CS}$ input low will not inhibit the operation of the device.

The STATUS produces two different types of output which is dependent upon whether the device is being operated in the single shot or continuous mode.

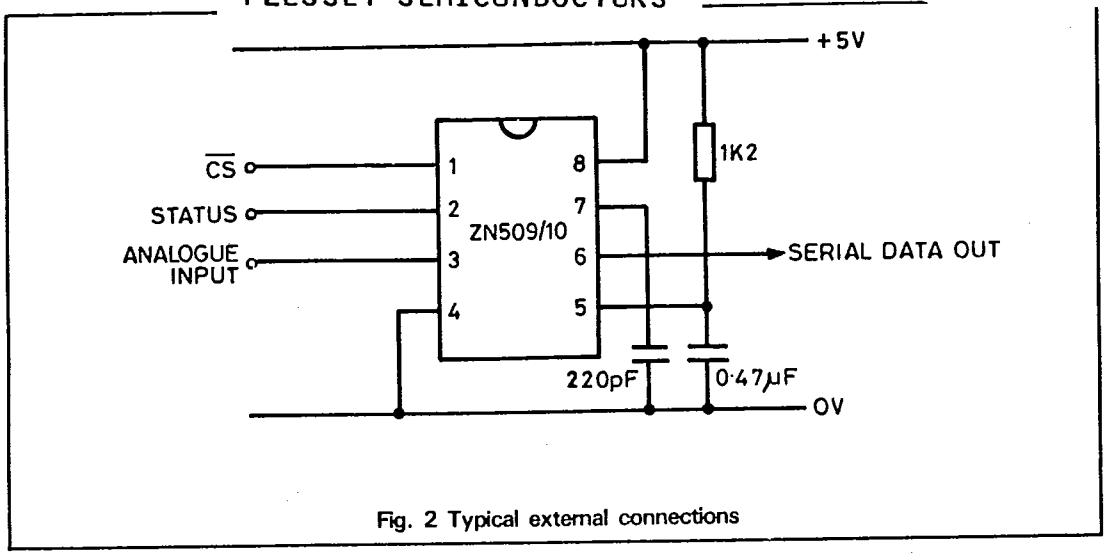

Fig. 2 Typical external connections

CONTINUOUS MODE OF OPERATION

The ZN509/10 can be made to cycle by simply tying the $\overline{CS}$ input low see Fig. 3 for timing diagram. It should be noted that after power up, valid data will only be available after the voltage reference has stabilised. This time is dependent upon the reference decoupling capacitor and load resistor, but is typically 2ms for a 1K6 resistor and a 0.47μF capacitor.

The synchronising status output goes low for one clock period every eight clock periods and coincides with the MSB data output.

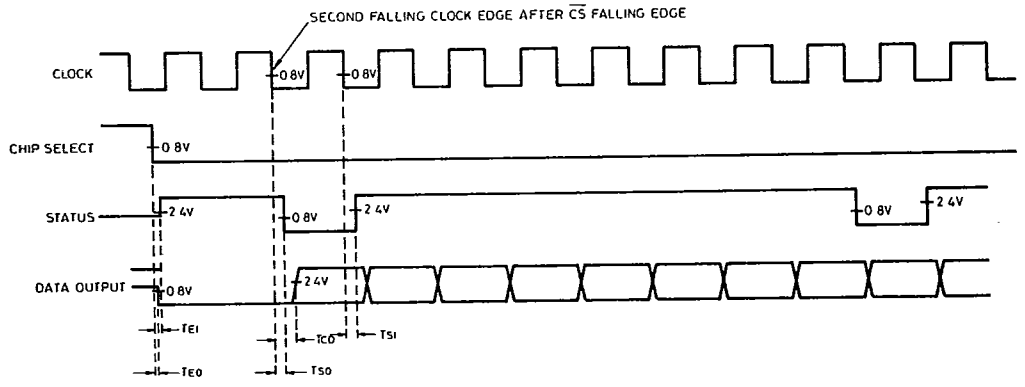

Fig. 3 Continuous (cycling) operation

SINGLE SHOT OPERATION

The ZN509/10 recognises that a single shot operation is to be performed if a $\overline{CS}$ pulse of greater than 150ns, but no longer than one clock period in length is applied. Once this pulse is applied, both the Status and Data outputs come out of 3-state, the Status going high and the data output low. Between one and two clock periods later valid data, MSB first, will appear on the data output (the status goes low to indicate when the valid data is available). When all 8 bits of data have appeared, the data output returns into a high impedance state, at which point the status goes high. One clock period later the Status output also returns to a high impedance state.

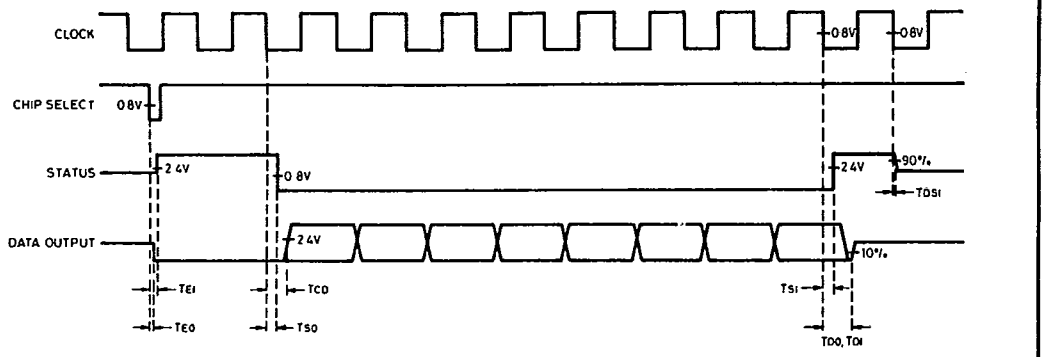

Fig. 4 Single shot operation

DIGITAL OUTPUTS

The digital outputs are provided with 3-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 5. When disabled (see timing diagrams for the conditions under which this applies) both output transistors are turned off and the device presents a high impedance load to the bus. When enabled the outputs will assume the logic states present on the input to the buffer.

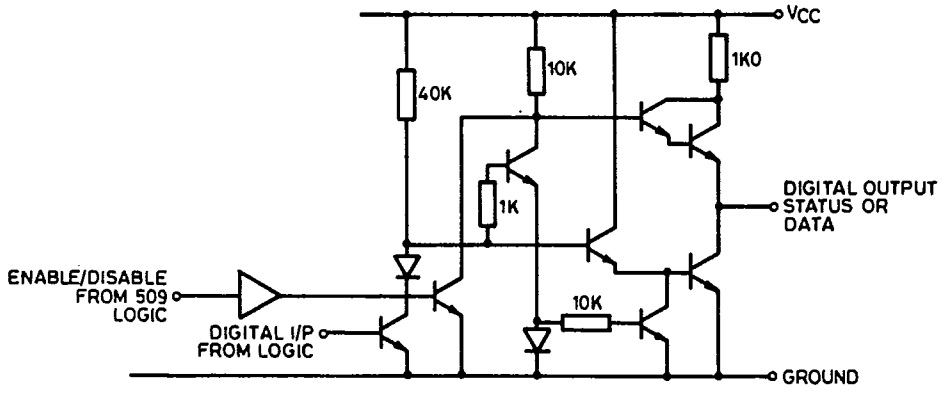

Fig. 5 Digital outputs

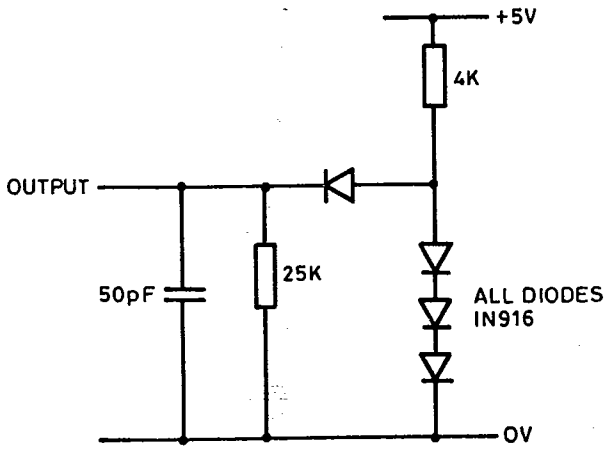

Fig. 6 Output load circuit

ON – CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 7 and ground as shown in Fig. 7(a). A graph of typical oscillator frequency versus capacitance is given in Fig. 8a. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Fig. 7(b). A graph of typical oscillator frequency versus resistance and capacitance is given in Fig. 8b. The oscillator input may be overdriven with an external clock signal from a TTL or CMOS gate as shown in Fig. 7(c).

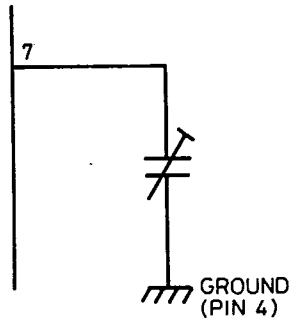

Fig. 7(a) Fixed/variable capacitor

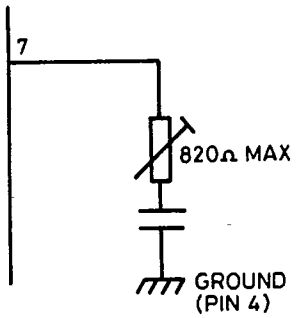

Fig. 7(b) Fixed capacitor and variable resistor

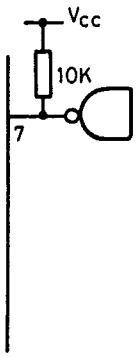

Fig. 7(c) External TTL or CMOS drive

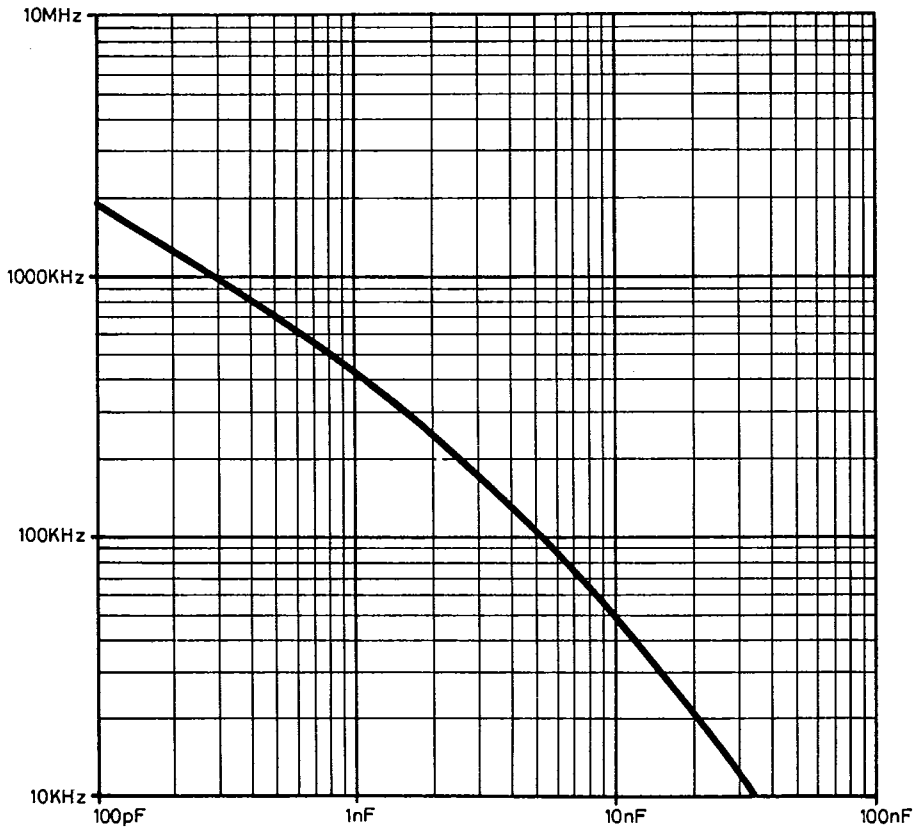

Fig. 8a Clock frequency v capacitance

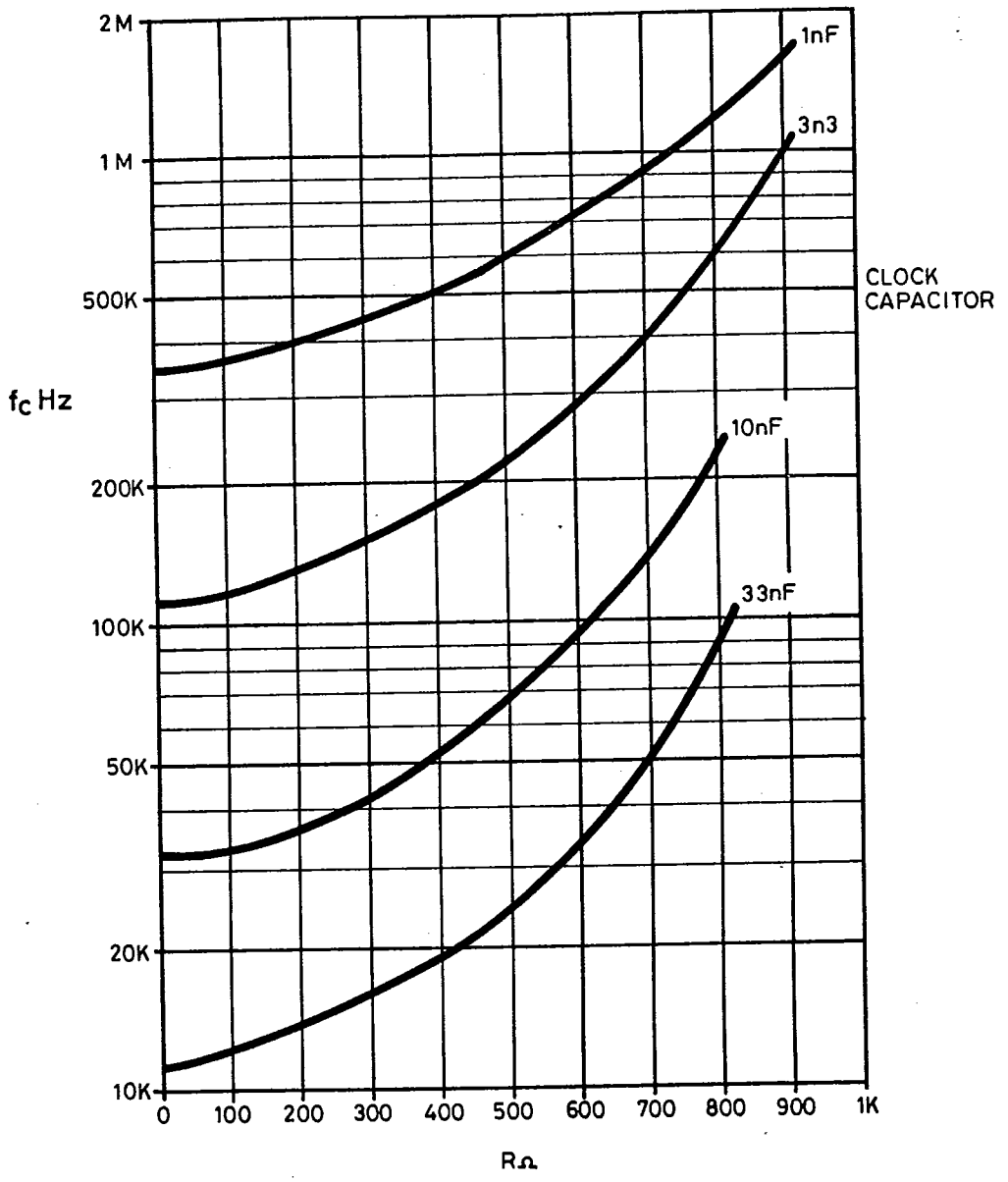

Fig. 8b Clock frequency v resistance and capacitance

ANALOGUE CIRCUITS

Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 9). A resistor (R_{ref}) should be connected between V_{CC} and $V_{REF\ OUT}$, and a decoupling capacitor, C_{REF} (0.47μF), is required between $V_{REF\ OUT}$ and GND.

A suitable current to drive a ZN509/10 is nominally 2mA and will be supplied by an R_{REF} of 1K2 [(5-2.535)/1K2 $\simeq$ 2mA].

With $R_{REF} = 620\Omega$, the ZN509/10 reference may also be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

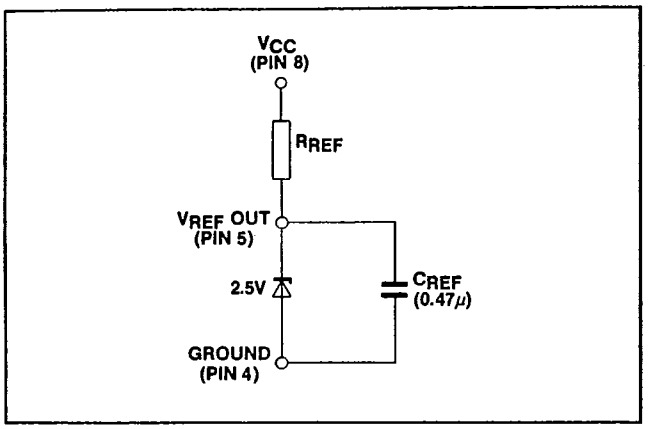

Fig. 9 Internal voltage reference

Analogue input

The equivalent analogue input is shown in Fig. 10.

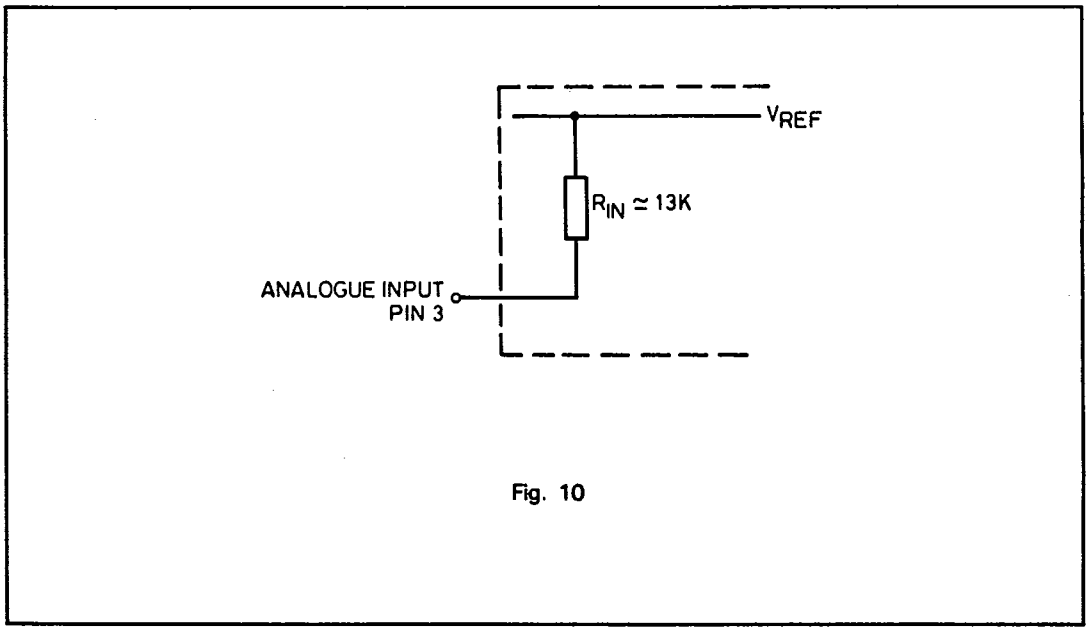

Fig. 10

D–A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 11. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

$$\text{D–A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

Where n is the digital input to the D–A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

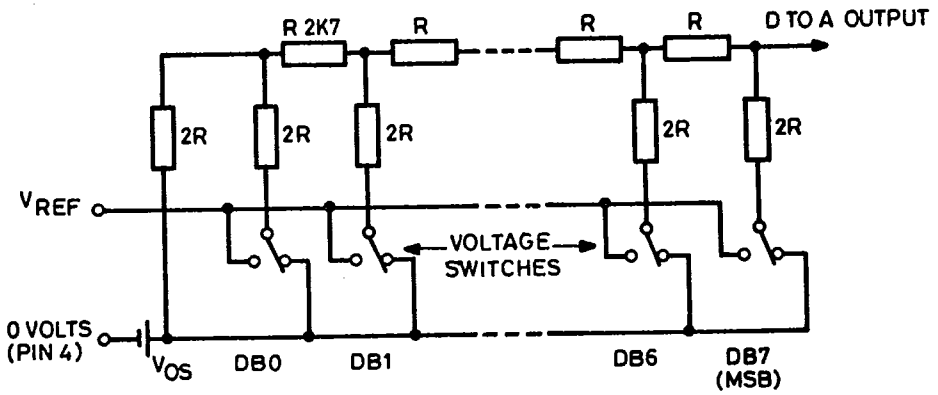

Fig. 11 R-2R ladder network