3A, 24V Asynchronous Step-Down DC/DC Converter

DESCRIPTION

The ZT1525 is a constant frequency peak current-mode step-down switching regulator. The range of input voltage is from 4V to 24V. The output current is up to 3A.

The switching frequency of the ZT1525 is programmable up to 2.5MHz, to achieve high input/output conversion ratio, and allowing the use of small inductors and ceramic capacitors for miniaturization.

Peak current mode PWM control of the ZT1525 provides fast transient response with simple loop compensation. Cycle-by-cycle current limiting and hiccup overload protection reduces power dissipation during output overload. Soft-start function reduces input start up current and prevents the output from overshooting during power up.

The ZT1525 is available in the SOP-8L package, and it is RoHS compliant and 100% lead (Pb) free.

FEATURES

- 4V to 24V input voltage
- Output current up to 3A
- 200kHz to 2.5MHz programmable frequency
- Precision 1V feedback voltage
- Peak current mode control
- Cycle-by-cycle current limiting
- Hiccup overload protection with frequency foldback
- Soft-start and enable
- Thermal shutdown
- RoHS Compliant and 100% Lead (Pb) Free

APPLICATIONS

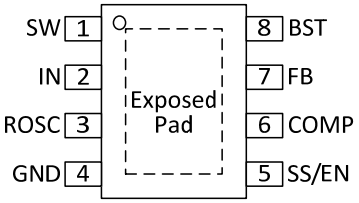
- XDSL and cable modems
- Set top boxes
- Point of load applications
- CPE equipment
- DSP power supplies
- LCD and plasma TVs

ORDERING INFORMATION

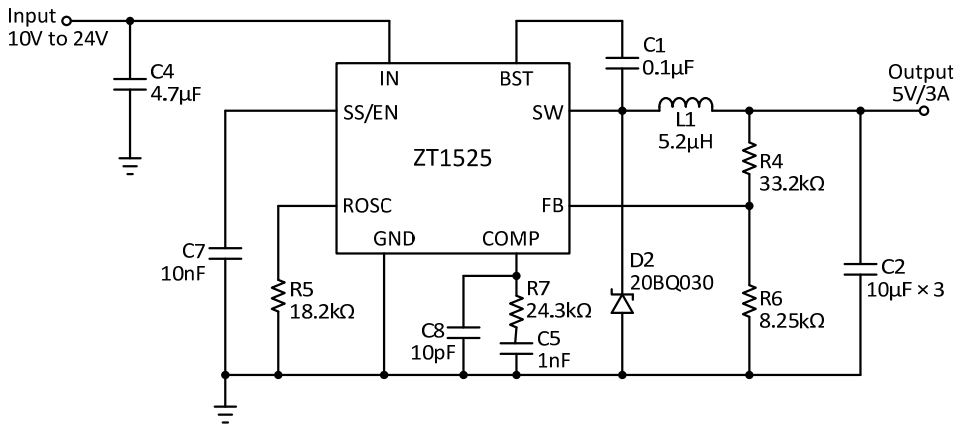
PART	PACKAGE	RoHS	Ship, Quantity
ZT1525S	SOP-8L(EP)	Yes	Tape and Reel

Pins Configuration

Top View



Typical Application Circuit



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Absolute Maximum Ratings

Supply Voltage V_{IN} ..... –0.3V to +28V
BST Voltage ..... V_{SW}–0.3V to V_{SW}+6V
SS Voltage ..... –0.3V to +3V
FB Voltage ..... –0.3V to +6V
SW Voltage ..... –0.6V to V_{IN}
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

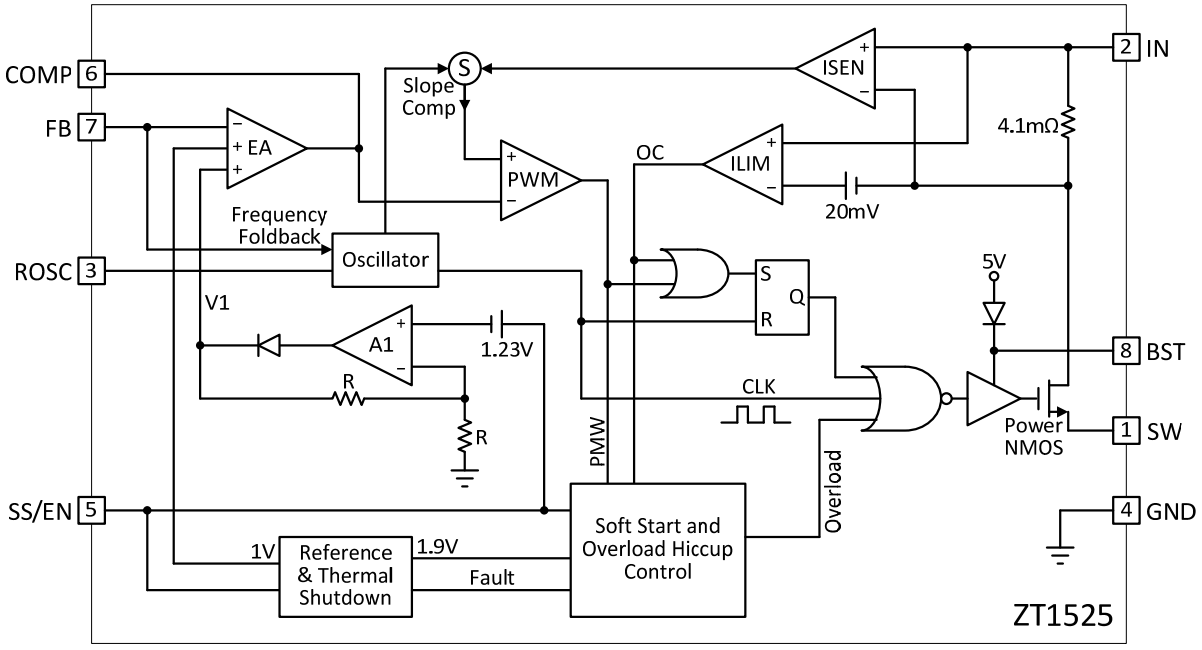
Package Thermal Characteristics

Thermal Resistance, θ_{JA} ..... 50°C/W
Thermal Resistance, θ_{JC} ..... 10°C/W

Pins Description

Pin	Symbol	Description
1	SW	Power switching output.
2	IN	Power input.
3	ROSC	Oscillator frequency setting.
4	GND	Ground.
5	SS/EN	Soft-start and enable input.
6	COMP	Internal error amplifier output.
7	FB	Feedback input.
8	BST	Gate drive boost input.
---	Exposed pad	To be soldered to ground to promote thermal performance.

Functional Block Diagram



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Electrical Specifications

(V_{IN} = +12V, V_{SS} = +2.2V, −40°C < T_A < +85°C, R_{OSC} = 12.1kΩ, unless otherwise noted.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply					
Input Voltage Range		4		24	V
V_{IN} Start Voltage	V_{IN} rising	2.70	2.82	2.95	V
V_{IN} Start Hysteresis			225		mV
V_{IN} Quiescent Current	V_{COMP} = 0V (Not switching)		2	2.6	mA
V_{IN} Quiescent Current in Shutdown	$V_{SS/EN}$ = 0V, V_{IN} = 12V		40	50	µA
Error Amplifier					
Feedback Voltage		0.980	1.000	1.020	V
Feedback Voltage Line regulation	V_{IN} = 4V to 24V		0.005		%/V
FB Pin Input Bias Current	V_{FB} = 1V, V_{COMP} = 0.8V		−170	−340	nA
Error Amplifier Transconductance			280		$\mu\Omega^{-1}$
Error Amplifier Open-Loop gain			60		dB
COMP Pin to Switch Current Gain			12		A/V
COMP Maximum Voltage	V_{FB} = 0.9V		2.35		V
COMP Source Current	V_{FB} = 0.8V, V_{COMP} = 0.8V		17		µA
COMP Sink Current	V_{FB} = 1.2V, V_{COMP} = 0.8V		25		µA
Internal Power Switch					
Switch Current Limit		3.9	5.1	6.6	A
Switch-On Resistance $R_{DS(ON)}$	(Note)		85		mΩ
Minimum Switch On-Time			150		ns
Minimum Switch Off-Time			100	150	ns
Switch Leakage Current				10	µA
Oscillator					
Switching Frequency	R_{OSC} = 12.1kΩ	1.04	1.3	1.56	MHz
	R_{OSC} = 93.1kΩ	240	300	360	kHz
Foldback Frequency	R_{OSC} = 12.1kΩ, V_{FB} = 0V	110	230	350	kHz
	R_{OSC} = 93.1kΩ, V_{FB} = 0V	50	110	170	kHz
Soft-start and Overload Protection					
SS/EN Shutdown Threshold		0.2	0.3	0.4	V
SS/EN Switching Threshold	V_{FB} = 0V	1.0	1.13	1.3	V
Soft-start Charging Current	$V_{SS/EN}$ = 0V		1.7		µA
	$V_{SS/EN}$ = 1.5V	1.2	2.0	2.8	µA
Soft-start Discharging Current			1.5		µA
Hiccup Arming SS/EN Voltage	$V_{SS/EN}$ rising		2.15		V
Hiccup SS/EN Overload Threshold	$V_{SS/EN}$ falling		1.9		V
Hiccup Retry SS/EN Voltage	$V_{SS/EN}$ falling	0.6	1.0	1.2	V
Over Temperature Protection					
Thermal Shutdown Temperature			150		°C
Thermal Shutdown Hysteresis			10		°C

Note: Guaranteed by design, not tested.

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APPLICATIONS INFORMATION

Overview

The ZT1525 is a constant-frequency, peak current-mode, step-down switching regulator with an integrated power NMOS transistor. Programmable switching frequency makes the regulator design more flexible. With the peak current-mode control, the double reactive poles of the output LC filter are reduced to a single real pole by the inner current loop. This simplifies loop compensation and achieves fast transient response with a simple Type-2 compensation network.

As shown in Functional Block Diagram, the switch drain current is sensed with an integrated 4.1mΩ sense resistor. The sensed current is summed with a slope-compensating ramp before it is compared with the transconductance error amplifier (EA) output. The PWM comparator trip point determines the switch turn-on pulse width. The current-limit comparator ILIM turns off the power switch when the sensed signal exceeds the 20mV current-limit threshold.

Driving the base of the power transistor above the input power supply rail minimizes the power transistor saturation voltage and maximizes efficiency. An external bootstrap circuit (formed by the capacitor C1 and the diode D1 in Typical Application Circuit) generates such a voltage at the BST pin for driving the power transistor.

Pins Description

SW: Connect this pin to the inductor, the freewheeling diode and the boostrap capacitor.

IN: Power supply to the regulator. It is also the drain of the internal power NMOS transistor. It must be closely by-passed to the ground plane.

ROSC: An external resistor from this pin to ground sets the oscillator frequency.

GND: Ground.

SS/EN: Soft-start and regulator enable pin. A capacitor from this pin to ground provides soft-start and overload hiccup functions. Hiccup can be disabled by overcoming the internal soft-start discharging current with an external pull up resistor connected between the SS/EN and the IN pins. Pulling the SS/EN pin below 0.2V completely shuts off the regulator to low current state.

COMP: The output of the internal error amplifier. The voltage at this pin controls the peak switch current. A RC compensation network at this pin stabilizes the regulator.

FB: The inverting input of the error amplifier. If V_{FB} falls below 0.8V, then the switching frequency will be reduced to improve short circuit robustness.

BST: Supply pin to the power transistor driver. Tie to an external diode-capacitor bootstrap circuit to generate drive voltage higher than V_{IN} in order to fully enhance the internal power NMOS transistor.

Exposed Pad: The exposed pad serves as a thermal contact to the circuit board. It is to be soldered to the ground plane of the PC board.

Shutdown and Soft-Start

The SS/EN pin is a multiple-function pin. An external capacitor (4.7nF to 22nF) connected from the SS pin to ground sets the soft-start and overload shutoff times of the regulator (Figure 1). The effect of $V_{SS/EN}$ on the ZT1525 is summarized in Table 1.

Pulling the SS/EN pin below 0.2V shuts off the regulator and reduces the input supply current to 18μA (V_{IN} = 5V). When the SS/EN pin is released, the soft-start capacitor is charged with an internal 1.6μA current source (not shown in Figure 1). As the SS/EN voltage exceeds 0.4V, the internal bias circuit of the ZT1525 turns on and the ZT1525 draws 2mA from V_{IN}. The 1.6μA charging current turns off and the 2μA current source I_C in Figure 1 slowly charges the soft-start capacitor.

The error amplifier EA in Functional Block Diagram has two non-inverting inputs. The non-inverting input with the lower voltage predominates. One of the non-inverting inputs is biased to a precision 1V reference and the other non-inverting input is tied to the output of the amplifier A1. Amplifier A1 produces an output $V_1 = 2 \times (V_{SS/EN} - 1.23V)$. V_1 is zero and COMP is forced low when $V_{SS/EN}$ is below 1.23V. During start up, the effective non-inverting input of EA stays at zero until the soft-start capacitor is charged above 1.23V. Once $V_{SS/EN}$ exceeds 1.23V, COMP is released. The regulator starts to switch when V_{COMP} rises above 0.4V. If the

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soft-start interval is made sufficiently long, then the FB voltage (hence the output voltage) will track V_1 during start up. $V_{SS/EN}$ must be at least 1.83V for the output to achieve regulation. Proper soft-start prevents output overshoot. Current drawn from the input supply is also well controlled.

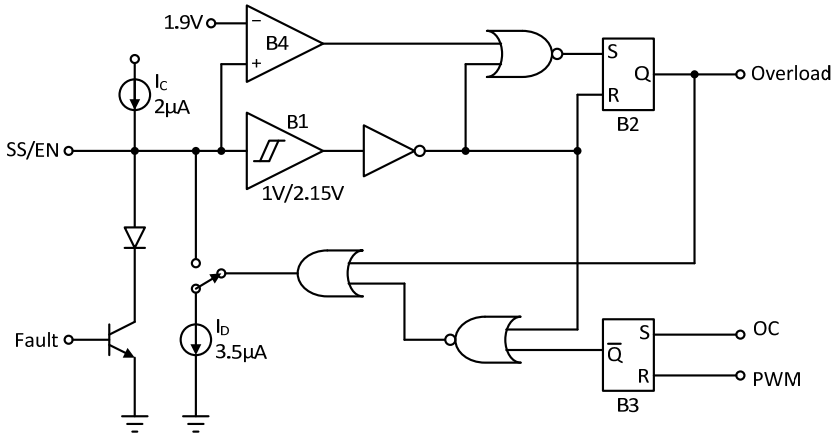

Figure 1: Soft-start and overload hiccup control circuit.

SS/EN	Mode	Supply Current
< 0.2V	Shutdown	18µA @ V_{IN} = 5V
0.4V to 1.23V	Not switching	2mA
1.23V to 2.1V	Switching & hiccup disabled	Load dependent
> 2.1V	Switching & hiccup armed	

Table 1: SS/EN operation modes.

Condition	Fault	Protective Action
$I_L > I_{Limit}$, $V_{FB} > 0.8V$	Over current	Cycle-by-cycle limit at programmed frequency
$I_L > I_{Limit}$, $V_{FB} < 0.8V$	Over current	Cycle-by-cycle limit with frequency foldback
$V_{SS/EN}$ falling & < 1.9V	Persistent over current or short circuit	Shutdown, then retry (Hiccup)
$T_j > 160°C$	Over temperature	Shutdown, then retry (Hiccup)

Table 2: Fault conditions and protections.

Overload / Short Circuit Protection

Table 2 lists various fault conditions and their corresponding protection schemes in the ZT1525.

As summarized in Table 1, overload shutdown is disabled during soft-start ($V_{SS/EN}$ < 2.1V). In Figure 1, the reset input of the overload latch B2 will remain high if the SS/EN voltage is below 2.1V. Once the soft-start capacitor is charged above 2.1V, the output of the Schmitt trigger B1 goes high, the reset input of B2 goes low and hiccup becomes armed.

As the load draws more current from the regulator, the current-limit comparator ILIM (Functional Block Diagram) will eventually limit the switch current on a cycle-by-cycle basis. The over-current signal OC goes high, setting the latch B3. The soft-start capacitor is discharged with (I_D − I_C) (Figure 1). If the inductor current falls below the current limit and the PWM comparator instead turns off the switch, then latch B3 will be reset and I_C will recharge the soft-start capacitor. If over-current condition persists or OC becomes asserted more often than PWM over a period of time, then the soft-start capacitor will be discharged below 1.9V. At this juncture, comparator B4 sets the overload latch B2. The soft-start capacitor will be continuously discharged with (I_D − I_C). The COMP pin is immediately pulled to ground. The switching regulator is shut off until the soft-start capacitor is discharged below 1.0V. At this moment, the overload latch is reset. The soft-start capacitor is recharged and the converter again undergoes soft-start. The regulator will go through

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soft-start, overload shutdown and restart until it is no longer overloaded.
If the FB voltage falls below 0.8V because of output overload, then the switching frequency will be reduced. Frequency foldback helps to limit the inductor current when the output is hard shorted to ground.
During normal operation, the soft-start capacitor is charged to 2.4V.

Setting the Output Voltage

The regulator output voltage, V_O, is set with an external resistive divider (Typical Application Circuit) with its center tap tied to the FB pin. For a given R6 value, R4 can be found by:

$$R4 = R6 \times (V_O/1.0V - 1) \quad \text{Eq. (1)}$$

Setting the Switching Frequency

The switching frequency of the ZT1525 is set with an external resistor from the ROSC pin to ground.

Minimum On Time Consideration

The operating duty cycle of a non-synchronous step-down switching regulator in continuous-conduction mode (CCM) is given by:

$$D = (V_O + V_D) / (V_{IN} + V_D - V_{CESAT}) \quad \text{Eq. (2)}$$

Where V_{IN} is the input voltage, V_{CESAT} is the switch saturation voltage, and V_D is voltage drop across the rectifying diode.
In peak current-mode control, the PWM modulating ramp is the sensed current ramp of the power switch. This current ramp is absent unless the switch is turned on. The intersection of this ramp with the output of the voltage feedback error amplifier determines the switch pulse width. The propagation delay time required to immediately turn off the switch after it is turned on is the minimum controllable switch on time $T_{ON(MIN)}$.
If the required switch on time is shorter than the minimum on time, the regulator will either skip cycles or it will jitter.
To allow for transient headroom, the minimum operating switch on time should be at least 20% to 30% higher than the worst case minimum on time.

Minimum OFF Time Limitation

The PWM latch in Functional Block Diagram is reset every cycle by the clock. The clock also turns off the power transistor to refresh the bootstrap capacitor. This minimum off time limits the attainable duty cycle of the regulator at a given switching frequency. The measured minimum off time is 100ns typically. If the required duty cycle is higher than the attainable maximum, then the output voltage will not be able to reach its set value in continuous-conduction mode.

Inductor Selection

The inductor ripple current for a non-synchronous step-down converter in continuous-conduction mode is:

$$\Delta I_L = (V_O + V_D) \times (1 - D) / (F_{SW} \times L1) \quad \text{Eq. (3)}$$

where F_{SW} is the switching frequency and L1 is the inductance.
An inductor ripple current between 20% to 50% of the maximum load current, I_O, gives a good compromise among efficiency, cost and size. Re-arranging Equation (3) and assuming 35% inductor ripple current, the inductor is given by:

$$L1 = (V_O + V_D) \times (1 - D) / (35\% \times I_O \times F_{SW}) \quad \text{Eq. (4)}$$

If the input voltage varies over a wide range, then choose L1 based on the nominal input voltage. Always verify converter operation at the input voltage extremes.
The peak current limit of ZT1525 power transistor is at least 3.6A. The maximum deliverable load current for the ZT1525 is 3.6A minus one half of the inductor ripple current.

Input Decoupling Capacitor

The input capacitor should be chosen to handle the RMS ripple current of a buck converter. This value is given by:

$$I_{RMS\_CIN} = I_O \times [D \times (1 - D)]^{1/2} \quad \text{Eq. (5)}$$

The input capacitance must also be high enough to keep input ripple voltage within specification. This is important in reducing the conductive EMI from the regulator. The input capacitance can be estimated from:

$$C_{IN} > I_O / (4 \times \Delta V_{IN} \times F_{SW}) \quad \text{Eq. (6)}$$

Where ΔV_{IN} is the allowable input ripple voltage.
Multi-layer ceramic capacitors, which have very low ESR (a few mΩ) and can easily handle high RMS ripple

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current, are the ideal choice for input filtering. A single 4.7µF X5R ceramic capacitor is adequate for 500kHz or higher switching frequency applications, and 10µF is adequate for 200kHz to 500kHz switching frequency. For high voltage applications, a small ceramic (1µF or 2.2µF) can be placed in parallel with a low ESR electrolytic capacitor to satisfy both the ESR and bulk capacitance requirements.

Output Capacitor

The output ripple voltage ΔV_O of a buck converter can be expressed as:

$$\Delta V_O = \Delta I_L \times [ESR + 1/(8 \times F_{SW} \times C_O)] \quad \text{Eq. (7)}$$

Where C_O is the output capacitance.

Since the inductor ripple current ΔI_L increases as D decreases (Equation (3)), the output ripple voltage is therefore the highest when V_{IN} is at its maximum.

A 22µF to 47µF X5R ceramic capacitor is found adequate for output filtering in most applications. Ripple current in the output capacitor is not a concern because the inductor current of a buck converter directly feeds C_O, resulting in very low ripple current. Avoid using Z5U and Y5V ceramic capacitors for output filtering because these types of capacitors have high temperature and high voltage coefficients.

Freewheeling Diode

Use of Schottky barrier diodes as freewheeling rectifiers reduces diode reverse recovery input current spikes, easing high-side current sensing in the ZT1525. These diodes should have an average forward current rating at least 3A and a reverse blocking voltage of at least a few volts higher than the input voltage. For switching regulators operating at low duty cycles (i.e. low output voltage to input voltage conversion ratios), it is beneficial to use freewheeling diodes with somewhat higher average current ratings (thus lower forward voltages). This is because the diode conduction interval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower.

The freewheeling diode should be placed close to the SW pin of the ZT1525 to minimize ringing due to trace inductance. 20BQ030 (International Rectifier), B320A, B330A (Diodes Inc.), SS33 (Vishay), CMSH3-20MA and CMSH3-40MA (Central-Semi.) are all suitable.

The freewheeling diode should be placed close to the SW pin of the ZT1525 on the PCB to minimize ringing due to trace inductance.

Bootstrapping the Power Transistor

The BST-SW voltage is supplied by a bootstrap circuit powered from the input of the converter (Figure 2). To maximize efficiency, tie the bootstrap diode to the converter output if $V_O > 2.5V$.

For the bootstrap circuit, a fast switching PN diode (such as 1N4148 or 1N914) and a small (0.1µF – 0.47µF) ceramic capacitor is sufficient for most applications. When bootstrapping from high input voltages (>20V), reduce the maximum BST voltage by connecting a Zener diode (D3) in series with D1.

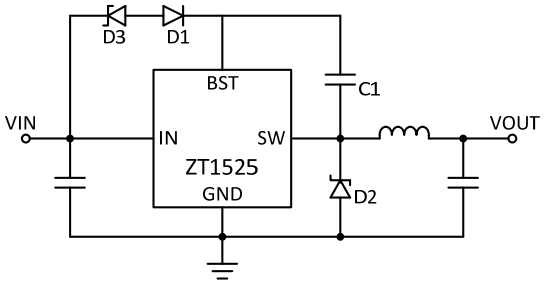

Figure 2: Bootstrapping the ZT1525.

Loop Compensation

The goal of compensation is to shape the frequency response of the converter so as to achieve high DC accuracy and fast transient response while maintaining loop stability.

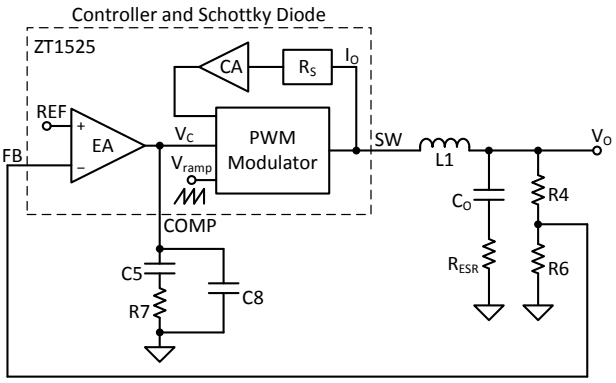

Figure 3: Block diagram of control loops.

The block diagram in Figure 3 shows the control loops of a buck converter with the ZT1525. The inner loop

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(current loop) consists of a current sensing resistor (R_S = 4.1mΩ) and a current amplifier (CA) with gain (G_{CA} = 28). The outer loop (voltage loop) consists of an error amplifier (EA), a PWM modulator, and a LC filter.

Since the current loop is internally closed, the remaining task for the loop compensation is to design the voltage compensator (C5, R7, and C8).

For a converter with switching frequency F_{SW}, output inductance L1, output capacitance C_O and loading R, the control (V_C) to output (V_O) transfer function in Figure 3 is given by:

$$V_O/V_C = [G_{PWM} \times (1 + s \times R_{ESR} \times C_O)] / \{(1 + s/\omega_p)[1 + s/(\omega_n Q) + s^2/\omega_n^2]\} \quad \text{Eq. (8)}$$

This transfer function has a finite DC gain:

$$G_{PWM} \approx R / (G_{CA} \times R_S)$$

An ESR zero F_Z is at:

$$\omega_Z = 1 / (R_{ESR} \times C_O)$$

A dominant low-frequency pole F_P is at:

$$\omega_P \approx 1 / (R \times C_O)$$

And double poles are at half the switching frequency.

Including the voltage divider (R4 and R6), the control to feedback transfer function is found and plotted in Figure 4 as the converter gain.

Since the converter gain has only one dominant pole at low frequency, a simple Type-2 compensation network is sufficient for voltage loop compensation. As shown in Figure 4, the voltage compensator has a low frequency integrator pole, a zero at F_{Z1}, and a high frequency pole at F_{P1}. The integrator is used to boost the gain at low frequency. The zero is introduced to compensate the excessive phase lag at the loop gain crossover due to the integrator pole (−90deg) and the dominant pole (−90deg). The high frequency pole nulls the ESR zero and attenuates high frequency noise.

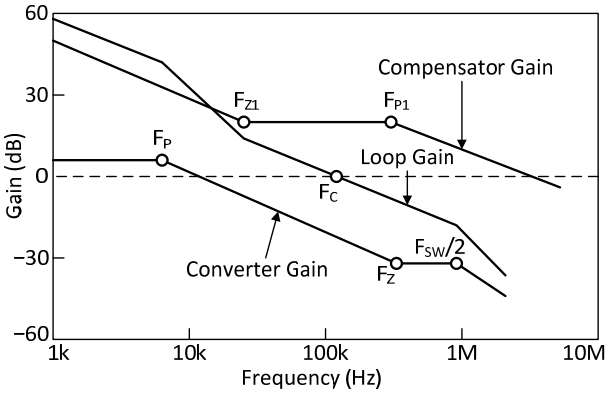

Figure 4: Bode plots for voltage loop design.

Therefore, the procedure of the voltage loop design for the ZT1525 can be summarized as:

(1) Plot the converter gain, i.e. control to feedback transfer function.

(2) Select the open loop crossover frequency, F_C, between 10% and 20% of the switching frequency. At F_C, find the required compensator gain, A_C. In typical applications with ceramic output capacitors, the ESR zero is neglected and the required compensator gain at F_C can be estimated by:

$$A_C = -20 \times \log\{[1/(G_{CA} \times R_S)] \times [1/(2\pi \times F_C \times C_O)] \times (V_{FB}/V_O)\} \quad \text{Eq. (9)}$$

(3) Place the compensator zero, F_{Z1}, between 10% and 20% of the crossover frequency, F_C.

(4) Use the compensator pole, F_{P1}, to cancel the ESR zero, F_Z.

(5) Then, the parameters of the compensation network can be calculated by:

$$R7 = 10^{Ac/20}/g_m$$

$$C5 = 1/(2\pi \times F_{Z1} \times R_7)$$

$$C8 = 1/(2\pi \times F_{P1} \times R_7)$$

Where g_m = 0.28mA/V is the EA gain of the ZT1525.

Example: Determine the voltage compensator for an 800kHz, 12V to 3.3V/3A converter with 47uF ceramic output capacitor.

As Below: Choose a loop gain crossover frequency of 80kHz, and place voltage compensator zero and pole at F_{Z1} = 16kHz (20% of F_C), and F_{P1} = 600kHz. From Equation (9), the required compensator gain at F_C is:

$$A_C = -20 \times \log\{[1/(28 \times 4.1 \times 10^{-3})] \times [1/(2\pi \times 80 \times 10^3 \times 47 \times 10^{-6})] \times (1.0/3.3)\} = 19\text{dB}$$

Then the compensator parameters are:

$$R7 = 10^{19/20}/(0.28 \times 10^{-3}) = 31.8\text{k}$$

$$C5 = 1/(2\pi \times 16 \times 10^3 \times 31.4 \times 10^3) = 0.31\text{nF}$$

$$C8 = 1/(2\pi \times 600 \times 10^3 \times 31.4 \times 10^3) = 8.5\text{pF}$$

Select R7 = 31.4k, C5 = 0.33nF, and C8 = 10pF for the design.

PCB Layout Considerations

In a step-down switching regulator, the input bypass capacitor, the main power switch and the freewheeling diode carry pulse current (Figure 5). For jitter-free operation, the size of the loop formed by these components should be minimized. Since the power

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switch is already integrated within the ZT1525, connecting the anode of the freewheeling diode close to the negative terminal of the input bypass capacitor minimizes size of the switched current loop. The input bypass capacitor should be placed close to the IN pin. Shortening the traces of the SW and BST nodes reduces the parasitic trace inductance at these nodes. This not only reduces EMI but also decreases switching voltage spikes at these nodes.

The exposed pad should be soldered to a large ground plane as the ground copper acts as a heat sink for the device. To ensure proper adhesion to the ground plane, avoid using vias directly under the device.

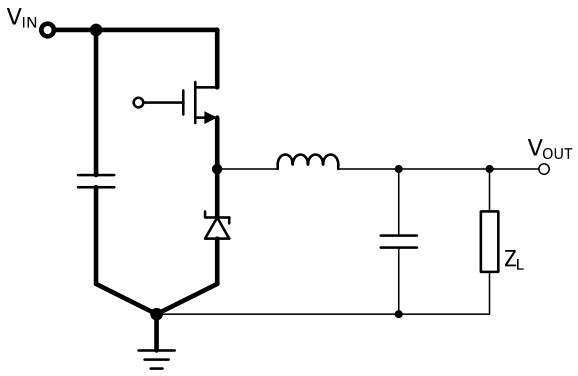

Figure 5: Heavy lines indicate the critical pulse current loop. The inductance of this loop should be minimized.

A Typical Application of 300kHz 24V to 1.5V/3A Step-Down Converter

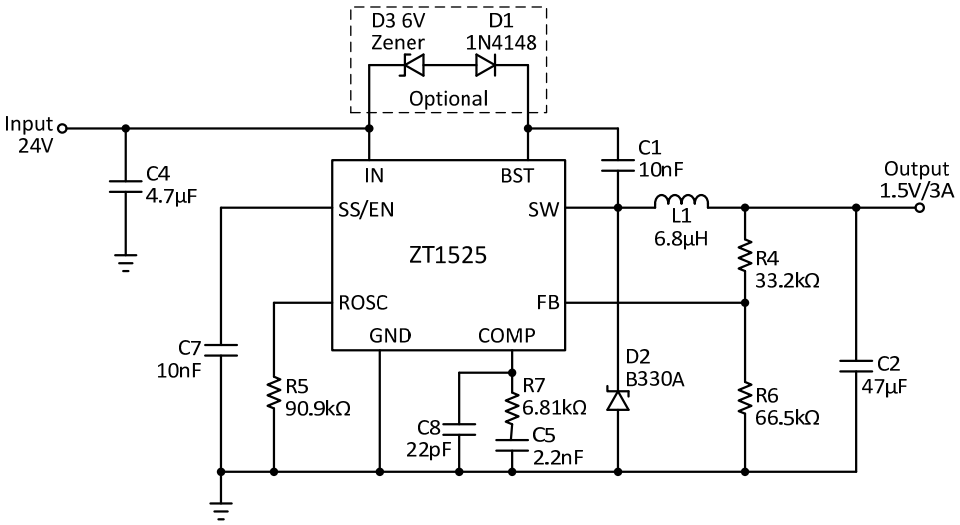

Figure 6: 300kHz 24V to 1.5V/3A step-down converter.

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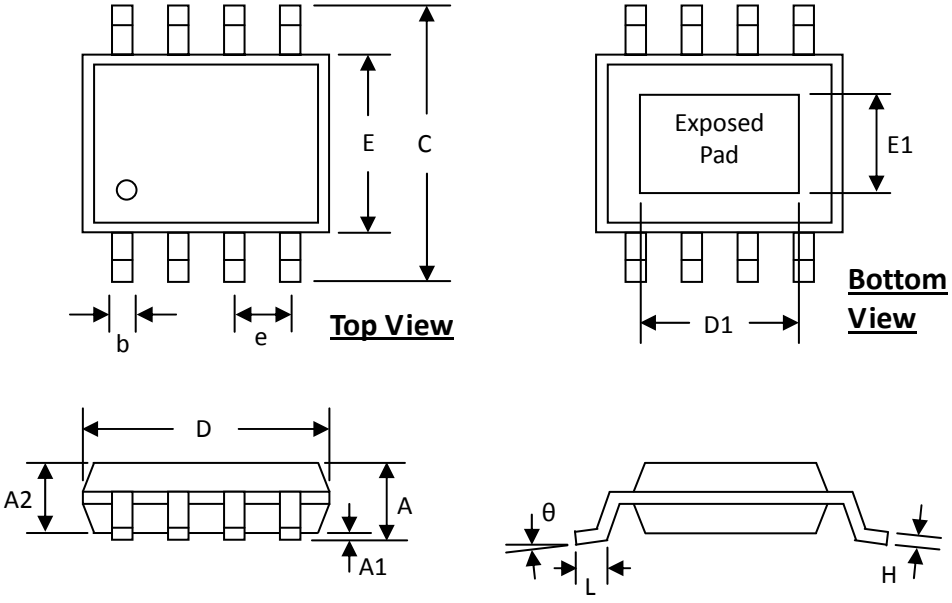
PACKAGE DIMENSION SOP-8L(EP)



SYMBOLS	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	1.30	1.70	0.051	0.067
A1	0.00	0.15	0.000	0.006
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
C	5.80	6.20	0.228	0.244
D	4.80	5.00	0.189	0.197
D1	3.15	3.45	0.124	0.136
E	3.80	4.00	0.150	0.157
E1	2.26	2.56	0.089	0.101
e	1.27 BSC		0.050 BSC	
H	0.19	0.25	0.0075	0.0098
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°

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