Li+ Charger Protection IC with Integrated P-MOSFET

DESCRIPTION

The ZT2306/A provides complete Li+ charger protection against input over-voltage, input over-current, and battery over-voltage. When any of the monitored parameters are over the threshold, the IC removes the power from the charging system by turning off an internal switch. All protections also have deglitch time against false triggering due to voltage spikes or current transients.

The ZT2306/A integrates a P-MOSFET with the body diode reverse protection to replace the external P-MOSFET and Schottky diode for charger function of cell phone's PMIC. When the CHRIN voltage drops below V_{BAT}+20mV, the internal power select circuit will reverse the body diode's terminal to prevent a reverse current flowing from the battery back to CHRIN pin.

The ZT2306/A is available in the TDFN 2x2-8L (EP) and SOT23-6L packages, and it is RoHS compliant and 100% lead (Pb) free.

FEATURES

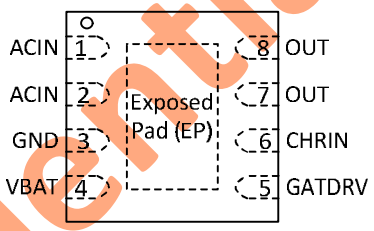
- Input over-voltage protection
- Input over-current protection
- Battery over-voltage protection
- High immunity of false triggering
- High accuracy protection threshold
- A built-in P-MOSFET
- Thermal shutdown protection
- RoHS Compliant and 100% Lead (Pb) Free

APPLICATIONS

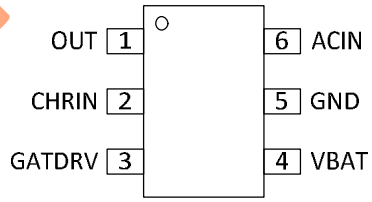
- Cell phones

Pins Configuration

Top View
TDFN 2x2-8L



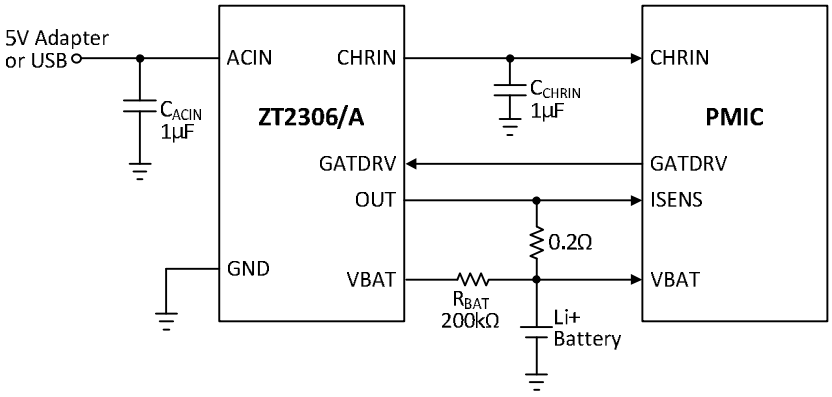
Top View
SOT23-6L



ORDERING INFORMATION

PART	PACKAGE	RoHS	Ship, Quantity
ZT2306D	TDFN 2x2-8L	Yes	Tape and Reel
ZT2306AD	TDFN 2x2-8L	Yes	Tape and Real
ZT2306S	SOT23-6L	Yes	Tape and Real
ZT2306AS	SOT23-6L	Yes	Tape and Real

Typical Application Circuit



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Absolute Maximum Ratings

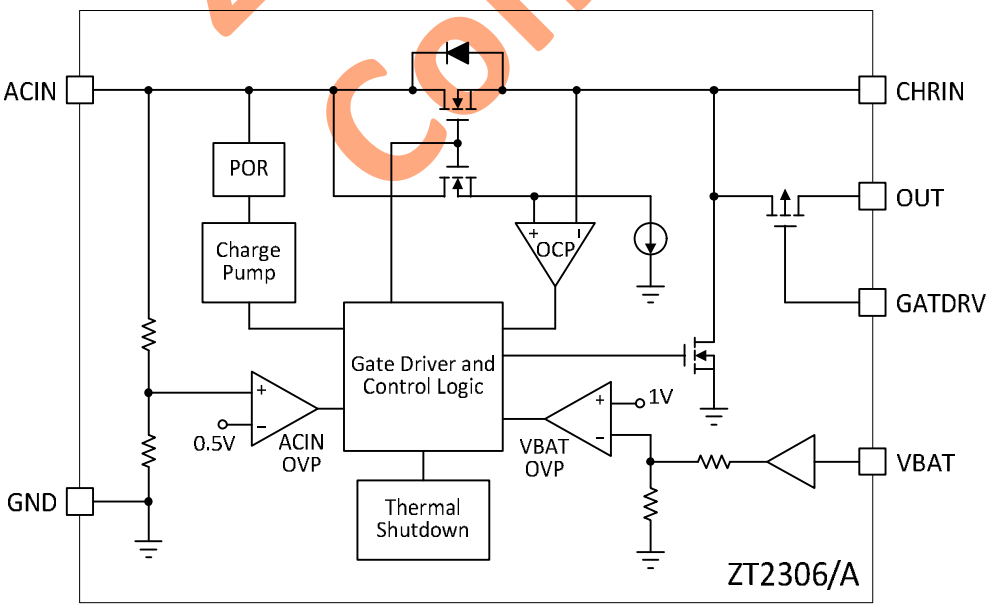
ACIN Input Voltage to GND (V_{ACIN}) ..... –0.3V to +30V
CHRIN to GND Voltage (V_{CHRIN}) ..... –0.3V to +7V
GATDRV to GND Voltage (V_{GATDRV}) ..... –0.3V to V_{CHRIN}
VBAT to GND Voltage (V_{BAT}) ..... –0.3V to +7V
OUT to GND Voltage (V_{OUT}) ..... –0.3V to +7V
OUT Output Current (I_{OUT}) 1.5A
Junction Temperature (T_J) ..... +150°C
Lead Temperature (T_{SDR}, Soldering, 10sec) ..... +260°C
Operating Temperature Range (T_A)..... –40°C to +85°C
Storage Temperature Range (T_{STG})..... –65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

Functional Block Diagram



Package Thermal Characteristics

TDFN 2x2-8L
Thermal Resistance, θ_{JA} ..... 80°C/W
SOT23-6L
Thermal Resistance, θ_{JA} ..... 220°C/W

Pins Description

TDFN	SOT	Symbol	Description
1	6	ACIN	Power supply input.
2		ACIN	
3	5	GND	Ground.
4	4	VBAT	Battery voltage sense input.
5	3	GATDRV	Internal P-MOSFET gate input.
6	2	CHRIN	Output pin. Provide supply voltage to PMIC.
7	1	OUT	Output pin. Supply source current for charging Li+ battery.
8		OUT	
EP	---	Exposed pad	To be soldered to ground to promote thermal performance.

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Recommended Operating Conditions

PARAMETER	Symbol	MIN	MAX	UNIT
ACIN Input Voltage	V_{ACIN}	4.5	5.5	V
Output Current	I_{OUT}	0	700	mA

Electrical Specifications

(V_{ACIN} = +5V, V_{BAT} = +3.8V, −40°C < T_A < +85°C, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	Symbol	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACIN Input Current and Power-On-Reset (POR)							
ACIN Supply Current	I_{ACIN}	I_{OUT} = 0A, I_{CHRIN} = 0A			250	350	µA
ACIN POR Threshold	V_{ACIN}	V_{ACIN} rising		2.4		2.8	V
ACIN POR Hysteresis				200	250	300	mV
ACIN Power-On-Blanking Time	$T_{B(ACIN)}$				8		ms
Internal Switch On Resistance							
ACIN to OUT On Resistance		I_{OUT} = 0.7A			0.5		Ω
CHRIN Discharge On Resistance					500		Ω
Input Over-Voltage Protection (OVP)							
Input OVP Threshold	V_{OVP}	V_{ACIN} rising	ZT2306	6	6.17	6.35	V
			ZT2306A	6.6	6.8	7	
Input OVP Hysteresis				200	300	400	mV
Input OVP Propagation Delay						1	µs
Input OVP Recovery Time	$T_{ON(OVP)}$				8		ms
Over Current Protection (OCP)							
OCP Threshold	I_{OCP}			1	1.15	1.3	A
OCP Blanking Time	$T_{B(OCP)}$				176		µs
OCP Recovery Time	$T_{ON(OCP)}$				64		ms
Battery Over Voltage Protection							
Battery OVP Threshold	V_{BOVP}	V_{BAT} rising		4.32	4.35	4.38	V
Battery OVP Hysteresis				220	270	320	mV
VBAT Pin Leakage Current	I_{VBAT}	V_{BAT} = +4.4V				20	nA
Battery OVP Blanking Time	$T_{B(BOVP)}$				176		µs
Internal P-MOSFET (CHRIN, OUT and GATDRV Pins)							
V_{CHRIN}-V_{BAT} Lockout Threshold		V_{CHRIN} from low to high, P-MOSFET is controlled by GATDRV			150		mV
		V_{CHRIN} from high to low, P-MOSFET is off			20		
OUT Input Current		V_{CHRIN} = 0V, V_{OUT} = +4.2V, GATDRV = GND				1	µA
GATDRV Leakage Current		V_{ACIN} = V_{CHRIN} = V_{OUT} = +5V, V_{GATDRV} = 0V				1	µA
OUT Leakage Current		V_{ACIN} = V_{CHRIN} = V_{GATDRV} = +5V, V_{OUT} = 0V				1	µA
P-MOSFET Input Capacitance					200		pF
GATDRV Input Resistance					15		Ω
Over-Temperature Protection (OTP)							
Over-Temperature Threshold	T_{OTP}	T_J rising			160		°C
Over-Temperature Hysteresis					40		°C

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FUNCTION DESCRIPTION

Pins Description

Symbol	Description
ACIN	Power Supply Input. Connect this pin to external DC supply. Bypass to GND with a 1µF (minimum) ceramic capacitor.
GND	Ground terminal.
VBAT	Battery Voltage Sense Input. Connect this pin to pack positive terminal through a resistor.
GATDRV	Internal P-MOSFET Gate Input.
CHRIN	Output Pin. This pin provides supply voltage to the PMIC input. Bypass to GND with a 1µF (minimum) ceramic capacitor.
OUT	Output Pins. These pins provide supply source current in series with a resistor to battery.
EP	Exposed Thermal Pad. This pad must be electrically connected to the GND pin.

ACIN Power-On-Reset (POR)

The ZT2306/A has a built-in power-on-reset circuit to keep the output shutting off until internal circuitry is operating properly. The POR circuit has hysteresis and a deglitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the POR threshold and after 8ms blanking time, the output voltage starts a soft-start to reduce the inrush current.

ACIN Over-Voltage Protection (OVP)

The input voltage is monitored by the internal OVP circuit. When the input voltage rises above the input OVP threshold, the internal FET will be turned off within 1ms to protect connected system on OUT pin. When the input voltage returns below the input OVP threshold minus the hysteresis, the FET is turned on again after 8ms recovery time. The input OVP circuit has a 300mV hysteresis and a recovery time of $T_{ON(OVP)}$ to provide noise immunity against transient conditions.

Over-Current Protection (OCP)

The output current is monitored by the internal OCP circuit. When the output current reaches the OCP threshold, the device limits the output current at OCP threshold level. If the OCP condition continues for a blanking time of $T_{B(OCP)}$, the internal power FET is turned off. After the recovery time of $T_{ON(OCP)}$, the FET will be turned on again. The ZT2306/A has a built-in counter. When the total count of OCP fault reaches 16, the FET is turned off permanently, requiring a V_{ACIN} POR again to restart.

Battery Over-Voltage Protection

The ZT2306/A monitors the VBAT pin voltage for battery over-voltage protection. The battery OVP threshold is internally set to 4.35V. When the VBAT pin voltage exceeds the battery OVP threshold for a blanking time of $T_{B(BOVP)}$, the internal power FET is turned off. When the VBAT voltage returns below the battery OVP threshold minus the hysteresis, the FET is turned on again. The ZT2306/A has a built-in counter. When the total count of battery OVP fault reaches 16, the FET is turned off permanently, requiring a V_{ACIN} POR again to restart.

Over-Temperature Protection

When the junction temperature exceeds 160°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 40°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J = +125°C.

Internal P-MOSFET

The ZT2306/A integrates a P-channel MOSFET with the body diode reverse protection to replace the external P-MOSFET and Schottky diode for cell phone's PMIC. The body diode reverse protection prevents a reverse current flowing from the battery back to CHRIN pin. During power-on, when CHRIN voltage rises above the

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VBAT voltage by more than 150mV, the body diode of the P-channel MOSFET is forward biased from OUT to CHRIN, and P-MOSFET is controlled by the external GATDRV voltage. When the CHRIN voltage drops below V_{BAT}+20mV, the body diode of the P-channel MOSFET is forward biased from CHRIN to OUT and P-channel MOSFET is turned off. When any of input OVP, OCP, battery OVP, is detected, the internal P-channel MOSFET is also turned off.

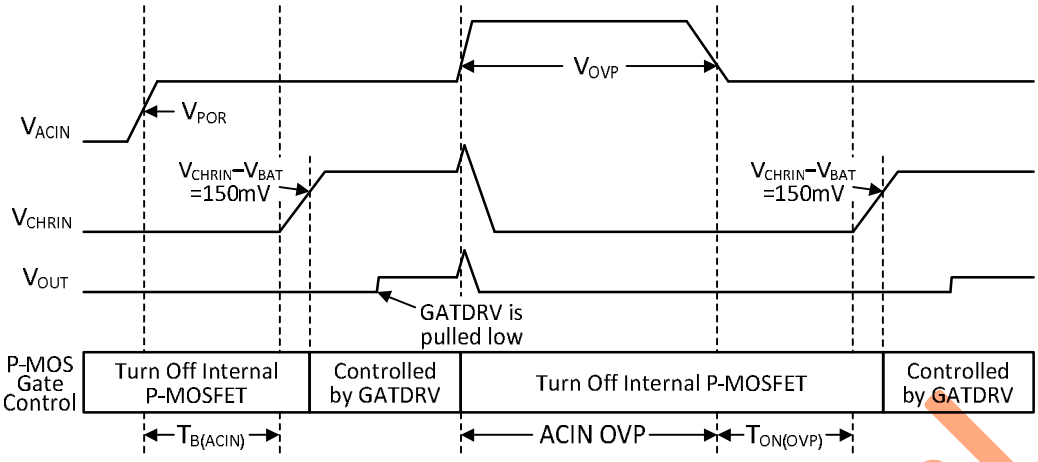

Figure 1: OVP timing diagram.

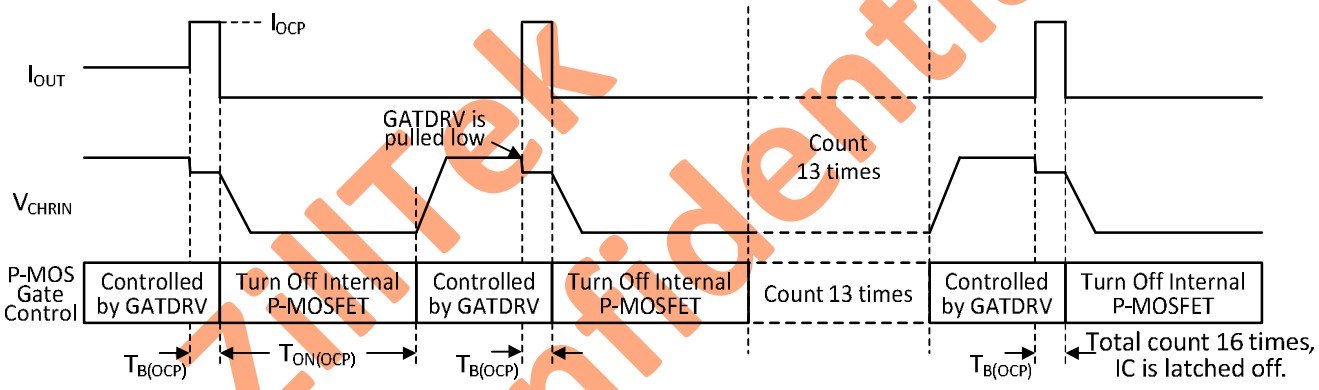

Figure 2: OCP timing diagram.

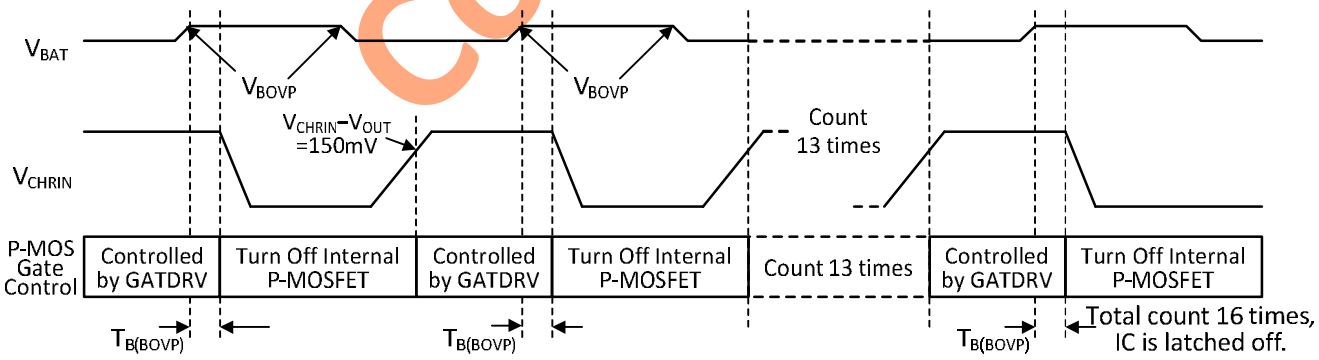

Figure 3: Battery OVP timing diagram.

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APPLICATION INFORMATION

R_{BAT} Selection

Connect the VBAT pin to the positive terminal of battery through a resistor R_{BAT} for battery OVP function. The R_{BAT} limits the current flowing from VBAT to battery in case of VBAT pin is shorted to ACIN pin under a failure mode. The recommended value of R_{BAT} is 200kΩ. In the worse case of an IC failure, the current flowing from the VBAT pin to the battery is:

(30V – 3V) / 200kΩ = 135μA

Where the 30V is the maximum ACIN voltage and the 3V is the minimum battery voltage. The current is so small and can be absorbed by the charger system.

Capacitor Selection

The input capacitor is for decoupling and prevents the input voltage from overshooting to dangerous levels. In the AC adapter hot plug-in applications or load current step-down transient, the input voltage has a transient spike due to the parasitic inductance of the input cable. A 25V, X5R, dielectric ceramic capacitor with a value between 1μF and 4.7μF placed close to the ACIN pin is recommended.

The output capacitor of CHRIN is for CHRIN voltage decoupling. And also can be as the input capacitor of the charging circuit. At least, a 1μF, 10V, X5R capacitor is recommended.

Layout Consideration

In some failure modes, a high voltage may be applied to the device. Make sure the clearance constraint of the PCB layout must satisfy the design rule for high voltage. The exposed pad of the TDFN 2x2-8L performs the function of channeling heat away. It is recommended that connect the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias to improve heat dissipation. The input and output capacitors should be placed close to the IC. The high current traces like input trace and output trace must be wide and short.

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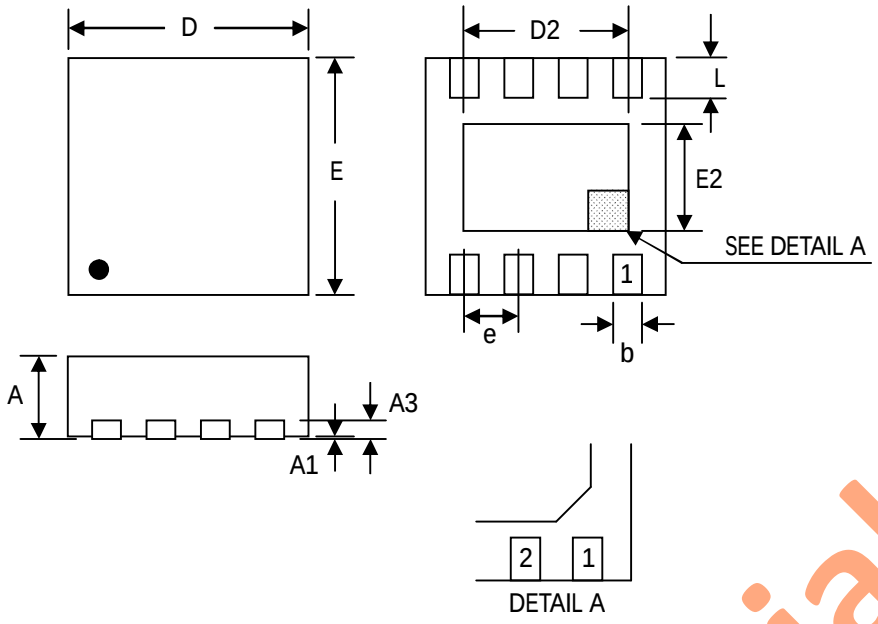
PACKAGE DIMENSION TDFN 2x2-8L



Symbol	Dimensions in mm		Dimensions in Inch	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500 BSC		0.020 BSC	
L	0.300	0.400	0.012	0.016

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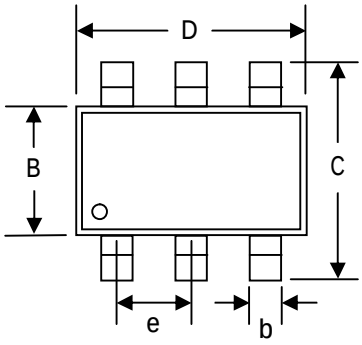
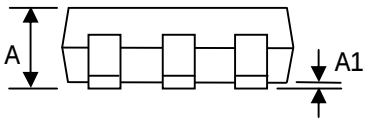
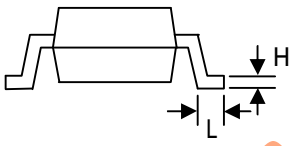
PACKAGE DIMENSION SOT23-6L







Symbol	Dimensions in mm		Dimensions in Inch	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.013	0.100	0.001	0.004
B	1.525	1.675	0.060	0.066
b	0.300	0.559	0.012	0.022
C	2.700	2.900	0.106	0.114
D	2.900	2.975	0.114	0.117
e	0.950 BSC		0.037 BSC	
H	0.250 BSC		0.010 BSC	
L	0.300	0.600	0.012	0.024

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