ZW0201
Z-Wave™ Single Chip

Low Power Z-Wave™ Transceiver with Microcontroller

SUMMARY

Z-Wave™ Single Chip

- ***RF Transceiver***
- ***Optimized 8051 Microcontroller***
- ***32 kbyte Flash Memory***
- ***2 kbyte SRAM***
- ***Triac Controller***
- ***Integrated I/O Peripherals: SPI, UART and PWM***
- ***12 bit Rail to Rail ADC***
- ***Sleep Mode with Wake Up Timer***
- ***Watchdog Timer***
- ***Power-On Reset / Brown-Out Detector***
- ***Battery Monitoring***
- ***On-Chip Supply Regulators***
- ***Supply Voltage: 2.1-3.6 V***
- ***Small Package: 32 pin 5x5x0.9mm QFN***

GENERAL DESCRIPTION

The **ZW0201** Z-Wave™ Single Chip is a complete wireless solution for home automation consisting of an integrated RF transceiver, an 8051 microcontroller, a Z-Wave™ SW Application Programming Interface (API) and flash memory storage for user application SW. All of the above is integrated into one single chip. Moreover the **ZW0201** contains a 12 bit ADC, 10 general purpose I/O pins, a Power-On-Reset circuit / Brown-out detector, a Triac Controller, a Serial Peripheral Interface (SPI), an Interrupt Controller and a UART for connecting to peripheral devices. The chip is designed for very low power and low voltage applications.

The Z-Wave™ API is described in a separate document: 'Z-Wave™ ZW0201 Application Programming Guide'.

FEATURES

RF Transceiver
- Freq.: 868.42 MHz (EU) / 908.42 MHz (US)
- Data rate 9.6 kbit/s and 40 kbit/s
- High sensitivity:
  - 9.6 kbit/s: -104 dBm
  - 40 kbit/s: -101 dBm
- Excellent receiver linearity, IIP3: -6 dBm
- Requires very few external components
- Programmable output power –20 to 0 dBm
- FSK modulation
- HW Manchester coding/decoding (9.6 kbit/s)
- Complies with EN 300 220 and FCC CFR47 part 15

8051 Compatible Microcontroller
- Optimized 8051 MCU core. Six times the performance of the original 8051
- 16 MHz MCU clock frequency

Memory
- 32 kbyte flash for Z-Wave™ API library and customer application SW
- Read-back and write protection of flash
- Read/write/erase access to flash from MCU
- 2 kbyte data SRAM (8051 XRAM)
- 256 byte MCU internal SRAM (8051 IRAM)

Timers
- Timers for Z-Wave™ API + Application SW
  - Two 8051 compatible timers
  - One 16 bit General Purpose Timer (programmable for PWM)
- Wake Up Timer in Sleep mode

Interfaces
- 10 configurable general purpose I/O pins
- Programmable pull-up on all GPIO pins
- High strength outputs ± 6 mA
- One Schmitt Trigger input (e.g. for zero crossing detection in triac controller app.)
- Two input pins for external interrupts

Triac Controller
- HW implementation

Serial Peripheral Interface (SPI)
- Slave in programming mode of internal flash
- Master when interfacing to external EEPROM

UART
- 9.6 kbaud, 38.4 kbaud or 115.2 kbaud

External Interrupts
- Two edge or level triggered interrupts
- One interrupt can initiate wake up from sleep mode

ADC
- 12 or 8 bit resolution
- Four multiplexed inputs
- Maximum sampling rate 23.6 ksamples/s
- Reference: Internal, supply or external input
- On-chip battery monitoring (not supported in Developers Kit v4.1x API)

Power Management
- Power down / Sleep mode with wake up timer

Power-On Reset (POR) / Brown-Out Detector
- Extremely low power consumption (also active in sleep mode)

Power Consumption (typical values)

• Sleep mode:	2.5 µA
• Normal mode (MCU, no RF):	5.2 mA
• Receiving:	23 mA
• Transmitting -5 dBm:	24 mA
• Transmitting +0 dBm:	36 mA

Development Tools

The user application SW can be compiled using the 8051 C-compiler from Keil Software GmbH. Please refer to the Keil homepage for Embedded Development Tools (**www.keil.com**). The ZW0201 can be programmed using an EPSILON 5 II, an FS2003 or a PPM3 programmer from Equinox Technologies Limited (www.equinox-tech.com).

ARCHITECTURAL OVERVIEW

Figure 1 shows a functional block diagram of the **ZW0201**.

The central parts of the **ZW0201** are the RF transceiver, the 8051 MCU including SRAM, and the flash memory. In addition to the central parts there are a number of peripheral functions supporting the Z-Wave™ system. All functional blocks are briefly described below:

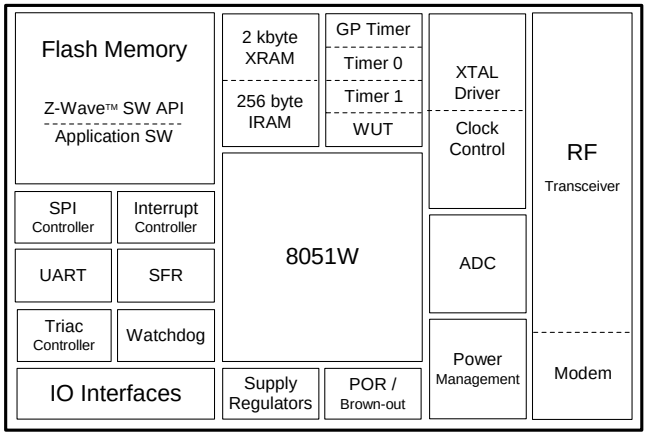


Figure 1: ZW0201 functional block diagram

Supply Regulators

The supply regulators regulate the external supply down to an internal 1.8 V supply. The on-chip supply regulators significantly improve the supply noise tolerance of the chip.

XTAL and System Clock

The **ZW0201** runs on a system clock that is derived from an external crystal (XTAL). The XTAL must be either 16 or 32 MHz with a maximum tolerance of 27 ppm including temperature and ageing.

The Clock Control divides the XTAL frequency into two internal clocks: an 8 MHz clock for RF circuits and a 16 MHz clock for MCU and peripherals.

Power-On-Reset / Brown-out Circuit

The Power-On-Reset (POR) circuit eliminates the need for external reset circuitry as it holds the **ZW0201** in reset during power-on and brown-out situations. The POR is designed with glitch immunity and hysteresis for noise and transient stability.

The POR circuit has an extremely low power consumption and is always active even in Sleep mode.

RF Transceiver

The transceiver is able to transmit and receive 9.6 kbit/s Manchester encoding and 40 kbit/s with NRZ encoding. The RF modem handles all the RF related functions such as Manchester encoding / decoding, pre-ample detection and serialization / deserialization.

The RF modem is able to listen for 9.6 kbit/s data and 40 kbit/s data simultaneously enabling systems where both speeds are used.

The output power of the transmitter PA (Power Amplifier) is adjustable in steps of 2 dB. The different parts of the RF transceiver can be powered up/down so only the required circuits are powered at all time.

The RF transceiver only needs external components for input/output matching.

A block diagram of the Transceiver including RF modem is given in Figure 2.

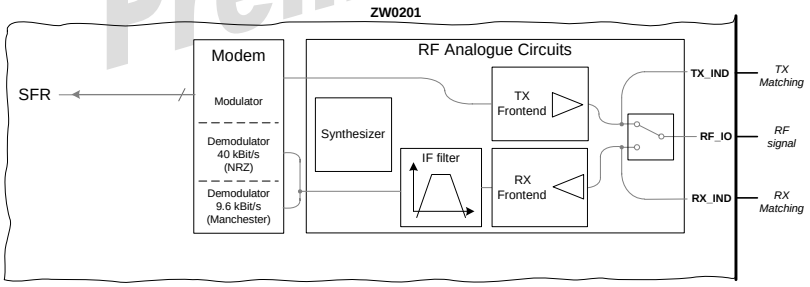


Figure 2: RF transceiver architecture

8051 MCU including Timer 0 & 1

The **ZW0201** contains an embedded 8051 MCU core (Inventra M8051 Warp) including two standard 8051 timers / counters.

The MCU is fully binary compatible with the industry standard 803x/805x micro controllers.

The MCU completes one instruction cycle per two clock cycles as opposed to the standard 8051 with 12 clock cycles per instruction cycle.

This makes the 8051W six times faster than the standard 8051.

GPT

The General Purpose Timer is a versatile 16 bit timer that can be polled or programmed to generate interrupts. The timer is an auto-reload counter with a fixed clock divider ratio of either 4 or 512.

The timer can also be set in PWM (Pulse Width Modulation) mode with the output on the *P1.6*

pin. The PWM is controlled using an 8 bit register to set the high period and an 8 bit register to set the low period.

The PWM timer counts using a fixed clock divider ratio of either 4 or 512. Figure 3 shows the timing of a PWM output.

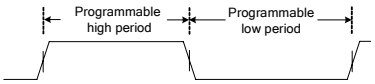


Figure 3: PWM output

Wake Up Timer

The Wake Up Timer (WUT) is an ultra low power timer that can be enabled in Sleep mode / power down to wake up the chip after a programmable time period. The sleep period is configurable in number of seconds and can be set from 1 to 256 seconds. The WUT is based on an internal oscillator that is automatically calibrated against the system clock.

SFR

The SFR contains the 8051 Special Function Registers that are used to control the operating mode of the 8051 and the built-in peripherals. The registers needed in a given application are operated through the API.

32 kbyte Flash Memory

The flash Memory is the MCU program memory containing the Z-Wave™ API and the customer application SW. The MCU also has the ability to read, write and erase the flash.

The flash has a built-in read back protection in order to prevent reverse engineering or design theft. Clearing a dedicated lock bit in the flash activates the read back protection. As long as the lock bit is low it is not possible to read from the flash externally (SPI). Other lock bits can protect parts of the flash against writing[I]. The lock bits can only be unlocked by erasing the entire flash memory.

The flash memory is accessed and programmed through the SPI serial interface.

Through the Developers Kit v4.0x API the **ZW0201** supports up to 70k write cycles for application data.

256 byte IRAM

This built-in IRAM is used by the MCU as 8051 internal data memory. The RAM may also be accessed through direct instructions from the MCU.

2 kbyte XRAM

The built-in 2 kbyte XRAM are used by the MCU as “8051 external data” memory.

Interrupt Controller

The **ZW0201** supports 10 interrupt sources including two external interrupt sources on the General Purpose I/O’s *P1.6* and *P1.7*. Some of the interrupt sources are reserved by the Z-Wave™ API. The Interrupt Controller controls the interrupt priority assignment. The priority is fixed by the Z-Wave™ protocol.

The external interrupt on *P1.7* can also be enabled to wake up the chip from Sleep mode.

Triac Controller

The **ZW0201** contains a Triac Controller for power regulating applications. The Triac Controller is compatible with 50-60 Hz. Using an external triac and a few extra external passive components a complete phase control circuit can be designed. The controller is completely implemented in HW in order to keep timing and operation independent of SW and to minimise MCU workload.

ADC

The ADC resolution can be set to 8 bit or 12 bit. An 8 bit conversion takes less than half the time of a 12 bit conversion.

[I] The boot page (page 0) can be write protected and a boot sector can be defined that is write protected. The boot sector starts from 7FFFF(hex) and downwards. The size of the boot sector is programmable from zero pages up to the entire flash. Neither MCU nor SPI can write to the boot sector.

The ADC is rail to rail and can be programmed to refer to V_{DD}, V_{SS}, a bandgap reference, or to external references (upper and lower). The ADC block includes a battery monitoring mode (no external connections needed). This mode is not supported by the API in Developers Kit v4.1x.

The ADC supports both single and (continuous) multi conversion mode. It has a built-in comparator for generating interrupts when a threshold set by SW is exceeded. The threshold can be either a low threshold or a high threshold. Multi conversion mode is only available for 8 bit mode.

It is possible to shut down the ADC for reducing power consumption.

Serial Peripheral Interface - SPI

The SPI has two purposes: 1) to provide external access to the flash memory and 2) to allow **ZW0201** to communicate with an external EEPROM.

The **ZW0201** acts as SPI master when interfacing to an external EEPROM. When using the SPI for accessing the flash the SPI acts as a slave.

UART

The **ZW0201** UART is independent of the 8051 MCU and does not occupy any timer resources. The UART supports full duplex and can operate with the following three baud rates : 9.6 kbaud, 38.4 kbaud, or 115.2 kbaud.

Power Control

The Power Control Block controls the chip's different power saving modes. The **ZW0201** basically supports two power saving modes below:

- *Normal mode*
  The MCU is running. The RF circuits and the ADC can be powered up or down.
- *Sleep mode / power down mode*
  Lowest power mode. Everything shut down except the RAM's, brown-out detection and an optional low power timer (WUT).

In addition the ADC can be powered up or down.

In Sleep mode it is possible to wake the MCU up using an external interrupt source on *P1.7.* The source can be active low or active high. The MCU can also be woken by the WUT or a reset on the *RESET_N* pin (or by power cycling).

I/O Interfaces

The **ZW0201** has 10 configurable General Purpose I/O (GPIO) pins with optional weak internal pull-up. The GPIO pins are organized as two ports: *P0.x* (2 bits) and *P1.x* (8 bits). The GPIO pins have dual or even triple functionality: User programmable from MCU and some special HW functions (for instance SPI, ADC, UART, TRIAC controller, etc.). Four of the GPIO pins can be either analogue (for ADC) or digital. In digital mode all GPIO pins are CMOS compatible inputs/outputs.

The *RESET_N* pin has two purposes: 1) External reset and 2) Enable programming mode. When the *RESET_N* pin is pulled low a master reset is generated. If the *RESET_N* is held low for an extended period (refer to the External Programming of Flash section) then the chip accepts programming commands on the SPI. The chip will not go into actual programming mode until an SPI 'Programming Enable' command is received.

Finally there are 5 dedicated analogue pins for RF interface and crystal connections.

All GPIO pins will be set as inputs during reset. This pin configuration is maintained after the reset is released (until the SW changes the setting).

Pin Definitions

The pin definitions for the **ZW0201** can be found in Table 1.

Table 1: ZW0201 – Pin definitions

Pin Name(s)	# of Pins	Input / Output	Pull-up [1), 2)]	Function
General Purpose I/O				
P0.0/ADC/ZEROX	1	I/O	Opt.	1) User programmable pin w. schmitt trigger input
		I	No	2) ADC (upper ref. / multiplexed input)
		I	No	3) ZEROX, Zero crossing detection input for TRIAC Ctrl. w. schmitt trigger input
P0.1/ADC/TRIAC	1	I/O	Opt.	1) User programmable pin
		I	No	2) ADC (lower ref. / multiplexed input)
		O	No	3) Triac output from Triac Ctrl (fire signal).
P1.0/ADC/TXD	1	I/O	Opt.	1) User programmable pin
		I	No	2) ADC (multiplexed input)
		O	Opt.	3) UART TxD - Transmit data
P1.1/ADC/RXD	1	I/O	Opt.	1) User programmable pin
		I	No	2) ADC (multiplexed input)
		I	Opt.	3) UART RxD - Receive data
P1.2/MISO	1	I/O	Opt.	1) User programmable pin
		I/O	Opt.	2) SPI interface – MISO [3)] (Master In Slave Out)
P1.3/MOSI	1	I/O	Opt.	1) User programmable pin
		I/O	Opt.	2) SPI interface – MOSI (Master Out Slave In)
P1.4/SCK	1	I/O	Opt.	1) User programmable pin
		I/O	Opt.	2) SPI interface - SCK (Clock signal)
P1.5	1	I/O	Opt.	User programmable pin
P1.6/PWM/INT0	1	I/O	Opt.	1) User programmable pin
		O	Opt.	2) PWM output of timer
		I	Opt.	3) External interrupt source 0
P1.7/INT1	1	I/O	Opt.	1) User programmable pin
		I	Opt.	2) External interrupt source 1
General Control				
RESET_N	1	I	Yes	Active low system reset input w. schmitt trigger. Also used for enabling flash programming mode
RF Interface				
RF_IO	1	I/O	NA	RF connection to antenna
RX_IND	1	NA	NA	RX matching
TX_IND	1	NA	NA	TX matching
Clock Inputs				
XOSC_Qx	2	NA	NA	Quartz crystal input (32 MHz / 16 MHz)

Pin Name(s)	# of Pins	Input / Output	Pull-up [1), 2)]	Function
Supply				
VSS	4	NA	NA	Ground
DVDD_IO	1	NA	NA	Positive supply digital IO cells
DVDD	3	NA	NA	Positive supply digital part
AVDD_CO	1	NA	NA	Positive analogue supply for analogue circuits (including ADC)
AVDD_SY	1	NA	NA	Positive analogue supply for synthesizer
AVDD_RF	1	NA	NA	Positive analogue supply for RF
AVDD_IF	1	NA	NA	Positive analogue supply for IF
SUPP	1	NA	NA	Internal voltage - Support circuit
MAIN	1	NA	NA	Internal voltage – Main circuit

[1)] Opt = optional. Can be set by MCU. The optional pull-up's are enabled by default at reset.
[2)] Weak internal pull-up. Pulls up a floating input. Cannot be used for external components.
[3)] The MISO pin will stay as an input until the **ZW0201** receives a 'Programming Enable' command on the MOSI pin.

SYSTEM INTERFACE

Figure 4 shows a typical **ZW0201** application circuit. The digital GPIO ports are programmable and can be used as interface to the user application. As the **ZW0201** contains a Power-On-Reset circuit, the *RESET_N* is only needed during initial programming of the flash memory and can be left unconnected (the *RESET_N* pin is active low and has internal pull-up) in the typical application. An optional filter may be added on the *RF_IO* pin in order to improve RF performance.

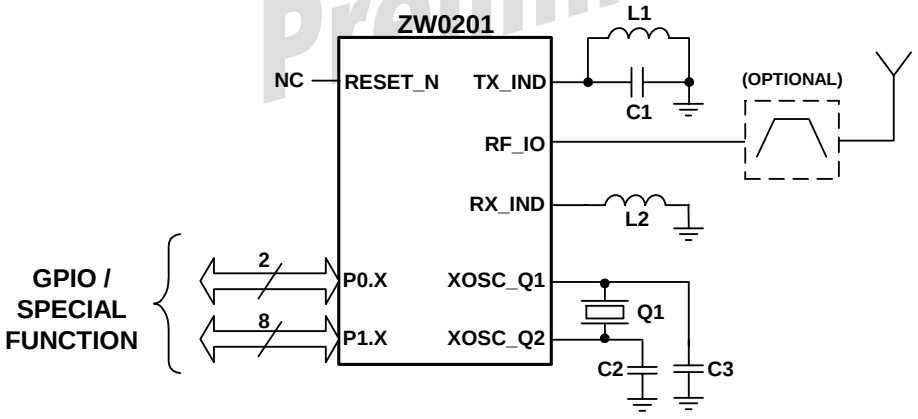


Figure 4: Typical ZW0201 application circuit

Clock Signals

The **ZW0201** includes an on-chip crystal oscillator making it possible to drive a crystal directly. The **ZW0201** can operate with either a 32 MHz or a 16 MHz crystal. Figure 5 shows the external crystal connections.

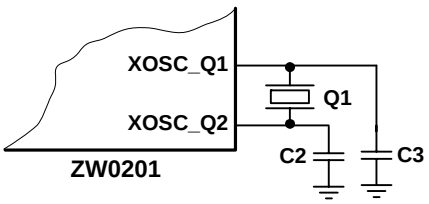


Figure 5: External crystal connections

An external load capacitor is required on each terminal of the crystal. The loading capacitor values depend on the total load capacitance, CL, specified for the crystal. The total load capacitance seen between the crystal terminals should equal CL for the crystal to oscillate at the specified frequency:

$$CL := \frac{1}{\frac{1}{C2} + \frac{1}{C3}} + C_{par}$$

where the parasitic capacitance (C_{par}) is constituted by the pin input capacitance and PCB stray capacitance. Typically the total parasitic capacitance is a few pF.

Reset

Figure 6 shows a simplified block diagram of the internal reset circuit.

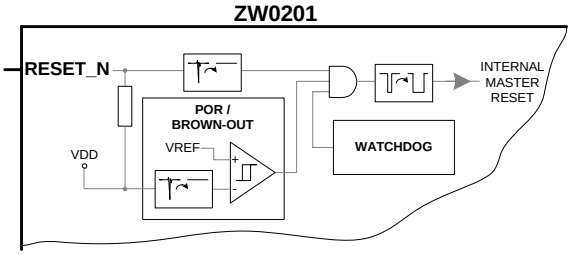


Figure 6: Reset interface

An internal master reset that resets the entire chip (except RAM's) occurs when one or more of the following conditions are true:

1) *RESET_N* is low
2) When POR / brown-out detection circuit detects low supply voltage
3) When the WATCHDOG times out

The *RESET_N* is an asynchronous input with internal pull-up, schmitt trigger, and glitch protection. The signal is synchronized internally, so that the reset can be asserted and deasserted asynchronously.

The POR circuit also contains a low pass filter for glitch protection and hysteresis for noise and transient stability.

The POR circuit is always active. In Sleep mode the POR goes into a low power mode that protects the circuit against brown-out while keeping the power consumption at an absolute minimum.

During master reset all GPIO pins will be configured as inputs and the RF will set in a power down condition.

RF Transceiver

External Components

Figure 7 shows the RF connections in a typical application.

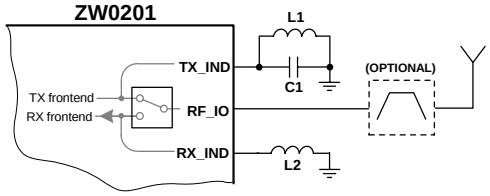


Figure 7: RF interface in typical application

The RF transceiver requires very few external passive components for input/output matching.

An internal T/R switch circuit makes it possible to match the RX and TX independently. L1/C1 is used for matching the transmitter output to 50 Ω. L2 is used for matching the receiver input to 50 Ω.

The values of the matching components will depend on the actual PCB layout but typical values are given in Table 2.

Table 2: Typical RF component values

Part	Component Value
C1	5.6 pF ± 0.25 pF
L1	3.3 nH, 2% (e.g. Coilcraft)
L2	12 nH, 2% (e.g. Coilcraft)

It is recommended to use high Q, low tolerance inductors for best performance. Moreover the matching components should be placed as close as possible to the **ZW0201** with efficient grounding in order to achieve best performance.

Additional external filter components may be added in order to filter the RF harmonics (if necessary) and improve the blocking performance.

Antenna Considerations

The **ZW0201** can be used together with various types of antennas. Please refer to the document: 'Antennas for Short Range Devices'.

RF PCB Layout Considerations

The PCB wires in the RF layout should be as short as possible to avoid stray inductance. The *RF_IO* wire should be routed over a GND layer in order to provide a good transmission line and well determined characteristic impedance. Vias should be avoided in routing of signals. Preferably the RF components should be SMD components and the RF section should be kept isolated from surrounding circuitry.

*NOTE: Proper decoupling of the RF is important to the RF performance of the **ZW0201**. Please refer to the Decoupling section for this topic.*

UART

The **ZW0201** includes a UART (Universal Asynchronous Receiver Transmitter) interface with a data rate of 9.6 kbaud, 38.4 kbaud, or 115.2 kbaud. The interface operates with 8 bit words, one start bit, one stop bit and no parity.

The interface is available on *P1.0/TxD* and *P1.1/RxD*. Figure 8 shows a typical RS232 UART application circuit.

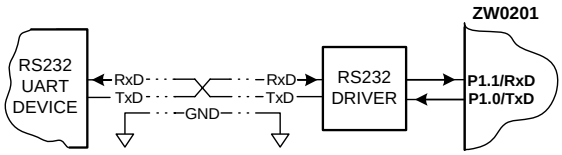


Figure 8: UART interface in typical application

The UART shifts data in/out in the following order: start bit, data bits (LSB first) and stop bit. Figure 9 gives the waveform of a serial byte.

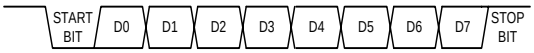


Figure 9: UART waveform

Reception

For noise rejection, the serial port establishes the content of each received bit by a majority voting on the sampled input. This is especially true for the start bit. If the falling edge on RxD is not verified by the majority voting over the start bit then the serial port stops reception and waits for another falling edge on RxD.

After 2/3 of the stop bit time, the serial port waits for another high-to-low transition (start bit) on the RxD pin.

External Interrupts

The **ZW0201** supports two external interrupts to the 8051W using pin *P1.6/INT0* and *P1.7/INT1*.The interrupts can be programmed to be either level-triggered (high/low) or edge-triggered (rising/falling).

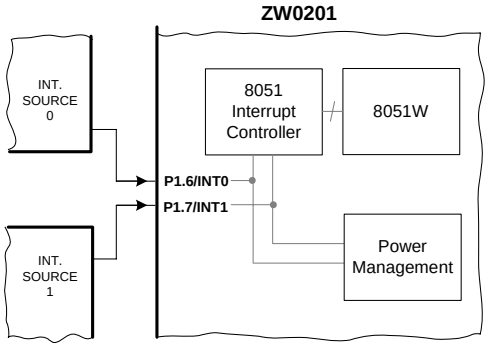


Figure 10: External interrupts

The **ZW0201** also supports interrupt(s) to the Power Management block enabling wake up from Sleep mode. The *P1.7/INT1* interrupt pin can be used to wake up the chip from Sleep mode. The interrupts to the Power Management can be level-triggered (high/low)[II].

When *P1.7/INT1* wakes up the chip from Sleep mode the clock oscillator must start up before program execution starts. The start up period is denoted t_{SON} and is listed in the Timing Parameters Table in the end of the datasheet.

Triac Controller

The **ZW0201** has a Triac Controller using phase control for power regulation of resistive loads and to some degree non-resistive loads. The Triac Controller is available on the following pins *P0.0/ZEROX* and *P0.1/TRIAC*. The *P0.0/ZEROX* input is a Schmitt trigger input to avoid ringing on zero cross detection. Figure 11 shows a simplified application circuit.

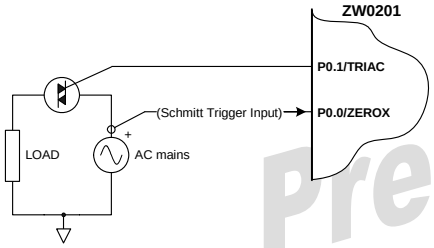


Figure 11: Simplified triac control application

The phase control method conducts power during a specific time period in each half of the AC power cycle. A triac is commonly used to switch on/off the power to the load in the AC power system application. A gate voltage is required to turn on the triac (fire pulse). Once "on", the triac will stay "on" until the AC sine wave reaches zero current regardless of the gate voltage. The power regulation is performed by controlling the fire angle (turn on start time). The triac will deliver the power to the load after the fire angle and turn off at the zero-crossing point.

The fire pulse must be of a certain duration in order to 1) provide sufficient charge for the triac to turn on and 2) ensure that is does not subsequently switch off due to potential noise.

[II] Edge-triggering is not supported to Power Management

The duration of the fire pulse can be programmed in SW.

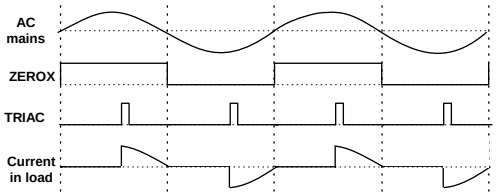


Figure 12: Typical triac waveforms

The zero cross detection can be disturbed by noise on the AC line. In case this noise is strong enough it could worst case cause additional triggering on the *ZEROX* as shown in Figure 13.

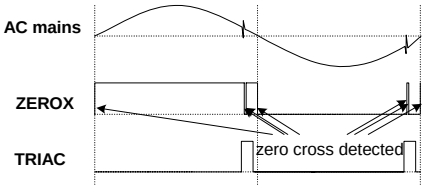


Figure 13: Zero cross signal noise

In order to avoid these extra zero crossing triggers a noise mask has been implemented in the Triac Controller. The mask masks out zero crossings from the true zero cross until a period before the next true zero cross, as shown in Figure 14.

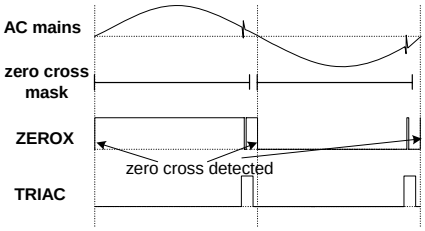


Figure 14: Zero cross signal noise mask

The zero cross detector can either be programmed to use both the rising edge and the falling edge of the zero cross signal (like the ZEROX signal in Figure 12) or it can be programmed to only use the rising edge of the zero cross signal (like the ZEROX signal in Figure 15).

The Triac Controller can be programmed to generate an interrupt request to the MCU whenever it detects a zero cross.

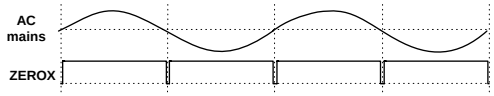


Figure 15: ZEROX input in circuits where the Triac Controller use the rising edge of the ZEROX signal to detect zero crosses

When detecting zero crosses on both rising and falling edges then the detection moments can be offset due to the threshold level of the ZEROX input, as shown in Figure 16.

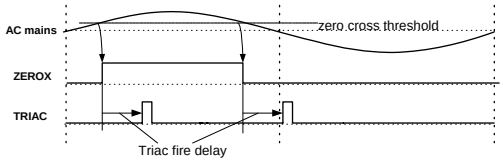


Figure 16: View of triac waveforms with exaggerated zero cross detection offset

Because of this offset the triac fire pulse will not be fired at the same distance from the beginning of the positive period and from the beginning of the negative period. It means that the AC load, which the triac controls, will have a DC voltage different from 0 V.

To make this DC voltage negligible, the Triac Controller can be programmed with a variable correction period to correct for the offset, as shown in Figure 17.

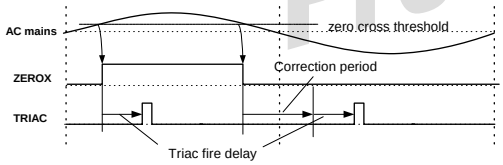


Figure 17: View of triac waveforms when zero cross detection offset is corrected (exaggerated offset)

ADC

The **ZW0201** includes a versatile rail to rail ADC which can operate in high resolution 12 bit mode or a fast 8 bit mode. The ADC can be connected to the external circuit using four of the GPIO pins: *P0.0*, *P0.1*, *P1.0* and *P1.1*. The ADC can sample an analogue signal on any of the four pins. The upper reference for the conversion can be *P0.0*, an internal 1.21 V bandgap reference or the VDD. The lower reference for the conversion can be *P0.1* or GND.

P0.0 is mainly for external upper reference as the input voltage range of this pin is limited. To avoid extra leakage current this input should be either ground or VDD when the **ZW0201** is in sleep mode.

The ADC is able to perform single conversion or continuous multi conversion (8 bit mode only). The ADC block can be programmed to generate an interrupt to the 8051W when a certain high or low threshold is exceeded.

Figure 18 gives an overview of the **ZW0201** internal ADC block.

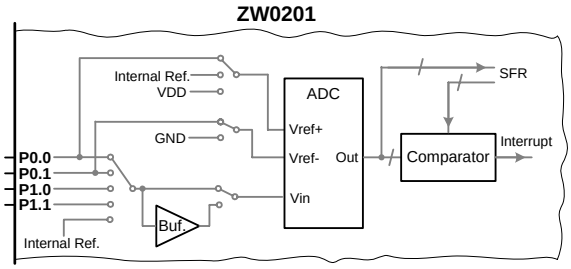


Figure 18: ADC block

The ADC can also be used for monitoring the supply level. In this setup the Internal Reference is measured with reference to the VDD. This mode is not supported by the API in Developers Kit v4.1x.

The ADC input signal is loaded by an internal sampling capacitor. In 8 bit mode the sampling time can be configured to fit the source impedance and frequency contents of the input signal. Alternatively an internal buffer can be switched in between the external source and the ADC to reduce capacitive loading of the input. The penalty for inserting the buffer is an increased offset error and degraded rail to rail performance.

Serial Peripheral Interface - SPI

The Serial Peripheral Interface (SPI) is used for synchronous data transfer between the **ZW0201** and an external EEPROM, used by some node types, or between a programming unit and the **ZW0201**. The SPI is not available to the application.

The **ZW0201** is master when interfacing to an external EEPROM and slave during programming mode. The programming mode is

enabled by setting *RESET_N* low for an extended period (refer to the External Programming of Flash section)

The interface consists of the three pins: *P1.2/MISO*, *P1.3/MOSI and P1.4/SCK.*

The *SCK* is the clock output in master mode and is the clock input in slave mode. During data transmission the SCK clocks the data from a 8-bit slave register into a 8-bit master register using the MISO connection (Master In Slave Out). At the same time data is clocked in the opposite direction from master to the slave using the MOSI (Master Out Slave In) connection. Consequently the two registers can be considered as one distributed 16-bit circular shift register. After 8 clock cycles the two registers will have swapped contents. The principle is illustrated in Figure 19.

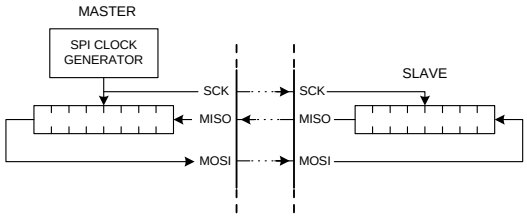


Figure 19: Data exchange between master and slave

Figure 20 shows a typical application where the **ZW0201** interfaces to an EEPROM. The SS_N (slave select) of the slave may be controlled by any available GPIO pin on the **ZW0201.**

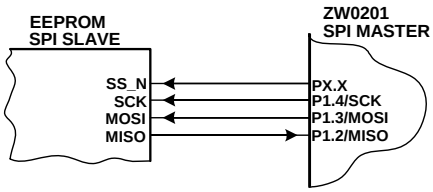


Figure 20: Typical interface to EEPROM

External Programming of Flash

In flash programming mode an external master must control of the SPI bus and the **ZW0201** will act as slave. In programming mode the flash can be erased, read, and/or written. Moreover it is possible to read a signature byte identifying the chip, enable/disable read/write protection, and/or read/write the HomeID.

Flash programming mode is entered by setting and keeping the *RESET_N* pin low. When the *RESET_N* has been held low for 2^{17} XTAL periods then the SPI will accept a 'Programming Enable' command on the *P1.3/MOSI* pin[III]. The programming commands including the 'Programming Enable' are described in the document: 'Programming the 200-Series Z-Wave Single Chip Flash'. The chip will not enter programming mode until the two first bytes of the 'Programming Enable' has been accepted.

After the chip has entered programming mode the *P1.2/MISO* pin will be set as output. The **ZW0201** will hereafter stay in programming mode as long as the *RESET_N* pin is held low. When the *RESET_N* pin is set high the chip will generate an internal master reset pulse and normal program execution will start up. The watchdog function will be disabled as long as the chip is in programming mode and all other GPIO's than the SPI interface will be tri-stated.

Figure 21 gives a simplified block diagram of a typical interface to programming equipment.

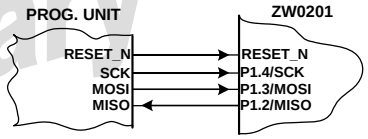


Figure 21: Interface to programming equipment

[III] If the **ZW0201** is powered up with the *RESET_N* pin low the pin must be held low for an additional delay to allow for the clock oscillator start up period. The clock oscillator start up period is denoted t_{SON} and is listed in the Timing Parameters Table in the back of the datasheet.

Decoupling and Supply Considerations

The **ZW0201** has on-chip supply regulators generating an internal supply with very high noise rejection. The low-drop-out regulators significantly improve the chip noise tolerance and make its performance more or less independent of external supply level variation. However in order to achieve the best performance of the **ZW0201** (and the supply regulators) a good decoupling strategy is important. Inadequate decoupling may degrade the ADC performance, the RF performance and/or produce significant noise transients on VDD, GND and I/O ports etc.

The rail to rail ADC and the IO ports are supplied directly by the external supply. The direct supply of these functions makes the ADC more susceptible to noise on the external supply. In order to achieve best performance of the ADC the *DVDD_IO* and the *AVDD_CO* should be carefully decoupled[IV].

The decoupling of the supply should be placed as close as possible to the supply pins with minimum stray inductance. One decoupling capacitor is recommended for each of the digital supplies. If the power supply voltage can drop below 2.7 V a decoupling capacitor is also recommended for the capacitor connection point *SUPP*. Two capacitors are recommended for each of the analog supplies. Best performance of the decoupling is achieved if the via is placed on the opposite side of the decoupling capacitor with respect to the **ZW0201** as shown on Figure 22.

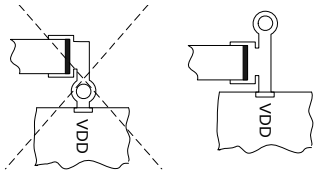


Figure 22: Optimal placement of via

When driving high current loads on GPIO pins (e.g. triac output) extra attention is needed on power routing and decoupling[V] in order to minimize noise on the supply.

A typical decoupling value is 33 nF for each digital supply and *SUPP* and 33 nF + 47 pF for each of the analogue supplies. The traces connecting the decoupling capacitors should be as wide as possible with good ground connection.

SMD components with low ESR are preferable for decoupling.

Connecting Unused Inputs

Unused digital inputs should have their internal pull-up enabled or be tied to VDD or GND to prevent the input from floating. If left floating, the power consumption of the device may increase.

[IV] The ADC is supplied by the *AVDD_CO*. The ADC input ports *P0.0*, *P01*, *P1.0* and *P1.1* are supplied by the DVDD_IO.

[V] Additional local decoupling may be added to decrease noise transients.

ZW0201 - SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_J	Junction operating temperature	-40 °C to 125 °C
T_A	Ambient operating temperature[VI]	-40 °C to 120 °C
T_{STG1}	Storage Temperature (un-programmed devices)	-40 °C to 150 °C
T_{STG2}	Storage Temperature (programmed devices)	-40 °C to 125 °C
T_{LEAD}	Lead Temperature (10 sec)	260 °C
$P_{RF,i}$	Input RF level..	10 dBm
V_{DD}	Supply voltage	-0.3 V to 4 V
V_I	Voltage on input pins	-0.3 V to V_{DD} + 0.3 V

Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the Recommended Operating Conditions section of this specification are not guaranteed. Exposure to maximum ratings conditions for extended periods may affect device reliability. Data retention for a programmed device is better than 7 years at 125 °C.

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

RECOMMENDED OPERATING CONDITIONS

Parameter			Min	Nom	Max	Unit
T_J	Junction operating temperature		-35		90	°C
T_A	Ambient operating temperature [VI]		-35		85	°C
V_{DD}	Supply voltage		2.1		3.6	V
I_C	Continuous output current – one GPIO		-20		20	mA
I_{CTOT}	Total continuous output source/sink current – all GPIO's		-100		100	mA
T_{XTAL}	Total crystal tolerance [1)]		-27		27	ppm
f_{XTAL}	Crystal frequency			32 / 16		MHz
$C_{L,XTAL}$	Crystal load capacitance	16 MHz crystal	12	16	30	pF
		32 MHz crystal	10	16	18	pF

NOTES
[1)] The tolerance (initial tolerance, ageing, temperature dependency, etc.) will determine the frequency accuracy of the transmitted signal and will influence the receivers frequency lock range.

[VI] Thermal resistance (θ_{JA}) of the package is approx. 34 °C/W.

ELECTRICAL CHARACTERISTICS – POWER CONSUMPTION

Supply Current / Power Consumption (T_J=25 °C, V_{DD} =3.3 V)

Parameter	Condition	Min	Typ	Max	Unit
POWER MODES					
I_{VDD1} Sleep mode (Lowest Power) [1)]			2.5		µA
I_{VDD2} Normal mode (MCU on, RF off) [2)]			5.2		mA
I_{VDD3} Receiving [3)]			23		mA
I_{VDD4} Transmitting +0 dBm [4)]			36		mA
I_{VDD5} Transmitting -5 dBm [5)]			24		mA
MODULES IN ON/OFF [6)]					
I_{ADC} ADC supply current [7)]			150		µA

NOTES

[1)] Lowest possible power configuration. The ADC, RF transceiver, MCU and flash are shut down. The chip can be woken by brown-out, an external reset pulse, external interrupt (if enabled) or periodical wakeup by WUT (if enabled).

[2)] Normal mode. The MCU is running a simple 'while 1;'-loop. The crystal is 32 MHz. The ADC and the RF transceiver are off.

[3)] Receive Mode. The RF transceiver is in receive mode with the MCU running. The ADC is off. The crystal is 32 MHz.

[4)] Transmission Mode with +0 dBm output power (power setting 0x2A / ZetupRF: High power, setting 10) measured on a Z-Wave™ Module PCB (refer to footnote [VII]). The RF transceiver is in transmit mode with the MCU running. The ADC is off. The crystal is 32 MHz.

[5)] Transmission Mode with –5 dBm output power (power setting 0x1B / ZetupRF: Low power, setting 11) measured on a Z-Wave™ Module PCB (refer to footnote [VII]). The RF transceiver is in transmit mode with the MCU running. The ADC is off. The crystal is 32 MHz.

[6)] Current consumption of sub-circuits that can be shut down or set in power saving mode.

[7)] With the ADC in continuous mode and not using bandgap reference and input buffer.

[VII] The Z-Wave Module is a PCB developed by Zensys that implements the typical application as stated on Figure 4.

ELECTRICAL CHARACTERISTICS - DC

DC Characteristics (T_J=25 °C, V_{DD} =2.1 V to 3.6 V, unless otherwise specified)

Parameter	Condition	Min	Typ	Max	Unit
POWER-ON-RESET (POR)					
$V_{th,PO}$ Threshold, power up	T_J= -35 °C to 85 °C	1.84		2.10	V
$V_{th,R}$ Threshold, reset (brown out)	T_J= -35 °C to 85 °C	1.80		2.06	V
V_h Hysteresis	T_J= -35 °C to 85 °C	27		37	mV
CLOCK OSCILLATOR					
C_{XI} Parasitic input capacitance			2.4		pF
DIGITAL INPUTS					
I_{IH} High-level input current	$V_{IH}=V_{DD}$			20	nA
I_{IL} Low-level input current	V_{IL}=0V, no pull-up [1]	-20			nA
I_{ILpMn} Low-level input current	V_{IL}=0V, V_{DD}=2.1V, pull-up [1]	-27	-18	-11	µA
I_{ILpTp} Low-level input current	V_{IL}=0V, V_{DD}=3.3V, pull-up [1]	-67	-48	-33	µA
I_{ILpMx} Low-level input current	V_{IL}=0V, V_{DD}=3.6V, pull-up [1]	-78	-57	-40	µA
RESET_N, Px.y except P0.0					
V_{IH} High-level input voltage	T_J= -35 °C to 85 °C	0.7·V_{DD}			V
V_{IL} Low-level input voltage	T_J= -35 °C to 85 °C			0.3·V_{DD}	V
P0.0/ZEROX [2]					
V_{T+} Positive-going threshold	V_{DD} = 3.3 V		1.47		V
V_{T-} Negative-going threshold	V_{DD} = 3.3 V		1.00		V
V_H Hysteresis voltage (V_{T+}-V_{T-})	V_{DD} = 3.3 V		0.47		V
DIGITAL OUTPUTS					
V_{OH} High-level output voltage	I_{OH}=6 mA, T_A= -35 °C to 85 °C	V_{DD} – 0.6			V
V_{OL} Low-level output voltage	I_{OL}=-6 mA, T_A= -35 °C to 85 °C			0.4	V
DIGITAL INPUTS					
C_{DI} Input capacitance				5	pF
ADC					
I_{il} Input leakage current	V_{DD} = 3.3 V			20	nA
V_I Input voltage range [3]		GND		V_{DD}	V
C_I Input capacitance	Internal buffer disabled		30		pF
C_{IB} Input capacitance w. buffer	Internal buffer enabled		2		pF
V_{Ru} External upper reference		V_{DD} – 0.9		V_{DD}	V
V_{Rl} External lower reference		0		1.4	V
R_{Ref} Internal ref. resistance	Between ref. terminals	90	100	110	kΩ
C Crosstalk between channels	V_{DD} = 3.3 V			1	LSB
V_{Ref} Internal Reference voltage	T_J= -35 °C to 85 °C	1.13	1.21	1.29	V
12 bit resolution					
INL Integral nonlinearity	Reference = V_{DD} = 3.3 V	-5	±3	5	LSB
DNL Differential nonlinearity [4]	Reference = V_{DD} = 3.3 V	-1	±0.5	1	LSB
O_{Er} Offset error	Reference = V_{DD} = 3.3 V	-5	±2	5	LSB
E_g Gain error	Reference = V_{DD} = 3.3 V	-5	±1	5	LSB
8 bit resolution					
INL Integral nonlinearity	Reference = V_{DD} = 3.3 V	-2	±1	2	LSB
DNL Differential nonlinearity [4]	Reference = V_{DD} = 3.3 V	-1	±0.5	1	LSB
O_{Er} Offset error	Reference = V_{DD} = 3.3 V	-2	±0.5	2	LSB
E_g Gain error	Reference = V_{DD} = 3.3 V	-2	±0.5	2	LSB

NOTES

[1] Internal pull-up for *RESET_N* is always enabled

[2] Schmitt trigger input

[3] Valid for P0.1, P1.0 and P1.1. For P0.0 use V_{Ru}. If the internal buffer is enabled the rail to rail performance will be degraded by up to 100 mV for both ends.

[4] No missing codes.

Output Characteristic

The **ZW0201** GPIO's are slew rate limited and have a typical drive capability as indicated on Figure 23.

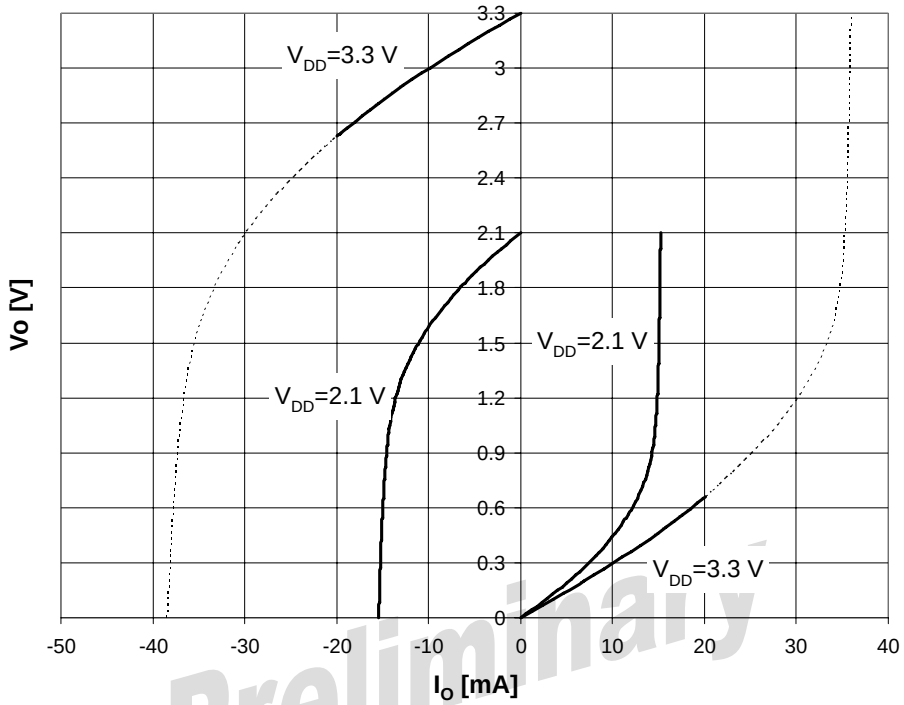


Figure 23: Typical output characteristic (T_J=25 °C)

ELECTRICAL CHARACTERISTICS - AC

AC Characteristics (C_L=50 pF, T_J=25 °C, V_{DD} =2.1 V to 3.6 V)

Parameter	Condition	Min	Typ	Max	Unit
POWER-ON-RESET (POR)					
G Glitch immunity[1)]		250	1000	2000	nVs
RISE/FALL TIME					
Px.y					
t_r Rise time	10% to 90%		5	9	ns
t_f Fall time	90% to 10%		5	9	ns

NOTES

[1)] Glitch immunity: Maximum transient duration multiplied by threshold overdrive without causing a reset pulse (i.e.: 1000 nVs glitch immunity ⇒ a 10 µs transient of 100 mV below threshold will not cause a reset pulse)

Capacitive Loading

Figure 24 shows the typical capacitive loading characteristic for the **ZW0201**

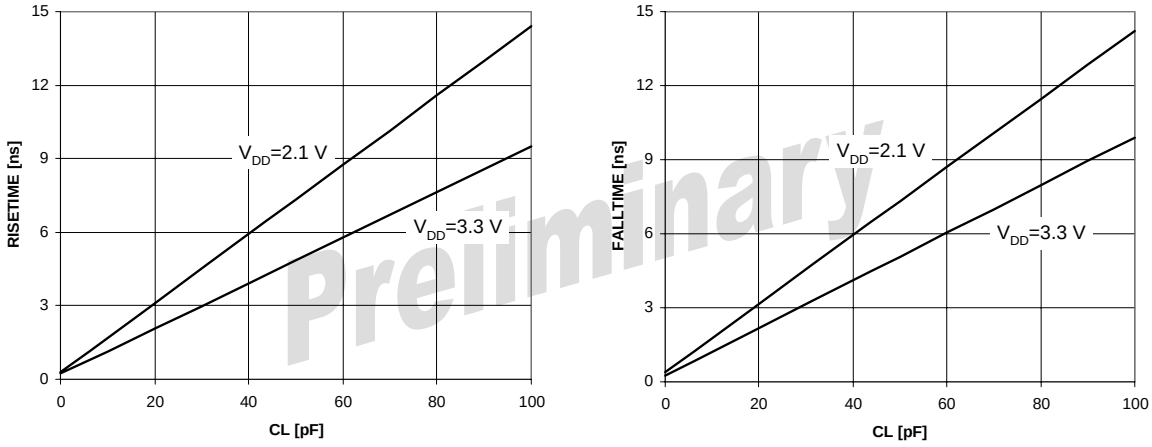


Figure 24: Typical rise / fall time vs. capacitive loading (T_J=25 °C, V_{DD}=3.3 V)

ELECTRICAL CHARACTERISTICS - RF

RF Characteristics (T_J= -35 °C to 85 °C, V_{DD} =2.1 V to 3.6 V, TX matched on *TX_IND*, RX matched on *RX_IND*, 50 Ω load on *RF_IO*)

Parameter		Condition	Min	Typ	Max	Unit
GENERAL						
F_{EU}	RF frequency EU	9.6 kbit/s		868.42		MHz
		40 kbit/s		868.40		MHz
F_{US}	RF frequency US	9.6 kbit/s		908.42		MHz
		40 kbit/s		908.40		MHz
TRANSMIT						
$P_{RF,oMx}$	Max output power [1]	High power mode		0		dBm
$P_{RF,oMx}$	Max output power [2]	High power mode		-2		dBm
$P_{RF,oMx}$	Max output power [3]	Low power mode		-5		dBm
$P_{RF,oMx}$	Max output power [4]	Low power mode		-7		dBm
$P_{RF,oMn}$	Min output power [5]			-20		dBm
P_S	Output power step size			2		dBm
$Z_{RF,o}$	RF output impedance			50		Ω
P_{h2}	2nd harmonics content [1, 6]			-47	-44	dBm
P_{h3}	3rd harmonics content [1, 6]			-30	-27	dBm
RECEIVE						
$P_{RF,Mx}$	Maximum input power				10	dBm
$P_{RF,9.6k}$	Sensitivity at 9.6 kbit/s [7]			-104		dBm
$P_{RF,9.6k}$	Sensitivity at 40 kbit/s [7]			-101		dBm
$P_{RF,L}$	LO leakage				-88	dBm
$Z_{RF,i}$	RF input impedance			50		Ω
IIP3	IIP3 [8]		-8,5	-6	-4,5	dBm
P_{CJ}	Co-channel rejection			6		dB
P_{B1}	Blocking, 1 MHz	3 dB above sensitivity limit		-55		dBm
P_{B2}	Blocking, 2 MHz	3 dB above sensitivity limit		-36		dBm
P_{B3}	Blocking, 5 MHz	3 dB above sensitivity limit		-28		dBm
P_{B4}	Blocking, 10 MHz	3 dB above sensitivity limit		-26		dBm
P_{B5}	Blocking, 100 MHz	3 dB above sensitivity limit		-24		dBm
FREQUENCY SYNTHESISER						
N_p	Output signal phase noise	150 kHz offset from carrier		-102		dBc /Hz

NOTES
[1] Power setting 0x2A. Specified in ZetupRF as “High power”, setting 10.
[2] Power setting 0x29. Specified in ZetupRF as “High power”, setting 9.
[3] Power setting 0x1B. Specified in ZetupRF as “Low power”, setting 11.
[4] Power setting 0x1A. Specified in ZetupRF as “Low power”, setting 10.
[5] Power setting 0x14. Specified in ZetupRF as “Low power”, setting 4
[6] Depends on the external matching components.
[7] Measured with Z-wave™ frames. FER (frame error rate) better than 10^{-2}. The sensitivity is measured at the IF center frequency (180 kHz for Manchester and 200 kHz for NRZ).
[8] Measured with $f_{spurious1} = f_{RF} + 20$ MHz and $f_{spurious2} = f_{RF} + 40$ MHz.

TIMING PARAMETERS

(T_J=25 °C, V_{DD}=3.3 V)

Parameter		Condition	Min	Typ	Max	Unit
POWER-ON-RESET (POR)						
t_P	Minimum reset pulse		29		175	µs
SYSTEM RESET						
t_{reset}	Min. reset pulse on *RESET_N* [1)]		50			ns
CLOCK OSCILLATOR						
t_{SON}	Turn-on time	32 MHz			5	ms
		16 MHz			3	ms
ADC						
f_s	Conversion time	8 bit	-	42	-	µs
		12 bit	-	92	-	µs
WUT						
E_{WUT}	Wake up time precision	10 seconds interval	-0.15	0.25	0.65	%
UART						
E_{UART}	UART RX baud rate tolerance		-2		2	%
SPI						
f_{SCK}	SCK frequency		0.5		4.0	MHz
D	SCK duty cycle		40		60	%
t_{Rise}	SCK rise time	10% to 90%			T_{XTAL} [1)]	
t_{Fall}	SCK fall time	90% to 10%			T_{XTAL} [1)]	
t_{Setup}	Data setup Time		62.5			Ns
t_{Hold}	Data hold Time		62.5			Ns
t_{Data}	Delay from SCK falling edge to valid data				62.5	ns
t_{ResetP}	Min. time of asserting *RESET_N* before entering prog. mode		$2^{17} \cdot T_{XTAL}$ [1)]			

NOTES
[1)] The T_{XTAL} is the period of clock oscillator frequency (= 1/ f_{XTAL}).

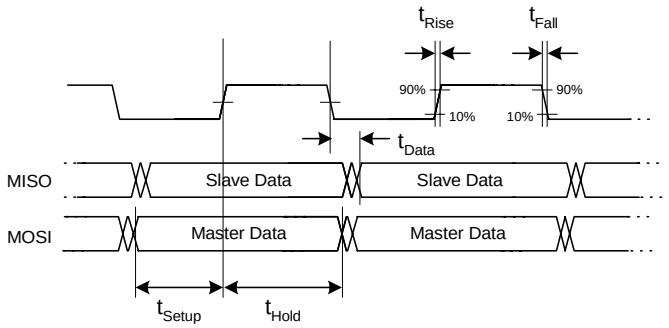
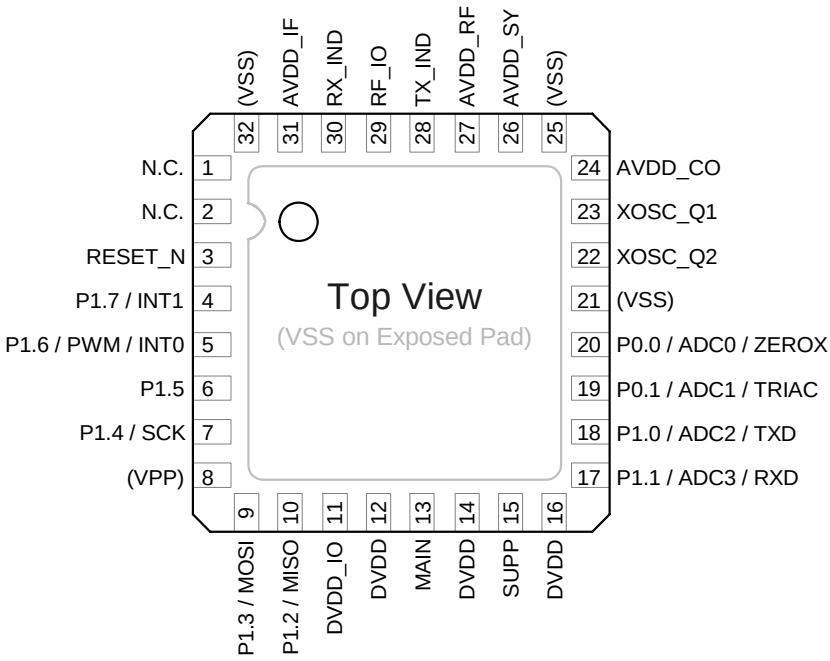


Figure 25: SPI timing

PIN CONFIGURATION

(32 PINS QFN, TOPVIEW)



Pin	Pin Name	Pin Type
E.P.[1]	VSS	Power
1	N.C. [2]	-
2	N.C. [2]	-
3	RESET_N	Digital input [3]
4	P1.7/INT1	Digital tristate I/O
5	P1.6/PWM/INT0	Digital tristate I/O
6	P1.5	Digital tristate I/O
7	P1.4/SCK	Digital tristate I/O
8	(VPP)	Reserved (connected to VSS internally)
9	P1.3/MOSI	Digital tristate I/O
10	P1.2/MISO	Digital tristate I/O
11	DVDD_IO	Power
12	DVDD	Power
13	MAIN	Power
14	DVDD	Power
15	SUPP	Power
16	DVDD	Power
17	P1.1/ADC3/RXD	Digital tristate I/O / analogue input

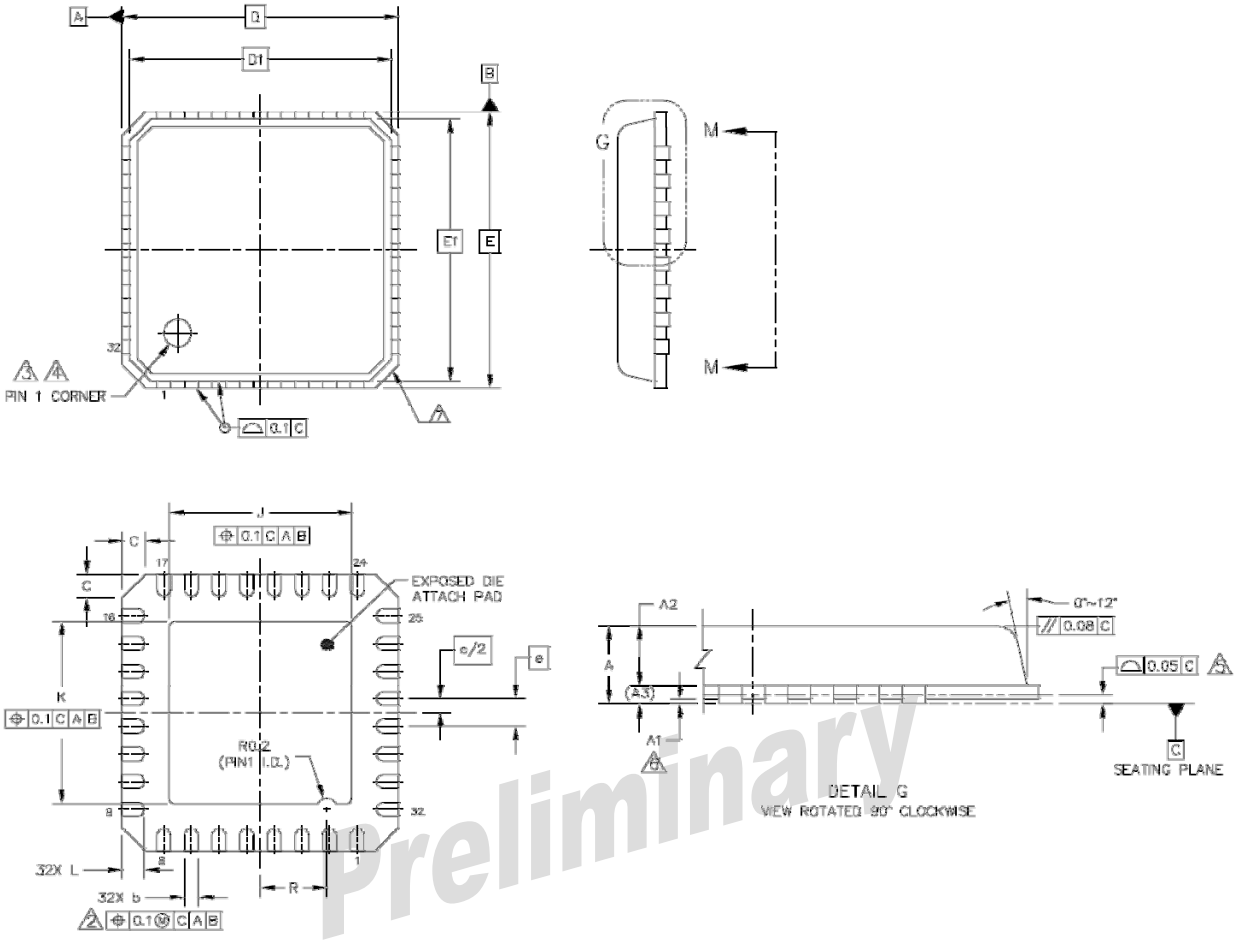
Pin	Pin Name	Pin Type
18	P1.0/ADC2/TXD	Digital tristate I/O / analogue input
19	P0.1/ADC1/TRIAC	Digital tristate I/O / analogue input
20	P0.0/ADC0/ZEROX	Digital tristate I/O [3] / analogue input
21	(VSS)	(Power)
22	XOSC_Q2	Analogue output
23	XOSC_Q1	Analogue input
24	AVDD_CO	Power
25	(VSS)	(Power)
26	AVDD_SY	Power
27	AVDD_RF	Power
28	TX_IND	RF
29	RF_IO	RF
30	RX_IND	RF
31	AVDD_IF	Power
32	(VSS)	Power, optional [4]

NOTES
[1] Exposed pad at bottom of chip.
[2] No connect. Leave pin unconnected.
[3] Schmitt trigger input.
[4] VSS pins 21, 25 and 32 are internally connected to the exposed pad. Connection of these pins to ground is optional.

IMPORTANT: Pin 8 is reserved for compatibility with future cost reduction chips. These will require a specific voltage to be applied to pin 8 during programming. In applications where the chip is programmed on the PCB pin 8 should be connected to a test pad on the PCB. This test pad must be accesible during programming. If the chip is always programmed prior to soldering it on the PCB pin 8 can be left unconnected. Any other design will require a PCB modification before the cost reduction can be implemented.

PACKAGE OUTLINE DIMENSIONS

(32 PINS PUNCHED QFN 5x5 mm, TOPVIEW, REF: JEDEC-MO-220-F)



Symbol	Min.	Nom.	Max.	Unit	Remark
A	0.8		0.9	mm	Package height
A1	0	0.02	0.05	mm	
A2	0.65		0.69	mm	
A3		0.203 REF.		mm	
b	0.18	0.25	0.3	mm	
C	0.24	0.42	0.6	mm	
D		5 BSC		mm	Outer body size
D1		4.75 BSC		mm	
E		5 BSC		mm	Outer body size
E1		4.75 BSC		mm	
e		0.5		mm	Pin pitch
J	3.2	3.3	3.4	mm	Exposed pad size
K	3.2	3.3	3.4	mm	Exposed pad size
L	0.30	0.40	0.50	mm	
R	1.1	1.2	1.3	mm	
M		0.07		g	Weight

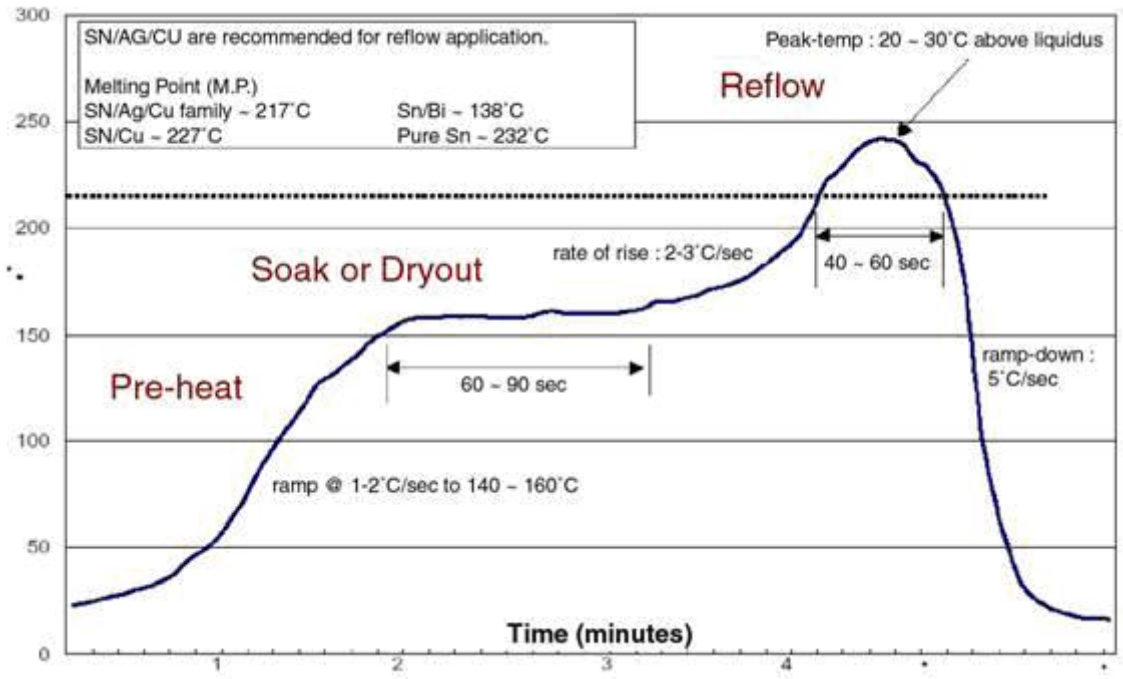
DEVICE MARKING

Marking	Meaning
R	Version number
CCCC	Date code (year, week)
B	Wafer lot code (identifier)
P	Package/test plant identification code

PROCESS SPECIFICATION

Specification	Description
MSL-3	Moisture Level Verification tested according to JEDEC J-STD-020C
RoHS	Designed in compliance with The Restiction of Hazardous Substances Directive (RoHS)

Reflow Profile



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