Description

The ZWIR4532 is a programmable low-power secure IPv6 communication module for internet of things (IOT) device networks. Sensors and devices can operate autonomously or connect to local or global IPv6 networks using the ZWIR4532. The ZWIR4532 serves as a universal secure radio communication module for applications with low bandwidth requirements.

The module incorporates an ultra-low-power ARM® Cortex™-M0+ 32-bit microcontroller which is running the network stack. In addition, the user application can run on the microcontroller. This helps minimizing the size, complexity and overall BOM. A rich set of digital and analog peripherals is available for interfacing with external application components. Approximately 128kB of flash and 4kB of RAM are available for user applications.

IDT offers the SensorShare user programmable royalty-free 6LoWPAN network stack with mesh routing capability for the ZWIR4532. 6LoWPAN is an Internet Engineering Task Force (IETF) standard for wireless low-power IPv6-based sensor and device networks.

Secure communication is provided by a standard-compliant implementation of the Internet Protocol Security (IPSec) protocol suite.

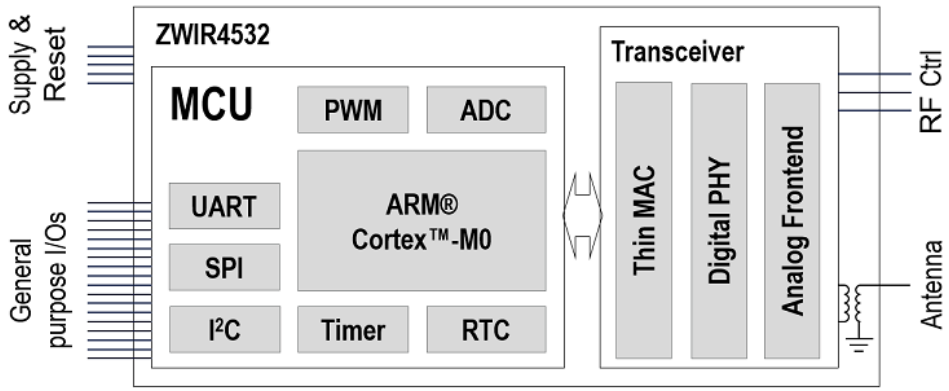
Typical Applications

- Industrial automation
- Home and building automation
- Health monitoring
- Telemetry

Features

- License-free 868/915 MHz frequency bands
  - 4 channels in EU frequency band (865.3 – 868.3 MHz)
  - 10 channels in US frequency band (906 – 924 MHz)
  - BPSK or O-QPSK modulation selectable
    - BPSK with 20kBps EU and 40kBps U
- ARM® Cortex™-M0+ 32-bit ultra-low-power microcontroller
  - 192kB flash and 20kB RAM
  - 6kByte EEPROM
  - 5 UART interfaces
  - 1 SPI interface
  - 3 I²C interfaces
  - 10 PWM outputs
  - 12 bit ADC with 10 input channels
  - 2 analog comparators
  - 31 GPIOs
- Network Stack
  - UDP/IPv6 communication
  - Mesh networking with hundreds of nodes
  - Self-healing defective routes
  - Over-the-Air update capable
  - Network layer security
- Ultra-low power stop mode: < 1µA with full RAM retention
- Supply voltage: 1.8V to 3.3V
- -40°C to +85°C ambient operating temperature
- 15.6 × 12 mm 43-LGA Package

Block Diagram



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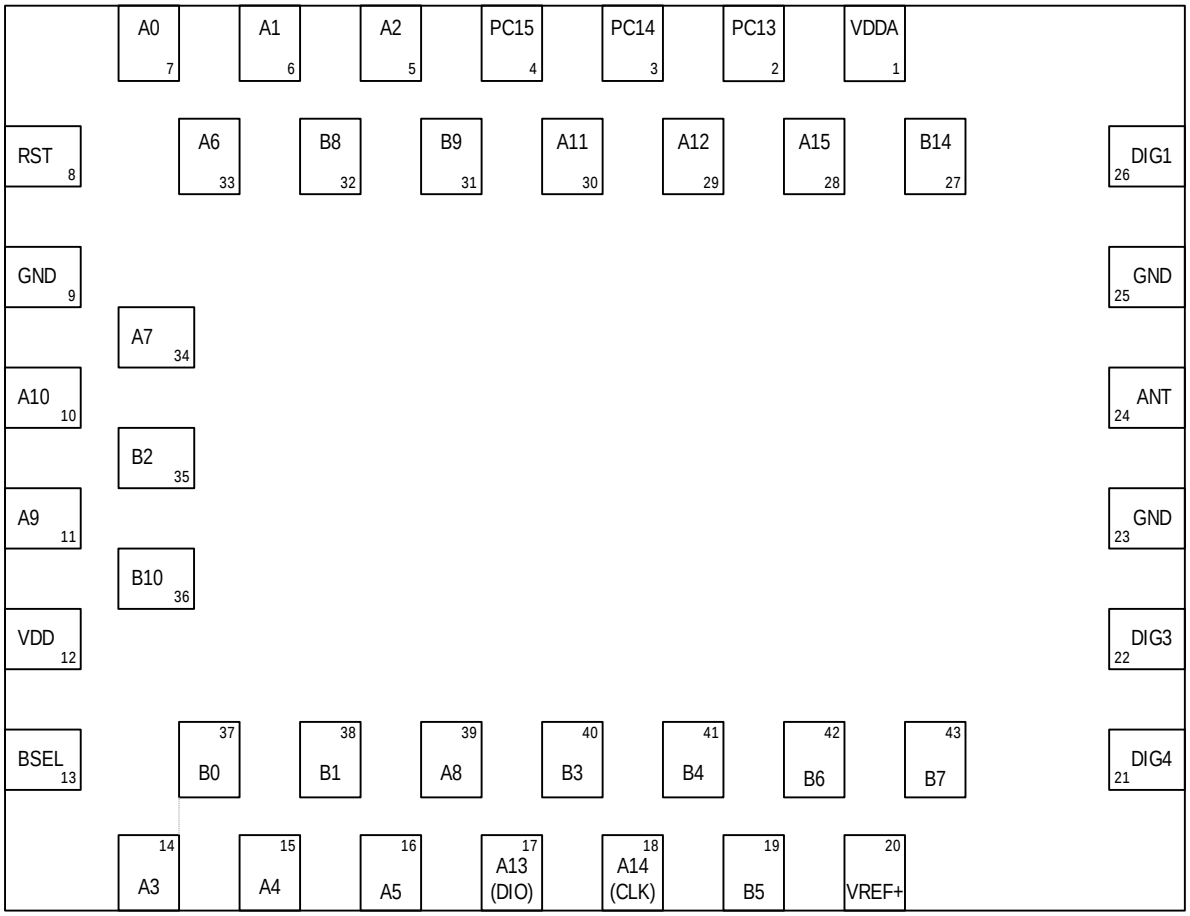
1. Pin Assignments

Figure 1. Pin Assignments for 15.6mm × 12.0mm LGA Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	5V	Description
1	VDDA	Supply		
2	PC13	GPIO	Y	RTC Tamper, TRC Timestamp, RTC output, Wakeup 2.
3	PC14	GPIO	Y	OSC32 In.
4	PC15	GPIO	TC	OSC32 Out.
5	PA2	GPIO	Y	Timer21 Ch1, Timer2 Ch3, USRT2 TX, LPUART1 TX, COMP2 Output, COMP2 INM, ADC Ch2.
6	PA1	GPIO	Y	Event Out, Timer2 Ch2, USART2 RTS/DE, TIM21 ETR, USART4 RX, COMP1 Input, ADC Ch1.
7	PA0	GPIO		Timer 2 Ch1, Timer 2 ETR, USART2 CTS, USART4 TX, COMP1 OUT, COMP1 INM, ADC Ch 0, RTC Tamper 2, Wakeup 1.

Pin Number	Name	Type	5V	Description
8	RST	I/O		Device reset, low active.
9	GND	Ground		
10	PA10	GPIO	Y	USART1 RX, I2C1 SDA.
11	PA9	GPIO	Y	MCO, USART1 TX, I2C1 SCL, I2C3 SMBA.
12	VDD	Supply		
13	BSEL	I		
14	PA3	GPIO	Y	Timer21 Ch2, Timer2 Ch4, USART2 RX, LPUART1 RX, COMP2 INP, ADC Ch3.
15	PA4	GPIO	N	SPI1 NSS, USART2 CK, Timer22 ETR, COMP1 INM, COMP2 INM, ADC Ch4.
16	PA5	GPIO	N	SPI1 SCK, Timer2 ETR, Timer2 Ch1, COMP1 INM, COMP2 INM, ADC Ch5.
17	PA13	GPIO	Y	SWDIO, LPUART1 RX.
18	PA14	GPIO	Y	SWCLK, USART2 TX, LPUART1 TX.
19	PB5	GPIO	Y	SPI1 MOSI, LPTimer1 In1, I2C1 SMBA, Timer3 Ch2, Timer22 Ch2, USART1 CK, USART5 CK, USART5 RTS/DE, Comp2 INP.
20	VREF+	Supply		
21	PA-	O		Differential power amplifier control output, internally tied to ground if not used. Leave unconnected if not used.
22	PA+	O		
23	GND	Ground		
24	ANT	Antenna		Antenna pin.
25	GND	Ground		
26	DIG1	O		
27	PB14	GPIO	Y	SPI2 MISO, I2S2 MCK, RTC Out, LPUART1 RTS/DE, I2C2 SDA, Timer21 Ch2.
28	PA15	GPIO	Y	SPI1 NSS, Timer2 ETR, Event Out, USART2 RX, Timer2 Ch1, USART4 RTS/DE.
29	PA12	GPIO	Y	SPI1 MOSI, Event Out, USART1 RTS/DE, COMP2 Out.
30	PA11	GPIO	Y	SPI1 MISO, Event Out, USART1 CTS, COMP1 Out.
31	PB9	GPIO	Y	Event Out, I2C1 SDA, SPI2 NSS, I2S2 WS.
32	PB8	GPIO	Y	I2C1 SCL.
33	PA6	GPIO	Y	SPI1 MISO, Timer3 Ch1, LPUART1 CTS, Timer22 Ch1, Event Out, COMP1 Out, ADC Ch6.
34	PA7	GPIO	Y	SPI1 MOSI, Timer3 Ch2, Timer22 Ch2, Event Out, COMP2 Out, ADC Ch7.
35	PB2	GPIO	Y	LPTimer 1 Out, I2C3 SMBA.
36	PB10	GPIO	Y	Timer 2 Ch3, LPUART1 TX, SPI2 SCK, I2C2 SCL, LPUART1 RX.
37	PB0	GPIO	Y	Event Out, Timer3 Ch3, ADC Ch8, VREF Out.
38	PB1	GPIO	Y	Timer3 Ch4, LPART1 RTS/DE, ADC Ch9, VREF Out.
39	PA8	GPIO	Y	MCO, Event Out, USART1 CK, I2C3 SCL.
40	PB3	GPIO	Y	SPI1 SCK, Timer2 Ch2, Event Out, USART2 RTS/DE, USART5 TX, COMP2 INM.

Pin Number	Name	Type	5V	Description
41	PB4	GPIO	Y	SPI1 MISO, Timer3 Ch1, Timer22 Ch1, USART1 CTS, USART5 RX, I2C3 SDA, COMP2 INP.
42	PB6	GPIO	Y	USART1 TX, I2C1 SCL, LPTimer1 ETR, COMP2 INP.
43	PB7	GPIO	Y	USART1 RX, I2C1 SDA, LPTimer1 In2, USART4 CTS, COMP2 INP, VREF PVD In.

Table 2. Module Pins Peripheral Function Mapping

MCU Port		Port A																Port B											
MCU Port Pin		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	14
Module Pin		7	6	5	14	15	16	33	34	39	11	10	30	29	17	18	28	37	38	35	40	41	19	42	43	32	31	36	27
USART1	TX										4													0						
	RX											4													0					
	RTS													4							5									
	CTS												4									5								
	CK									4													5							
USART2	TX			4												4														
	RX				4												4													
	RTS		4																											
	CTS	4																												
	CK					4																								
USART4	TX	6																												
	RX		6																											
	RTS																6													
	CTS																								6					
USART5	TX																				6									
	RX																					6								
	CK																						6							
LPUART1	TX			6												6												4		
	RX				6										6															
	RTS																		4									7		
	CTS							4																						
SPI1	MOSI								0					0									0							
	MISO							0					0									0								
	SCK						0														0									
	NSS					0											0													
I2C1	SCL										6													1		4				
	SDA											6													1		4			
I2C2	SCL																											6		
	SDA																												5	
I2C3	SCL									7																				
	SDA																					7								
TIM2	Ch1	2					5										5													
	Ch2		2																		2									
	Ch3			2																								2		
	Ch4				2																									
	ETR	5					2										2													
TIM3	Ch1							2														2								
	Ch2								2														4							
	Ch3																	2												
	Ch4																		2											
TIM21	Ch1			0																										
	Ch2				0																									
	ETR		5																											
TIM22	Ch1							5														4								
	Ch2								5														4							
	ETR					5																								
LPTIM1	IN1																						2							
	IN2																								2					
	OUT																			2										
	ETR																							2						
COMP 1	IN	M	P		P*	M	M															P*	P*	P*	P*					
	OUT	7						7					7																	
COMP 2	IN			M	P	M	M														M	P	P	P	P					
	OUT			7					7					7																
ADC_IN		0	1	2	3	4	5	6	7									8	9											
EVENTOUT			0					6	6	3			2	2			3	0			4						2			
MCO_OUT										0	0																			
SWD	IO														0															
	CLK															0														

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZWIR4532 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
T_S	Storage temperature	-50	150	°C
V_{ESD}	ESD – Human Body Model	-	2000	V
	ESD – Charged Device Model	-	500	
$V_{DD} – V_{SS}$	External supply voltage	-0.3	3.6	
V_{IN}	Voltage on 5V tolerant input pin	$V_{SS} – 0.3$	$V_{DD} + 4.0$	
	Voltage on BSEL	V_{SS}	$V_{DD} + 4.0$	
	Voltage on any other input pin	$V_{SS} – 0.3$	4	
$\lvert V_{DDA} – V_{DD} \rvert$	Variation between V_{DDA} and V_{DD} power pins	-	300	mV
$V_{REF+} – V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	400	
I_{VDD}	Maximum total current consumption		140	mA
I_{GPIO}	Output current sunk by any I/O and control pin except FTf pins		16	
	Output current sunk by FTf pins		22	
	Output current sourced by any I/O and control pin		-16	
$\sum I_{GPIO}$	Total output current sunk by sum of all IOs and control pins except PA11 and PA12(2)		90	
	Total output current sunk by PA11 and PA12		25	
	Total output current sourced by sum of all IOs and control pins(2)		-90	
I_{INJ}	Injected current on FT, FFf, RST and B pins		-5 / +0	
	Injected current on TC pin		±5	
$\sum I_{INJ}$	Total injected current (sum of all I/O and control pins)(5)		±25	

4. Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter		Symbol	Minimum	Typical	Maximum	Units
Electrical Characteristics						
Main supply voltage – ADC used		V_{DD}	1.8		3.6	V
Digital I/O high level input voltage		V_{IH}	$0.7V_{DD}$			
Digital I/O low level input voltage		V_{IL}			$0.3V_{DD}$	
Digital I/O high level output voltage		V_{OH}	V_{DD} – 0.4			
Digital I/O low level output voltage		V_{OL}			0.4	
MCU Clock Characteristics						
MCU core clock frequency [1)]		f_{AHB}	8		32	MHz
MCU core clock frequency accuracy range		Δf_{AHB}	-2		2.5	%
MCU peripheral bus 1 clock frequency [2)]		f_{APB1}		4		MHz
MCU peripheral bus 2 clock frequency [2)]		f_{APB2}		8		
RF Parameters						
Frequency range		f_{RF}	865		928	MHz
Output power			-11			dBm
Output power tolerance			-3		+3	dB
Receiver sensitivity	BPSK, EU Mode			-110		dBm
	BPSK, US Mode			-108		
	QPSK, EU Mode			-101		
	QPSK, US Mode			-101		
Gross data rate	BPSK, EU Mode			20		kBit/s
	BPSK, US Mode			40		
	QPSK, EU Mode			100		
	QPSK, US Mode			250		
Channel spacing	EU Mode			1		MHz
	US Mode			2		
Number of channels	EU Mode [3)]			1 (+3)		
	US Mode			10		
Input/output impedance				50		Ω
Frequency offset			-10		+10	kHz

1) The f_{CORE} clock can be configured to be 8, 16 or 32 MHz. After reset, the clock is set to 8MHz.

2) f_{APB1} and f_{APB2} are derived from f_{AHB}. Therefore, the same tolerances apply to these clocks.

3) The IEEE802.15.4 standard defines only 1 channel for EU Mode, but extension channels are available in almost all EU countries.

5. Functional Overview

The ZWIR4532 is a programmable wireless IPv6 communication module which can host the user application. This removes the need for an external application processor, consequently minimizing space requirements, BOM cost and the potential for communication errors. Applications benefit from the mesh networking functionality, which allows covering large areas with a single network, even if the communicating nodes have no direct radio link. The mesh network stack takes care of routing packets through the network transparently for the application. Routing failures are detected and repaired automatically, thus, a failing node will not impair the overall network.

ZWIR4532 modules communicate using the User Datagram Protocol (UDP) over IPv6 (Internet Protocol version 6). They are interoperable with ZWIR45xx based networks. ZWIR45xx networks operate autonomously or integrate with nearly any existing computer network or the Internet. If integrated in an existing network, ZWIR45xx based devices are accessible in the same way as any other IPv6 networking device. Opposed to many competing solutions gateway devices connecting ZWIR45xx, networks are application independent and do not limit the network functionality to a certain scope.

IDT provides a C-based Application Programming Interface (API) which is linked with the user application. Besides standard networking, different supplemental and advanced functionalities are provided using a modular approach. This allows tailoring the network stack to the applications requirements. The list of features below summarizes the functionalities provided by IDTs network stack components.

- UDP/IPv6 network layer
  - Packet oriented communication with arbitrary number of communication partners
  - Support for multicast communication (communication targeted at more than one receiver)
  - Event based reception – incoming packets are handled in dedicated user defined callbacks1
- Highly configurable mesh-layer
  - Allows hundreds of nodes per network
  - Works out of the box for simple networks; allows tailoring for complex networks
- IPSec based security
  - Authentication and encryption
  - Allows real end-to-end secure communication (ZWIR-to-ZWIR, ZWIR-to-LAN or ZWIR-to-Internet)
  - Same technology as typically used in Virtual Private Networks (VPNs)
- Over-the-Air Updates
  - Updates enabled simply by linking OTAU library into application
  - Host library provided for easy update transmission from own applications
  - Standalone graphical frontend for update transmission provided
- Network monitoring and administration protocol
  - IDT protocol to analyze network topology and query device parameters and status
  - Extended version allows remote configuration of devices
- Hardware abstraction libraries
  - Different libraries providing a high level interfaces for the MCU hardware components

The prime design goal of the API has been ease of use. Detailed documentation of all network stack features can be found in the ZWIR45xx Programming Guide and the accompanying application notes.

The application firmware is executed on an ARM Cortex-M0+ 32 bit microcontroller (MCU). Applications have full access to the rich set of peripherals provided by this microcontroller. The list below summarizes the MCU features. Table 2 provides a detailed mapping of peripherals to GPIO pins.

- Internal RC or external crystal clock with up to 32MHz frequency
- 192kB of flash and 20kB of RAM memory – approximately 128kB flash and 4kB RAM available for user applications
- Communication interfaces: 4x U(S)ART, 1x UART, 1x SPI, 3x I2C
- 4 timers with up to 12 PWM inputs/outputs
- 12-bit ADC (10 channels accessible), 2 comparators
- RTC and Watchdog timer
- 7-channel DMA controller

5.1 Low Power Modes

The network stack provided for ZWIR4532 modules is designed to consume minimal power, even in active mode. If the module is idle in active operating mode, the MCU enters a low power mode to minimize its current consumption. All peripherals and the transceiver remain active and wake up the MCU from sleep mode as soon as an event occurs that needs to be serviced. Power consumption in active mode can be optimized further by adapting the clock frequency to the application needs.

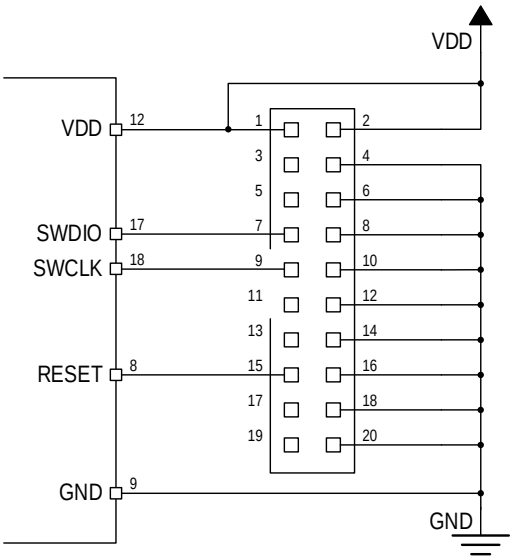
For battery operated devices the ultra-low-power Suspend Mode is provided. In this mode the transceiver and most of the MCUs peripherals are turned off. The MCU core resides in the ARM Corex-M0 stop mode. The total power consumption is lowered to less than 1µA while all RAM contents and application state is retained. Wake-up from Suspend mode is possible through external GPIOs or the internal Real-Time-Clock.

5.2 Device Programming and Debugging

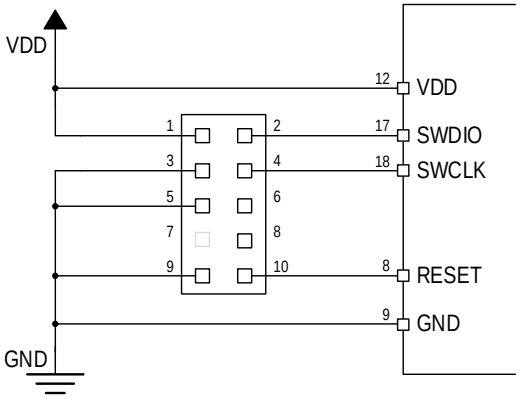
In system programming and debugging is supported through ARMs Serial Wire Debug (SWD) interface. SWD is a two wire interface designed as an alternative to the 4 wire JTAG interface. Figure 2 shows how SWD is connected to the ARM standard connectors. These connectors are supported by a wide variety of debug adaptors. Alternatively the microcontroller can be programmed using its embedded serial boot loader which allows programming through UART or SPI. However, no debugging functionality is available through this interface.

Figure 2. Serial Wire Debug Connection with Standard ARM Connectors

A) 20 Pin ARM Header



B) 10 Pin Cortex Debug Connector



6. Package Outline Drawing

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/zwir4532-package-outline-drawing-120-x-156-x-215-mm-body08mm-pitch-mod0

Figure 3. Package Outline Drawing (Top, Left and Bottom View)

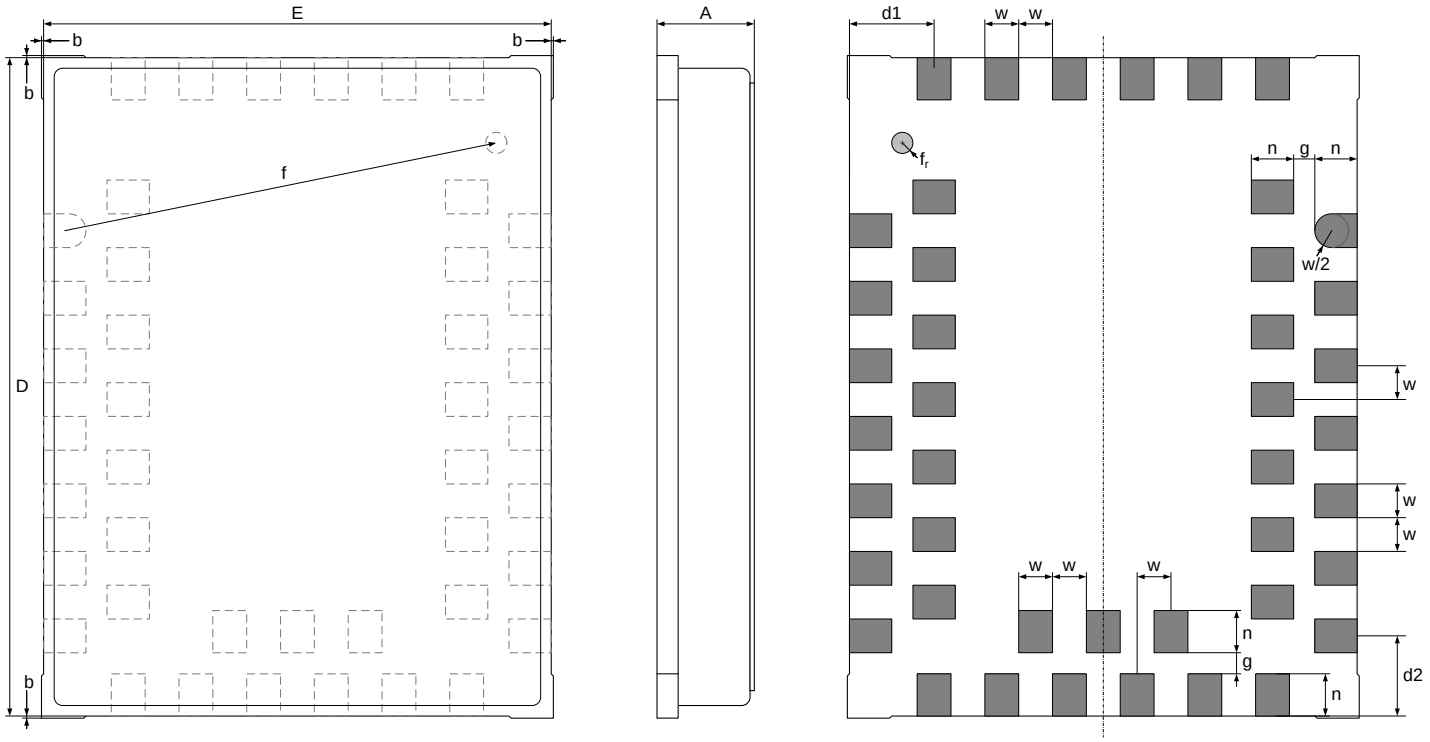


Table 5. ZWIR4532 Physical Dimensions and Tolerances

Symbol	Millimeters			Symbol	Millimeters		
	Minimum	Typical	Maximum		Minimum	Typical	Maximum
A	2.4	2.5	2.6	d1		2.0	
D	15.4	15.6	15.8	d2		1.9	
E	11.8	12.0	12.2	g		0.5	
w		0.8		f_x 1)		10.2	
n		1		f_y 1)		2.08	
b			0.3	f_r		0.25	

1) Fiducial mark position is relative to center point of pad 1.

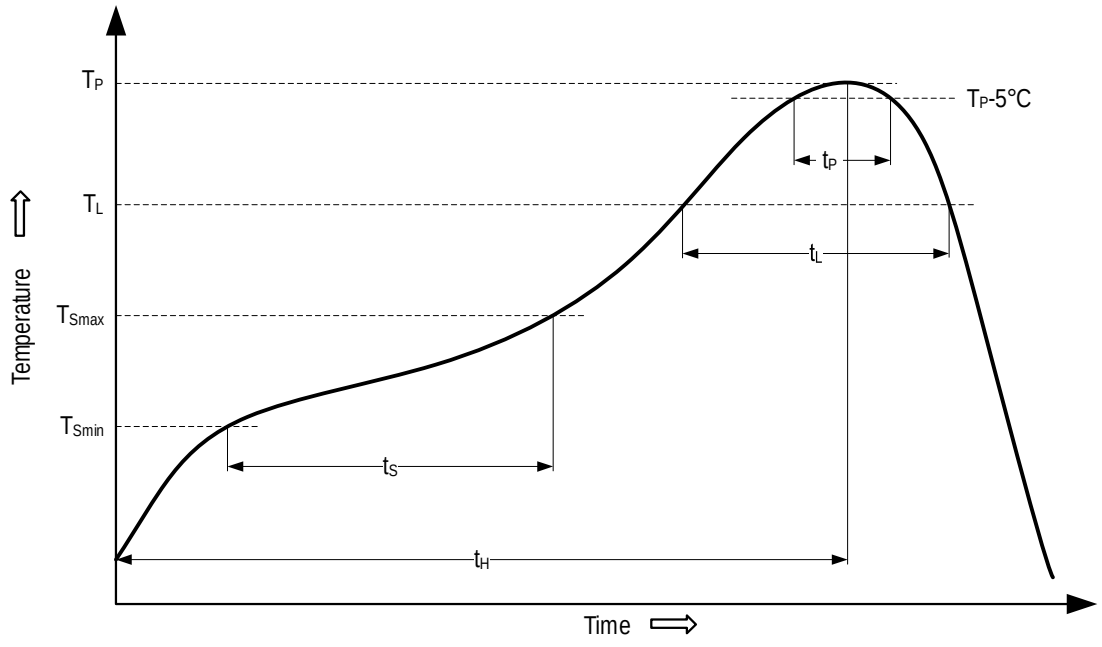
7. Soldering Information

To ensure that soldered connections do not break during the reflow soldering process of the application PCB, the soldering profile described in and Figure 4 must be maintained. This profile is aligned with the profile defined in the IPC/JEDEC standard J-STD-020D.

Table 6. Soldering Profile Parameters (according to J-STD-020D)

Profile Feature	Symbol	Minimum	Maximum	Units
Time 25°C to T_P	t_H		8	min
Peak package body temperature	T_P		260	°C
Preheat / Soak				
Soak temperature	T_S	100	150	°C
Soak time	t_S	60	120	s
Ramp-up				
Ramp-up rate	T_L to T_P		3	°C/s
Time maintained above T_L	t_L		150	s
Time within 5°C of T_P	t_P		30	s
Ramp-down				
Ramp-down rate	T_P to T_L		6	°C/s

Figure 4. Recommended Temperature Profile for Reflow Soldering (according to J-STD-020D)



8. Certification

8.1 European RED Statement

The ZWIR4532 module has been tested and found to comply with the Radio Equipment Directive and is subject of a notified body opinion. The module has been approved for antennas with gains of 4 dBi or less. If the module should be used with antennas with higher gain, the modular approval is void and the end product must be fully certified.

Important Notice: End products targeted at geographic regions which are covered by the RED must ensure that a transmission duty cycle of less than 1% is maintained during normal operation. The duty cycle observation period is one hour. That means the cumulated transmission time of all transmissions during normal operation must not exceed 36 seconds when observed over one hour. IDTs network stack provides duty cycle monitoring and alarm mechanisms to support software developers in meeting the duty cycle requirements. For detailed information please refer to the ZWIR45xx Programming Guide.

8.2 Federal Communication Commission Certification Statements

8.2.1 Statements

This equipment has been tested and found to comply with the limits for a Class B Digital Device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from where the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Modifications not expressly approved by ZMD AG could void the user's authority to operate the equipment.

The internal/external antennas used for this mobile transmitter must provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

8.2.2 Requirements

The ZWIR4532 complies with Part 15 of the FCC rules and regulations. In order to retain compliance with the FCC certification requirements, the following conditions must be met:

1. Modules must be installed by original equipment manufacturers (OEM) only.
2. The module must only be operated with antennas adhering to the requirements defined in section 8.2.3
3. The OEM must place a clearly visible text label on the outside of the end-product containing the text shown in Figure 5, below.

IMPORTANT: The compliance statement as shown in Figure 5 must be used without modifications for the ZWIR4532 product.

Figure 5. FCC Compliance Statement to be Printed on Equipment Incorporating ZWIR4532 Devices

Contains FCC ID: COR-ZWIR4532

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

8.2.3 Supported Antennas

The FCC compliance testing of the ZWIR4532 has been carried out using the MEXE902RPSM antenna from PCTEL Inc. This antenna has an omnidirectional radiation pattern at an antenna gain of 2 dBi. In order to be allowed to use the module without re-certification, the product incorporating the ZWIR4532 module must either use the antenna mentioned above or must use an antenna with an omnidirectional radiation pattern and a gain being less than or equal to 2 dBi.

9. Ordering Information

Orderable Part Number	Description and Package	Carrier Type	Temperature
ZWIR4532-U	6LoWPAN wireless radio module, unprogrammed 15.6 × 12 × 2.5 mm 43-LGA	Tape/Reel	-40°C to +85°C
ZWIR4532-S001	6LoWPAN wireless radio module, standard firmware 15.6 × 12 × 2.5 mm 43-LGA	Tape/Reel	-40°C to +85°C

10. Revision History

Revision Date	Description of Change
August 30, 2018	Initial release.

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1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
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ZWIR4532 Package Outline Drawing

12.0 x 15.6 x 2.15 mm Body,0.8mm Pitch

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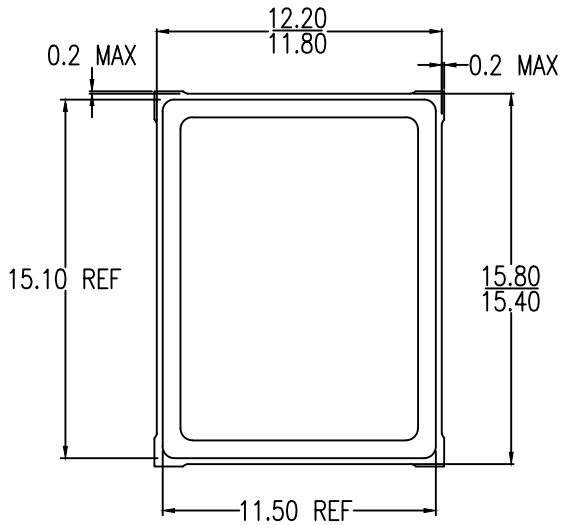
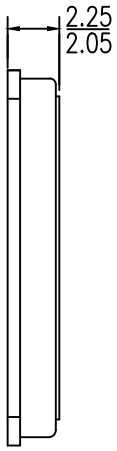
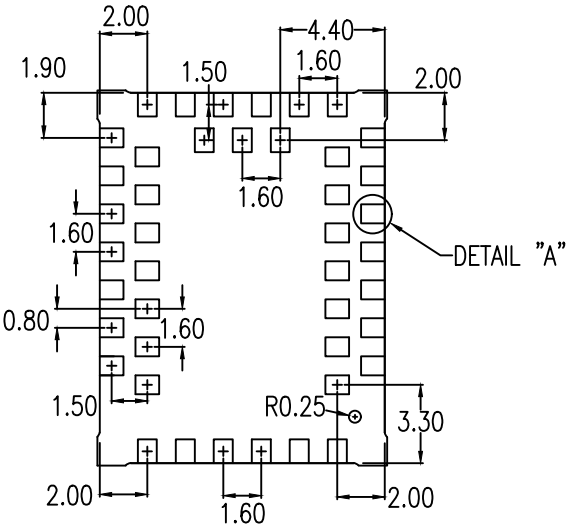


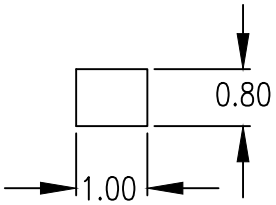
TOP VIEW



SIDE VIEW



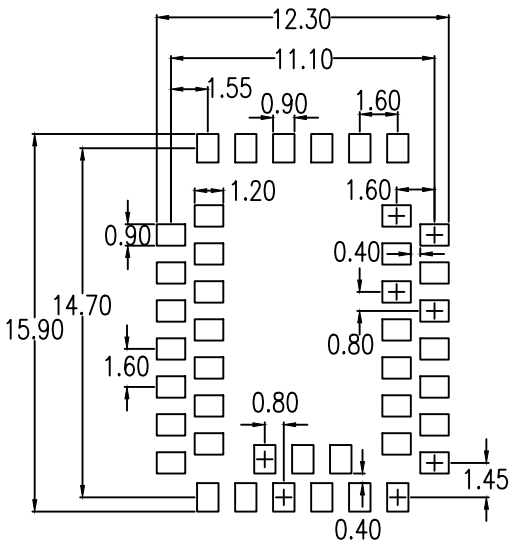
BOTTOM VIEW



DETAIL "A"

(SAME DIMENSION FOR ALL PINS)

NOTE: ALL DIMENSIONS AND ANGLES IN MM.



LAND PATTERN DIMENSION

NOTE:
1. ALL DIMENSIONS AND ANGLES IN MM.

Package Revision History		
Date Created	Rev No.	Description
July 13, 2018	Rev 00	Initial Release