AUTOMOTIVE COMPLIANT 60V HIGH ACCURACY BUCK/ BOOST/BUCK-BOOST LED DRIVER-CONTROLLER

Description

The ZXLD1371Q is an LED driver controller IC for driving external MOSFETs to drive high current LEDs. It is a multi-topology controller enabling it to efficiently control the current through series connected LEDs. The multi-topology enables it to operate in buck, boost and buck-boost configurations.

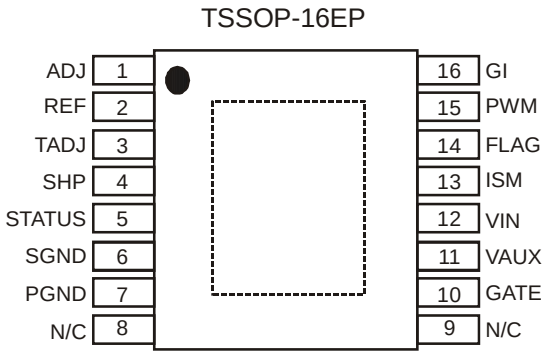
The 60V capability coupled with its multi-topology capability enables it to be used in a wide range of applications and drive in excess of 15 LEDs in series.

The ZXLD1371Q is a modified hysteretic controller using a patent pending control scheme providing high output current accuracy in all three modes of operation. High accuracy dimming is achieved through DC control and high frequency PWM control.

The ZXLD1371Q uses two pins for fault diagnosis. A flag output highlights a fault, while the multi-level status pin gives further information on the exact fault.

The ZXLD1371Q has been qualified to AEC-Q100 Grade 1 and is Automotive Grade supporting PPAPs.

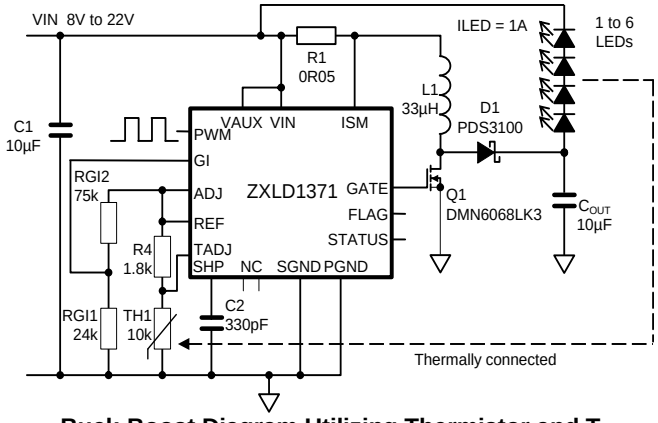
Pin Assignments



Features

- 0.5% Typical Output Current Accuracy
- 5 to 60V Operating Voltage Range
- LED Driver Supports Buck, Boost and Buck-Boost Configurations
- Wide Dynamic Range Dimming
  - 10:1 DC Dimming
  - 1000:1 Dimming Range at 500Hz
- Up to 1MHz Switching
- High Temperature Control of LED Current Using T_{ADJ}
- Available in Thermally Enhanced TSSOP-16EP Package with Green Molding Compound
  - **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
  - **Halogen and Antimony Free. "Green" Device (Note 3)**
- Automotive Grade
  - **Qualified to AEC-Q100 Standards for High Reliability**
  - TS16949 Certification
  - **PPAP Capable (Note 4)**

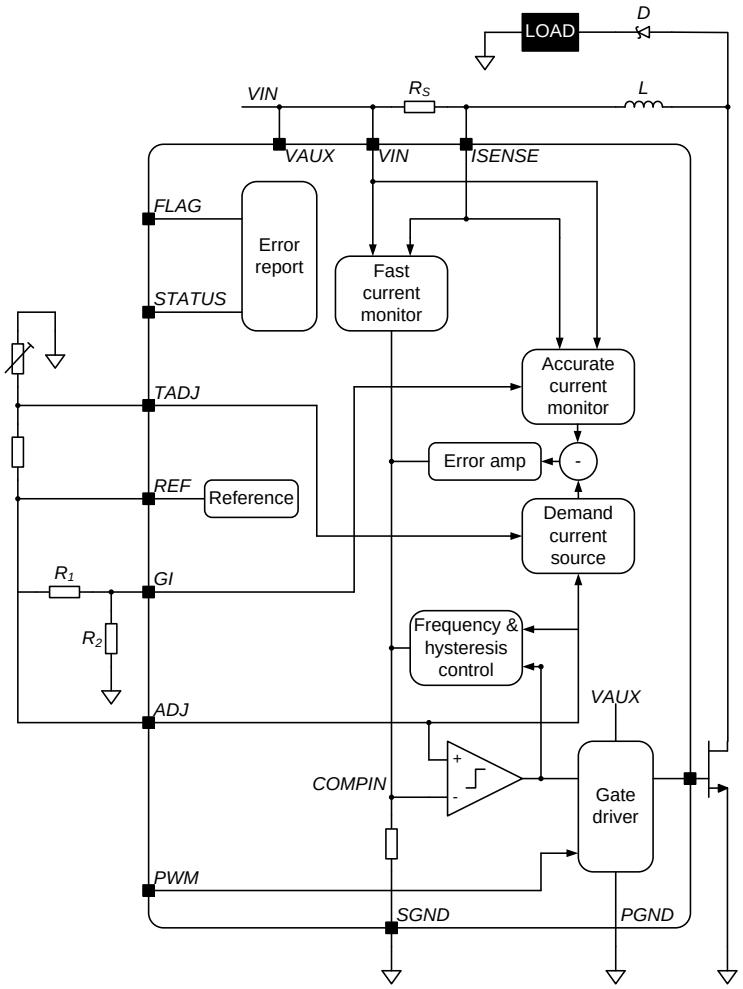
Typical Application Circuit



Buck-Boost Diagram Utilizing Thermistor and T_{ADJ}

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q100 qualified and are PPAP capable. Refer to http://www.diodes.com/quality/product_compliance_definitions/.

Functional Block Diagram



Pin Descriptions

Pin Name	Pin	Type (Note 5)	Description
ADJ	1	I	Adjust Input (for DC output current control) Connect to REF to set 100% output current. Drive with DC voltage (125mV<V_{ADJ}< 1.25V) to adjust output current from 10% to 100% of set value. The ADJ pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should they get overdriven
REF	2	O	Internal 1.25V Reference Voltage Output
TADJ	3	I	Temperature Adjust input for LED thermal current control Connect thermistor/resistor network to this pin to reduce output current above a preset temperature threshold. Connect to REF to disable thermal compensation function. (See section on thermal control.)
SHP	4	I/O	Shaping Capacitor for Feedback Control Loop Connect 330pF ±20% capacitor from this pin to ground to provide loop compensation
STATUS	5	O	Operation Status Output (analog output) Pin is at 4.5V (nominal) during normal operation. Pin switches to a lower voltage to indicate specific operation warnings or fault conditions. (See section on STATUS output.) Status pin voltage is low during shutdown mode

Note: 5. Type refers to whether or not pin is an Input, Output, Input/Output or power supply pin.

Pin Descriptions (continued)

Pin Name	Pin	Type (Note 5)	Function
SGND	6	P	Signal Ground (Connect to 0V)
PGND	7	P	Power Ground - Connect to 0V and pin 8 to maximize copper area
N/C	8	-	Not Connected Internally – recommend connection to pin 7, (PGND), to maximize PCB copper for thermal dissipation
N/C	9		Not Connected Internally – recommend connection pin 10 (GATE) to permit wide copper trace to gate of MOSFET
GATE	10	O	Gate Drive Output to External NMOS Transistor – Connect to Pin 9
V_{AUX}	11	P	Auxiliary Positive Supply to Internal Switch Gate Driver At V_{IN} < 8V; a bootstrap circuit (where applicable) is recommended to ensure adequate gate drive voltage (see Applications section) At V_{IN} > 8V; connect to V_{IN} At V_{IN} >24V; to reduce power dissipation, V_{AUX} can be connected to an 8V to 15V auxiliary power supply (see Applications section). Decouple to ground with capacitor close to device (see Applications section)
V_{IN}	12	P	Input Supply to Device 5V to 60V Decouple to ground with capacitor close to device (refer to Applications section)
ISM	13	I	Current Monitor Input Connect current sense resistor between this pin and V_{IN} The nominal voltage, V_{SENSE}, across the resistor is 218mV fixed in Buck mode and initially 225mV in Boost and Buck-Boost modes, varying with duty cycle.
FLAG	14	O	Flag Open Drain Output Pin is high impedance during normal operation Pin switches low to indicate a fault, or warning condition
PWM	15	I	Digital PWM Output Current Control Pin driven either by open Drain or push-pull 3.3V or 5V logic levels. Drive with frequency higher than 100Hz to gate output 'on' and 'off' during dimming control. The device enters standby mode when PWM pin is driven with logic low level for more than 15ms nominal (Refer to application section for more details)
GI	16	I	Gain Setting Input Used to set the device in Buck mode or Boost, Buck-boost modes and to control the sense voltage in Boost and Buck-boost modes Connect to ADJ pin for Buck mode operation For Boost and Buck-boost modes, connect to resistive divider from ADJ to SGND. The GI divider is required to compensate for duty cycle gating in the internal feedback loop (see Application section). The GI pin has an internal clamp that limits the internal node to less than 3V. This provides some failsafe should it become overdriven.
EP	PAD	P	Exposed Paddle Connect to 0V plane for electrical and thermal management

Note: 5. Type refers to whether or not pin is an Input, Output, Input/Output or power supply pin.

Absolute Maximum Ratings (Voltages to GND Unless Otherwise Stated) (Note 6)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Supply Voltage	-0.3 to 65	V
V_{AUX}	Auxiliary Supply Voltage	-0.3 to 65	V
V_{ISM}	Current Monitor Input Relative to GND	-0.3 to 65	V
V_{SENSE}	Current Monitor Sense Voltage (V_{IN}-V_{ISM})	-0.3 to 5	V
V_{GATE}	Gate Driver Output Voltage	-0.3 to 20	V
I_{GATE}	Gate Driver Continuous Output Current	18	mA
V_{FLAG}	Flag Output Voltage	-0.3 to 40	V
V_{PWM}, V_{ADJ}, V_{TADJ}, V_{GI}, V_{PWM}	Other Input Pins	-0.3 to 5.5	V
T_J	Maximum Junction Temperature	+150	°C
T_{ST}	Storage Temperature	-55 to +150	°C

Note: 6. For correct operation, SGND and PGND should always be connected together.

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at conditions between maximum recommended operating conditions and absolute maximum ratings is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

ESD Susceptibility

ESD Susceptibility		Rating	—
HBM	Human Body Model	1,500	V
CDM	Charged Device Model	1,000	V

Caution: Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Package Thermal Data

Thermal Resistance	Package	Typical	Unit
Junction-to-Ambient, θ_{JA} (Note 7)	TSSOP-16EP	50	°C/W
Junction-to-Case, θ_{JC}	TSSOP-16EP	23	°C/W

Recommended Operating Conditions (Note 6) (-40°C ≤ T_J ≤ +125°C)

Symbol	Parameter	Performance/Comment	Min	Max	Unit
V_{IN}	Input supply voltage range	Normal Operation	8.0	60	V
		(Note 8) Reduced performance operation	5.0	8.0	
V_{AUX}	Auxiliary supply voltage range (Note 9)	Normal Operation	8.0	60	V
		(Note 8) Reduced performance operation	5.0	8.0	
V_{SENSE}	Differential input voltage	V_{IN}-V_{ISM}, with 0 ≤ V_{ADJ} ≤ 2.5	0	450	mV
V_{ADJ}	External DC control voltage applied to ADJ pin to adjust output current	DC brightness control mode from 10% to 100%	0.125	1.25	V
I_{REF}	Reference external load current	REF sourcing current	—	1	mA
f_{max}	Recommended switching frequency range	(Note 10)	300	1,000	kHz
V_{TADJ}	Temperature adjustment (T_{ADJ}) input voltage range	—	0	V_{REF}	V
f_{PWM}	Recommended PWM dimming frequency range	To achieve 1000:1 resolution	100	500	Hz
		To achieve 500:1 resolution	100	1,000	Hz
$t_{PWMH/L}$	PWM pulse width in dimming mode	PWM input high or low	0.002	10	ms
V_{PWMH}	PWM pin high level input voltage	—	2	5.5	V
V_{PWML}	PWM pin low level input voltage	—	0	0.4	V
T_J	Operating Junction Temperature Range	—	-40	+125	°C
GI	Gain setting ratio for boost and buck-boost modes	Ratio= V_{GI}/V_{ADJ}	0.20	0.50	—

Notes:
7. Measured on "High Effective Thermal Conductivity Test Board" according to JESD51.
8. Device starts up above 5.4V and as such the minimum applied supply voltage has to be above 5.4V (plus any noise margin). The ZXLD1371Q will, however, continue to function when the input voltage is reduced from ≥ 8V down to 5.0V.
   When operating with input voltages below 8V the output current and device parameters may deviate from their normal values; and is dependent on power MOSFET switch, load and ambient temperature conditions. To ensure best operation in Boost and Buck-Boost Modes with input voltages, V_{IN}, between 5.0 and 8V a suitable bootstrap network on V_{AUX} pin is recommended.
   Performance in Buck Mode will be reduced at input voltages (V_{IN}, V_{AUX}) below 8V – a bootstrap network cannot be implemented in Buck Mode and so a suitable low V_T MOSFET should be selected.
9. V_{AUX} can be driven from a voltage higher than V_{IN} to provide higher efficiency at low V_{IN} voltages, but to avoid false operation; a voltage should not be applied to V_{AUX} in the absence of a voltage at V_{IN}. V_{AUX} can also be operated at a lower voltage than V_{IN} to increase efficiencies at high V_{IN}.
10. The device contains circuitry to control the switching frequency to approximately 400kHz.

Electrical Characteristics (Test conditions: V_{IN} = V_{AUX} = 12V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply and Reference Parameters						
V_{UV-}	Undervoltage Detection Threshold Normal Operation to Switch Disabled	V_{IN} or V_{AUX} falling (Note 11)	—	4.5	—	V
V_{UV+}	Undervoltage Detection Threshold Switch Disabled to Normal Operation	V_{IN} or V_{AUX} rising (Note 11)	—	4.9	—	V
I_{Q-IN}	Quiescent Current into V_{IN}	PWM pin floating	—	1.5	3	mA
I_{Q-AUX}	Quiescent Current into V_{AUX}	Output not switching	—	150	300	µA
I_{SB-IN}	Standby Current into V_{IN}	PWM pin grounded	—	90	150	µA
I_{SB-AUX}	Standby Current into V_{AUX}	for more than 15ms	—	0.7	10	µA
V_{REF}	Internal Reference Voltage	No load	1.237	1.25	1.263	V
ΔV_{REF}	Change in Reference Voltage with Output Current	Sourcing 1mA	-5	—	—	mV
		Sinking 25µA	—	—	5	
V_{REF_LINE}	Reference Voltage Line Regulation	V_{IN} = V_{AUX}, 8.0V<V_{IN} = <60V	-60	-90	—	dB
V_{REF-TC}	Reference Temperature Coefficient	—	—	±50	—	ppm/°C
DC-DC Converter Parameters						
I_{ADJ}	ADJ Input Current (**Note 12**)	V_{ADJ} ≤ 1.25V	—	—	100	nA
		V_{ADJ} = 5.0V	—	—	5	µA
V_{GI}	GI Voltage threshold for Boost and Buck-Boost Modes Selection (**Note 12**)	V_{ADJ} = 1.25V	—	—	0.8	V
I_{GI}	GI Input Current (**Note 12**)	V_{GI} ≤ 1.25V	—	—	100	nA
		V_{GI} = 5.0V	—	—	5	µA
I_{PWM}	PWM Input Current	V_{PWM} = 5.5V	—	36	100	µA
t_{PWMoff}	PWM Pulse Width (to enter shutdown state)	PWM input low	10	15	25	ms
T_{SDH}	Thermal Shutdown Upper Threshold (GATE output forced low)	Temperature rising	—	150	—	°C
T_{SDL}	Thermal Shutdown Lower Threshold (GATE output re-enabled)	Temperature falling	—	125	—	°C
High-Side Current Monitor (Pin ISM)						
I_{ISM}	Input Current	Measured into ISM pin V_{ISM} = 12V	—	11	20	µA
V_{SENSE_acc}	Accuracy of nominal V_{SENSE} Threshold Voltage	V_{ADJ} = 1.25V	—	±0.25	±2	%
$V_{SENSE-OC}$	Over-Current Sense Threshold Voltage		300	350	375	mV

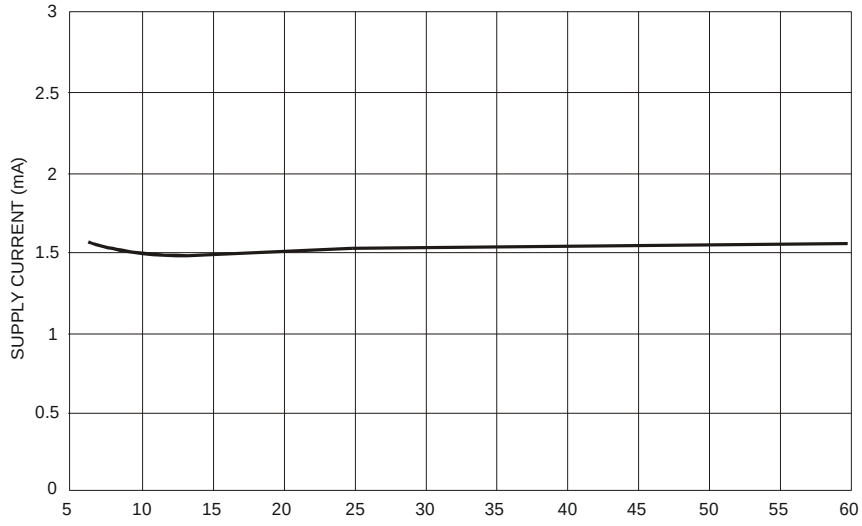
Notes: 11. UVLO levels are such that all ZXLD1371Q will function above 5.4V for rising supply voltages and function down to 5V for falling supply voltages.
12. The ADJ and GI pins have an internal clamp that limits the internal node to less than 3V. This provides some failsafe should those pins get overdriven.

Electrical Characteristics (continued) (Test conditions: V_{IN} = V_{AUX} = 12V, T_A = +25°C, unless otherwise specified.)

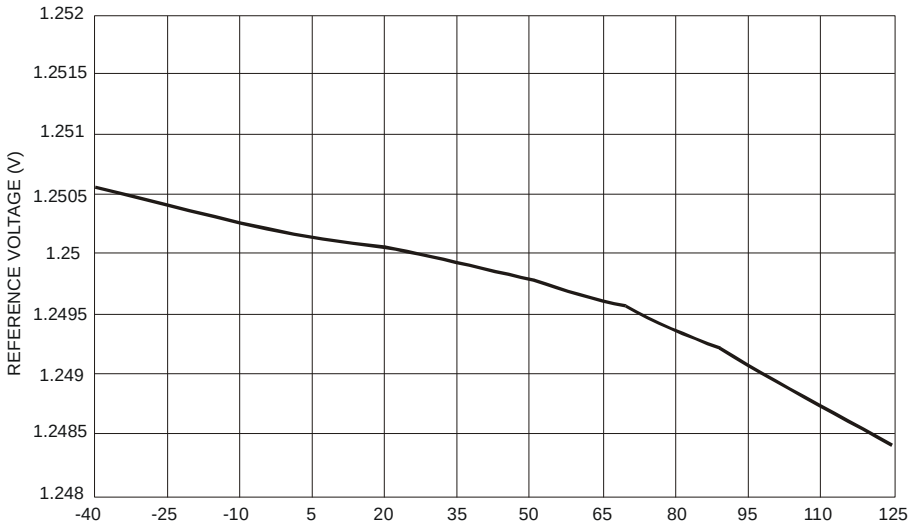
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Parameters						
V_{FLAGL}	FLAG pin low level output voltage	Output sinking 1mA	—	—	0.5	V
$I_{FLAGOFF}$	FLAG pin open-drain leakage current	V_{FLAG} = 40V	—	—	1	µA
V_{STATUS}	STATUS Flag no-load output voltage (**Note 13**)	Normal operation	4.2	4.5	4.8	V
		Out of regulation (V_{SHP} out of range) (**Note 14**)	3.3	3.6	3.9	
		V_{IN} under-voltage (V_{IN} < UVLO)	3.3	3.6	3.9	
		Switch stalled (t_{ON} or t_{OFF} > 100µs)	3.3	3.6	3.9	
		Over-temperature (T_J > +125°C)	1.5	1.8	2.1	
		Excess sense resistor current (V_{SENSE} > 0.32V)	0.6	0.9	1.2	
R_{STATUS}	Output impedance of STATUS output	Normal operation	—	10	—	kΩ
Driver output (PIN GATE)						
V_{GATEH}	High level output voltage	No load Sourcing 1mA (Note 15); V_{IN} = V_{AUX} = 12V	9.5	10.5	—	V
V_{GATEL}	Low level output voltage	Sinking 1mA, (**Note 16**)	—	—	0.5	V
V_{GATECL}	High level GATE CLAMP voltage	V_{IN} = V_{AUX} = V_{ISM} = 18V; I_{GATE} = 1mA	—	12.8	15	V
I_{GATE}	Dynamic peak current available during rise or fall of output voltage	Charging or discharging gate of external switch with Q_G = 10nC and 400kHz	—	±300	—	mA
t_{STALL}	Time to assert 'STALL' flag and warning on STATUS output (**Note 17**)	GATE low or high	—	100	170	µs
LED Thermal control circuit (T_{ADJ}) parameters						
V_{TADJH}	Upper threshold voltage	Onset of output current reduction (V_{TADJ} falling)	560	625	690	mV
V_{TADJL}	Lower threshold voltage	Output current reduced to <10% of set value (V_{TADJ} falling)	380	440	500	mV
I_{TADJ}	T_{ADJ} pin Input current	V_{TADJ} = 1.25V	—	—	1	µA

Notes:
13. In the event of more than one fault/warning condition occurring, the higher priority condition will take precedence. For example 'Excessive coil current' and 'Out of regulation' occurring together will produce an output of 0.9V on the STATUS pin. These STATUS pin voltages apply for an input voltage to V_{IN} of 7.5V < V_{IN} < 60V. Below 7.5V the STATUS pin voltage levels reduce and therefore may not report the correct status. For 5.4V < V_{IN} < 7.5V the flag pin still reports any error by going low. At low V_{IN} in Boost and Buck-boost modes an overcurrent status may be indicated when operating at high boost ratios – this is due to the feedback loop increasing the sense voltage. For more information see the Application Information section about Flag/Status levels.
14. Flag is asserted if V_{SHP} < 1.5V or V_{SHP} > 2.5V.
15. GATE is switched to the supply voltage V_{AUX} for low values of V_{AUX} (5V ≤ V_{AUX} ≤ ~12V). For V_{AUX} > 12V, GATE is clamped internally to prevent it exceeding 15V. Below 12V, the minimum gate pin voltage will be 2.5V below Vaux.
16. GATE is switched to PGND by an NMOS transistor.
17. If t_{ON} exceeds t_{STALL}, the device will force GATE low to turn off the external switch and then initiate a restart cycle. During this phase, ADJ is grounded internally and the SHP pin is switched to its nominal operating voltage, before operation is allowed to resume. Restart cycles will be repeated automatically until the operating conditions are such that normal operation can be sustained. If t_{OFF} exceeds t_{STALL}, the switch will remain off until normal operation is possible.

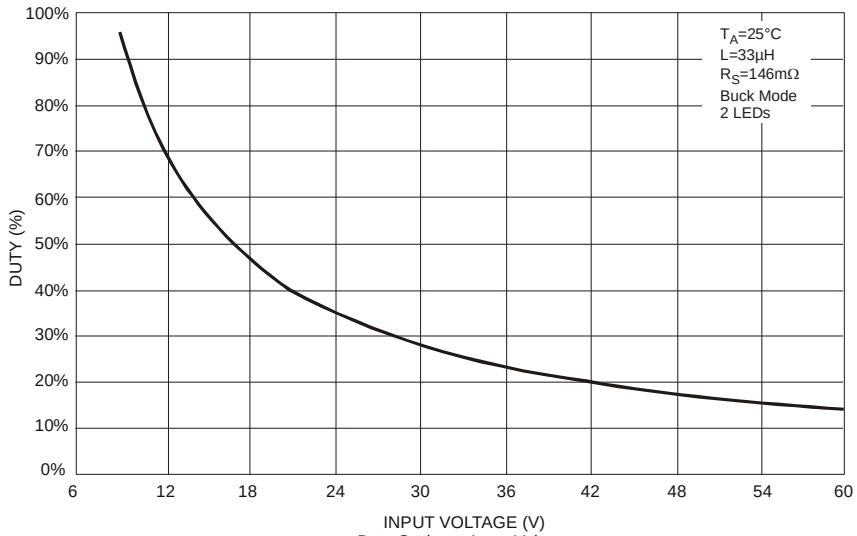
Typical Characteristics



Supply Voltage vs. Supply Current

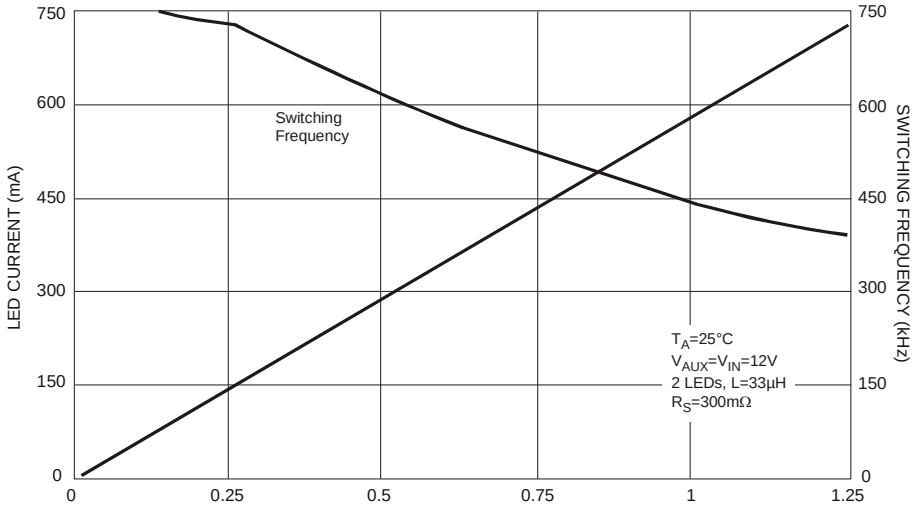


Reference Voltage vs. Junction Temperature

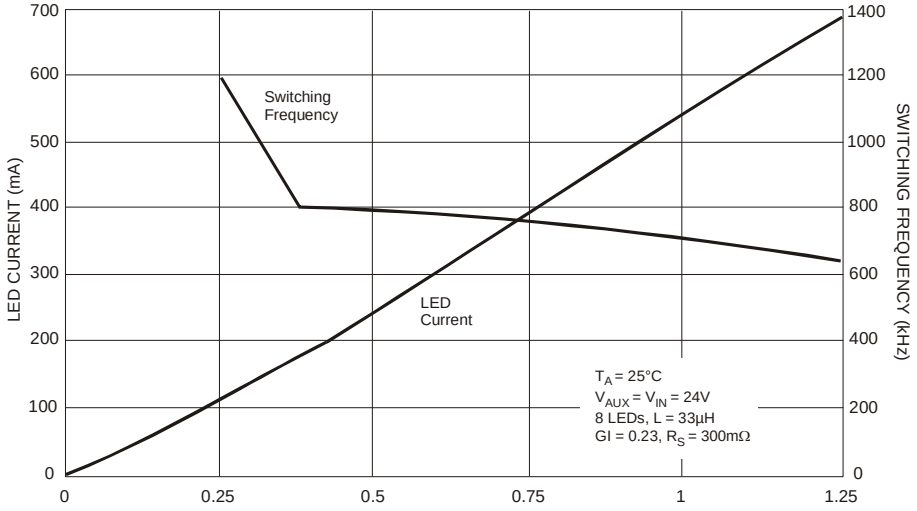


Duty Cycle vs. Input Voltage

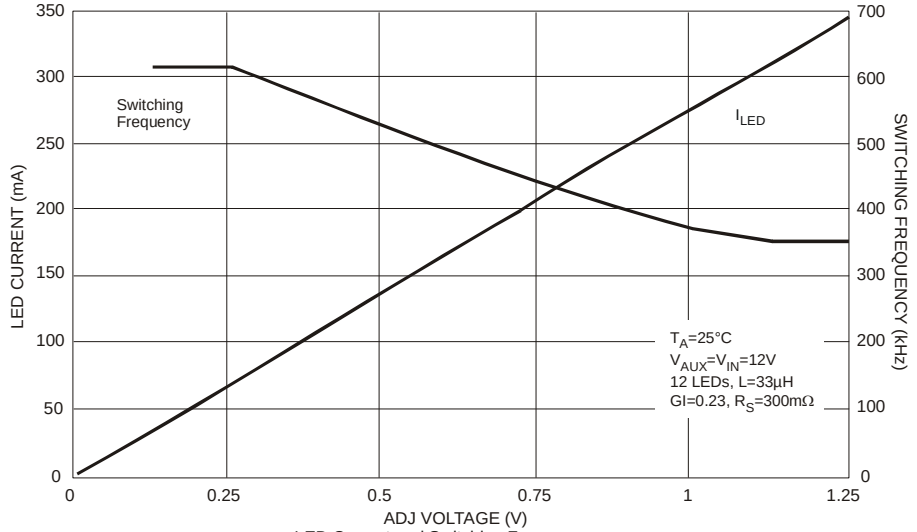
Typical Characteristics – Linear/DC Dimming



Led Current and Switching Frequency vs. ADJ Voltage in Buck Mode

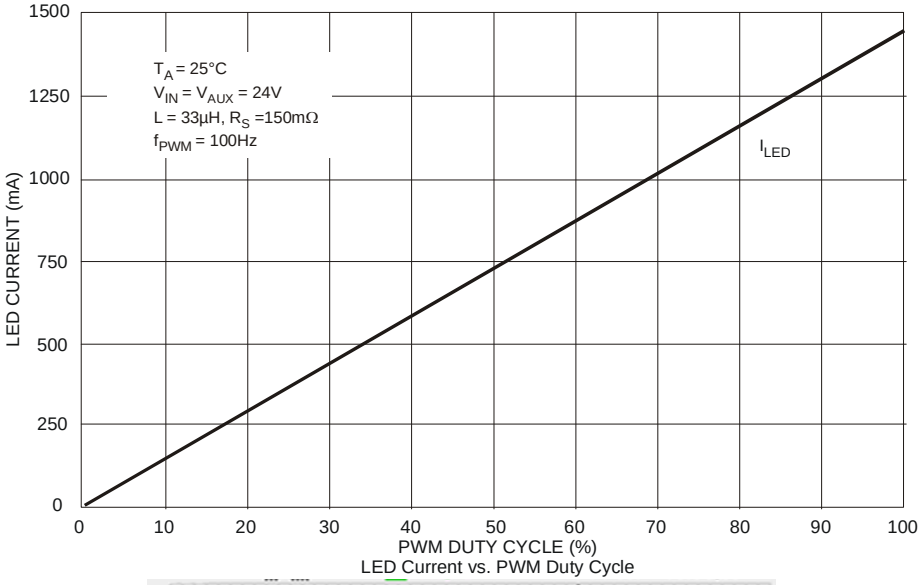


LED Current and Switching Frequency vs. ADJ Voltage in Buck-Boost Mode

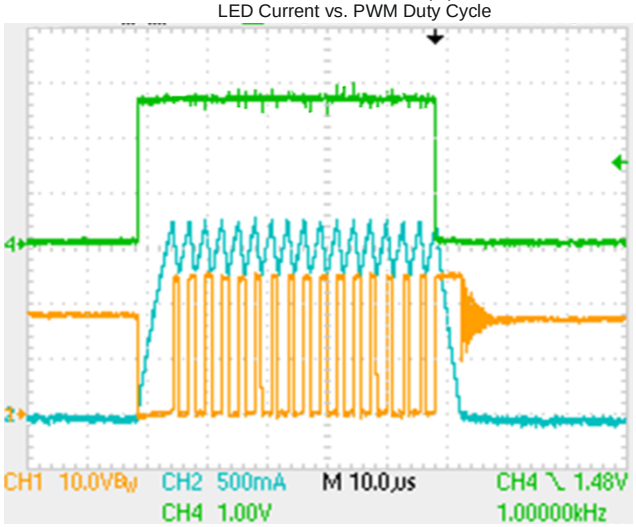


LED Current and Switching Frequency vs. ADJ Voltage in Boost Mode

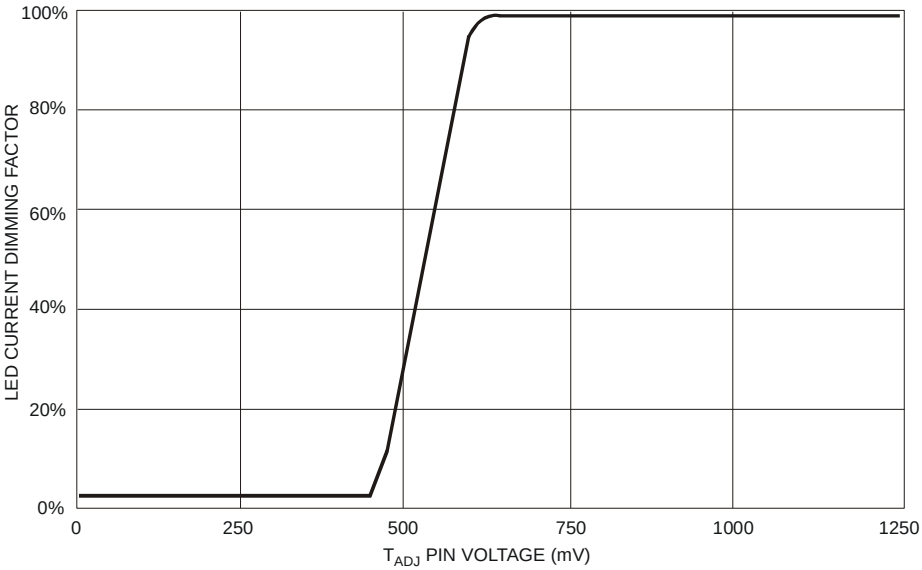
Typical Characteristics – PWM/Thermal Dimming



LED Current vs. PWM Duty Cycle

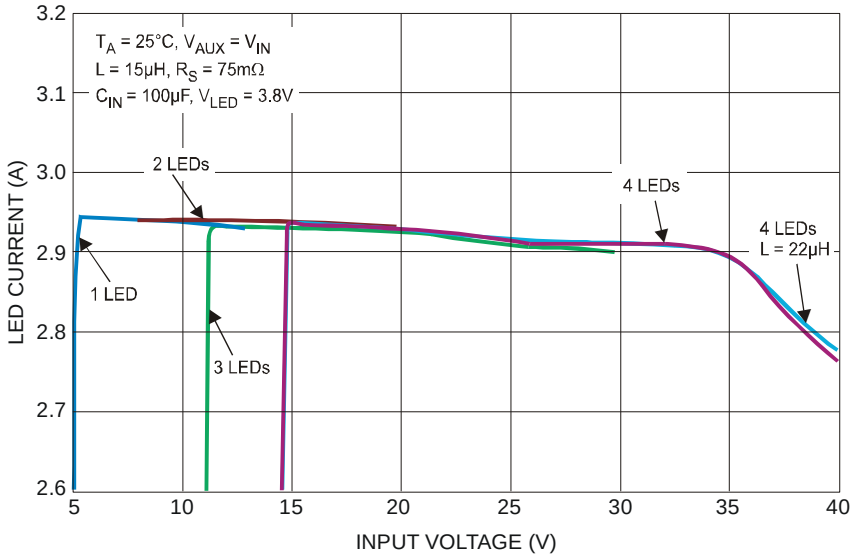


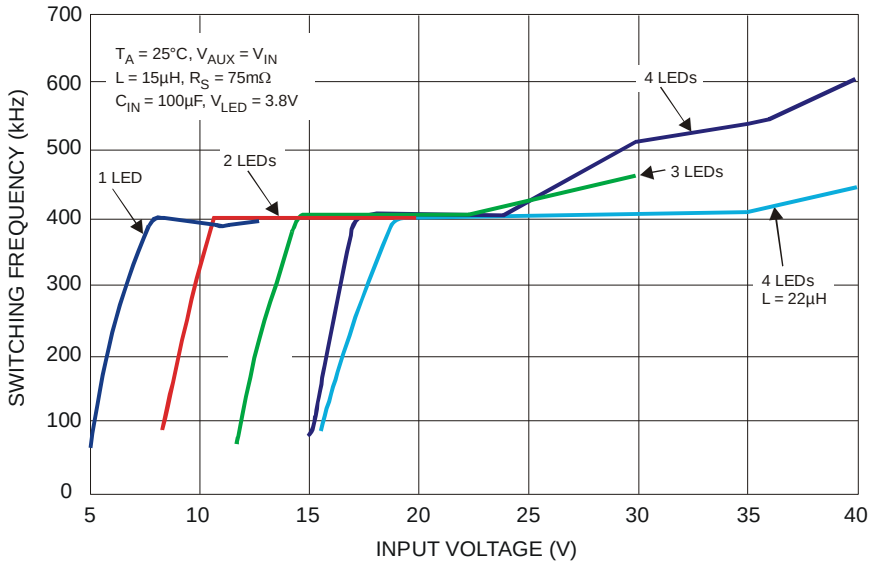
I_{LED} vs. Time - PWM Pin Transient Response

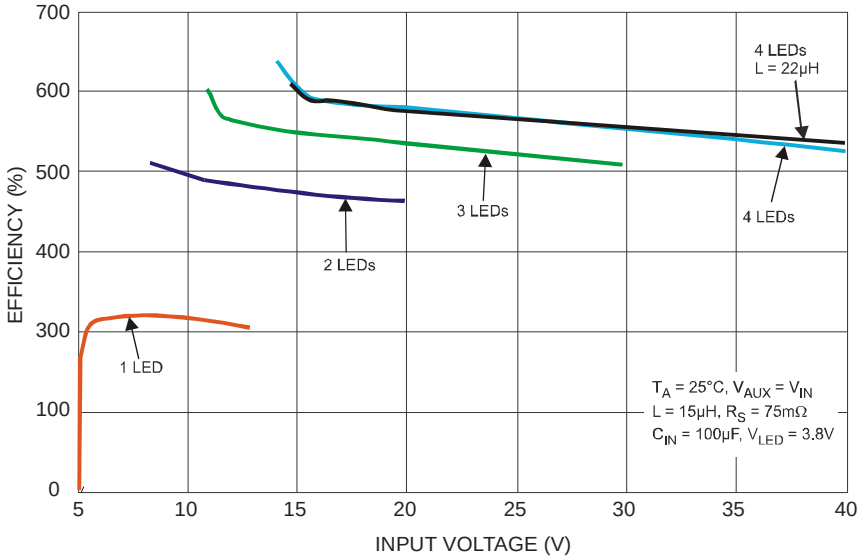


LED Current Dimming Factor vs. T_{ADJ} Voltage

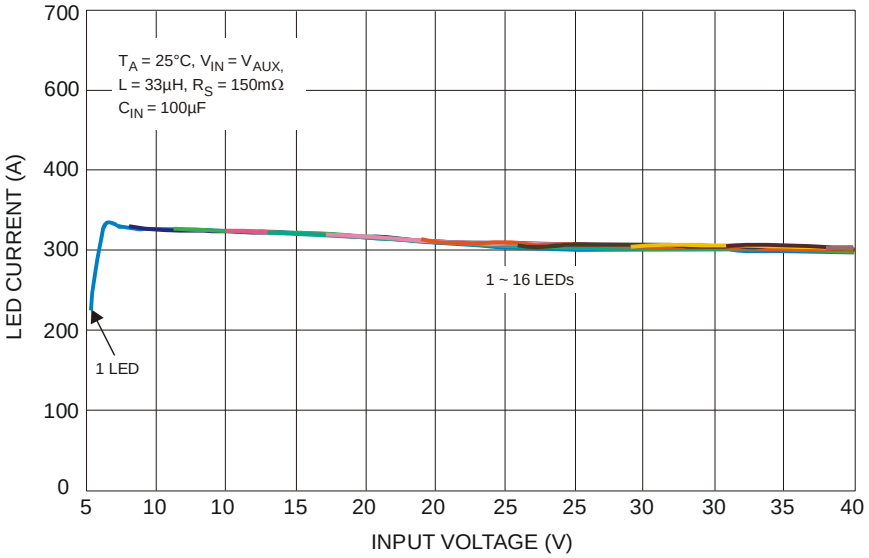
Typical Characteristics – Buck Mode – R_S = 75mΩ – L = 33µH – I_{LED} = 2.9A

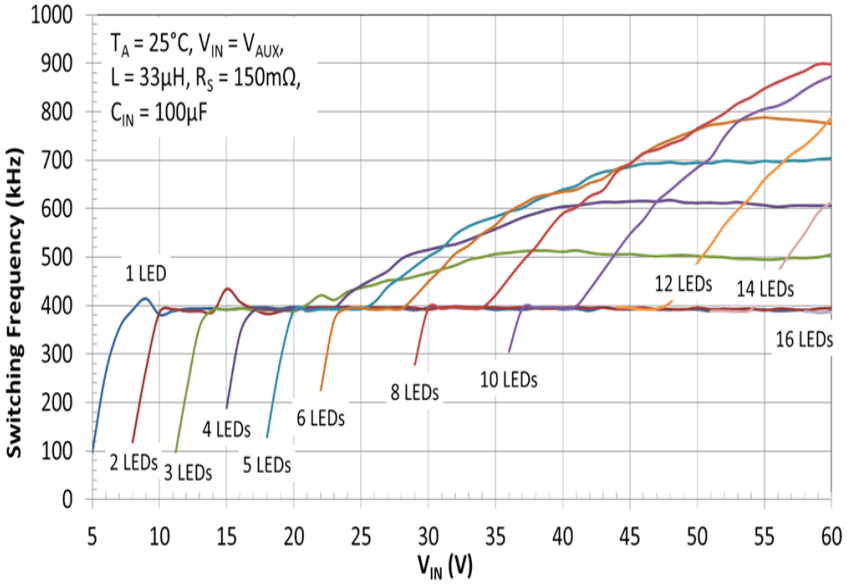


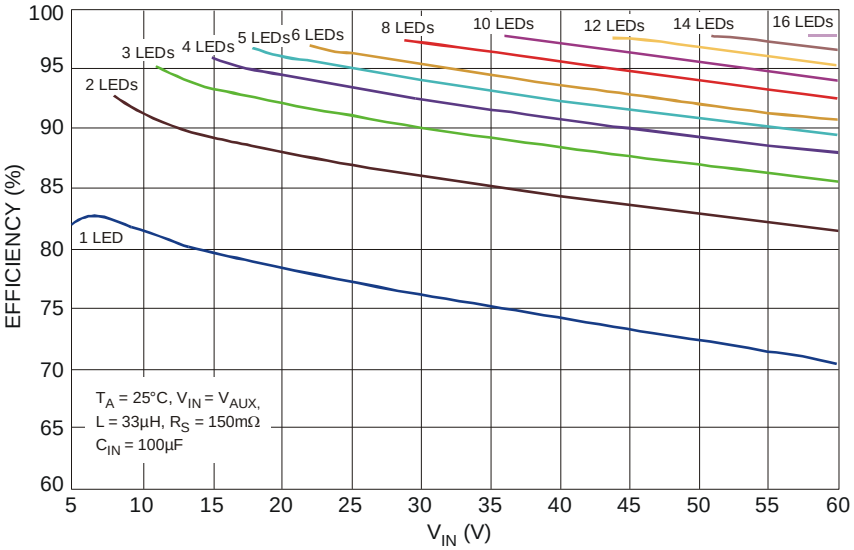




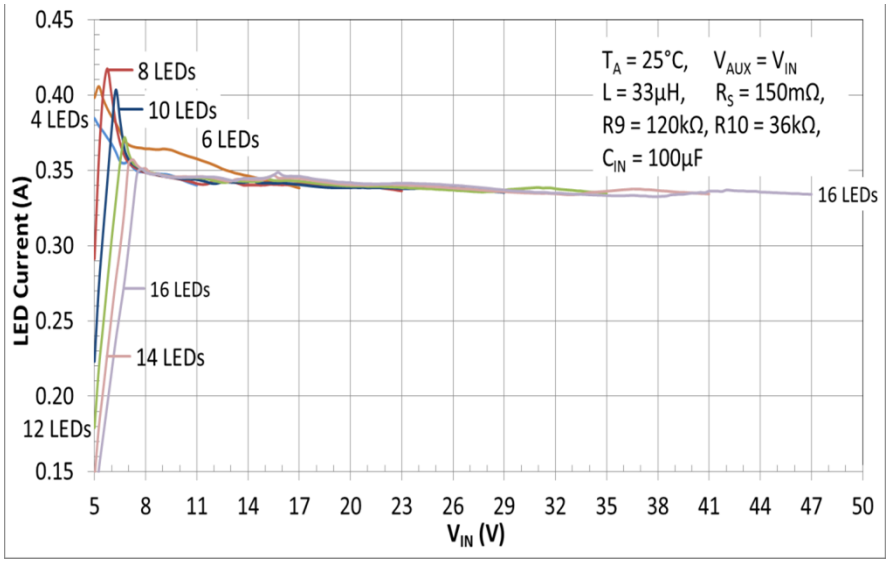
Typical Characteristics – Buck Mode – R_S =150mΩ - L = 33µH – I_{LED} = 1.45A

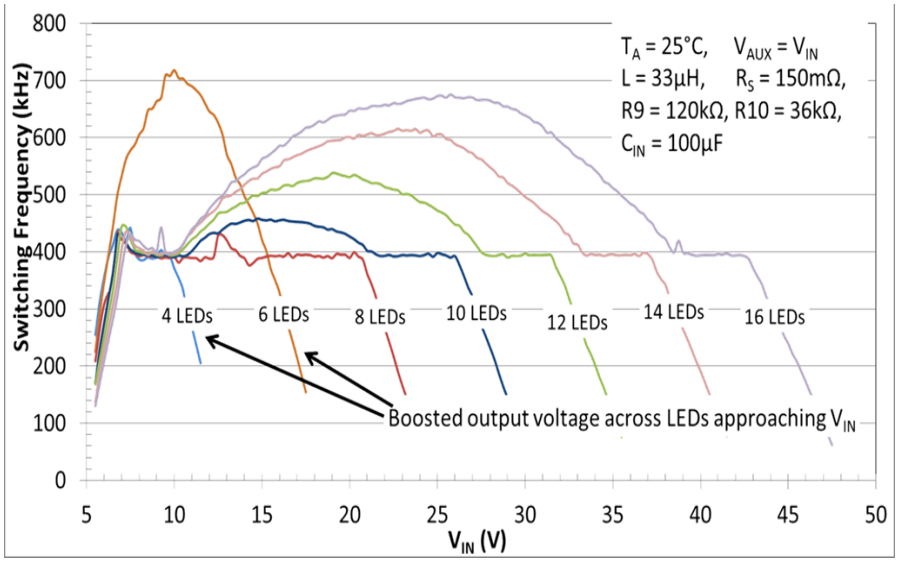


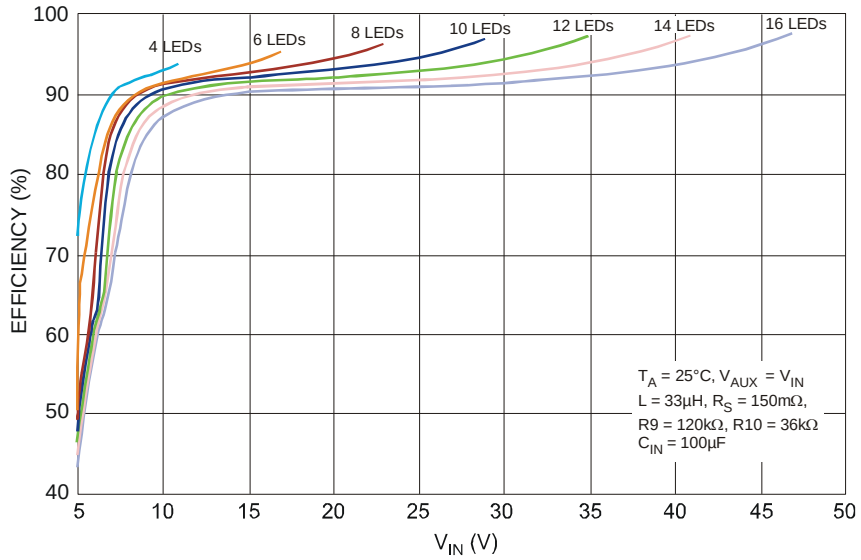




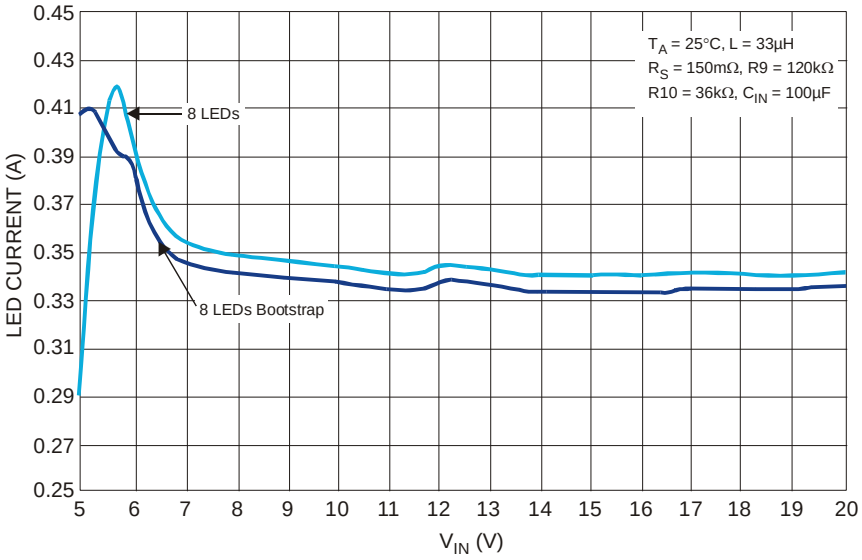
Typical Characteristics – Boost Mode – I_{LED} = 350mA – R_S = 150mΩ – GI_{RATIO} = 0.23

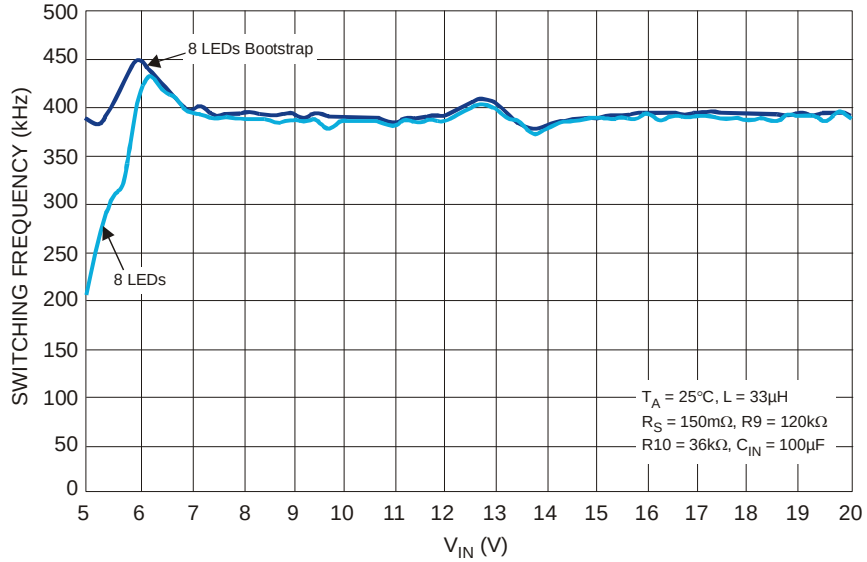


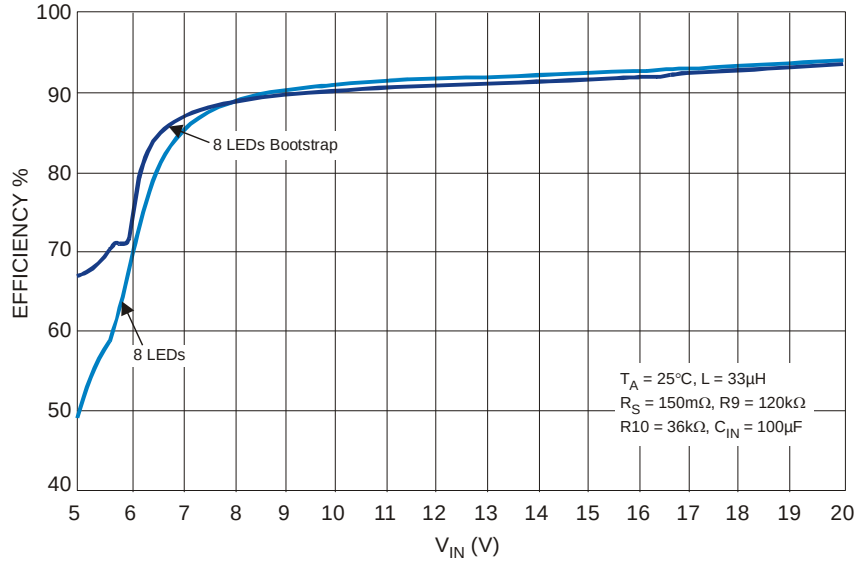




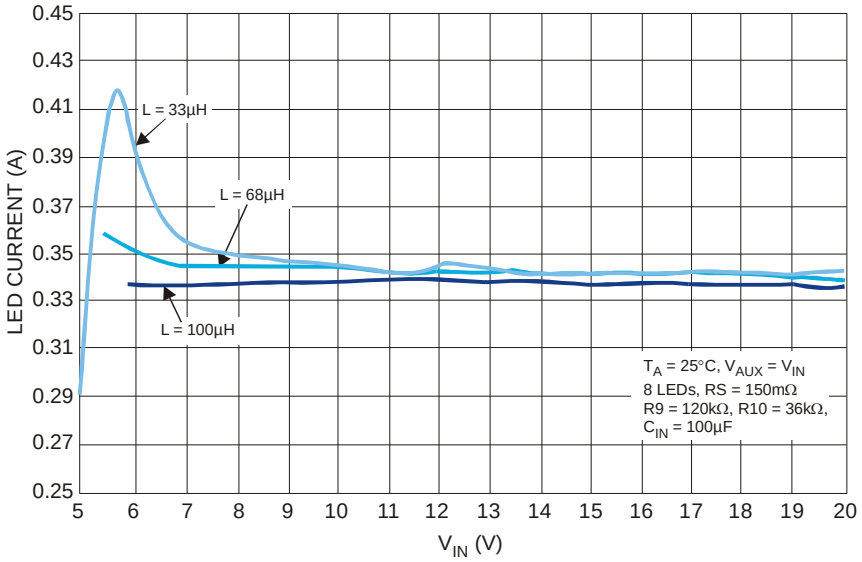
Typical Characteristics – Boost Mode – I_{LED} = 350mA – GI_{RATIO} = 0.23 – Bootstrap comparison

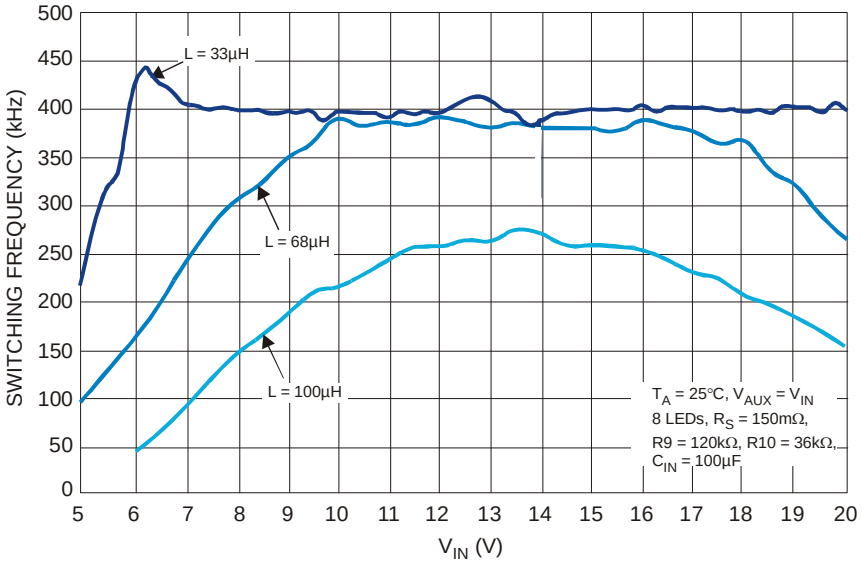


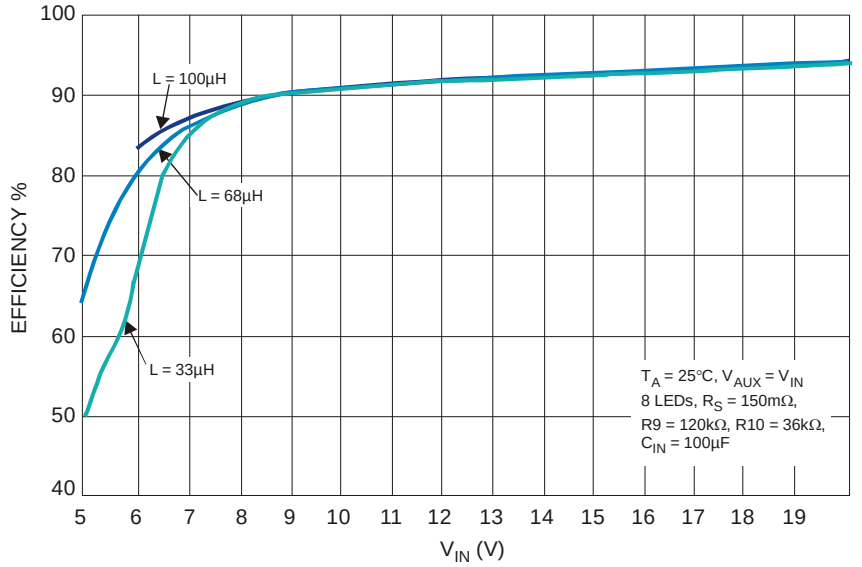




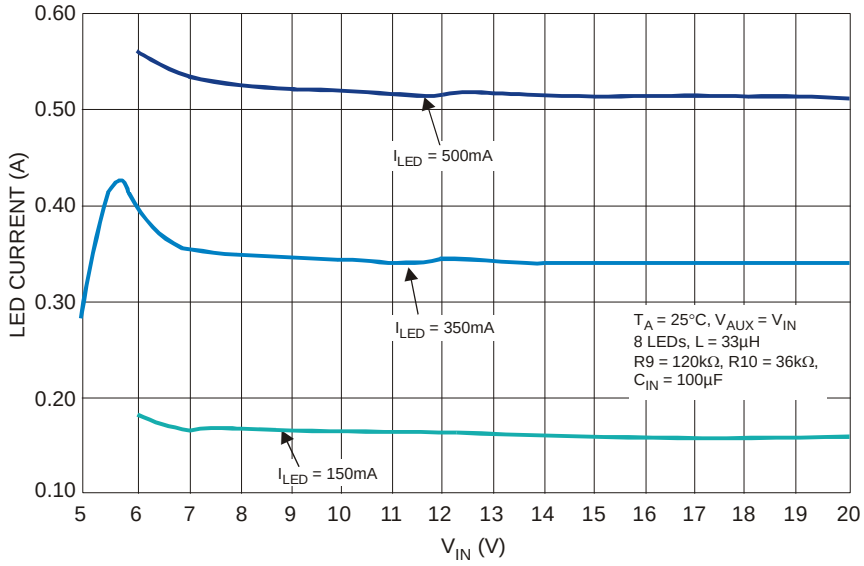
Typical Characteristics – Boost Mode – I_{LED} = 350mA – R_S = 150mΩ – GI_{RATIO} = 0.23

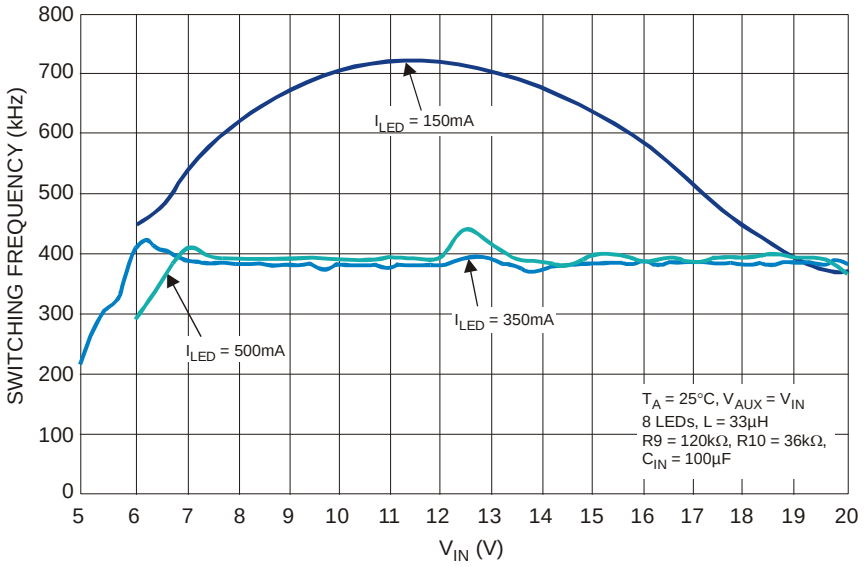


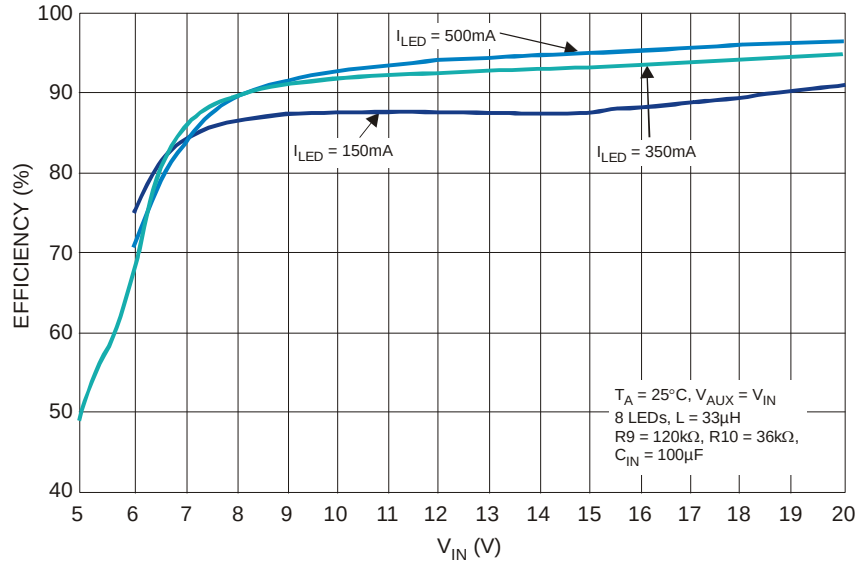




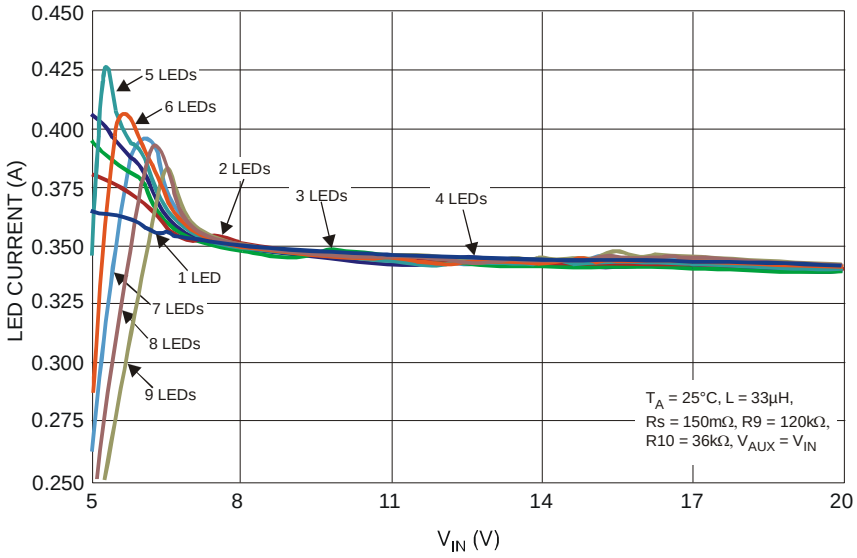
Typical Characteristics – Boost Mode – 8 LEDs – GI_{RATIO} = 0.23

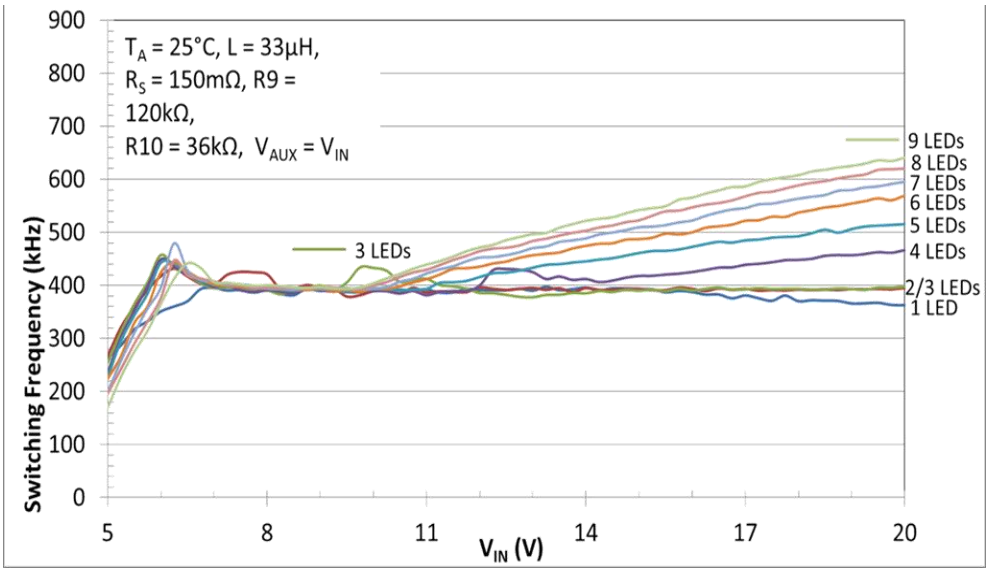


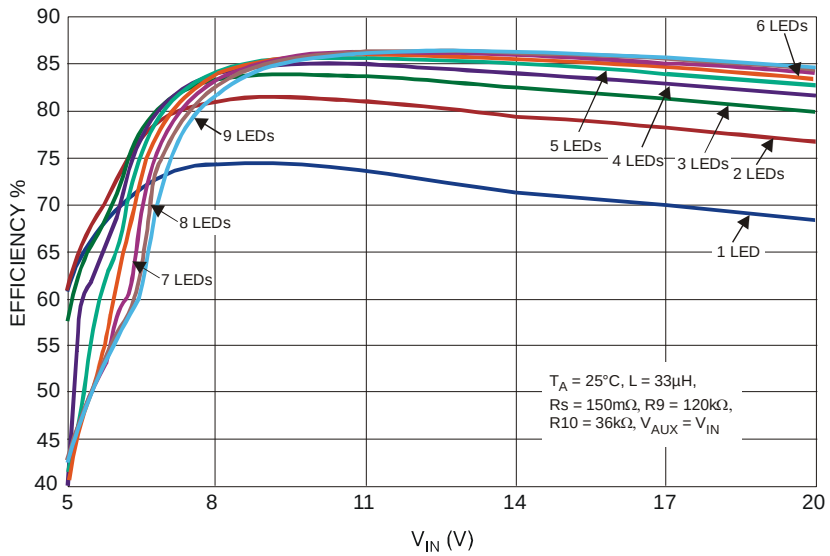




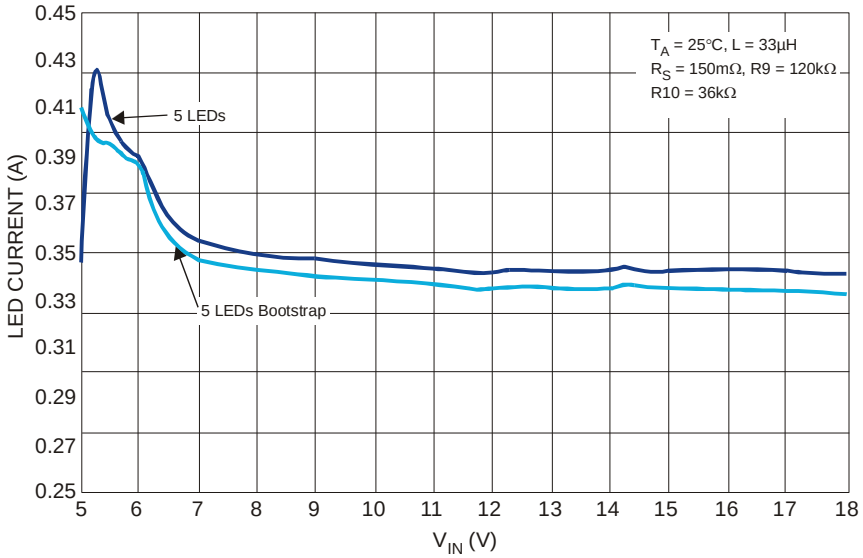
Typical Characteristics – Buck-Boost Mode – R_S = 150mΩ - I_{LED} = 350mA – GI_{RATIO} = 0.23

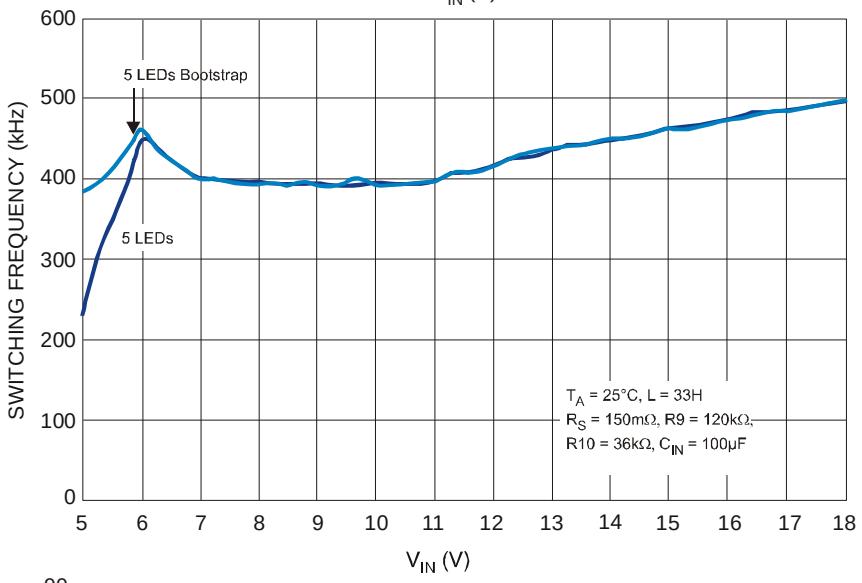


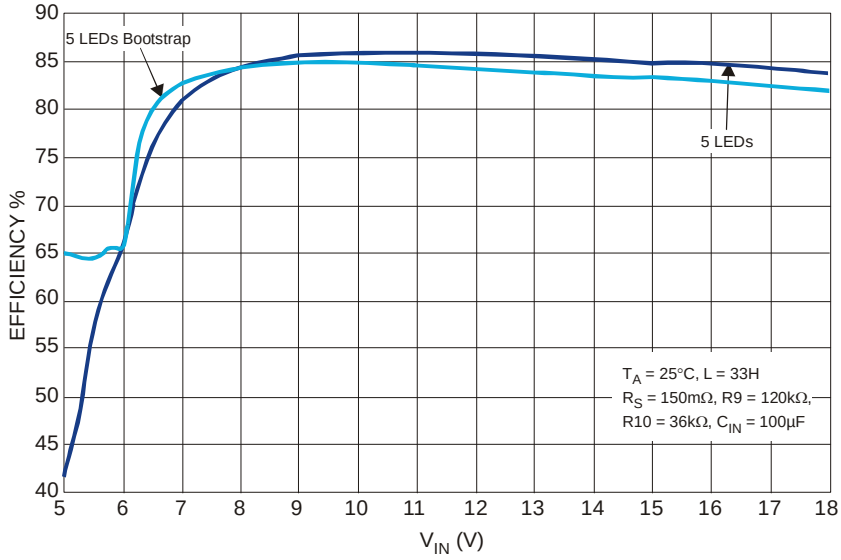




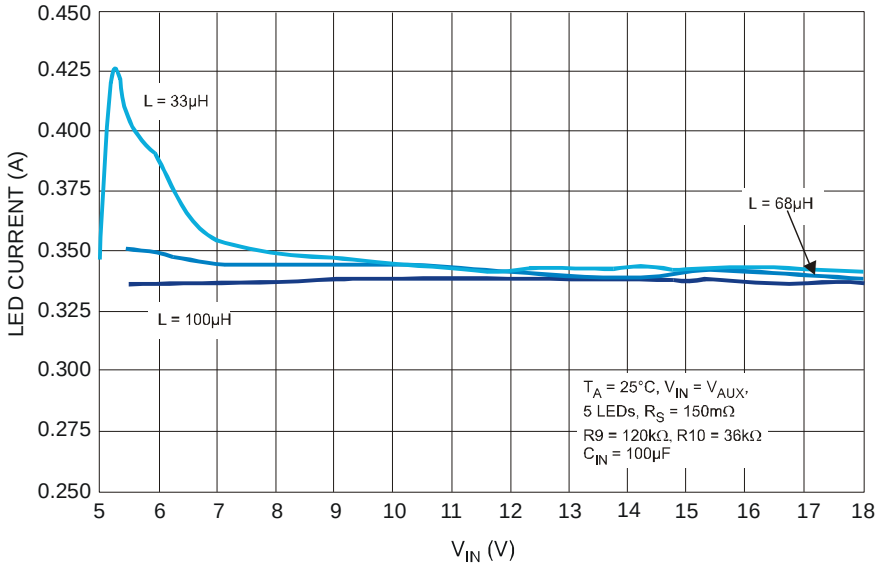
Typical Characteristics – Buck-Boost Mode – R_S = 150mΩ - I_{LED} = 350mA – GI_{RATIO} = 0.23

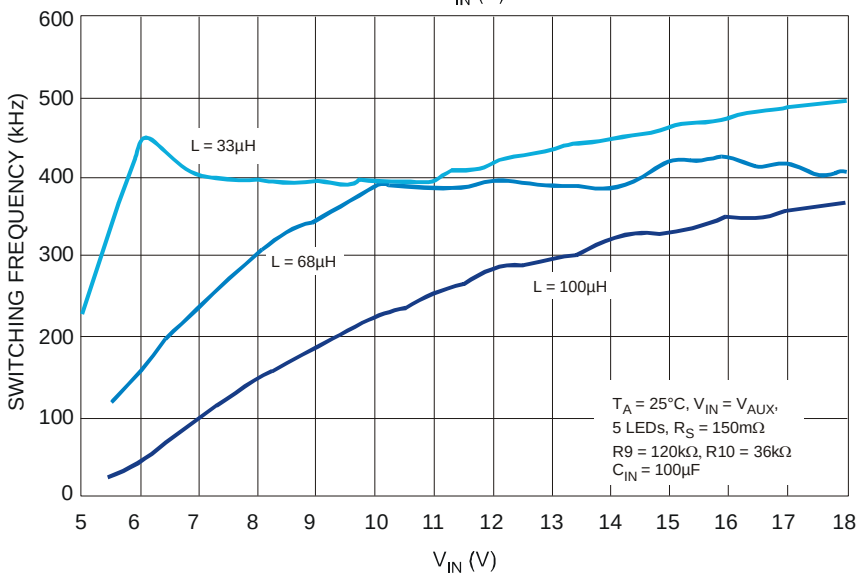


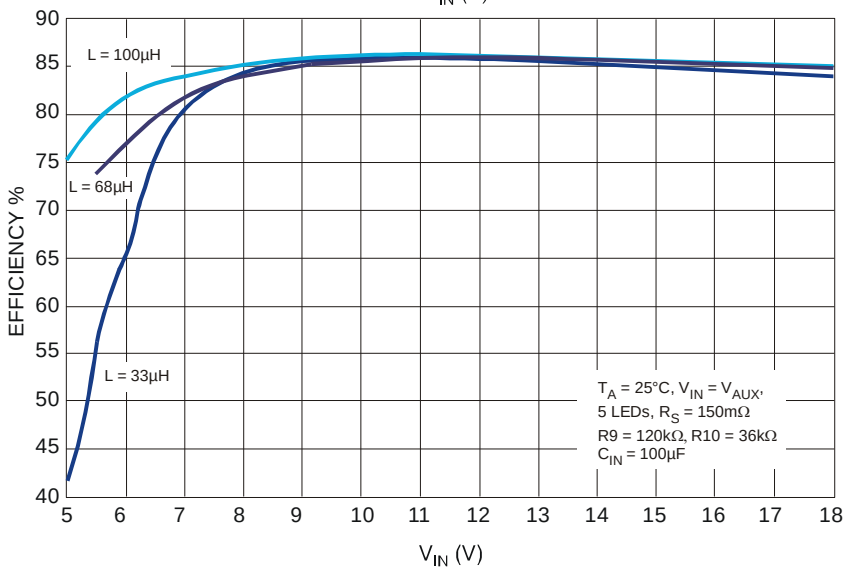




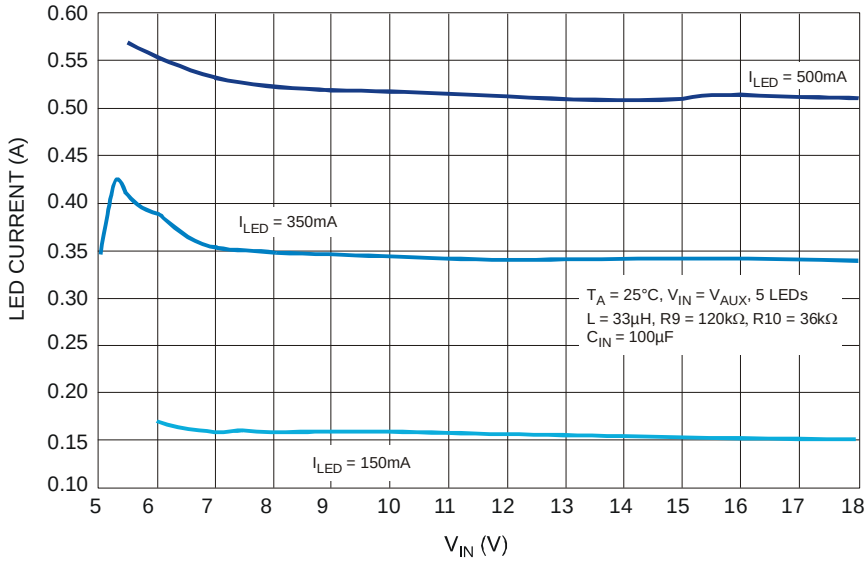
Typical Characteristics – Buck-Boost Mode – R_S = 150mΩ - I_{LED} = 350mA – GI_{RATIO} = 0.23

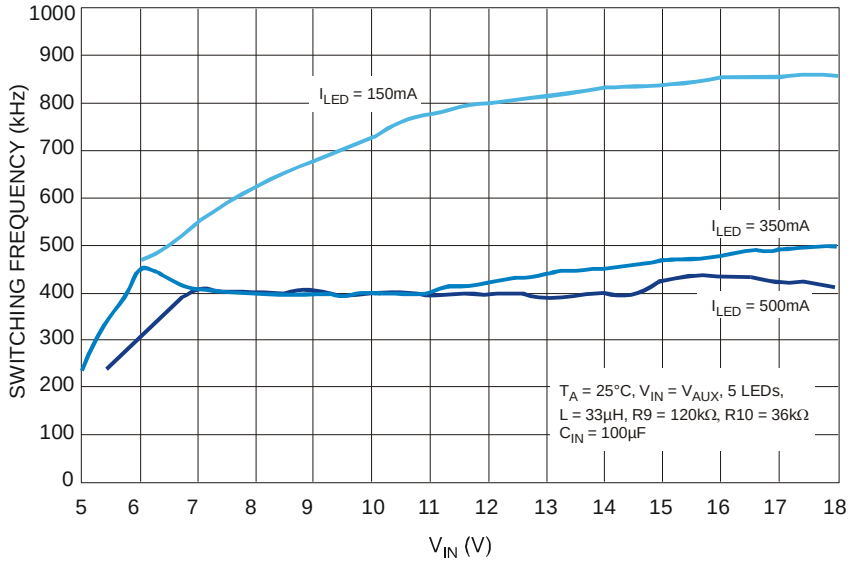


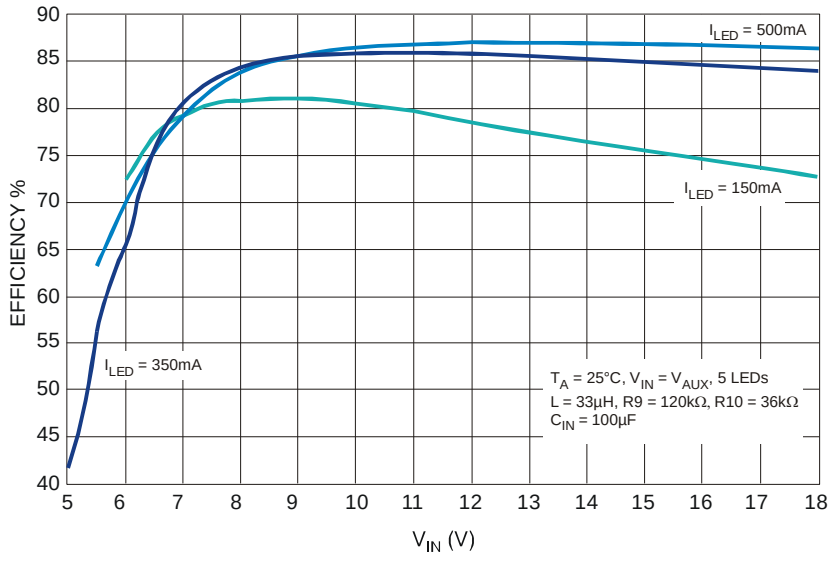




Typical Characteristics – Buck-Boost Mode –5 LEDs GI_{RATIO} = 0.23







Application Information

The ZXLD1371Q is a high-accuracy hysteretic inductive buck/boost/buck-boost controller designed to be used with an external NMOS switch for current-driving single or multiple series-connected LEDs. The device can be configured to operate in buck, boost, or buck-boost modes by suitable configuration of the external components as shown in the schematics shown in the device operation description.

DEVICE DESCRIPTION

a) Buck Mode – the most simple buck circuit is shown in Figure 1

Control of the LED current buck mode is achieved by sensing the coil current in the sense resistor Rs, connected between the two inputs of a current monitor within the control loop block. An output from the control loop drives the input of a comparator which drives the gate of the external NMOS switch transistor Q1 via the internal Gate Driver. When the switch is on, the drain voltage of Q1 is near zero. Current flows from V_{IN}, via Rs, LED, coil and switch to ground. This current ramps up until an upper threshold value is reached (see **Figure 2**). At this point GATE goes low, the switch is turned off and the drain voltage increases to V_{IN} plus the forward voltage, V_F, of the Schottky diode D1. Current flows via Rs, LED, coil and D1 back to V_{IN}. When the coil current has ramped down to a lower threshold value, GATE goes high, the switch is turned on again and the cycle of events repeats, resulting in continuous oscillation. The feedback loop adjusts the NMOS switch duty cycle to stabilize the LED current in response to changes in external conditions, including input voltage and load voltage.

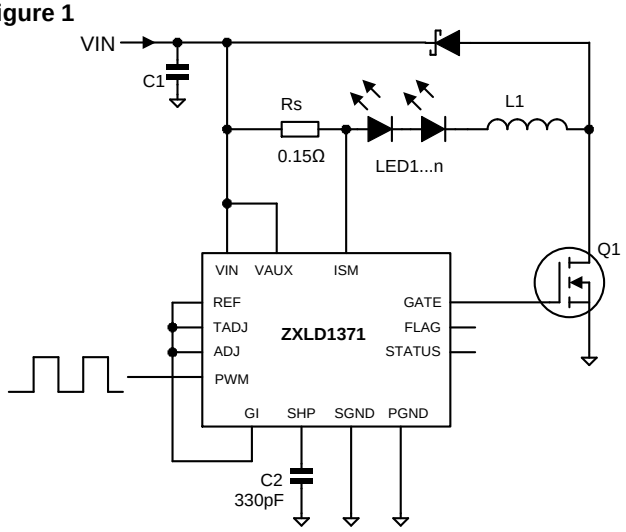


Figure 1. Buck configuration

The average current in the sense resistor, LED and coil is equal to the average of the maximum and minimum threshold currents. The ripple current (hysteresis) is equal to the difference between the thresholds. The control loop maintains the average LED current at the set level by adjusting the switch duty cycle continuously to force the average sense resistor current to the value demanded by the voltage on the ADJ pin. This minimizes variation in output current with changes in operating conditions.

The control loop also regulates the switching frequency by varying the level of hysteresis. The hysteresis has a defined minimum (typ 5%) and a maximum (typ 30%). The frequency may deviate from nominal in some conditions. This depends upon the desired LED current, the coil inductance and the voltages at the input and the load. Loop compensation is achieved by a single external capacitor C2, connected between SHP and SGND.

The control loop sets the duty cycle so that the sense voltage is

$$V_{SENSE} = 0.218\left(\frac{V_{ADJ}}{V_{REF}}\right)$$

Therefore,

$$I_{LED} = \left(\frac{0.218}{R_S}\right)\left(\frac{V_{ADJ}}{V_{REF}}\right) \text{ (Buck mode)} \qquad \textbf{Equation 1}$$

If the ADJ pin is connected to the REF pin, this simplifies to

$$I_{LED} = \left(\frac{0.218}{R_S}\right) \text{ (Buck mode).}$$

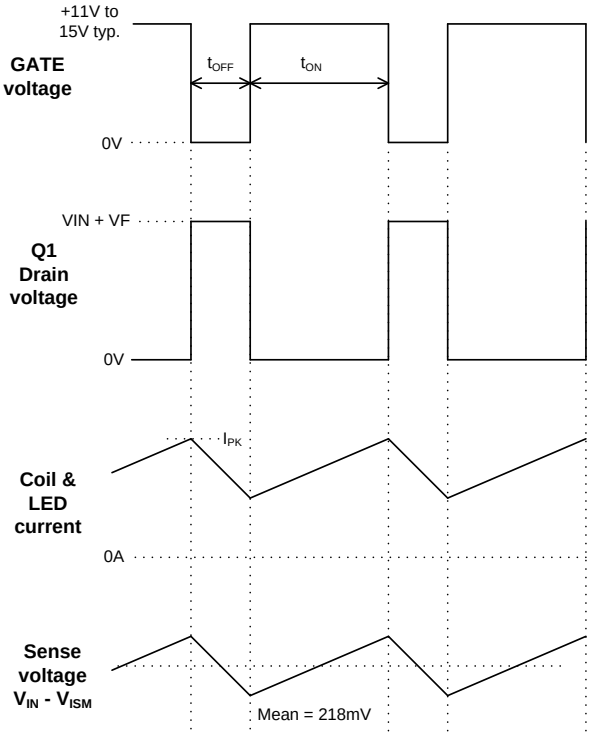


Figure 2. Operating waveforms (Buck mode)

Application Information (continued)

b) Boost and Buck-Boost Modes – the most simple boost/buck-boost circuit is shown in Figure 3

Control in Boost and Buck-boost mode is achieved by sensing the coil current in the series resistor Rs, connected between the two inputs of a current monitor within the control loop block. An output from the control loop drives the input of a comparator which drives the gate of the external NMOS switch transistor Q1 via the internal Gate Driver. When the switch is on, the drain voltage of Q1 is near zero. Current flows from V_{IN}, via Rs, coil and switch to ground. This current ramps up until an upper threshold value is reached (see **Figure 4**). At this point GATE goes low, the switch is turned off and the drain voltage increases to either:

1) the load voltage VLEDS plus the forward voltage of D1 in Boost configuration,

or

2) the load voltage VLEDS plus the forward voltage of D1 plus VIN in Buck-boost configuration.

Current flows via Rs, coil, D1 and LED back to VIN (Buck-boost mode), or GND (Boost mode). When the coil current has ramped down to a lower threshold value, GATE goes high, the switch is turned on again and the cycle of events repeats, resulting in continuous oscillation.

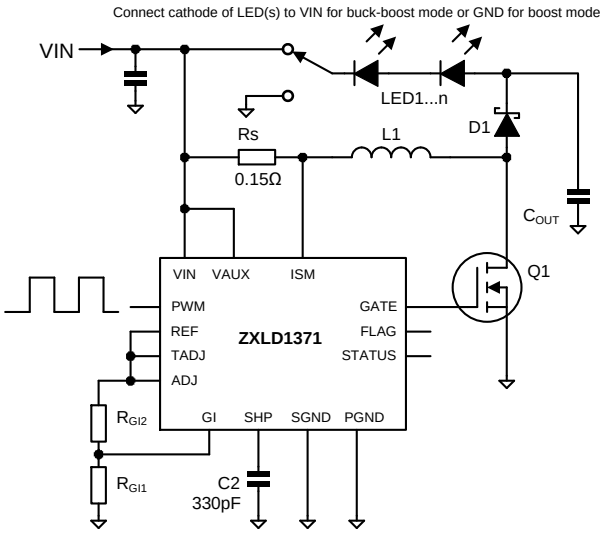


Figure 3. Boost and Buck-Boost Configuration

The feeback loop adjusts the NMOS switch duty cycle to stabilize the LED current in response to changes in external conditions, including input voltage and load voltage. Loop compensation is achieved by a single external capacitor C2, connected between SHP and SGND. Note that in reality, a load capacitor C_{OUT} is used, so that the LED current waveform shown is smoothed.

The average current in the sense resistor and coil, I_{RS}, is equal to the average of the maximum and minimum threshold currents and the ripple current (hysteresis) is equal to the difference between the thresholds.

The average current in the LED, I_{LED}, is always less than I_{RS}. The feedback control loop adjusts the switch duty cycle, D, to achieve a set point at the sense resistor. This controls I_{RS}. During the interval t_{OFF}, the coil current flows through D1 and the LED load. During t_{ON}, the coil current flows through Q1, not the LEDs. Therefore, the set point is modified by D using a gating function to control I_{LED} indirectly. In order to compensate internally for the effect of the gating function, a control factor, GI_ADJ is used. GI_ADJ is set by a pair of external resistors, R_{GI1} and R_{GI2}. (**Figure 3.**) This allows the sense voltage to be adjusted to an optimum level for power efficiency without significant error in the LED controlled current.

$$GI\_ADJ = \left(\frac{RGI1}{RGI1 + RGI2}\right) \qquad \textbf{Equation 2}$$

(Boost and Buck-boost modes)

The control loop sets the duty cycle so that the sense resistor current is

$$I_{RS} = \left(\frac{0.225}{R_S}\right)\left(\frac{GI\_ADJ}{1-D}\right)\left(\frac{V_{ADJ}}{V_{REF}}\right) \qquad \textbf{Equation 3}$$

(Boost and Buck-boost modes)

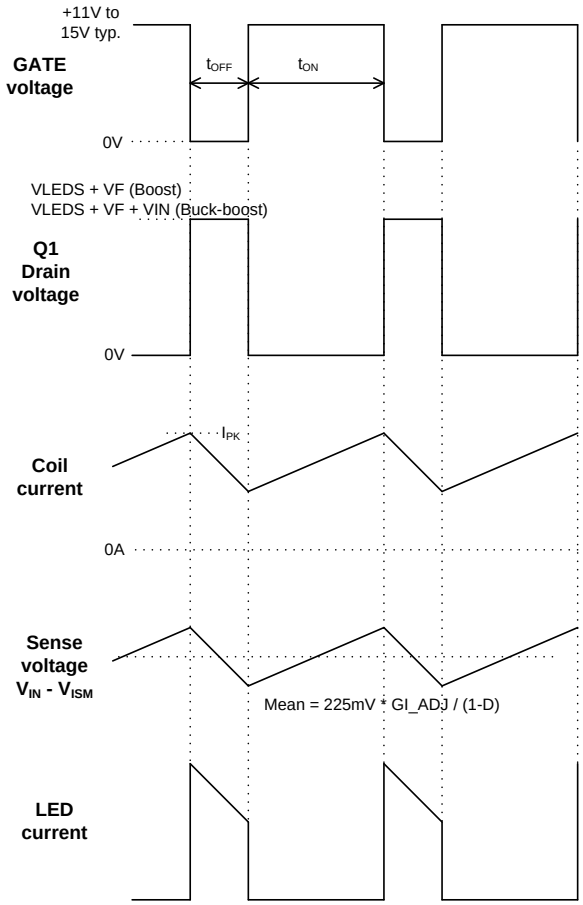


Figure 4 Operating Waveforms (Boost and Buck-Boost Modes)

I_{RS} equals the coil current. The coil is connected only to the switch and the Schottky diode. The Schottky diode passes the LED current. Therefore, the average LED current is the coil current multiplied by the Schottky diode duty cycle, 1-D.

Application Information (cont.)

$$I_{LED} = I_{RS}\,(1\text{-}D) = \left(\frac{0.225}{R_S}\right) GI\_ADJ \left(\frac{V_{ADJ}}{V_{REF}}\right) \quad \text{(Boost and Buck-boost)} \qquad \textbf{Equation 4}$$

This shows that the LED current depends on the ADJ pin voltage, the reference voltage and 3 resistor values (RS, RGI1 and RGI2). It is independent of the input and output voltages.

If the ADJ pin is connected to the REF pin, this simplifies to

$$I_{LED} = \left(\frac{0.225}{R_S}\right) GI\_ADJ \quad \text{(Boost and Buck-boost)}$$

Now I_{LED} is dependent only on the 3 resistor values.

Considering power dissipation and accuracy, it is useful to know how the mean sense voltage varies with input voltage and other parameters.

$$V_{RS} = I_{RS}\,R_S = 0.225 \left(\frac{GI\_ADJ}{1\text{-}D}\right) \left(\frac{V_{ADJ}}{V_{REF}}\right) \text{(Boost and Buck-boost)} \qquad \textbf{Equation 5}$$

This shows that the sense voltage varies with duty cycle in Boost and Buck-boost configurations.

Application Circuit Design

External component selection is driven by the characteristics of the load and the input supply, since this will determine the kind of topology being used for the system. Component selection begins with the current setting procedure, the inductor/frequency setting and the MOSFET selection. Finally, after selecting the freewheeling diode and the output capacitor (if needed), the application section will cover the PWM dimming and thermal feedback. The full procedure is greatly accelerated by the web **Calculator** spreadsheet, which includes fully automated component selection, and is available on the Diodes website. However, the full calculation is also given here.

Please note the following particular feature of the web Calculator. The GI ratio can be set for Automatic calculation, or it can be fixed at a chosen value. When optimizing a design, it is best first to optimize for the chosen voltage range of most interest, using the Automatic setting. In order to subsequently evaluate performance of the circuit over a wider input voltage range, fix the GI ratio in the Calculator input field, and then set the desired input voltage range.

Some components depend upon the switching frequency and the duty cycle. The switching frequency is regulated by the ZXLD1371Q to a large extent, depending upon conditions. This is discussed in a later paragraph dealing with coil selection.

Duty Cycle Calculation and Topology Selection

The duty cycle is a function of the input and output voltages. Approximately, the MOSFET switching duty cycle is:

$$D_{BUCK} \approx \frac{V_{OUT}}{V_{IN}} \quad \text{for Buck}$$

$$D_{BOOST} \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad \text{for Boost} \qquad \textbf{Equation 6}$$

$$D_{BB} \approx \frac{V_{OUT}}{V_{OUT} + V_{IN}} \quad \text{for Buck-Boost}$$

Because D must always be a positive number less than 1, these equations show that:

$V_{OUT} < V_{IN}$ for Buck (voltage step-down)

$V_{OUT} > V_{IN}$ for Boost (voltage step-up)

V_{OUT} > or = or < V_{IN} for Buck-boost (voltage step-down or step-up)

This allows us to select the topology for the required voltage range.

More exact equations are used in the web Calculator. These are:

$$D_{BUCK} = \frac{V_{OUT} + V_F + I_{OUT}(R_S + R_{COIL})}{V_{IN} + V_F - V_{DSON}} \quad \text{for Buck}$$

$$D_{BOOST} = \frac{V_{OUT} - V_{IN} + I_{IN}(R_S + R_{COIL}) + V_F}{V_{OUT} + V_F - V_{DSON}} \quad \text{for Boost} \qquad \textbf{Equation 7}$$

$$D_{BB} = \frac{V_{OUT} + V_F + (I_{IN} + I_{OUT})(R_S + R_{COIL})}{V_{OUT} + V_{IN} + V_F - V_{DSON}} \quad \text{for Buck-boost}$$

where: V_F = Schottky diode forward voltage, estimated for the expected coil current, I_{COIL}

V_{DSON} = MOSFET drain source voltage in the ON condition (dependent on R_{DSON} and drain current = I_{COIL})

R_{COIL} = DC winding resistance of L1

Application Information (cont.)

The additional terms are relatively small, so the exact equations will only make a significant difference at lower operating voltages at the input and output, i.e. low input voltage or a small number of LEDs connected in series. The estimates of V_F and V_{DSON} depend on the coil current. The mean coil current, I_{COIL} depends upon the topology and upon the mean terminal currents as follows:

$$I_{COIL} = I_{LED} \quad \text{for Buck}$$
$$I_{COIL} = I_{IN} \quad \text{for Boost} \qquad \textbf{Equation 8}$$
$$I_{COIL} = I_{IN} + I_{LED} \quad \text{for Buck-Boost}$$

I_{LED} is the target LED current and is already known. I_{IN} will be calculated with some accuracy later, but can be estimated now from the electrical power efficiency. If the expected efficiency is roughly 90%, the output power P_{OUT} is 90% of the input power, P_{IN}, and the coil current is estimated as follows.

$$P_{OUT} \approx 0.9\, P_{IN}$$

or

$$I_{LED}\, N\, V_{LED} \approx 0.9\, I_{IN}\, V_{IN}$$

where N is the number of LEDs connected in series, and V_{LED} is the forward voltage drop of a single LED at I_{LED}.

So $$I_{IN} \approx \frac{I_{LED}\, N\, V_{LED}}{0.9\, V_{IN}} \qquad \textbf{Equation 9}$$

Equation 9 can now be used to find I_{COIL} in **Equation 8**, which can then be used to estimate the small terms in **Equation 7**. This completes the calculation of Duty Cycle and the selection of Buck, Boost or Buck-boost topology.

An initial estimate of duty cycle is required before we can choose a coil. In **Equation** 7, the following approximations are recommended:

V_F	= 0.5V
$I_{IN} \times (R_S+R_{COIL})$	= 0.5V
$I_{OUT} \times (R_S+R_{COIL})$	= 0.5V
V_{DSON}	= 0.1V
$(I_{IN}+I_{OUT})(R_S+R_{COIL})$	= 1.1V

Then **Equation 7** becomes:

$$D_{BUCK} \approx \frac{V_{OUT} + 1}{V_{IN} + 0.4} \quad \text{for Buck}$$
$$D_{BOOST} \approx \frac{V_{OUT} - V_{IN} + 1}{V_{OUT} + 0.4} \quad \text{for Boost} \qquad \textbf{Equation 7a}$$
$$D_{BB} \approx \frac{V_{OUT} + 1.6}{V_{OUT} + V_{IN} + 0.4} \quad \text{for Buck-boost}$$

Setting the LED Current

The LED current requirement determines the choice of the sense resistor Rs. This also depends on the voltage on the ADJ pin and the voltage on the GI pin, according to the topology required.

The ADJ pin may be connected directly to the internal 1.25V reference (V_{REF}) to define the nominal 100% LED current. The ADJ pin can also be driven with an external DC voltage between 125mV and 1.25V to adjust the LED current proportionally between 10% and 100% of the nominal value.

For a divider ratio GI_ADJ greater than 0.65V, the ZXLD1371Q operates in Buck mode when V_{ADJ} = 1.25V. If GI_ADJ is less than 0.65V (typical), the device operates in Boost or buck-Boost mode, according to the load connection. This 0.65V threshold varies in proportion to V_{ADJ}, i.e., the Buck mode threshold voltage is 0.65 V_{ADj} /1.25 V.

ADJ and GI are high-impedance inputs within their normal operating voltage ranges. An internal 1.3V clamp protects the device against excessive input voltage and limits the maximum output current to approximately 4% above the maximum current set by V_{REF} if the maximum input voltage is exceeded.

Application Information (cont.)

Buck Topology

In Buck mode, GI is connected to ADJ as in **Figure 5**. The LED current depends only upon R_S, V_{ADJ} and V_{REF}. From **Equation 1** above,

$$R_{SBuck} = \left(\frac{0.218}{I_{LED}}\right)\left(\frac{V_{ADJ}}{V_{REF}}\right) \qquad \textbf{Equation 10}$$

If ADJ is directly connected to VREF, this becomes:

$$R_{SBuck} = \left(\frac{0.218}{I_{LED}}\right)$$

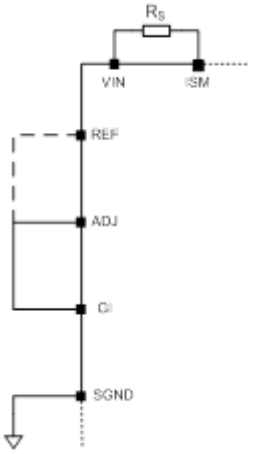


Figure 5 Setting LED current in Buck Configuration

Boost and Buck-Boost Topology

For Boost and Buck-boost topologies, the LED current depends upon the resistors, R_S, R_{GI1}, and R_{GI2} as in **Equations 4** and **2** above. There is more than one degree of freedom. That is to say, there is not a unique solution. From **Equation 4**,

$$R_{SBoostBB} = \left(\frac{0.225}{I_{LED}}\right) GI\_ADJ \left(\frac{V_{ADJ}}{V_{REF}}\right) \qquad \textbf{Equation 11}$$

If ADJ is connected to REF, this becomes

$$R_{SBoostBB} = \left(\frac{0.225}{I_{LED}}\right) GI\_ADJ$$

GI_ADJ is given by **Equation 2,** repeated here for convenience:

$$GI\_ADJ = \left(\frac{RGI1}{RGI1 + RGI2}\right)$$

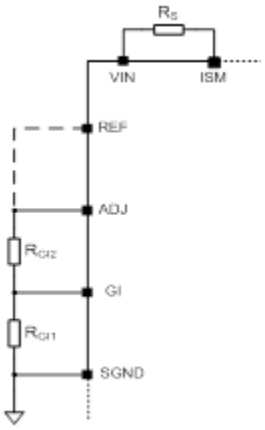


Figure 6 Setting LED current in Boost and Buck-Boost Configurations

Note that from considerations of ZXLD1371Q input bias current, the recommended limits for R_{GI1} are:

$$22k\Omega < R_{GI1} < 100k\Omega \qquad \textbf{Equation 12}$$

The additional degree of freedom allows us to select GI_ADJ within limits but this may affect overall performance a little. As mentioned above, the working voltage range at the GI pin is restricted. The permitted range of GI_ADJ in Boost or Buck-boost configuration is

$$0.2 < GI\_ADJ < 0.5 \qquad \textbf{Equation 13}$$

The mean voltage across the sense resistor is

$$V_{RS} = I_{COIL} R_S \qquad \textbf{Equation 14}$$

Note that if GI_ADJ is made larger, these equations show that R_S is increased and V_{RS} is increased. Therefore, for the same coil current, the dissipation in R_S is increased. So, in some cases, it is better to minimize GI_ADJ. However, consider **Equation 5**. If ADJ is connected to REF, this becomes

$$V_{RS} = 0.225 \left(\frac{GI\_ADJ}{1-D}\right)$$

This shows that V_{RS} becomes smaller than 225mV if GI_ADJ < 1 - D. If also D is small, V_{RS} can become too small. For example if D = 0.2, and GI_ADJ is the minimum value of 0.2, then V_{RS} becomes 0.225* 0.2 / 0.8 = 56.25 mV. This will increase the LED current error due to small offsets in the system, such as mV drop in the copper printed wiring circuit, or offset uncertainty in the ZXLD1371Q. If now, GI_ADJ is increased to 0.4 or 0.5, V_{RS} is increased to a value greater than 100mV.

Application Information (cont.)

This will give small enough I_{LED} error for most practical purposes. Satisfactory operation will be obtained if V_{RS} is more than about 80mV. This means GI_ADJ should be greater than $(1-D_{MIN}) * 80/225 = (1- D_{MIN}) * 0.355$.

There is also a maximum limit on V_{RS} which gives a maximum limit for GI_ADJ. If V_{RS} exceeds approximately 300mV, or 133% of 225mV, the STATUS output may indicate an overcurrent condition. This will happen for larger D_{MAX}. Therefore, together with the requirement of **Equation 13**, the recommended range for GI_ADJ is

$$0.355\ (1-D_{MIN}) < GI\_ADJ < 1.33\ (1-D_{MAX}) \qquad \textbf{Equation 15}$$

An optimum compromise for GI_ADJ has been suggested, i.e.

$$GI\_ADJ_{AUTO} = 1 - D_{MAX} \qquad \textbf{Equation 16}$$

This value has been used for the "Automatic" setting of the web Calculator. If $1-D_{MAX}$ is less than 0.2, then GI_ADJ is set to 0.2. If $1- D_{MAX}$ is greater than 0.5 then GI_ADJ is set to 0.5.

Once GI_ADJ has been selected, a value of RGI1 can be selected from **Equation 12**. Then RGI2 is calculated as follows, rearranging **Equation 2**:

$$R_{GI2} = R_{GI1}\left(\frac{1-GI\_ADJ}{GI\_ADJ}\right) \qquad \textbf{Equation 17}$$

For example to drive 12 LEDS at a current of 350mA from a 12V supply requires Boost configuration. Each LED has a forward voltage of 3.2V at 350mA, so Vout = 3.2*12 = 38.4V. From **Equation 6**, the duty cycle is approximately

$$\frac{(V_{OUT}-V_{IN})}{V_{OUT}} = \frac{(38.4-12)}{38.4} = 0.6875$$

From **Equation 16**, we set GI_ADJ to 1 – D = 0.3125.

IF R_{GI1} = 33kΩ, then from **Equation 17**, R_{GI2} = 33000 * (1 -0.3125) / 0.3125 = 72.6kΩ. Let us choose the preferred value R_{GI2} = 75kΩ. Now GI_ADJ is adjusted to the new value, using **Equation 2**.

$$GI\_ADJ = \left(\frac{RGI1}{RGI1 + RGI2}\right) = \frac{33k}{33k + 75k} = 0.305$$

Now we calculate Rs from **Equation 11**. Assume ADJ is connected to REF.

$$R_{SBoostBB} = \left(\frac{0.225}{I_{LED}}\right) GI\_ADJ \left(\frac{V_{ADJ}}{V_{REF}}\right) = \frac{0.225}{0.35} * 0.305 = 0.196\ \Omega$$

A preferred value of $R_{SBoostBB}$ = 0.2Ω will give the desired LED current with an error of 2% due to the preferred value selection.

Table 1 shows typical resistor values used to determine the GI_ADJ ratio with E24 series resistors.

Table 1

GI ratio	RGI1	RG2
0.2	30kΩ	120kΩ
0.25	33kΩ	100kΩ
0.3	39kΩ	91kΩ
0.35	30kΩ	56kΩ
0.4	100kΩ	150kΩ
0.45	51kΩ	62kΩ
0.5	30kΩ	30kΩ

This completes the LED current setting.

Application Information (cont.)

Inductor Selection and Frequency Control

The selection of the inductor coil, L1, requires knowledge of the switching frequency and current ripple, and also depends on the duty cycle to some extent. In the hysteretic converter, the frequency depends upon the input and output voltages and the switching thresholds of the current monitor. The peak-to-peak coil current is adjusted by the ZXLD1371Q to control the frequency to a fixed value. This is done by controlling the switching thresholds within particular limits. This effectively much reduces the overall frequency range for a given input voltage range. Where the input voltage range is not excessive, the frequency is regulated to approximately 390kHz. This is helpful in terms of EMC and other system requirements. **Figure 7** shows practical results of switching frequency driving 8 LEDs at 350mA.

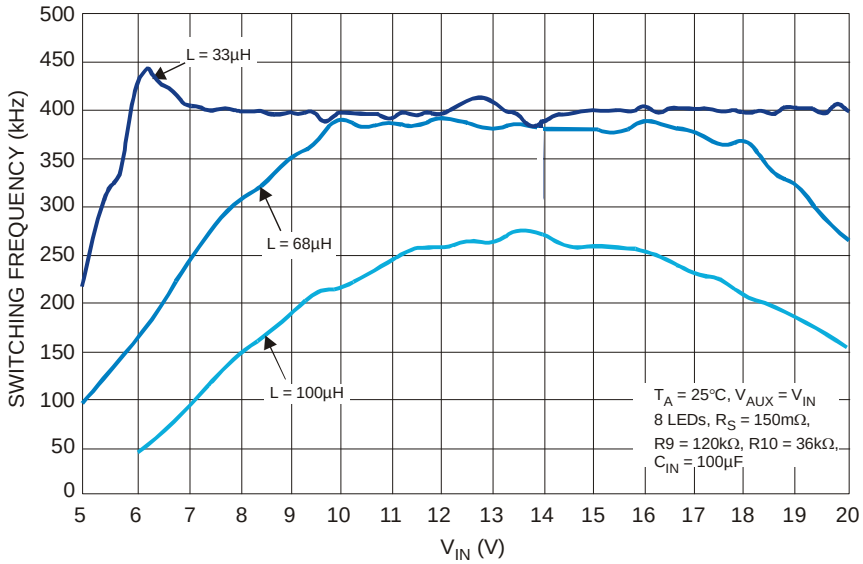


Figure 7. Frequency vs. V_{IN} for Boost LED Driver with 350mA LED Current and Various Inductor Values

For larger input voltage variation, or when the choice of coil inductance is not optimum, the switching frequency may depart from the regulated value, but the regulation of LED current remains successful. If desired, the frequency can to some extent be increased by using a smaller inductor, or decreased using a larger inductor. The web Calculator will evaluate the frequency across the input voltage range and the effect of this upon power efficiency and junction temperatures.

Determination of the input voltage range for which the frequency is regulated may be required. This calculation is very involved, and is not given here. However, the performance in this respect can be evaluated within the web Calculator for the chosen inductance.

The inductance is given as follows in terms of peak-to-peak ripple current in the coil, ΔI_L and the MOSFET on time, t_{ON}.

$$L1 = \{ V_{IN} - N V_{LED} - I_{OUT} (R_{DSON} + R_{COIL} + R_S) \} \frac{t_{ON}}{\Delta I_L} \quad \text{for Buck}$$

$$L1 = \{ V_{IN} - I_{IN}(R_{DSON} + R_{COIL} + R_S) \} \frac{t_{ON}}{\Delta I_L} \quad \text{for Boost} \qquad \textbf{Equation 18}$$

$$L1 = \{ V_{IN} - (I_{IN} + I_{OUT}) (R_{DSON} + R_{COIL} + R_S) \} \frac{t_{ON}}{\Delta I_L} \quad \text{for Buck-boost}$$

Therefore In order to calculate L1, we need to find I_{IN}, t_{ON}, and ΔI_L. The effects of the resistances are small and will be estimated.

I_{IN} is estimated from **Equation 9**.

t_{ON} is related to switching frequency, f, and duty cycle, D, as follows:

$$t_{ON} = \frac{D}{f} \qquad \textbf{Equation 19}$$

As the regulated frequency is known, and we have already found D from **Equation 7** or the approximation **Equation 7b**, this allows calculation of t_{ON}.

Application Information (cont.)

The ZXLD1371Q sets the ripple current, ΔI_L, to between nominally 10% and 30% of the mean coil current, I_{COIL}, which is found from **Equation 8**. The device adjusts the ripple current within this range in order to regulate the switching frequency. We therefore need to use a ΔI_L value of 20% of I_{COIL} to find an inductance which is optimized for the input voltage range. The range of ripple current control is also modulated by other circuit parameters as follows:

$$\Delta I_{LMAX} = \left\{ 0.06 + 0.24 \left(\frac{V_{ADJ}}{V_{REF}} \right) \right\} \frac{1-D}{GI\_ADJ} \; I_{COIL}$$

$$\Delta I_{LMIN} = \left\{ 0.02 + 0.08 \left(\frac{V_{ADJ}}{V_{REF}} \right) \right\} \frac{1-D}{GI\_ADJ} \; I_{COIL} \qquad \textbf{Equation 20}$$

$$\Delta I_{LMID} = \left\{ 0.04 + 0.16 \left(\frac{V_{ADJ}}{V_{REF}} \right) \right\} \frac{1-D}{GI\_ADJ} \; I_{COIL}$$

If ADJ is connected to REF, this simplifies to

$$\Delta I_{LMAX} = 0.3 \frac{1-D}{GI\_ADJ} \; I_{COIL}$$

$$\Delta I_{LMIN} = 0.1 \frac{1-D}{GI\_ADJ} \; I_{COIL} \qquad \textbf{Equation 20a}$$

$$\Delta I_{LMID} = 0.2 \frac{1-D}{GI\_ADJ} \; I_{COIL}$$

Where ΔI_{LMID} is the value we must use in **Equation 18**. We have now established the inductance value.

The chosen coil should saturate at a current greater than the peak sensed current. This saturation current is the DC current for which the inductance has decreased by 10% compared to the low current value.

Assuming ±10% ripple current, we can find this peak current from **Equation 8**, adjusted for ripple current:

$$I_{COILPEAK} = 1.1 \; I_{LED} \quad \text{for Buck}$$
$$I_{COILPEAK} = 1.1 \; I_{INMAX} \quad \text{for Boost} \qquad \textbf{Equation 21}$$
$$I_{COILPEAK} = 1.1 \; I_{INMAX} + I_{LED} \quad \text{for Buck-boost}$$

where I_{INMAX} is the value of I_{IN} at minimum V_{IN}.

The mean current rating is also a factor, but normally the saturation current is the limiting factor.

The following websites may be useful in finding suitable components:

www.coilcraft.com
www.niccomp.com
www.wuerth-elektronik.de

MOSFET Selection

The ZXLD1371Q requires an external NMOS FET as the main power switch with a voltage rating at least 15% higher than the maximum circuit voltage to ensure safe operation during the overshoot and ringing of the switch node. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the resistive and switching power losses.

$$P = P_{resistive} + P_{switching}$$

Resistive Power Losses

The resistive power losses are calculated using the RMS transistor current and the MOSFET on-resistance.
Calculate the current for the different topologies as follows:

Buck Mode

$$I_{MOSFETMAX} = I_{LED}$$

When operating at low V_{IN} in Buck mode a MOSFET with a suitably low V_T must be chosen to ensure that the MOSFET is properly enhanced. This is of most importance in buck mode where a Bootstrap cannot be implemented.

Boost / Buck-Boost Mode

$$I_{MOSFETMAX} = \frac{I_{LED}}{1 - D_{MAX}}$$

When operating at low V_{IN} in Boost or Buck-boost modes, a Bootstrap circuit (see figure 17) to V_{AUX} is recommended to fully enhance the external MOSFET. If a Bootstrap circuit is not implemented, then a MOSFET with a suitably low V_T must be chosen to ensure that the MOSFET is properly enhanced.

Application Information (cont.)

During the on-time, the MOSFET switch current is equal to the coil current. The rms MOSFET current is I_{COIL} √D where I_{COIL} is the mean coil current. Therefore, the approximate RMS current in the MOSFET during t_{ON} is:

Buck Mode

$$I_{MOSFETRMS} = I_{LED}\sqrt{D}$$

Boost / Buck-Boost Mode

$$I_{MOSFETRMS} = \frac{\sqrt{D}}{1-D} x\ I_{LED}$$

The resistive power dissipation of the MOSFET is:

$$P_{resistive} = I_{MOSFETRMS}^{2} x R_{DS(ON)}$$

Switching Power Losses
Calculating the switching MOSFET's switching loss depends on many factors that influence both turn-on and turn-off. Using a first order rough approximation, the switching power dissipation of the MOSFET is:

$$P_{switching} = \frac{C_{RSS} x V_{IN}^{2} x f_{SW} x I_{LOAD}}{I_{GATE}}$$

Where:

C_{RSS} is the MOSFET's reverse-transfer capacitance (a data sheet parameter),
f_{SW} is the switching frequency,
I_{GATE} is the MOSFET gate-driver's sink/source current at the MOSFET's turn-on threshold.

Matching the MOSFET with the controller is primarily based on the rise and fall time of the gate voltage. The best rise/fall time in the application is based on many requirements, such as EMI (conducted and radiated), switching losses, lead/circuit inductance, switching frequency, etc. How fast a MOSFET can be turned on and off is related to how fast the gate capacitance of the MOSFET can be charged and discharged. The relationship between C (and the relative total gate charge Qg), turn-on/turn-off time and the MOSFET driver current rating can be written as:

$$dt = \frac{dV \cdot C}{I} = \frac{Qg}{I}$$

Where:

dt = turn-on/turn-off time
dV = gate voltage
C = gate capacitance = Qg/V
I = drive current – constant current source (for the given voltage value)

Here the constant current source" I " usually is approximated with the peak drive current at a given driver input voltage.

Example 1:

Using the DMN6068 MOSFET ($V_{DS(MAX)}$ = 60V, $I_{D(MAX)}$ = 8.5A):

→ Q_G = 10.3nC at V_{GS} = 10V

ZXLD1371Q I_{PEAK} = I_{GATE} = 300mA

$$dt = \frac{Q_g}{I_{PEAK}} = \frac{10.3nC}{300mA} = 35ns$$

Assuming that cumulatively the rise time and fall time can account for a maximum of 10% of the period, the maximum frequency allowed in this condition is:

t_{PERIOD} = 20*dt → f = 1/ t_{PERIOD} = 1.43MHz

This frequency is well above the max frequency the device can handle, therefore the DNM6068 can be used with the ZXLD1371Q in the whole spectrum of frequencies recommended for the device (from 300kHz to 1MHz).

Application Information (cont.)

Example 2:

Using the ZXMN6A09KQ ($V_{DS(MAX)}$ = 60V, $I_{D(MAX)}$ = 12.2A):

→ Q_G = 29nC at V_{GS} = 10V

ZXLD1371Q I_{PEAK} = 300mA

$$dt = \frac{Q_g}{I_{PEAK}} = \frac{29nC}{300mA} = 97ns$$

Assuming that cumulatively the rise time and fall time can account for a maximum of 10% of the period, the maximum frequency allowed in this condition is:

t_{PERIOD} = 20*dt → f = 1/ t_{PERIOD} = 515kHz

This frequency is within the recommended frequency range the device can handle, therefore the ZXMN6A09KQ is recommended to be used with the ZXLD1371Q for frequencies from 300kHz to 500kHz).

The recommended total gate charge for the MOSFET used in conjunction with the ZXLD1371Q is less than 30nC.

Junction Temperature Estimation

Finally, the ZXLD1371Q junction temperature can be estimated using the following equations:

Total supply current of ZXLD1371Q:

$I_{QTOT} \approx I_Q + f \bullet Q_G$

Where I_Q = total quiescent current $I_{Q\text{-}IN} + I_{Q\text{-}AUX}$

Power consumed by ZXLD1371Q:

$P_{IC} = V_{IN} \bullet (I_Q + f \bullet Qg)$

Or in case of separate voltage supply, with V_{AUX} < 15V

$P_{IC} = V_{IN} \bullet I_{Q\text{-}IN} + V_{aux} \bullet (I_{Q\text{-}AUX} + f \bullet Qg)$

$T_J = T_A + P_{IC} \bullet \theta_{JA} =$

$T_A + P_{IC} \bullet (\theta_{JC} + \theta_{CA})$

Where the total quiescent current I_{QTOT} consists of the static supply current (I_Q) and the current required to charge and discharge the gate of the power MOSFET. Moreover, the part of thermal resistance between case and ambient depends on the PCB characteristics.

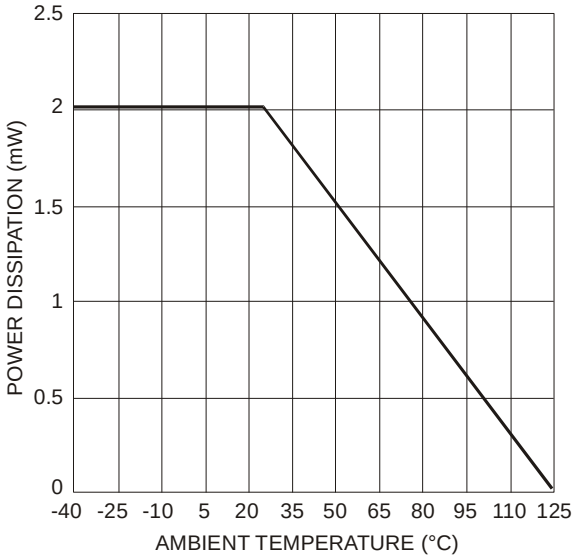


Figure 8. Power derating curve for ZXLD1371 mounted on test board according to JESD51

Application Information (cont.)

Diodes Selection

For maximum efficiency and performance, the rectifier (D1) should be a fast low capacitance Schottky diode* with low reverse leakage at the maximum operating voltage and temperature. The Schottky diode also provides better efficiency than silicon PN diodes, due to a combination of lower forward voltage and reduced recovery time.

It is important to select parts with a peak current rating above the peak coil current and a continuous current rating higher than the maximum output load current. In particular, it is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode.

The higher forward voltage and overshoot due to reverse recovery time in silicon diodes will increase the peak voltage on the Drain of the external MOSFET. If a silicon diode is used, care should be taken to ensure that the total voltage appearing on the Drain of the external MOSFET, including supply ripple, does not exceed the specified maximum value.

*A suitable Schottky diode for a switching current of up to about 1.5A would be PDS3100Q (Diodes Inc).

Output Capacitor

An output capacitor may be required to limit interference or for specific EMC purposes. For boost and buck-boost regulators, the output capacitor provides energy to the load when the freewheeling diode is reverse biased during the first switching subinterval. An output capacitor in a buck topology will simply reduce the LED current ripple below the inductor current ripple. In other words, this capacitor changes the current waveform through the LED(s) from a triangular ramp to a more sinusoidal version without altering the mean current value.

In all cases, the output capacitor is chosen to provide a desired current ripple of the LED current (usually recommended to be less than 40% of the average LED current).

Buck:

$$C_{OUTPUT} = \frac{\Delta I_{L-PP}}{8 x f_{SW} x r_{LED} x \Delta I_{LED-PP}}$$

Boost and Buck-Boost

$$C_{OUTPUT} = \frac{D x \Delta I_{L-PP}}{f_{SW} x r_{LED} x \Delta I_{LED-PP}}$$

Where:

- ΔI_{L-PP} is the ripple of the inductor current, usually ± 20% of the average sensed current
- ΔI_{LED-PP} is the ripple of the LED current, it should be <40% of the LEDs average current
- f_{sw} is the switching frequency (From graphs and calculator)
- r_{LED} is the dynamic resistance of the LEDs string (n times the dynamic resistance of the single LED from the datasheet of the LED manufacturer).

The output capacitor should be chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. The minimum RMS current for the output capacitor is calculated as follows:

Buck

$$I_{COUTPUTRMS} = \frac{I_{LED-PP}}{\sqrt{12}}$$

Boost and Buck-Boost

$$I_{COUTPUTRMS} = I_{LED} \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

Ceramic capacitors with X7R dielectric are the best choice due to their high ripple current rating, long lifetime, and performance over the voltage and temperature ranges.

Application Information (cont.)

Input Capacitor

The input capacitor can be calculated knowing the input voltage ripple ΔV_{IN-PP} as follows:

Buck

$$C_{IN} = \frac{D \times (1-D) \times I_{LED}}{f_{SW} \times \Delta V_{IN-PP}}$$ Use D = 0.5 as worst case

Boost

$$C_{IN} = \frac{\Delta I_{L-PP}}{8 \times f_{SW} \times \Delta V_{IN-PP}}$$

Buck-boost

$$C_{IN} = \frac{D \times I_{LED}}{f_{SW} \times \Delta V_{IN-PP}}$$ Use D = D_{MAX} as worst case

The minimum RMS current for the output capacitor is calculated as follows:

Buck

$$I_{CIN-RMS} = I_{LED} \times \sqrt{D \times (1-D)}$$ use D=0.5 as worst case

Boost

$$I_{CIN-RMS} = \frac{I_{L-PP}}{\sqrt{12}}$$

Buck-boost

$$I_{CIN-RMS} = I_{LED} \times \sqrt{\frac{D}{(1-D)}}$$ Use D=D_{MAX} as worst case

LED Current Dimming

The ZXLD1371Q has 3 dimming methods for reducing the average LED current:

1. DC dimming using the ADJ pin
2. PWM dimming using the PWM pin
3. DC dimming for thermal protection using the TADJ pin.

DC or Analog Dimming

The ZXLD1371Q has a clamp on the ADJ pin to prevent over-driving of the LED current which results in the maximum voltage being applied to internal circuitry is the reference voltage. This provides a 10:1 dynamic range of dc LED current adjustment.

The equation for DC dimming of the LED current is approximately:

$$I_{LED\_DIM} = I_{LED\_NOM} \left(\frac{V_{ADJ}}{V_{REF}} \right)$$

Where

I_{LED_DIM} is the dimmed LED current

I_{LED_NOM} is the LED current with V_{ADJ} = 1.25V

One consequence of DC dimming is that as the ADJ pin voltage is reduced, the sense voltage will also be reduced which has an impact on accuracy and switching frequency especially at lower ADJ pin voltages.

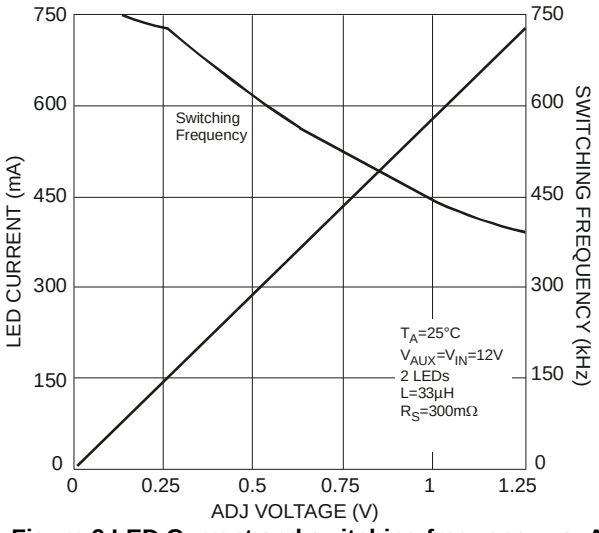


Figure 9 LED Current and switching frequency vs. ADJ Voltage

Application Information (cont.)

PWM Output Current Control & Dimming

The ZXLD1371Q has a dedicated PWM dimming input that allows a wide dimming frequency range from 100Hz to 1kHz with up to 1000:1 resolution; however higher dimming frequencies can be used – at the expense of dimming dynamic range and accuracy.

Typically, for a PWM frequency of 1kHz, the error on the current linearity is lower than 5%; in particular the accuracy is better than 1% for PWM from 5% to 100%. This is shown in the graph below:

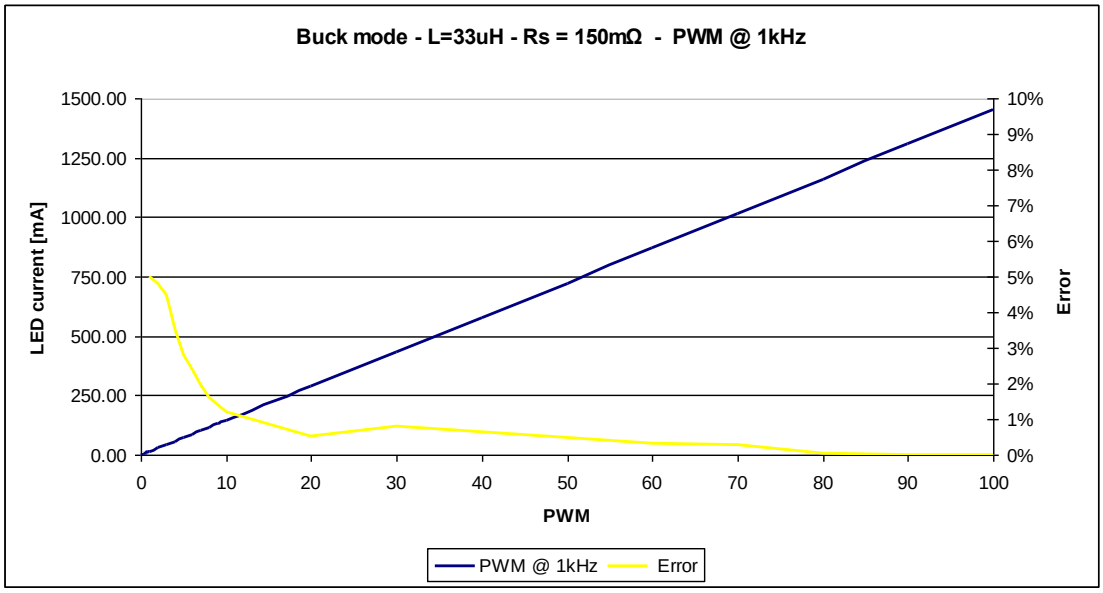


Figure 10. LED Current Linearity and Accuracy with PWM Dimming at 1kHz

For a PWM frequency of 100Hz, the error on the current linearity is lower than 2.5%; it becomes negligible for PWM greater than 5%. This is shown in the graph below:

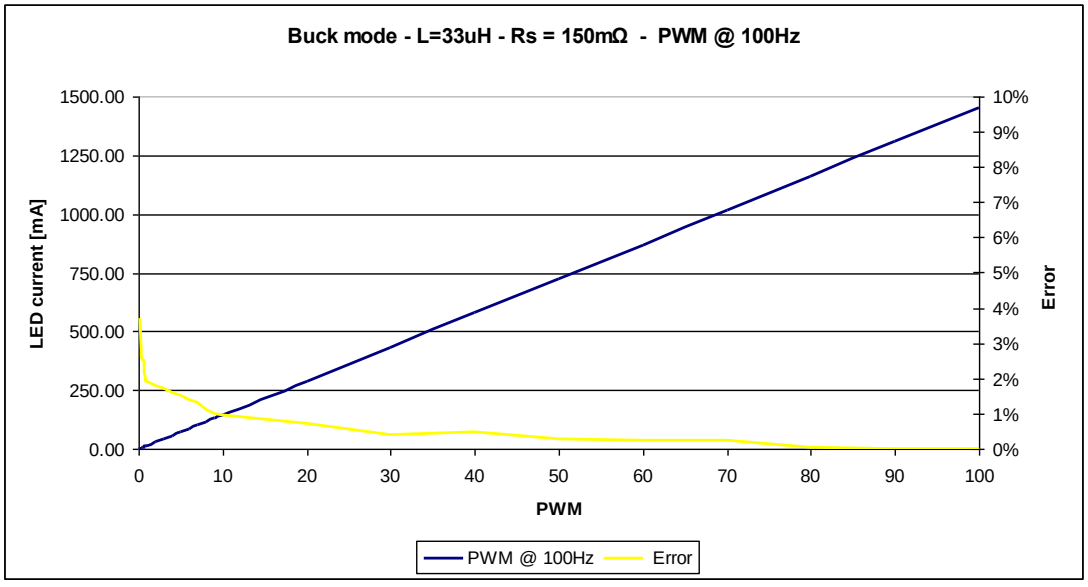


Figure 11. LED Current Linearity and Accuracy with PWM Dimming at 100Hz

The PWM pin is designed to be driven by both 3.3V and 5V logic levels and as such doesn't require open collector/drain drive. It can also be driven by an open drain/collector transistor. In this case the designer can either use the internal pull-up network or an external pull-up network in order to speed-up PWM transitions, as shown in the Boost/ Buck-Boost section.

Application Information (cont.)

LED current can be adjusted digitally, by applying a low-frequency PWM logic signal to the PWM pin to turn the controller on and off. This will produce an average output current proportional to the duty cycle of the control signal. During PWM operation, the device remains powered up and only the output switch is gated by the control signal.

The PWM signal can achieve very high LED current resolution. In fact, dimming down from 100% to 0, a minimum pulse width of 2µs can be achieved resulting in very high accuracy. While the maximum recommended pulse for the PWM signal is 10ms.

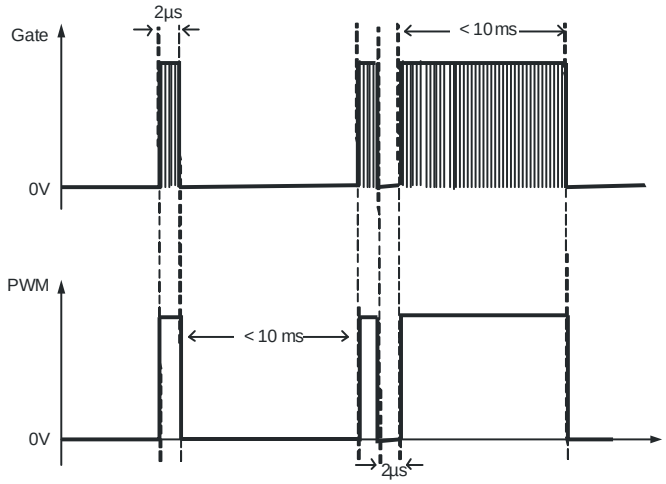


Figure 12 PWM Dimming Minimum and Maximum Pulse

The device can be put in standby by taking the PWM pin to ground, or pulling it to a voltage below 0.4V with a suitable open collector NPN or open drain NMOS transistor, for a time exceeding 15ms (nominal). In the shutdown state, most of the circuitry inside the device is switched off and residual quiescent current will be typically 90µA. In particular, the Status pin will go down to GND while the FLAG and REF pins will stay at their nominal values.

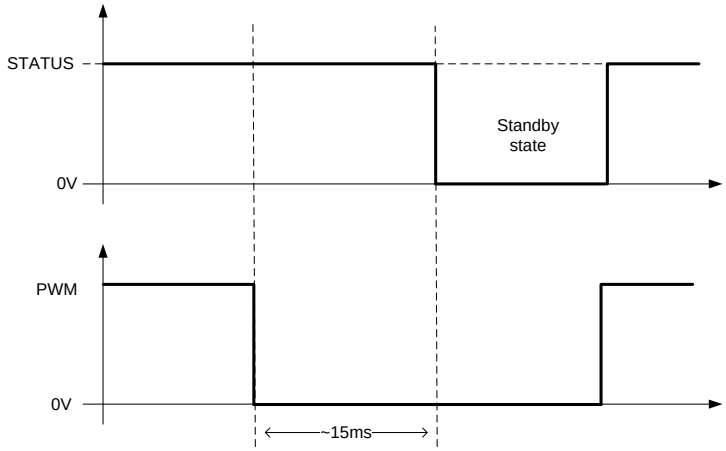


Figure 13 Stand-by State from PWM Signal

Thermal Control of LED Current

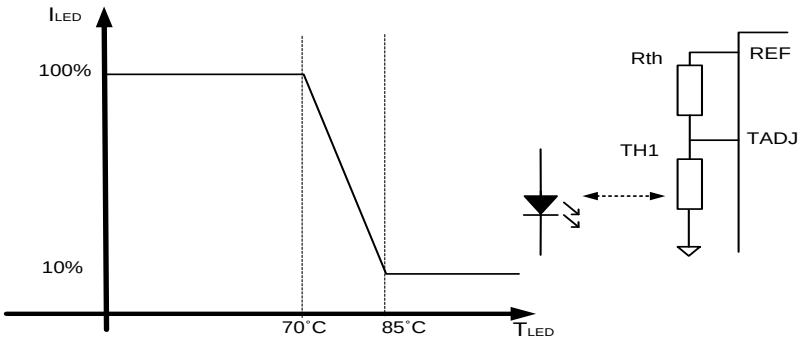
For thermal control of the LEDs, the ZXLD1371Q monitors the voltage on the TADJ pin and reduces output current if the voltage on this pin falls below 625mV. An external NTC thermistor and resistor can therefore be connected as shown below to set the voltage on the TADJ pin to 625mV at the required temperature threshold. This will give 100% LED current below the threshold temperature and a falling current above it as shown in the graph. The temperature threshold can be altered by adjusting the value of Rth and/or the thermistor to suit the requirements of the chosen LED.

The Thermal Control feature can be disabled by connecting TADJ directly to REF.

Here is a simple procedure to design the thermal feedback circuit:

1) Select the temperature threshold $T_{threshold}$ at which the current must start to decrease
2) Select the Thermistor TH1 (both resistive value at +25˚C and beta)
3) Select the value of the resistor R_{th} as R_{th} = TH at $T_{threshold}$

Application Information (cont.)



Thermal network response in Buck configuration with:
Rth = 1.8kΩ and TH1=10kΩ (beta =3900)

Figure 14 Thermal Feedback Network

The thermistor resistance, R_T, at a temperature of T degrees Kelvin is given by

$$R_T = R_R e^{B\left(\frac{1}{T} - \frac{1}{T_R}\right)}$$

Where:

R_R is the thermistor resistance at the reference temperature, T_R

T_R is the reference temperature, in Kelvin, normally 273 + 25 = 298K (+25°C)

B is the "beta" value of the thermistor.

For example,

1) Temperature threshold $T_{threshold}$ = 273 + 70 = 343K (+70˚C)
2) TH1 = 10kΩ at +25˚C and B = 3900 → R_T = 1.8kΩ @ +70˚C
3) $R_{th} = R_T$ at $T_{threshold}$ = 1.8kΩ

Overtemperature Shutdown

The ZXLD1371Q incorporates an overtemperature shutdown circuit to protect against damage caused by excessive die temperature. A warning signal is generated on the STATUS output when die temperature exceeds +125°C nominal and the output is disabled when die temperature exceeds +150°C nominal. Normal operation resumes when the device cools back down to +125°C.

Application Information (cont.)

FLAG/STATUS Outputs

The FLAG/STATUS outputs provide a warning of extreme operating or fault conditions. FLAG is an open-drain logic output, which is normally off, but switches low to indicate that a warning, or fault condition exists. STATUS is a DAC output, which is normally high (4.5V), but switches to a lower voltage to indicate the nature of the warning/fault.

Conditions monitored, the method of detection and the nominal STATUS output voltage are given in the following table (Note 18):

Table 2

Warning/Fault Condition	Severity (Note 19)	Monitored Parameters	FLAG	Nominal STATUS Voltage
Normal operation			H	4.5V
Supply undervoltage	1	V_{AUX} < 5.0V	L	4.5V
	2	V_{IN} < 5.6V	L	< 3.6V
Output current out of regulation (Note 20)	2	V_{SHP} outside normal voltage range	L	3.6V
Driver stalled with switch 'on', or 'off' (Note 21)	2	t_{ON}, or t_{OFF} > 100µs	L	3.6V
Device temperature above maximum recommended operating value	3	T_J > 125°C	L	1.8V
Sense resistor current I_{RS} above specified maximum	4	V_{SENSE} > 0.3V	L	0.9V

Notes:
18. These STATUS pin voltages apply for an input voltage, V_{IN}, of 7.5V < V_{IN} < 60V. Below 7.5V the STATUS pin voltage levels reduce and therefore may not report the correct status. For 5.4V < V_{IN} < 7.5V the flag pin still reports an error by going low. At low V_{IN} in Boost and Buck-boost modes an over-current status may be indicated when operating at high boost ratios -– this due to the feedback loop increasing the sense voltage.
19. Severity 1 denotes lowest severity.
20. This warning will be indicated if the output power demand is higher than the available input power; the loop may not be able to maintain regulation.
21. This warning will be indicated if the gate pin stays at the same level for greater than 100µs (e.g. the output transistor cannot pass enough current to reach the upper switching threshold).

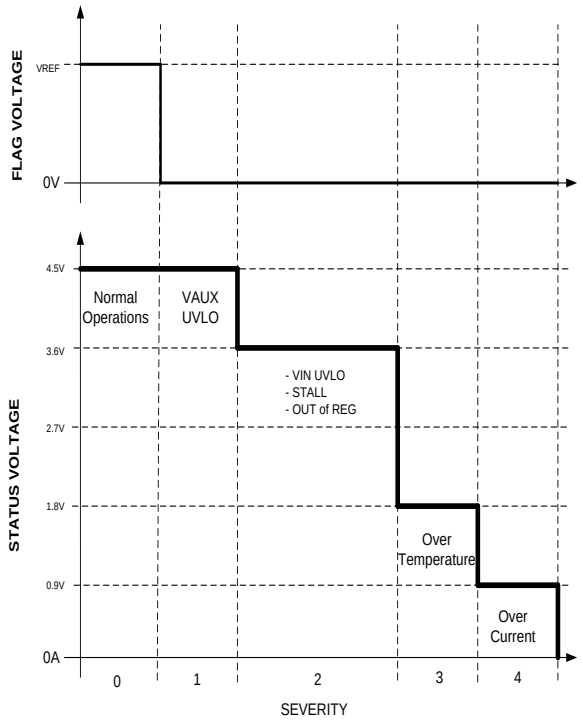


Figure 15. Status levels

Application Information (cont.)

In the event of more than one fault/warning condition occurring, the higher severity condition will take precedence. E.g. 'Excessive coil current' and 'Out of regulation' occurring together will produce an output of 0.9V on the STATUS pin.

If V_{ADJ}>1.7V, V_{SENSE} may be greater than the excess coil current threshold in normal operation and an error will be reported. Hence, STATUS and FLAG are only guaranteed for V_{ADJ}<=V_{REF}.

Diagnostic signals should be ignored during device start-up for 100µs. The device start-up sequence will be initiated both during the first power on of the device or after the PWM signal is kept low for more than 15ms, initiating the standby state of the device.

In particular, during the first 100µs the diagnostic is signaling an over-current then an out-of-regulation status. These two events are due to the charging of the inductor and are not true fault conditions.

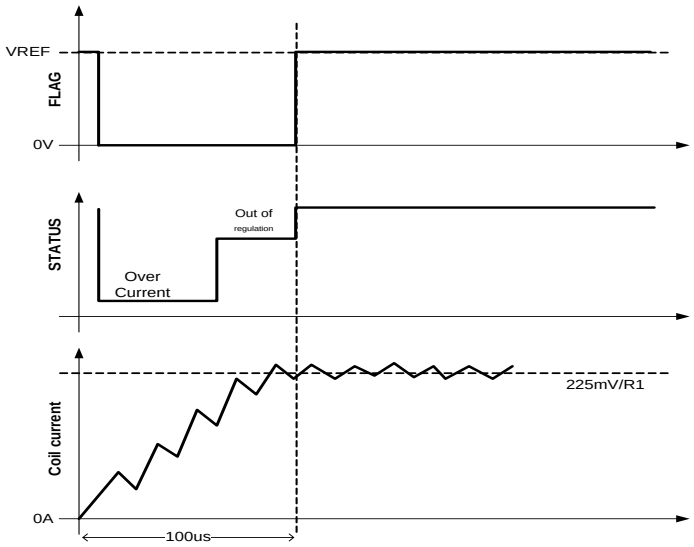


Figure 16 Diagnostic during Start-up

Reduced Input Voltage Operation

To facilitate operation in automotive and other applications, that have large transient reductions in system supply voltage, the ZXLD1371Q is now capable of operating down to input voltages as low as 5.0V. Care must be taken when operating at these lower supply voltages to ensure that the external MOSFET is correctly enhanced and that the boosting ratio is not increased to excessive amounts where both the duty cycle and peak-switch current limits are not exceeded. The device will operate down to 5.0V, but for reliable start-up, V_{IN} must be higher than 5.4V. The designer should also take into account any noise that may occur on the supply lines.

In Buck-Boost and Boost Modes (most common topologies for applications likely to require transient operation down to supply voltages approaching 5.0V) as the input voltage reduces then the peak switch current will increase the ZXLD1371Q compensates for this by allowing the sense voltage to increase while maintaining regulation of the LED current. However, if the boost ratio (switch output voltage/input voltage) is increased too much then the sense voltage could be increased too much causing an overcurrent flag to be triggered and/or loss of regulation.

In addition to this, increased power dissipation will occur in the external MOSFET switch – especially if the external MOSFET has a large threshold. One way of overcoming this is to apply a bootstrap network to the V_{AUX} pin (see next section).

If the ZXLD1371Q is used in Buck Mode at low voltages, then the bootstrap network cannot be implemented and so a low threshold MOSFET with low gate capacitance should be used. Some loss of regulation is expected to occur at voltages below 6V – see Buck mode Typical Characteristics Section.

When using the ZXLD1371Q in applications with transient input voltage excursions we recommend using the web calculator to optimize operation over the normal operating band. Then change the input range to include the transient excursion while keeping the optimized component selection to check expected function during the transient input voltage conditions.

Application Information (cont.)

Boosting V_{AUX} Supply Voltage in Boost and Buck-Boost Mode

At low V_{IN}, depending on the characteristics of the external MOSFET, the gate voltage may not be enough to fully enhance the power MOSFET. A bootstrap boosting technique can be used to increase the gate drive voltage at low input voltage. See Figure 17 for circuit diagram. This can be particularly important for extended use at low input voltages as this is when the switch current will be at its greatest – resulting in greatest heat generation within the MOSFET.

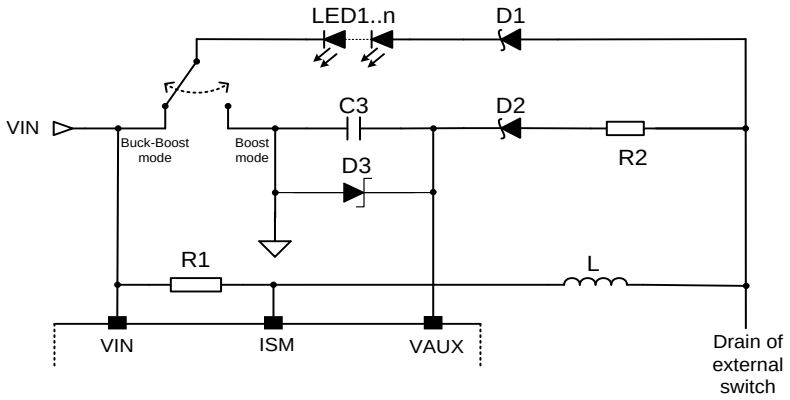


Figure 17 Bootstrap Circuit for Boost and Buck-Boost Low Voltage Operations

The Bootstrap circuit guarantees that the MOSFET is fully enhanced, reducing both the power dissipation and the risk of thermal runaway of the MOSFET itself. The bootstrap circuit consists of an extra diode D2 and decoupling capacitor C3 which are used to generate a boosted voltage at V_{AUX}. This enables the device to operate with full output current when V_{IN} is at the minimum value of 5V. The resistor R2 can be used to limit the current in the bootstrap circuit in order to reduce the impact of the circuit itself on the LED accuracy. A typical value would be 100Ω. The impact on the LED current is usually a decrease of maximum 5% compared to the nominal current value set by the sense resistor.

The Zener diode D3 is used to limit the voltage on the V_{AUX} pin to less than 60V.

Due to the increased number of components and the loss of current accuracy, the bootstrap circuit is recommended only when the system has to operate continuously in conditions of low input voltage (between 5 and 8V) and high load current. Other circumstances such as low input voltage at low load current, or transient low input voltage at high current should be evaluated keeping account of the external MOSFET's power dissipation.

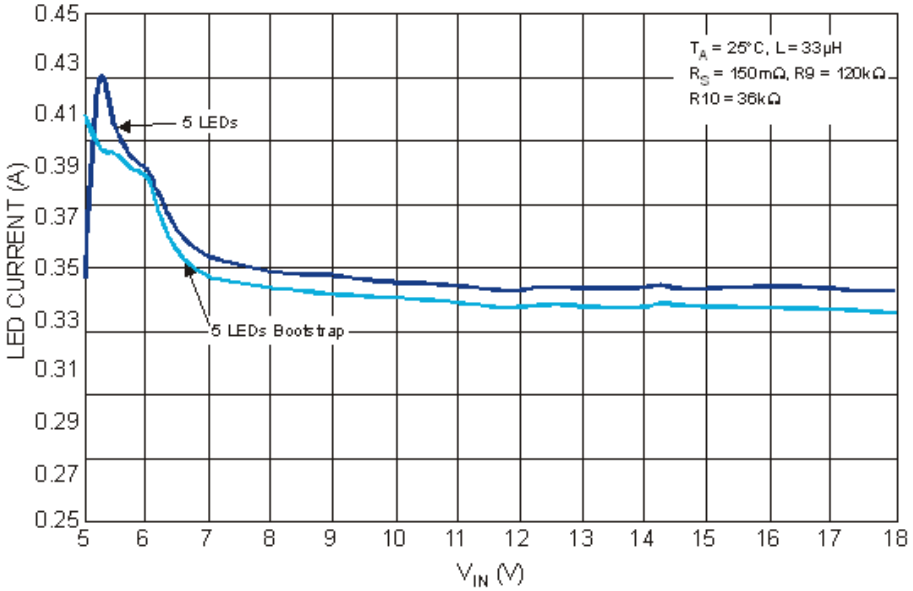


Figure 18 Effect of Bootstrap on LED Current in Buck-Boost Mode

Application Information (cont.)

Overvoltage Protection

The ZXLD1371Q is inherently protected against open-circuit load when used in Buck configuration. However, care has to be taken with open-circuit load conditions in Buck-Boost or Boost configurations. This is because in these configurations there is no internal open-circuit protection mechanism for the external MOSFET. In this case, an Overvoltage-Protection (OVP) network should be provided externally to the MOSFET to avoid damage due to open circuit conditions. This is shown in Figure 19 below, highlighted in the dotted blue box.

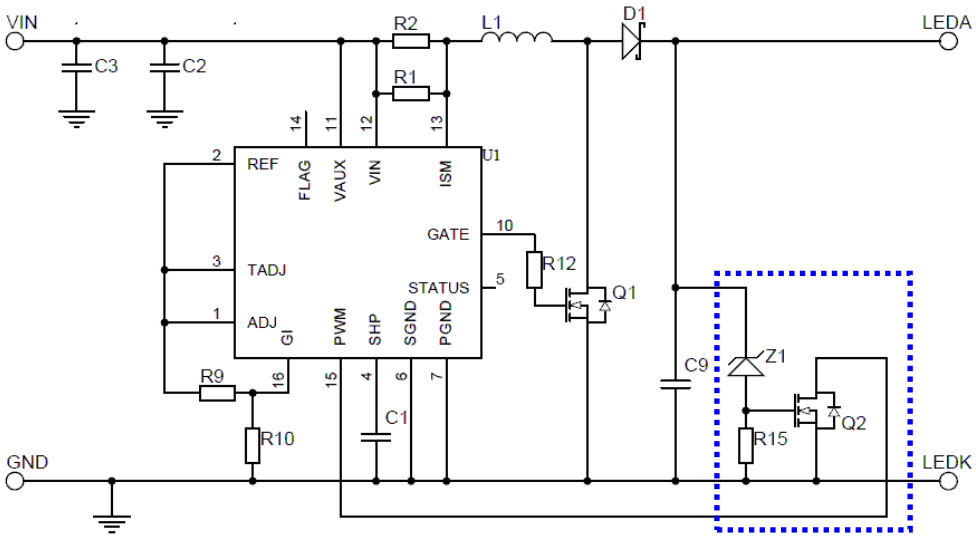


Figure 19 OVP Circuit

The zener voltage is determined according to: Vz = V_{LEDMAX} +10% where V_{LEDMAX} is maximum LED chain voltage.

If the LEDA voltage exceeds V_Z, the gate of MOSFET Q2 will rise turning Q2 on. This will pull the PWM pin low and switch off Q1 until the voltage on the drain of Q1 falls below Vz. If the voltage at LEDA remains above V_Z for longer than 20ms then the ZXLD1371Q will enter into a shutdown state.

Care should be taken to ensure that the maximum gate voltage of the Q2 MOSFET is not exceeded.

Take care of the max voltage drop on the Q2 MOSFET gate. Typical devices for Z1 and Q2 are BZX84C and 2N7002.

Application Information (cont.)

PCB Layout Considerations

PCB layout is fundamental to device performance in all configurations. **Figure 20** shows a section of a proven ZXLD1371Q PCB layout.

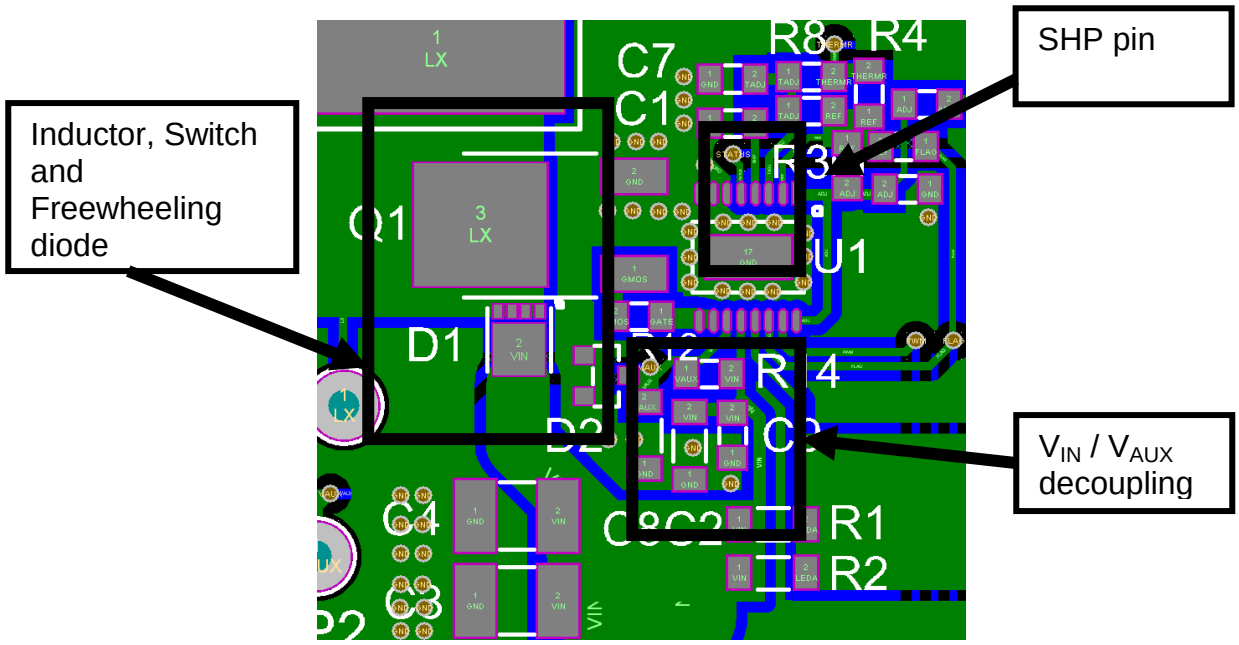


Figure 20. Circuit Layout

Here are some considerations useful for the PCB layout using ZXLD1371Q in Buck, Boost and Buck-Boost configurations:

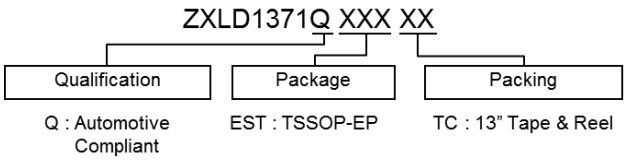
- In order to avoid ringing due to stray inductances, the inductor L1, the anode of D1 and the drain of Q1 should be placed as close together as possible.
- The shaping capacitor C1 is fundamental for the stability of the control loop. To this end it should be placed no more than 5mm from the SHP pin.
- Input voltage pins, V_{IN} and V_{AUX}, need to be decoupled. It is recommended to use two ceramic capacitors of 2.2µF, X7R, 100V (C3 and C4). In addition to these capacitors, it is suggested to add two ceramic capacitors of 1µF, X7R, 100V each (C2, C8), as well as a further decoupling capacitor of 100nF close to the V_{IN}/V_{AUX} pins (C9). V_{IN} and V_{AUX} pins can be short-circuited when the device is used in buck mode, or can be driven from a separate supply.
- The underside of the PCB should be a solid copper ground plane, electrically bonded to top ground copper at regular intervals using plated-through via holes. The ground plane should be unbroken as far as possible, particularly in the area of the switching circuit including the ZXLD1371Q, L1, Q1 D, C3 and C4. Plated via holes are necessary to provide a short electrical path to minimize stray inductance. Critical positions of via holes include the decoupling capacitors, the source connection of the MOSFET and the ground connections of the ZXLD1371Q, including the center paddle. These via holes also serve to conduct heat away from the semiconductors and minimize the device junction temperatures.

Evaluation Boards

To support easier evaluation of the ZXLD1371Q, three evaluation boards have been developed which are available via your Diodes sales representative for qualified opportunities:

ZXLD1371EV4	Buck Configuration
ZXLD1371EV5	Buck-Boost Configuration
ZXLD1371EV6	Boost Configuration

Ordering Information



Part Number	Packaging (Note 22)	Package Code	Packing: 13" Tape and Reel			Qualification (Note 23)
			Reel Quantity	Tape Width	Part Number Suffix	
ZXLD1371QESTTC	TSSOP-16EP	EST	2,500	16mm	TC	Automotive Compliant

Notes: 22. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
23. ZXLD1371Q has been qualified to AEC-Q100 grade 1 and is classified as "Automotive Compliant" supporting PPAP documentation. See ZXLD1371 datasheet for commercial qualified versions.

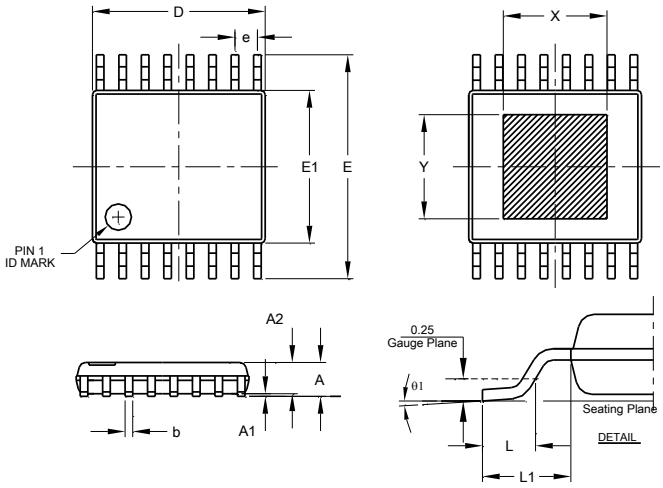
Marking Information

TSSOP-16EP

Where YY is Last Two Digits of Year and WW is Two Digit Week Number

Package Outline Dimensions (All Dimensions in mm)

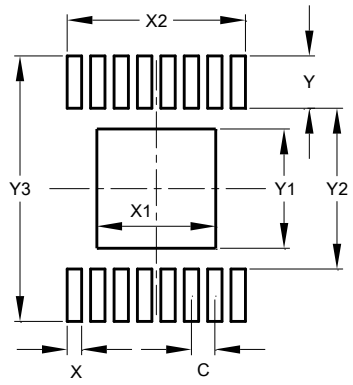
Please see http://www.diodes.com/package-outlines.html for the latest version.



TSSOP-16EP			
Dim	**Min**	**Max**	**Typ**
A	-	1.20	-
A1	0.025	0.100	-
A2	0.80	1.05	0.90
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	5.00
E	6.20	6.60	6.40
E1	4.30	4.50	4.40
e	0.65 BSC		
L	0.45	0.75	0.60
L1	1.0 REF		
L2	0.65 BSC		
X	-	-	2.997
Y	-	-	2.997
θ1	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)
C	0.650
X	0.450
X1	3.290
X2	5.000
Y	1.450
Y1	3.290
Y2	4.450
Y3	7.350

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