

30V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(on)} max	I _D max T _A = 25°C (Notes 4 & 7)
Q1 3	201/	120m Ω @ V _{GS} = 10V	3.7A
	30V	180mΩ @ $V_{GS} = 4.5V$	3.0A
Q2	-30V	210mΩ @ V _{GS} = -10V	-2.7A
		330mΩ @ V _{GS} = -4.5V	-2.2A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance (R_{DS(on)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- MOSFET gate drive
- LCD backlight inverters
- Motor control
- Portable applications

Features and Benefits

- Low profile package, for thin applications
- Low $R_{\theta JA}$, thermally efficient package
- 6mm² footprint, 50% smaller than TSOP6 and SOT23-6
- Low on-resistance
- Fast switching speed
- "Lead-Free", RoHS Compliant (Note 1)
- Halogen and Antimony Free. "Green" Device (Note 2)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

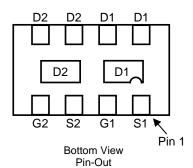
- Case: DFN3020B-8
- Terminals: Pre-Plated NiPdAu leadframe
- Nominal package height: 0.8mm
- UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Solderable per MIL-STD-202, Method 208
- Weight: 0.013 grams (approximate)

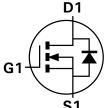


Top View



Bottom View







Q1 N-Channel

Q2 P-Channel

D2

Equivalent Circuit

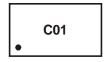
Ordering Information (Note 3)

ĺ	Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
	ZXMC3AMCTA	C01	7	8	3000

Notes:

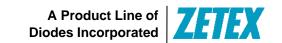
- 1 No purposefully added lead
- 2. Diodes Inc's "Green" policy can be found on our website at http://www.diodes.com.
- 3. For packaging details, go to our website at http://www.diodes.com.

Marking Information



C01 = Product Type Marking Code Top view, Dot Denotes Pin 1





Maximum Ratings @T_A = 25°C unless otherwise specified

C	Symbol	N-channel – Q1	P-channel – Q2	Unit		
Drain-Source Voltage			V_{DSS}	30	-30	V
Gate-Source Voltage	Gate-Source Voltage			±20	±20	V
		(Notes 4 & 7)		3.7	-2.7	
Continuous Drain Current	$V_{GS} = 10V$	T _A = 70°C (Notes 4 & 7)	I _D	3.0	-2.2	^
		(Notes 3 & 7)		2.9	-2.1	A
Pulsed Drain Current	$V_{GS} = 10V$	(Notes 6 & 7)	I _{DM}	13	-9.2	
Continuous Source Current (Body diode) (Notes 4 & 7)		(Notes 4 & 7)	Is	3.2	-2.8	
Pulse Source Current (Body diode) (Notes 6 & 7)			I _{SM}	13	-9.2	

Thermal Characteristics @TA = 25°C unless otherwise specified

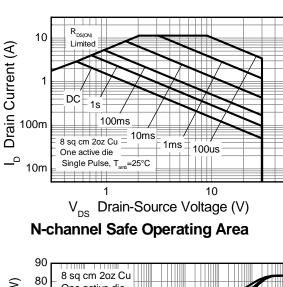
Characteristic	_	Symbol	N-channel – Q1 P-channel – Q2	Unit	
	(Notes 3 & 7)		1.50 12		
Power Dissipation	(Notes 4 & 7)		2.45 19.6	W	
Linear Derating Factor	(Notes 5 & 7)	- P _D	1.13 9	mW/°C	
	(Notes 5 & 8)		1.70 13.6		
	(Notes 3 & 7)		83.3		
Thermal Desistance Investigate Archiest	(Notes 4 & 7)		51.0		
Thermal Resistance, Junction to Ambient	(Notes 5 & 7)	R _{0JA}	111	°C/W	
	(Notes 5 & 8)		73.5		
Thermal Resistance, Junction to Lead (Notes 7 & 9)		$R_{ heta JL}$	17.1		
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C		

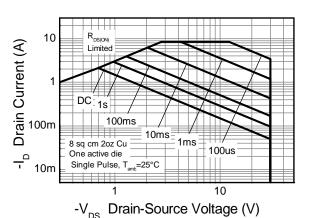
Notes:

- 3. For a device surface mounted on 28mm x 28mm (8cm²) FR4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady-state condition. The heatsink is split in half with the exposed drain pads connected to each half.
- 4. Same as note (3) except the device is measured at t < 5 sec.
- 5. Same as note (3), except the device is surface mounted on 31mm x 31mm (10cm²) FR4 PCB with high coverage of single sided 1oz copper.
- 6. Same as note (3), except the device is pulsed with D = 0.02 and pulse width 300µs. The pulse current is limited by the maximum junction temperature.
- 7. For a dual device with one active die.
- 8. For dual device with 2 active die running at equal power.
- 9. Thermal resistance from junction to solder-point (at the end of the drain lead).

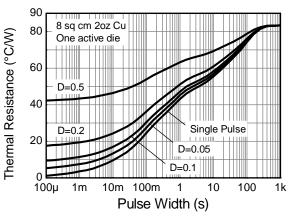


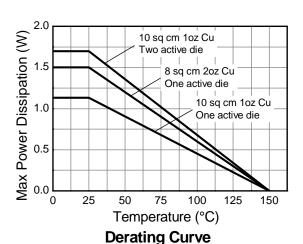
Thermal Characteristics



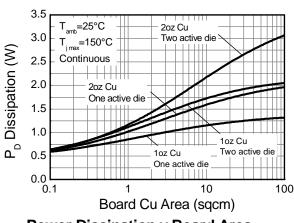


P-channel Safe Operating Area





Transient Thermal Impedance

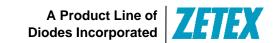


225 200 Thermal Resistance (°C/W) 1oz Cu One active die 175 1oz Cu 150 Two active die 125 100 75 2oz Cu 50 One active die 25 Two active die 0.1 100 Board Cu Area (sqcm)

Power Dissipation v Board Area

Thermal Resistance v Board Area





Electrical Characteristics – Q1 N-Channel @TA = 25°C unless otherwise specified

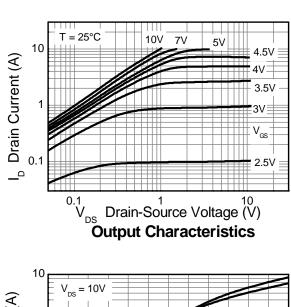
Characteristic	Symbol	Min	Тур	Max	Unit	Test (Condition	
OFF CHARACTERISTICS						1		
Drain-Source Breakdown Voltage	BV _{DSS}	30	-	-	V	$I_D = 250 \mu A, V_{GS} = 0 V$		
Zero Gate Voltage Drain Current	I _{DSS}	-	-	0.5	μΑ	$V_{DS} = 30V, V_{GS} = 0V$		
Gate-Source Leakage	I _{GSS}	-	-	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$		
ON CHARACTERISTICS								
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	$I_D = 250 \mu A, V_E$	os = Vgs	
Static Drain-Source On-Resistance (Note 10)	D		0.100	0.120	Ω	$V_{GS} = 10V, I_D$	= 2.5A	
Static Drain-Source On-Nesistance (Note 10)	R _{DS (ON)}	,	0.140	0.180	22	$V_{GS} = 4.5V, I_D$	= 2.0A	
Forward Transconductance (Note 10 & 11)	g fs	1	3.5	-	S	V _{DS} = 10V, I _D = 2.5A		
Diode Forward Voltage (Note 10)	V_{SD}	ì	0.85	0.95	V	I _S = 1.7A, V _{GS} = 0V		
Reverse Recover Time (Note 11)	t _{rr}	ı	17.7	-	ns	I _S = 2.5A, di/dt= 100A/µs		
Reverse Recover Charge (Note 11)	Q _{rr}	ì	13.0	-	nC	1S = 2.5A, di/di	ι= 100Α/μS	
DYNAMIC CHARACTERISTICS (Note 11)								
Input Capacitance	C _{iss}	•	190	-	pF	V 05V V 0V		
Output Capacitance	Coss	•	38	-	pF	$V_{DS} = 25V, V_{G}$ - $f = 1.0MHz$	ss = UV,	
Reverse Transfer Capacitance	C _{rss}	-	20	-	рF	1 = 1.000112		
Total Gate Charge (Note 12)	Q_{g}	1	2.3	-	nC	$V_{GS} = 4.5V$		
Total Gate Charge (Note 12)	Qg	-	3.9	-	nC		$V_{DS} = 15V$	
Gate-Source Charge (Note 12)	Q_gs	-	0.6	-	nC	$V_{GS} = 10V \qquad I_{D} = 2.5A$		
Gate-Drain Charge (Note 12)	Q_{gd}	-	0.9	-	nC			
Turn-On Delay Time (Note 12)	t _{D(on)}	-	1.7	-	ns			
Turn-On Rise Time (Note 12)	t _r	-	2.3	-	ns	$V_{DS} = 15V, I_{D}$	= 2.5A	
Turn-Off Delay Time (Note 12)	t _{D(off)}	-	6.6	-	ns	$V_{GS} = 10V, R_G = 6\Omega$		
Turn-Off Fall Time (Note 12)	t _f	1	2.9	-	ns			

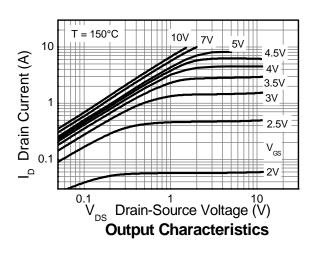
Notes:

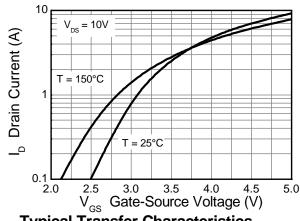
- 10. Measured under pulsed conditions. Width ≤ 300µs. Duty cycle ≤ 2%.
 11. For design aid only, not subject to production testing.
 12. Switching characteristics are independent of operating junction temperature.

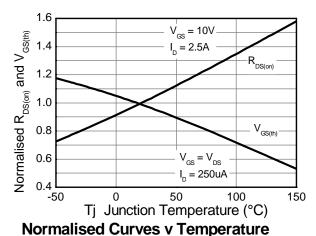


Typical Electrical Characteristics – Q1 N-Channel

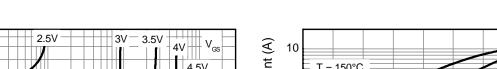


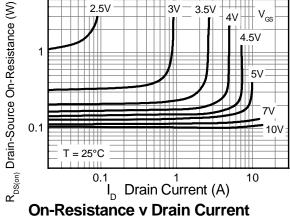


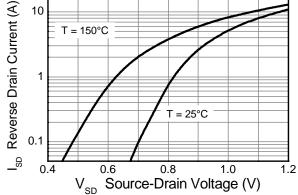




Typical Transfer Characteristics



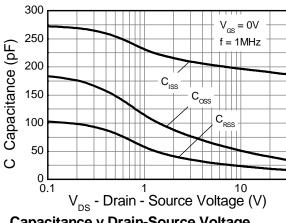


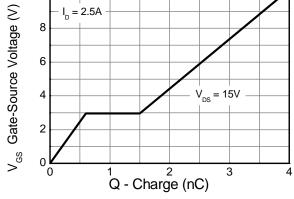


Source-Drain Diode Forward Voltage



Typical Electrical Characteristics - Q1 N-Channel - Continued



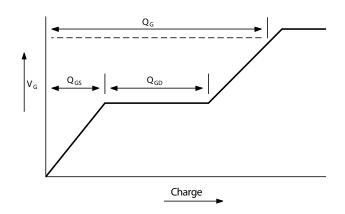


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Capacitance v Drain-Source Voltage

Gate-Source Voltage v Gate Charge

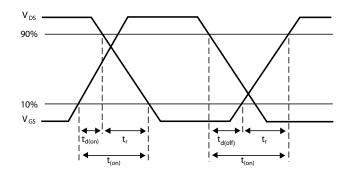
Test Circuits

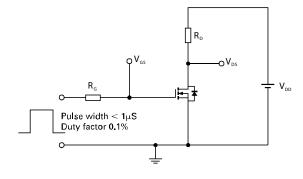


Current regulator (1) Ic J⊑T D.U.T

Basic gate charge waveform

Gate charge test circuit

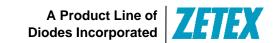




Switching time waveforms

Switching time test circuit





Electrical Characteristics – Q2 P-Channel @TA = 25°C unless otherwise specified

Characteristic	Symbol	Min	Тур	Max	Unit	Test C	Condition
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV _{DSS}	-30	-	-	V	$I_D = -250 \mu A, V_{GS} = 0 V$	
Zero Gate Voltage Drain Current	I _{DSS}	-	-	-0.5	μΑ	$V_{DS} = -30V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	-	-	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS							
Gate Threshold Voltage	V _{GS(th)}	-1.0	-	-3.0	V	$I_D = -250 \mu A, V_1$	$DS = V_{GS}$
Static Drain-Source On-Resistance (Note 13)	Ь		0.150	0.210	Ω	$V_{GS} = -10V, I_D$	= -1.4A
Static Drain-Source Off-Resistance (Note 13)	R _{DS (ON)}	-	0.280	0.330	12	$V_{GS} = -4.5V, I_{D}$	e -1.1A
Forward Transconductance (Note 13 & 14)	g fs	-	2.48	-	S	$V_{DS} = -15V, I_D$	= -1.4A
Diode Forward Voltage (Note 13)	V_{SD}	-	-0.85	-0.95	V	I _S = -1.1A, V _{GS} = 0V	
Reverse Recover Time (Note 14)	t _{rr}	-	18.6	-	ns		
Reverse Recover Charge (Note 14)	Q _{rr}	-	14.8 -		nC	$I_S = -0.95A$, di/dt = 100A/ μ s	
DYNAMIC CHARACTERISTICS (Note 14)							
Input Capacitance	C _{iss}	-	206	-	pF	4514.14	
Output Capacitance	Coss	-	59.3	-	pF	$V_{DS} = -15V, V_{C}$ f = 1.0MHz	SS = UV,
Reverse Transfer Capacitance	C _{rss}	-	49.2	-	pF	1 = 1.01/11/12	
Total Gate Charge (Note 15)	Q_{g}	-	3.8	-	nC	$V_{GS} = -4.5V$	
Total Gate Charge (Note 15)	Qq	-	6.4	-	nC		$V_{DS} = -15V$
Gate-Source Charge (Note 15)	Q_{gs}	-	0.69	-	nC	$V_{GS} = -10V$	$I_D = -1.4A$
Gate-Drain Charge (Note 15)	Q _{qd}	-	2.0	-	nC		
Turn-On Delay Time (Note 15)	t _{D(on)}	-	1.5	-	ns		
Turn-On Rise Time (Note 15)	t _r	-	2.8	-	ns	$V_{DS} = -15V, I_{D}$	= -1A
Turn-Off Delay Time (Note 15)	t _{D(off)}	-	11.3	-	ns $V_{GS} = -10V$, $R_G = 6\Omega$		3 = 6Ω
Turn-Off Fall Time (Note 15)	t _f	-	7.5	-	ns		

Notes:

- 13. Measured under pulsed conditions. Width \leq 300 μ s. Duty cycle \leq 2%.
- 14. For design aid only, not subject to production testing.15. Switching characteristics are independent of operating junction temperature.



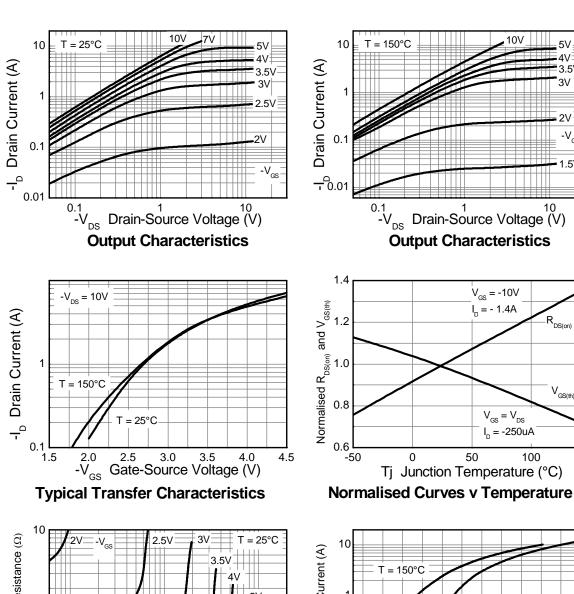
'3V

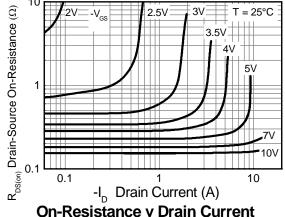
1.5V

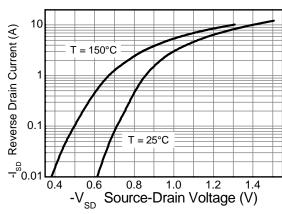
R_{DS(on)}

 $V_{\text{GS(th)}}$

Typical Electrical Characteristics - Q2 P-Channel

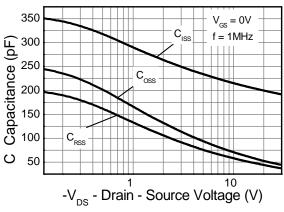




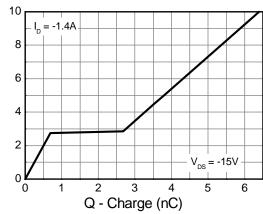




Typical Electrical Characteristics - Q2 P-Channel - Continued



-V_{GS} Gate-Source Voltage (V)

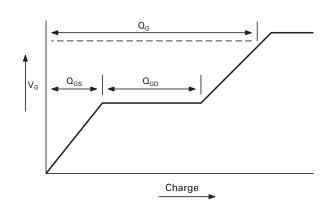


Capacitance v Drain-Source Voltage

Gate-Source Voltage v Gate Charge

Current regulator

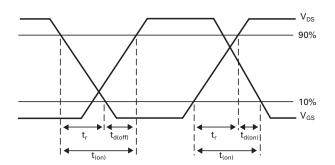
Test Circuits

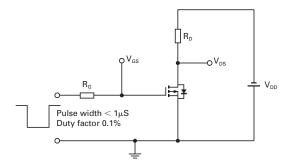


J**云**‡D.U.T

Basic gate charge waveform

Gate charge test circuit



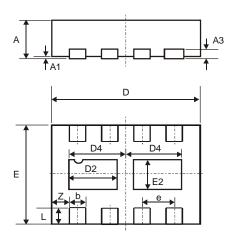


Switching time waveforms

Switching time test circuit

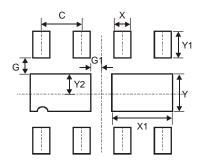


Package Outline Dimensions



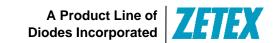
DFN3020B-8						
Dim	Min	Max	Тур			
Α	0.77	0.83	0.80			
A1	0	0.05	0.02			
A3	-	-	0.15			
b	0.25	0.35	0.30			
D	2.95	3.075	3.00			
D2	0.82	1.02	0.92			
D4	1.01	1.21	1.11			
е	-	-	0.65			
Е	1.95	2.075	2.00			
E2	0.43	0.63	0.53			
L	0.25	0.35	0.30			
Z	-	-	0.375			
All Dimensions in mm						

Suggested Pad Layout



Dimensions	Value (in mm)
С	0.650
G	0.285
G1	0.090
X	0.400
X1	1.120
Y	0.730
Y1	0.500
Y2	0.365





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