

# Data Sheet

## aIVR341N – 341 sec

### **APLUS INTEGRATED CIRCUITS INC.**

**Address:**

3 F-10, No. 32, Sec. 1, Chenggung Rd., Taipei,  
Taiwan 115, R.O.C.  
(115)台北市南港區成功路一段 32 號 3 樓之 10.

**TEL:** 886-2-2782-9266

**FAX:** 886-2-2782-9255

**WEBSITE :** <http://www.aplusinc.com.tw>

**Sales E-mail:**

[sales@aplusinc.com.tw](mailto:sales@aplusinc.com.tw)

**Support E-mail:**

[service@aplusinc.com.tw](mailto:service@aplusinc.com.tw)

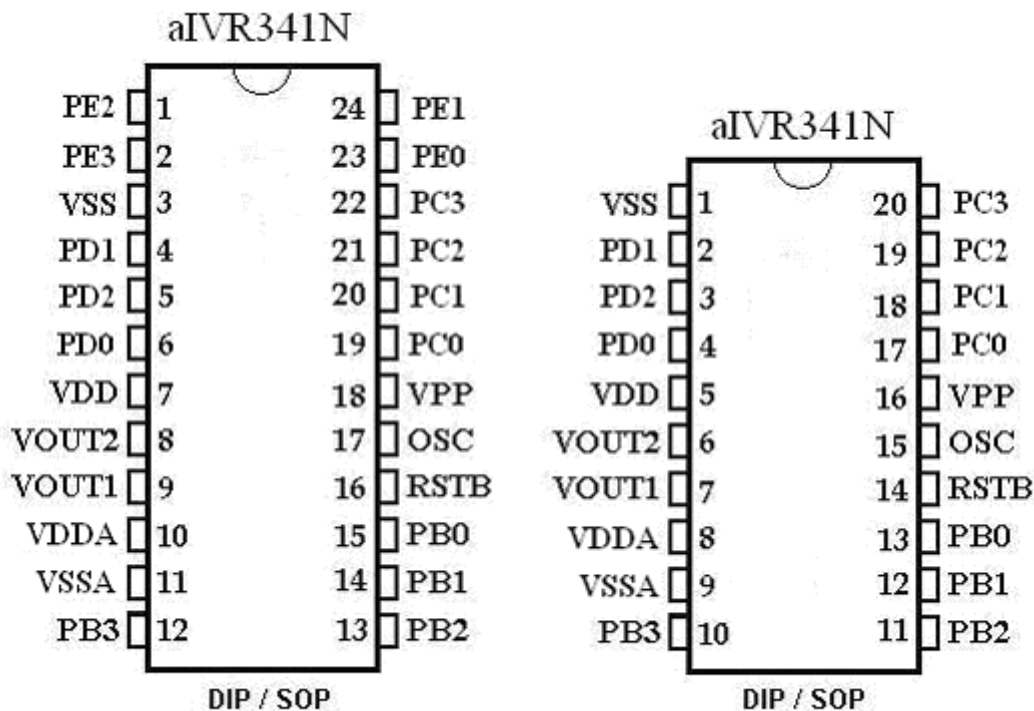
**FEATURES**

- Standard CMOS process.
- Embedded EPROM.
- Embedded 8-bit MCU.
- 341sec voice duration at 6 KHz sampling with 4-bit ADPCM compression.
- Combination of voice building blocks to extend playback duration.
- Table entries are available for voice block combinations.
- User selectable PCM or ADPCM data compress.
- Voice Group Trigger Options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
- Programmable I/Os, Timer Interrupt and Watch Dog Timer.
- Built-in oscillator with fixed  $R_{osc}$ , software control sampling frequency
- 2.4V – 3.6V single power supply and < 5uA low stand-by current.
- PWM Vout1 and Vout2 drive speaker directly.
- D/A COUT with ramp-up ramp-down option to drive speaker through an external BJT.
- Volume control.
- Maximum 9-bit resolution.
- Internal Power-up reset circuit built-in; RSTB provides external controlled reset to the chip.

**DESCRIPTION**

Aplus' aIVR341N is a 8-bit MCU based Voice chip. It is fabricated with Standard CMOS process with embedded voice storage memory. It can store 341sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 8-bit PCM is also available as user selectable option to improve sound quality. There are upto fifteen programmable I/O pins. Key trigger and Parallel CPU trigger mode can be configured according to different application requirement. User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 9-bit resolution current mode D/A output and PWM direct speaker driving minimize the number of external components. Volume control for both DAC and VOUT output is available.

**PIN CONFIGURATION**



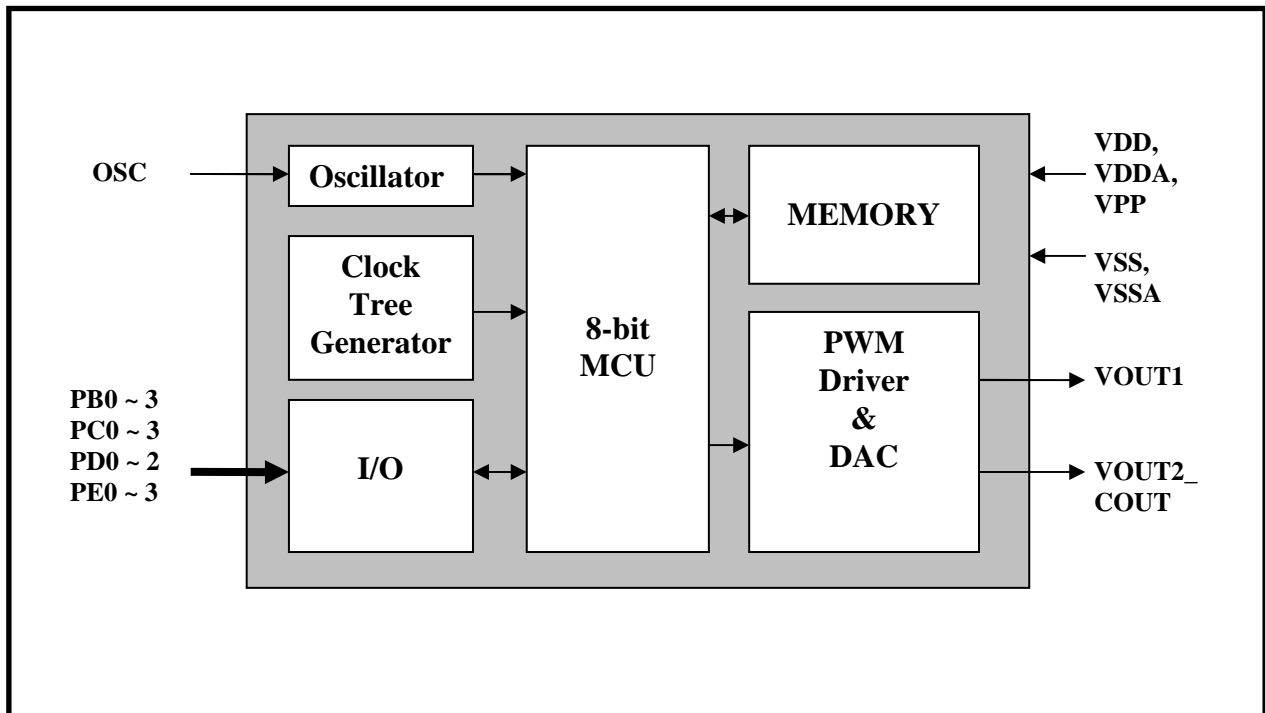
**PIN DESCRIPTIONS**

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2_COUT	PWM output or COUT DAC output select by programmable option
VSS	Power Ground
VSSA	Analog Power Ground
OSC	Oscillator input
VDD	Positive Power Supply
VDDA	Analog Positive Power Supply
VPP	Positive Power for EPROM programming, NC during voice playback
PB0~PB3	Programmable I/O port B
PC0~PC3	Programmable I/O port C
PD0~PD2	Programmable I/O port D
PE0~PE3	Programmable I/O port E
RSTB	Reset pin, Low active;

Note:

- PB, PC, PD and PE ports are software programmable I/O pins that can be set to different configurations such as pure input, input with pull-up, input with pull-down and output. The programmable I/O pins set up will take effect immediately after chip RESET is applied.
- Pins for memory programming are: VDD, VDDA, VSS, VSSA, VPP, PB0, PB1, OSC, VOUT2 and RSTB.

**BLOCK DIAGRAM**



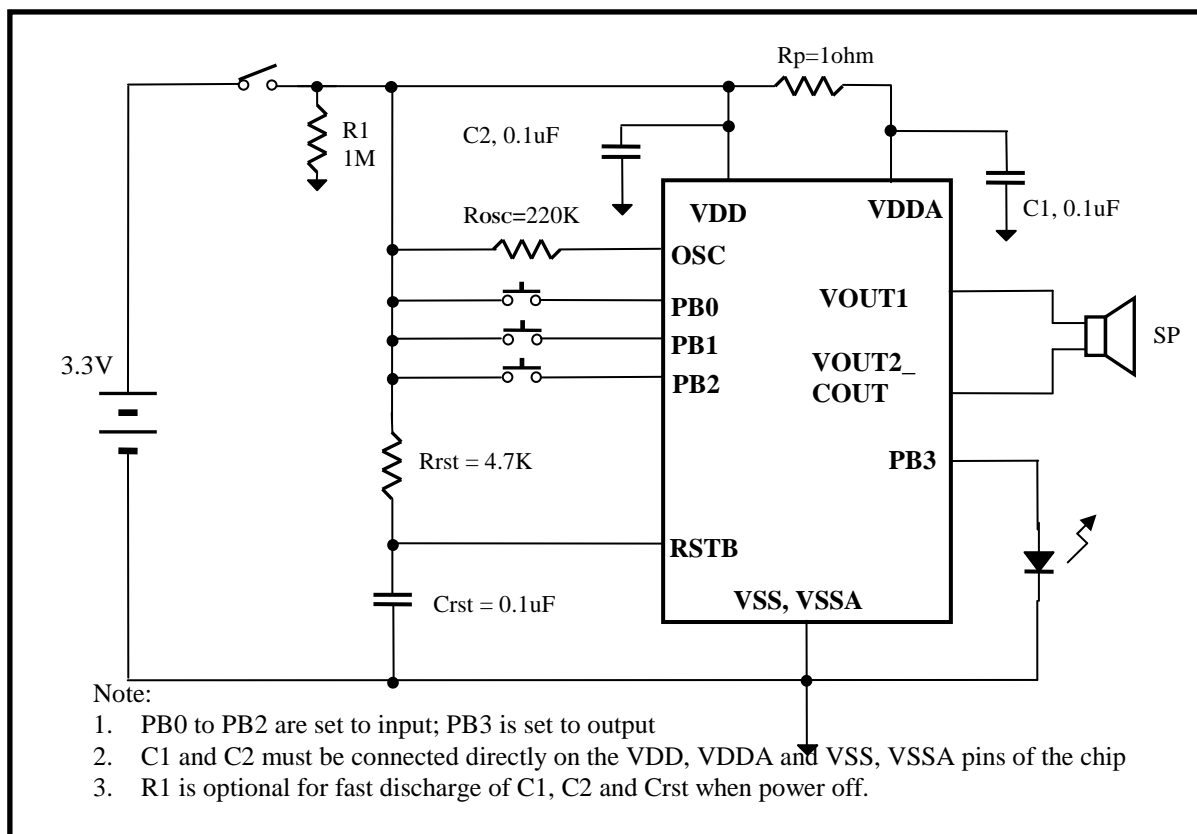
**ABSOLUTE MAXIMUM RATINGS**

Symbol	Rating	Unit
$V_{DD} - V_{SS}$	-0.5 ~ +4.0	V
$V_{IN}$	$V_{SS} - 0.3 < V_{IN} < V_{DD} + 0.3$	V
$V_{OUT}$	$V_{SS} < V_{OUT} < V_{DD}$	V
T (Operating):	0 ~ +85	°C
T (Junction)	-40 ~ +125	°C
T (Storage)	-55 ~ +125	°C

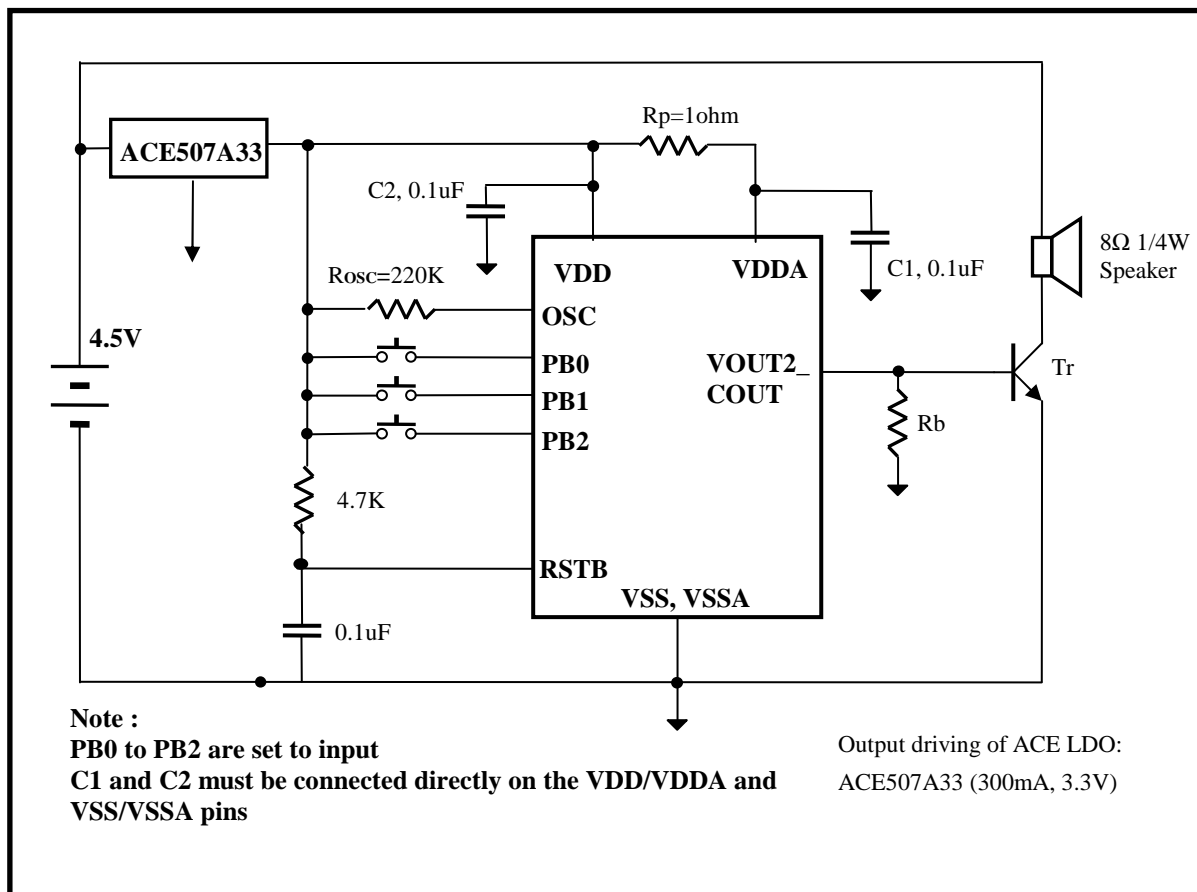
**DC CHARACTERISTICS** (  $T_A = 0$  to  $70^\circ\text{C}$ ,  $V_{DD} = 3.0\text{V}$ ,  $V_{SS} = 0\text{V}$  )

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$V_{DD}$	Operating Voltage	2.2	3.0	3.6	V	
$I_{SB}$	Standby current	—	1	5	$\mu\text{A}$	I/O properly terminated
$I_{OP}$	Operating current	—	7	—	mA	I/O properly terminated
$V_{IH}$	"H" Input Voltage	2.5	3.0	3.5	V	$V_{DD}=3.0\text{V}$
$V_{IL}$	"L" Input Voltage	-0.3	0	0.5	V	$V_{DD}=3.0\text{V}$
$I_{VOUTL\_N}$	$V_{OUT}$ low O/P Current (Normal Volume)	—	130	—	mA	$V_{out}=1.0\text{V}$
$I_{VOUTL\_H}$	$V_{OUT}$ low O/P Current (High Volume)	—	200	—	mA	$V_{out}=1.0\text{V}$
$I_{VOUTH\_N}$	$V_{OUT}$ high O/P Current (Normal Volume)	—	-130	—	mA	$V_{out}=2.0\text{V}$
$I_{VOUTH\_H}$	$V_{OUT}$ high O/P Current (High Volume)	—	-200	—	mA	$V_{out}=2.0\text{V}$
$I_{CO}$	$C_{OUT}$ O/P Current	—	-2	—	mA	Data = 80h
$I_{OH}$	O/P High Current	—	-10	—	mA	$V_{OH}=2.5\text{V}$
$I_{OL}$	O/P Low Current	—	17	—	mA	$V_{OL}=0.3\text{V}$
$R_{NVOUT}$	$V_{OUT}$ pull-down resistance	—	100K	—	$\Omega$	$V_{OUT}$ pin set to internal pull-down
$R_{NPIO}$	Programmable IO pin pull-down resistance	—	1M	—	$\Omega$	PBx, PCx, PDx set to internal pull-down
$R_{UPIO}$	Programmable IO pin pull-up resistance	3.3K	4.7K	—	$\Omega$	PBx, PCx, PDx set to internal pull-up
$\Delta F_s/F_s$	Frequency stability	-3	—	+3	%	$V_{DD} = 3\text{V} \pm 0.4\text{V}$
$\Delta F_c/F_c$	Chip to chip Frequency Variation	-5	—	+5	%	Also apply to lot to lot variation

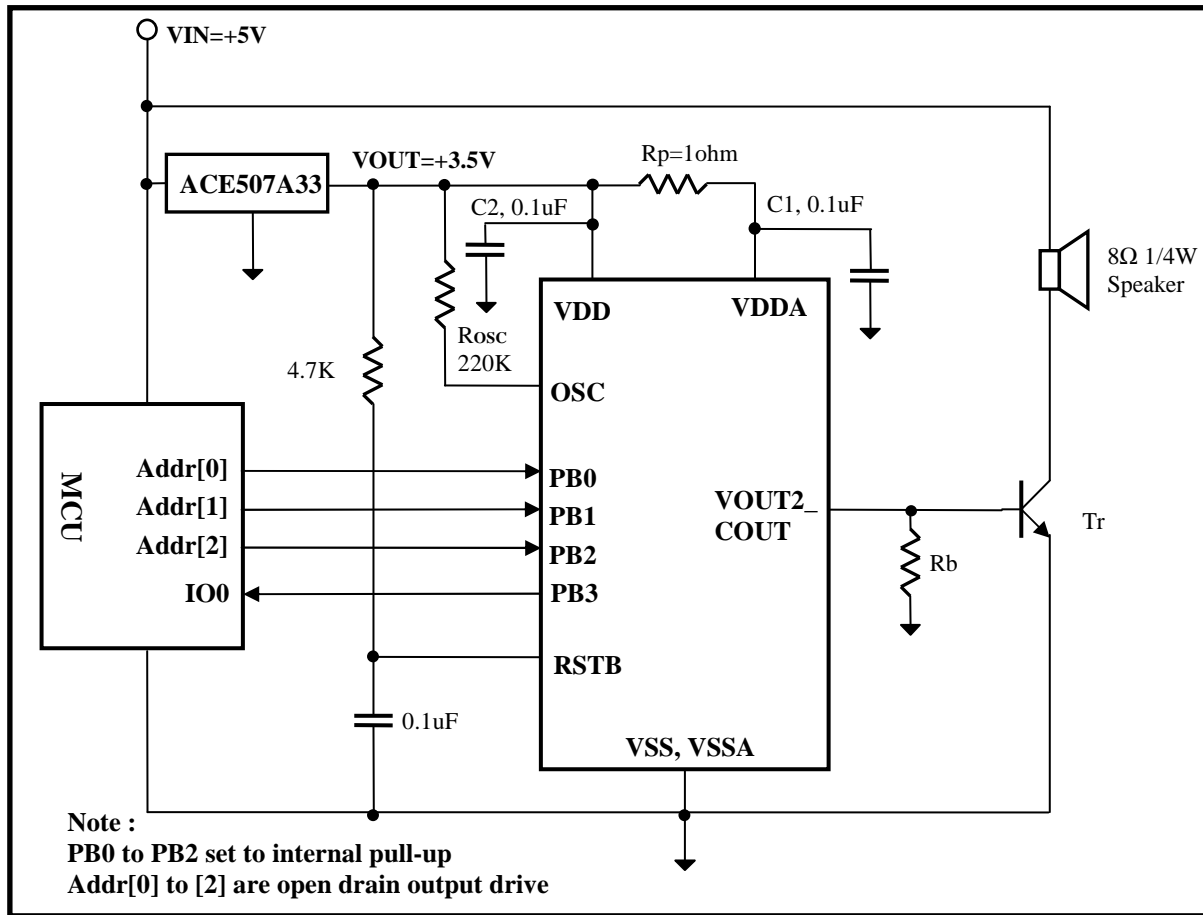
**TYPICAL APPLICATIONS**



Using 3.3V Battery Direct Drive Speaker



Using 4.5V Battery with COUT speaker drive

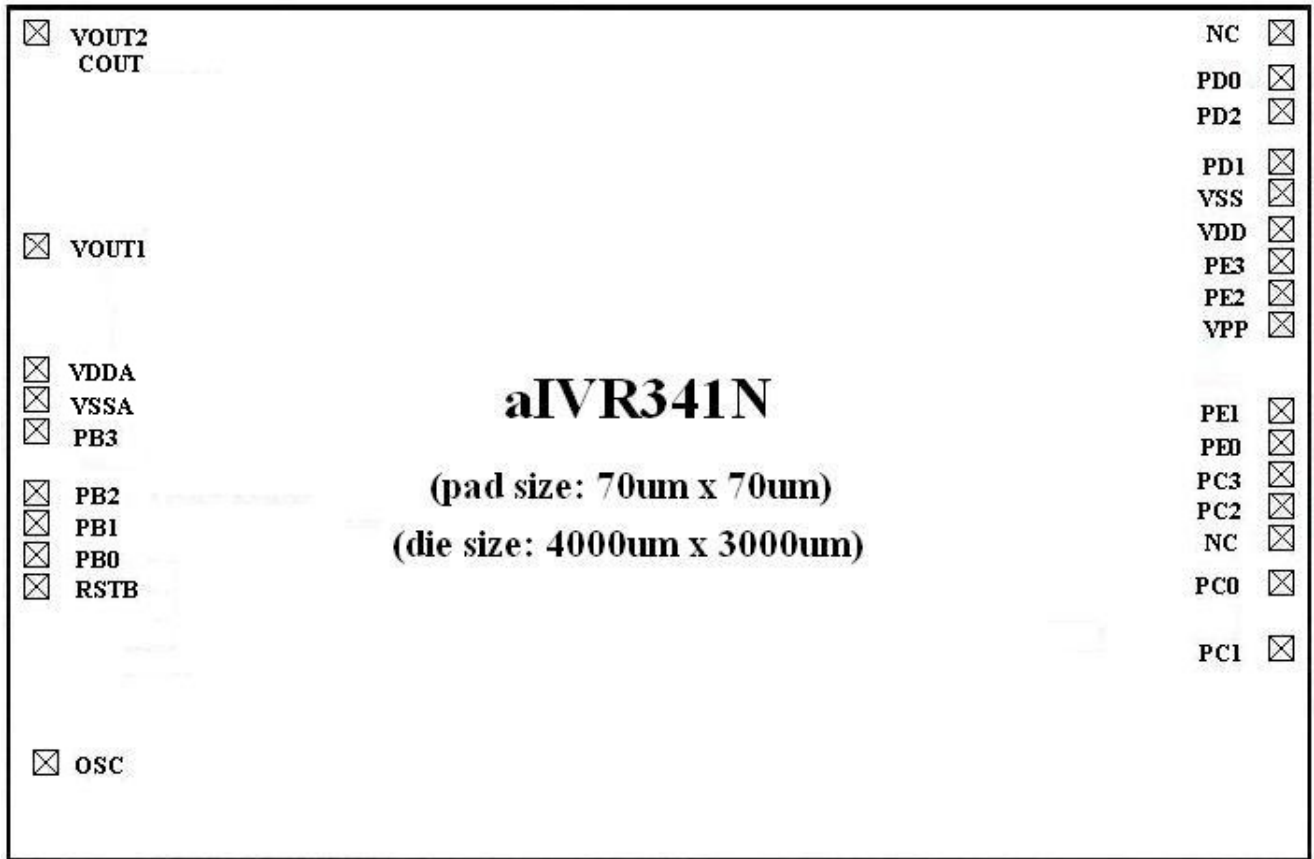


5V CPU Control with COUT

Note for COUT speaker drive:

1. C1 and C2 must be connected as close to the VDD/VDDA and VSS/VSSA pins as possible.
2. Rb is base resistor from 120 Ohm to 390 Ohm depends on value of VDD and transistor gain.
3. Tr is an NPN transistor with beta larger than 150, e.g. 8050D.
4. Rosc = 220K Ohm with Vdd=3.0V can support sampling rate up to 14KHz.

**Bonding Diagrams**

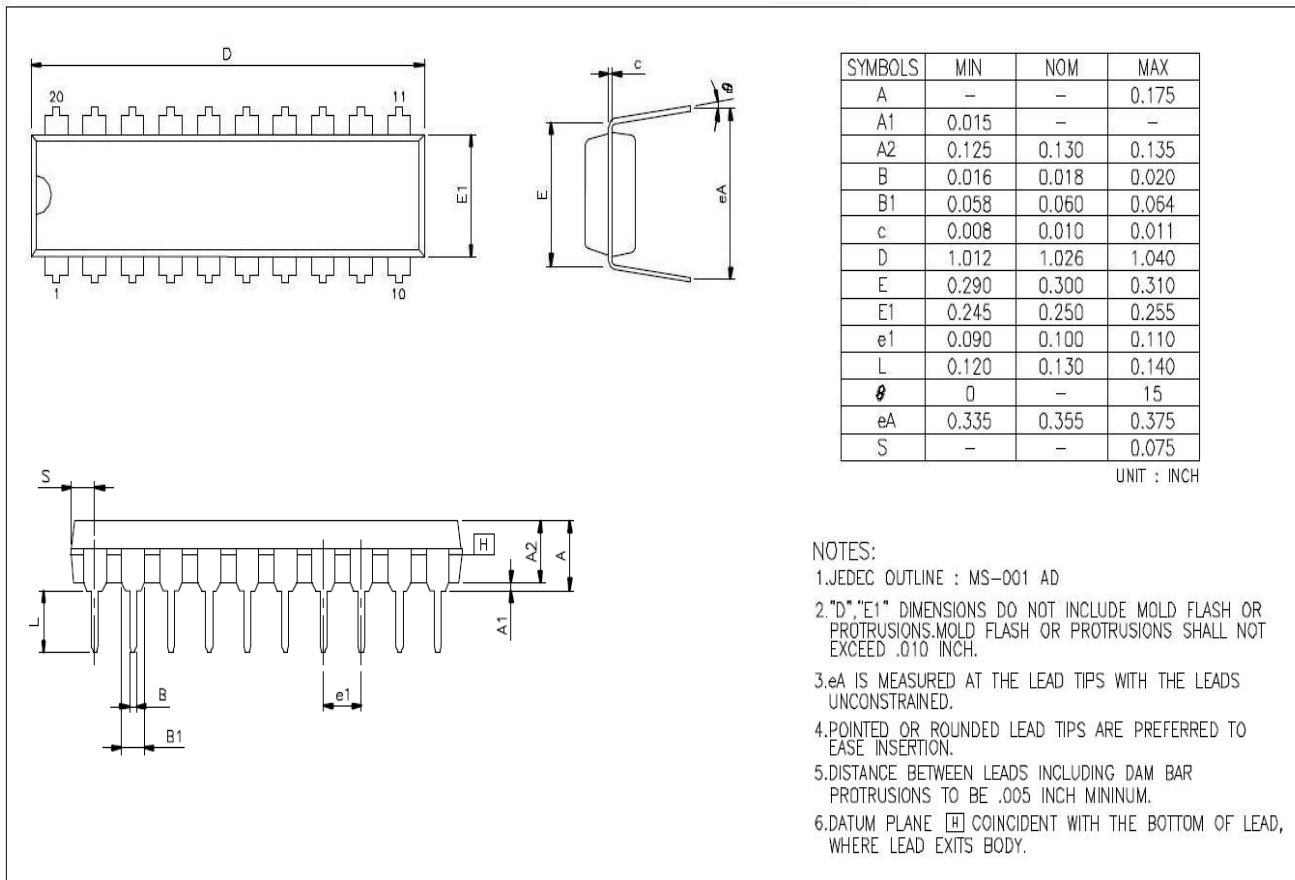


Note: Substrate must be connected to VSS

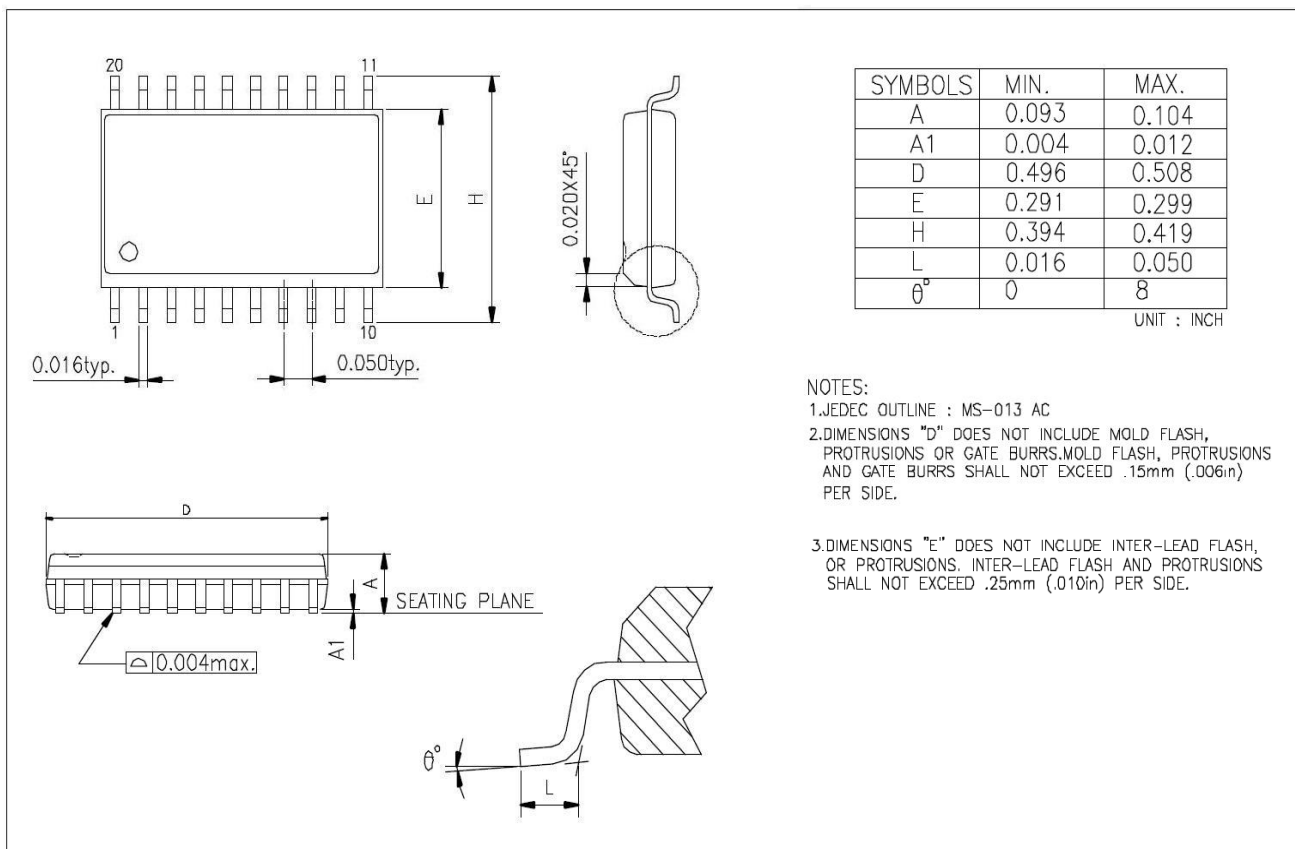


## Packages Dimension Outlines

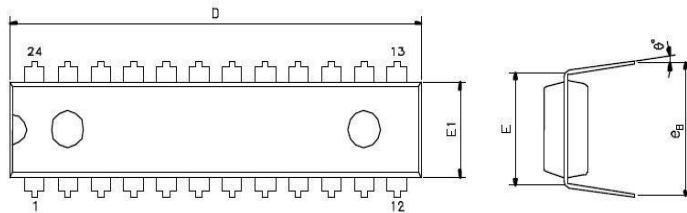
### 20PIN 300mil DIP Package



### 20PIN 300mil SOP Package

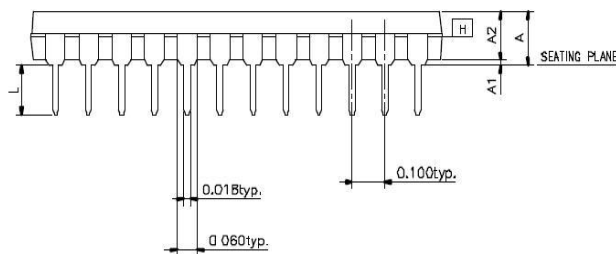


## 24PIN 300mil DIP Package



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E	0.300 BSC.		
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
e <sub>B</sub>	0.335	0.355	0.375
θ°	0	7	15

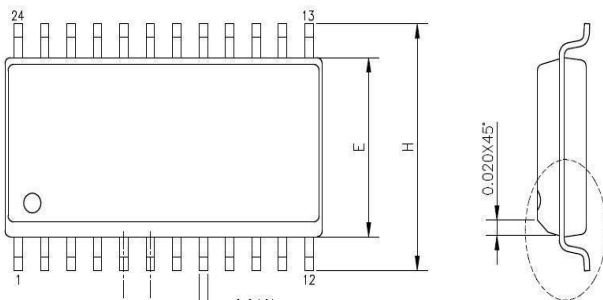
UNIT : INCH



### NOTES:

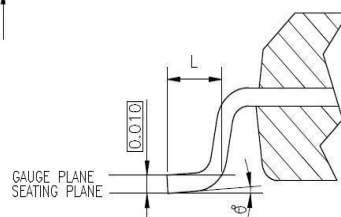
1. JEDEC OUTLINE : MS-001 AF
2. "D" "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. e<sub>B</sub> IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

## 24PIN 300mil SOP Package



SYMBOLS	MIN.	NOM	MAX.
A	—	—	0.104
Δ A1	0.004	—	—
Δ D	0.612	0.618	0.624
Δ E	0.292	0.296	0.299
Δ H	0.405	0.412	0.419
Δ L	0.021	0.031	0.041
θ°	0	4	8

UNIT : INCH



### NOTES:

1. JEDEC OUTLINE : MO-119 AA
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .25mm (.010in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.