Data Sheet

aIVR3K10 – 10 sec
aIVR3K21 – 21 sec
aIVR3K42 – 42 sec

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FEATURES

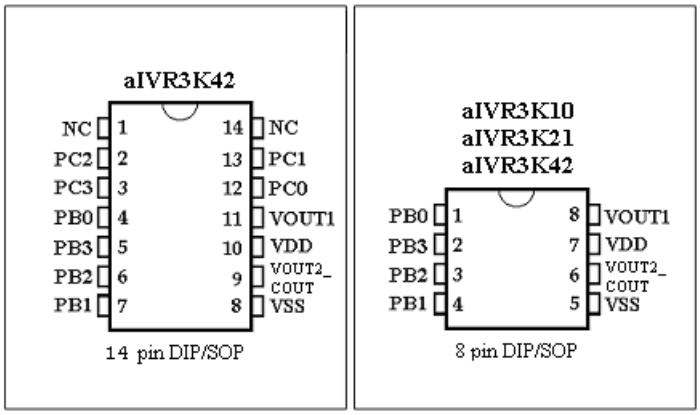
- Embedded OTP memory and 8-bit MCU
- Built-in oscillator and Power On Reset circuits to reduce external components.
- 2.2V – 3.6V single power supply and < 5uA low stand-by current.
- 10, 21 and 42sec voice duration at 6 KHz sampling with 4-bit ADPCM compression.
- Combination of voice building blocks to extend playback duration.
- Table entries are available for voice block combinations.
- User selectable PCM or ADPCM data compress.
- Voice Group Trigger Options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
- Programmable I/Os, Timer Interrupt and Watch Dog Timer.
- PWM Vout1 and Vout2 drive speaker directly with 2 levels volume control.
- D/A COUT with ramp-up ramp-down option to drive speaker through an external BJT.
- Windows based development system and USB programmer support.

DESCRIPTION

Aplus' aIVR3K is a 8-bit CPU based Voice chip series. It is fabricated with Standard CMOS process with embedded voice storage OTP memory. It can store from 10 to 42sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 8-bit PCM is also available as user selectable option to improve sound quality. Depending on IC body, there are up to eight programmable I/O pins. Key trigger and Parallel CPU trigger mode can be configured according to different application requirements. User selectable triggering and output signal options provide maximum flexibility to various applications. Fully integrated system oscillator, power-on reset, 8-bit current mode D/A output and PWM direct speaker driving output to minimize external components count. Two level volume control for PWM direct speaker driving output.

Part Number	Duration	Programmable IO
aIVR3K10	10 sec	4
aIVR3K21	21 sec	4
aIVR3K42	42 sec	8

PIN CONFIGURATIONS



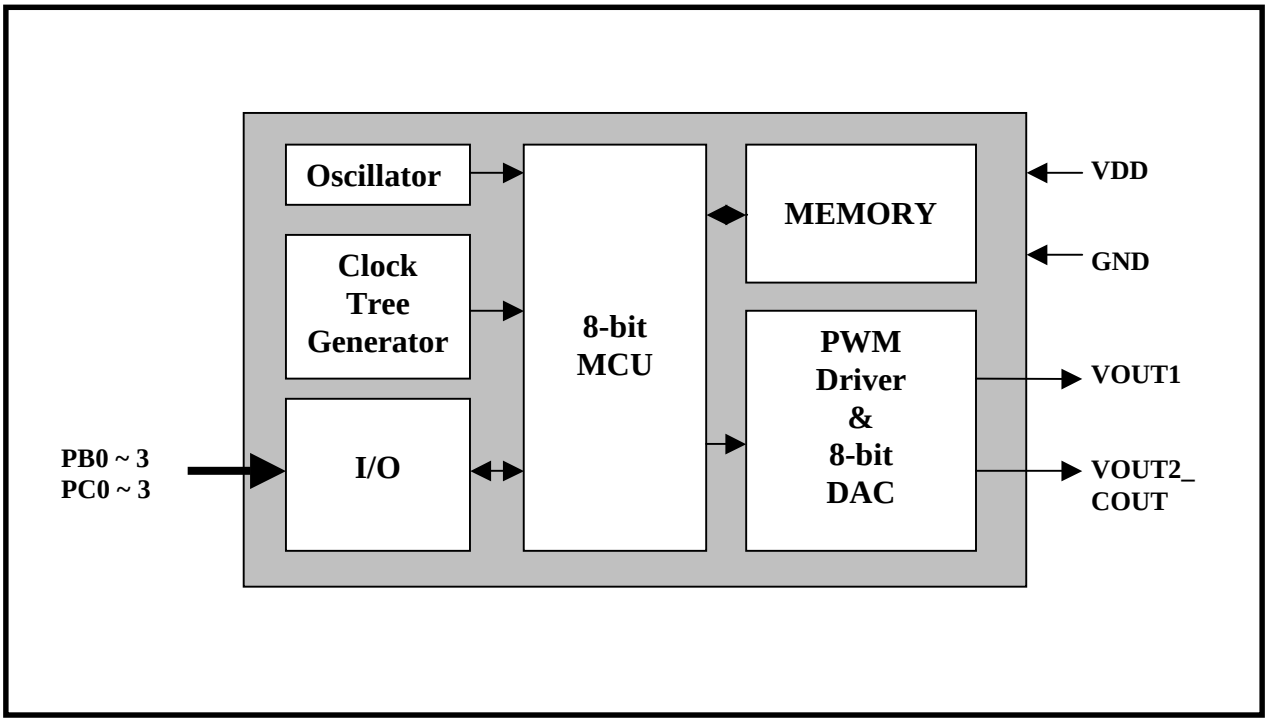
Note: 14 pins and 8 pins packages are available for aIVR3K42

PIN DESCRIPTIONS

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2_ COUT	PWM output or COUT DAC output select by programmable option (COUT is not available on aIVR3K10)
VSS	Power Ground
VDD	Positive Power Supply
PBm	Programmable I/O pins (m: 0 to 2)
PB3	Input pin with programmable pull-down
PCn	Programmable I/O pins (n: 0 to 3 for aIVR3K42 only)

Note:
1. Pins required for OTP program include PB0 to PB3, VOUT1, VOUT2_COUT, VDD and VSS.
2. PBm and PCn are software programmable I/O pins that can be set to different configurations such as pure input, input with pull-up, input with pull-down and output. The programmable I/O pins set up will take effect immediately after power-on reset.
3. 8-pin and 14-pin packages are available for aIVR3K42.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +4.0	V
V_{IN}	V_{SS} - 0.3<V_{IN}<V_{DD} + 0.3	V
V_{OUT}	V_{SS} <V_{OUT}<V_{DD}	V
T (Operating):	-40 ~ +85	℃
T (Junction)	-40 ~ +125	℃
T (Storage)	-55 ~ +125	℃

DC CHARACTERISTICS

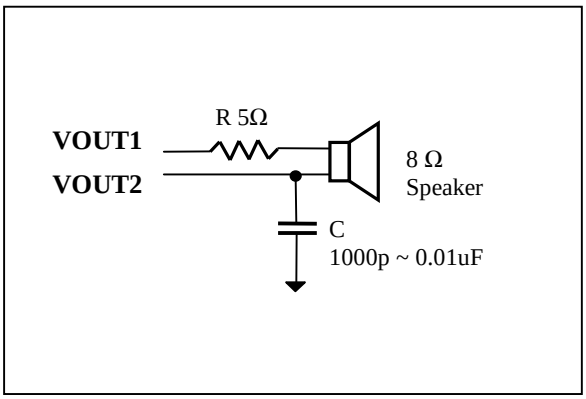
➢ T_A = 0 to 70℃, V_{DD} = 3.0V, V_{SS} = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	2.2	3.0	3.6	V	
I_{SB}	Standby current	—	1	5	μA	I/O properly terminated
I_{OP}	Operating current	—	4	15	mA	I/O properly terminated
V_{IH}	"H" Input Voltage	2.5	3.0	3.5	V	V_{DD}=3.0V
V_{IL}	"L" Input Voltage	-0.3	0	0.5	V	V_{DD}=3.0V
I_{VOUTL}	V_{OUT} low O/P Current	—	130	—	mA	Vout=1.0V (Note 1)
I_{VOUTH}	V_{OUT} high O/P Current	—	-130	—	mA	Vout=2.0V (Note 1)
I_{CO}	C_{OUT} O/P Current	—	-2	—	mA	Data = 80h
I_{OH}	O/P High Current	—	-5	—	mA	V_{OH}=2.5V
I_{OL}	O/P Low Current	—	20	—	mA	V_{OL}=0.3V
RN_{VOUT}	VOUT pull-down resistance	—	100K	—	**Ω**	VOUT pin set to internal pull-down
RN_{PB3}	Programmable I/P pin pull-down resistance	—	1M	—	**Ω**	PB3 is set to internal pull-down
RN_{PIO}	Programmable IO pin pull-down resistance	—	1M	—	**Ω**	PBm, PCn, are set to internal pull-down
RU_{PIO}	Programmable IO pin pull-up resistance	3.3K	4.7K	—	**Ω**	PBm, PCn, set to internal pull-up
ΔFs/Fs	Frequency stability	-3	—	+3	%	V_{DD} = 3V +/- 0.4V
ΔFc/Fc	Chip to chip Frequency Variation	-5	—	+5	%	Also apply to lot to lot variation

Note:
1. The current value is for normal volume. It is double for high volume. The VOUT volume is selected by using the development system software provided.
2. Where PBm stands for programmable I/O pins PB0, PB1 and PB2; PCn stands for programmable I/O pins PC0, PC1, PC2 and PC3.

PWM DIRECT DRIVE FOR 8 OHM SPEAKER

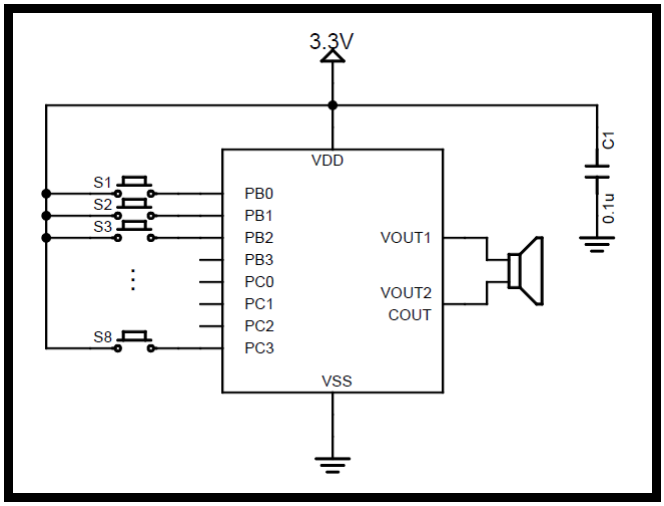
When PWM output is selected, the VOUT1 and VOUT2 pins can direct drive a speaker to provide sound playback. The VOUT1 and VOUT2 are powerful driving pins. To reduce the digital noise from affecting the VDD and VSS stability, the following filter connection should be applied to the VOUT1 and VOUT2 pins. The exact filter used is dependent on the sound type and sound volume.



Note: No additional filter connection is needed for 16Ω speaker.

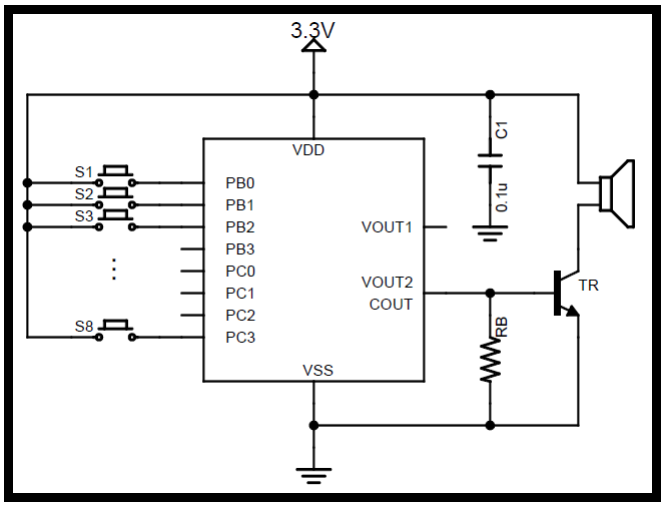
TYPICAL APPLICATIONS

- Key single mode with speaker direct drive (PWM)



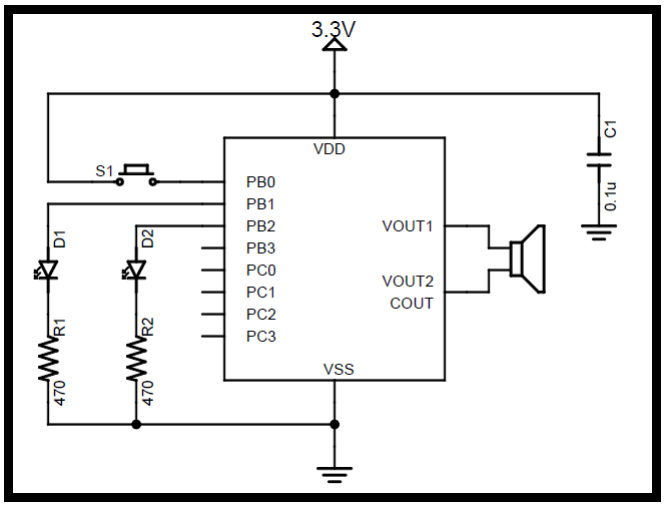
  - C1 must be connected directly on the VDD and VSS pins of the chip

- Key single mode with COUT speaker drive (DAC)



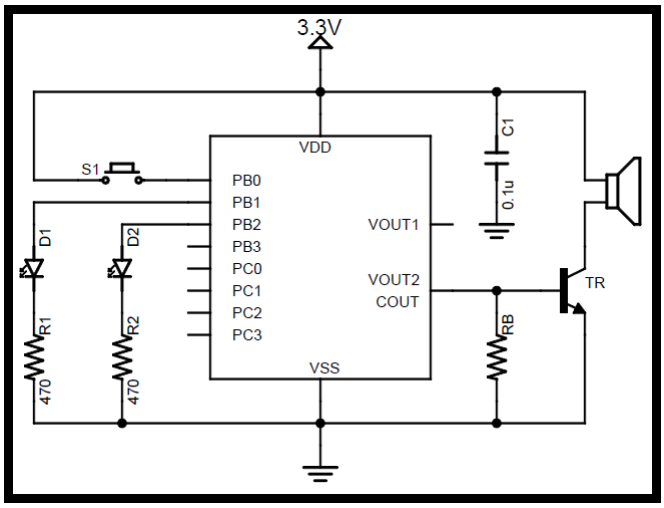
  - C1 must be connected directly on the VDD and VSS pins of the chip
  - Rb is base resistor from 120 Ohm to 390 Ohm depends on value of VDD and transistor gain.
  - Tr is an NPN transistor with beta larger than 150, e.g. 8050D.

- Key sequence mode with speaker direct drive (PWM)



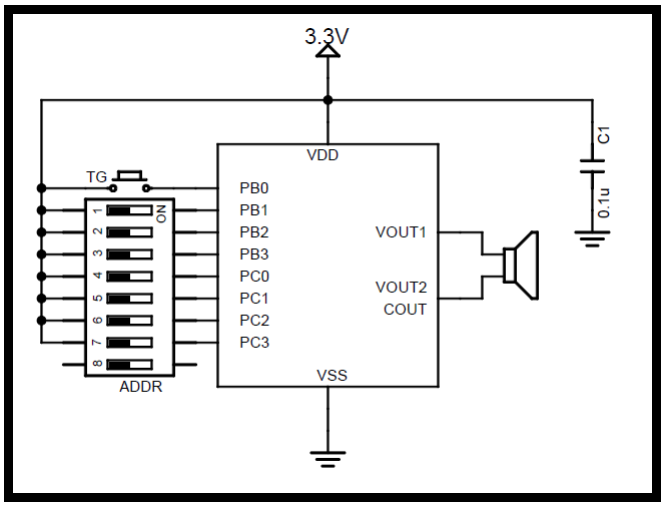
  - C1 must be connected directly on the VDD and VSS pins of the chip

- Key sequence mode with COUT speaker drive (DAC)



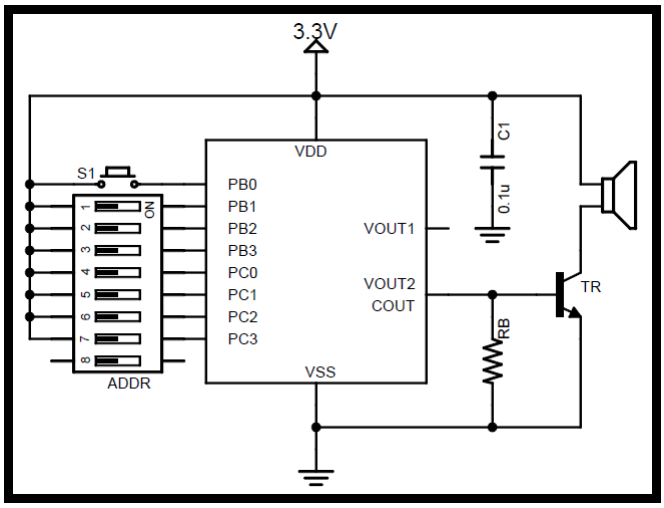
  - C1 must be connected directly on the VDD and VSS pins of the chip
  - Rb is base resistor from 120 Ohm to 390 Ohm depends on value of VDD and transistor gain.
  - Tr is an NPN transistor with beta larger than 150, e.g. 8050D.

- CPU address mode with speaker direct drive (PWM)



  - C1 must be connected directly on the VDD and VSS pins of the chip

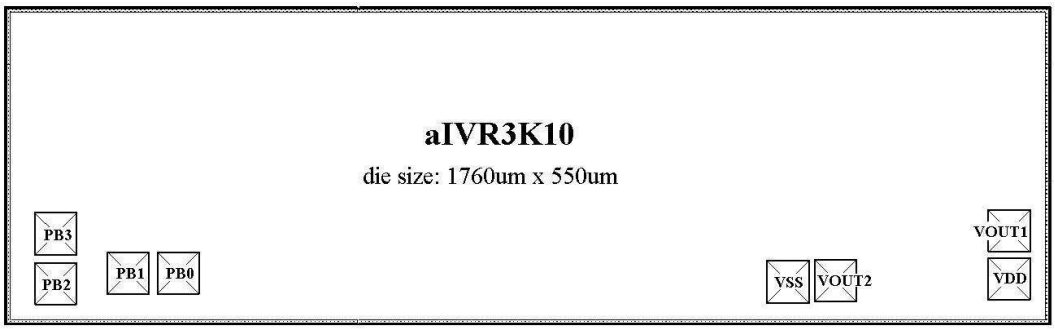
- CPU address mode with COUT speaker drive (DAC)

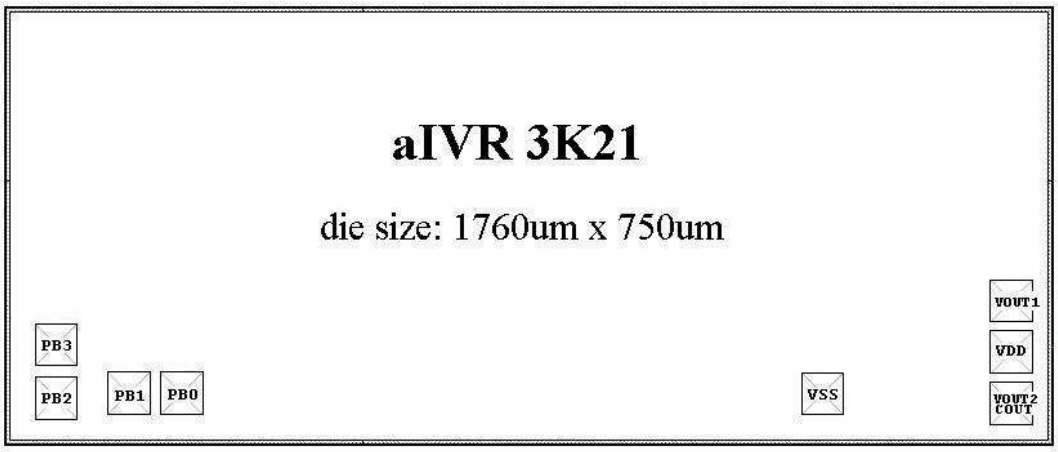


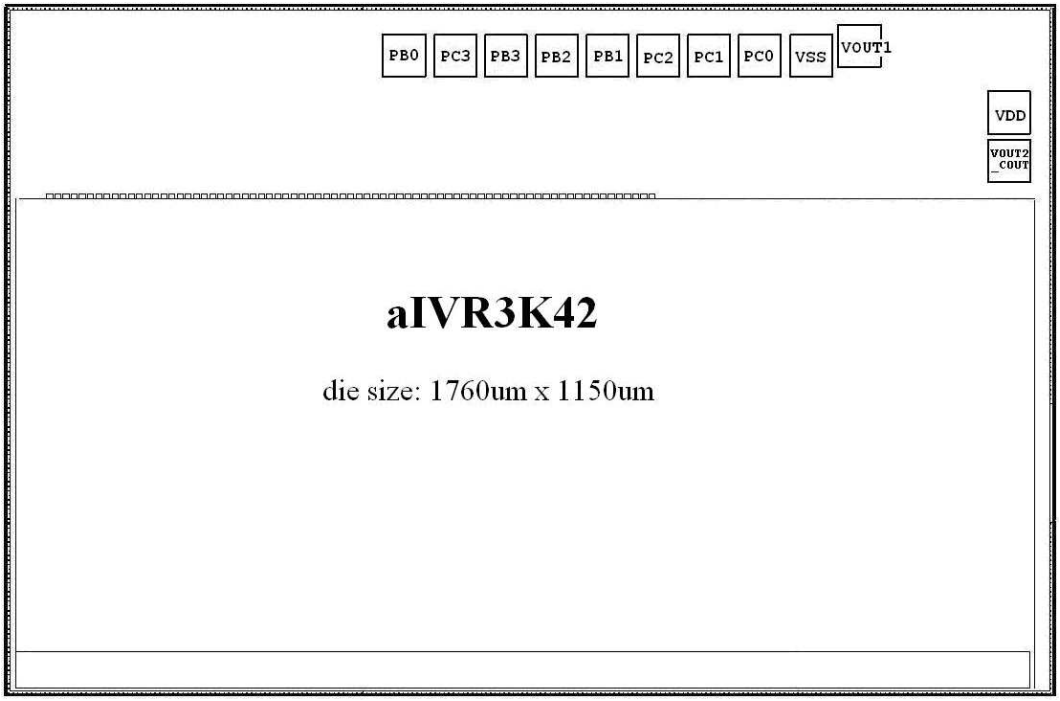
  - C1 must be connected directly on the VDD and VSS pins of the chip
  - Rb is base resistor from 120 Ohm to 390 Ohm depends on value of VDD and transistor gain.
  - Tr is an NPN transistor with beta larger than 150, e.g. 8050D.

BONDING DIAGRAMS

- Pad opening 70x70um.
- Substrate should be connected to VSS.







HISTORY

2012/03/27 Modify section: TYPICAL APPLICATIONS.
2010/01/26 The 1St release version.