apm1689 WiFi 802.11 b/g/n Single System Module

DESCRIPTION

With a small form factor of 18×18×2.2mm (max.), the apm1689 is a full-featured WiFi 802.11b/g/n WiFi single system module that includes support for high linear output power, IEEE 802.11i security, IEEE 802.11e QoS,. By providing SDIO (1-bit, 4-bit) host interface combined with support for Linux operation systems, the apm1689 enables rapid integration of WiFi technology into a variety of host devices. The pre-tested module eliminates the need to create custom WLAN designs, resulting in greatly reduced development risk, costs and time-to-market.

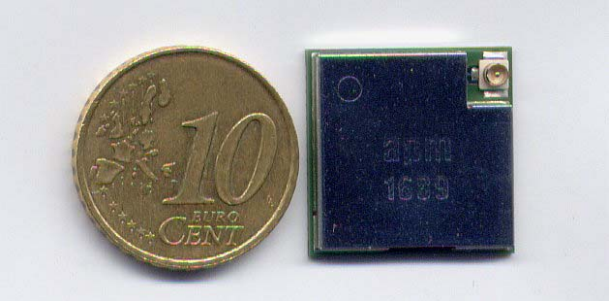
GENERAL FEATURES

- Small footprint: 18×18×2.2 mm (max.)
- IEEE 802.11b/g/n compliant
- Frequency band: 2.4 to 2.472GHz (1 to 13 channels) and Channel 14 at 11b only.
- 11b data rates: 1, 2, 5.5, 11 Mbps
- 11g data rates: 6, 9, 12, 18, 24, 36, 48, and 54 Mbps
- 11n data rates: CS0-7, 400/800ns 72.2, 65, 58.5, 57.8, 52, 43.3, 39, 28.9, 26, 21.7, 19.5, 14.4, 13, 7.2, 6.5Mbps
- Modulation: DSSS (CCK, DQPSK, DBPSK) and OFDM (BPSK, QPSK, 16QAM, 64QAM)
- Host interface:
  - SDIO: SDIO 1-bit, SDIO 4-bit, SDIO SPI
- Support for IEEE 802.11e QoS
- Support for IEEE 802.11i advanced security
- Support soft AP and Wifi direct
- GSM/GPRS/DCS/PCS/WCDMA/GPS radio non-interference
- EEPROM, LNA, and full RF front end integrated
- Embedded OS supported
- RoHS complaint

APPLICATIONS

- WiFi plug-in modules for non-wireless systems
- Smartphone / PDA / PDA phone / WiFi phone / DSC / DVC with WiFi connectivity
- Printer Server / Multifunctional peripheral with WiFi connectivity
- Support Bluetooth co-existence

APPEARANCE



REVISION HISTORY

Date	Release	Author	Description
12-Feb-14	0.1	Bookmid	Initial release
12-May-16	0.2	Tu Yen Chang	Modified the block diagram, deleted Windows CE.
12-June-19	0.3	Tu Yen Chang	Modified the Pin Defined. (Pin9 and Pin13)
13-Jan-31	1.0	pol	Modified the pin assignment in section 1-3-1(Pin28) Modified operating temperature in section 1-6-2
13-Mar-14	1.1	pol	Modified CSPI Pins in section 1-4-2 Modified Debug SPI Pins in section 1-4-3

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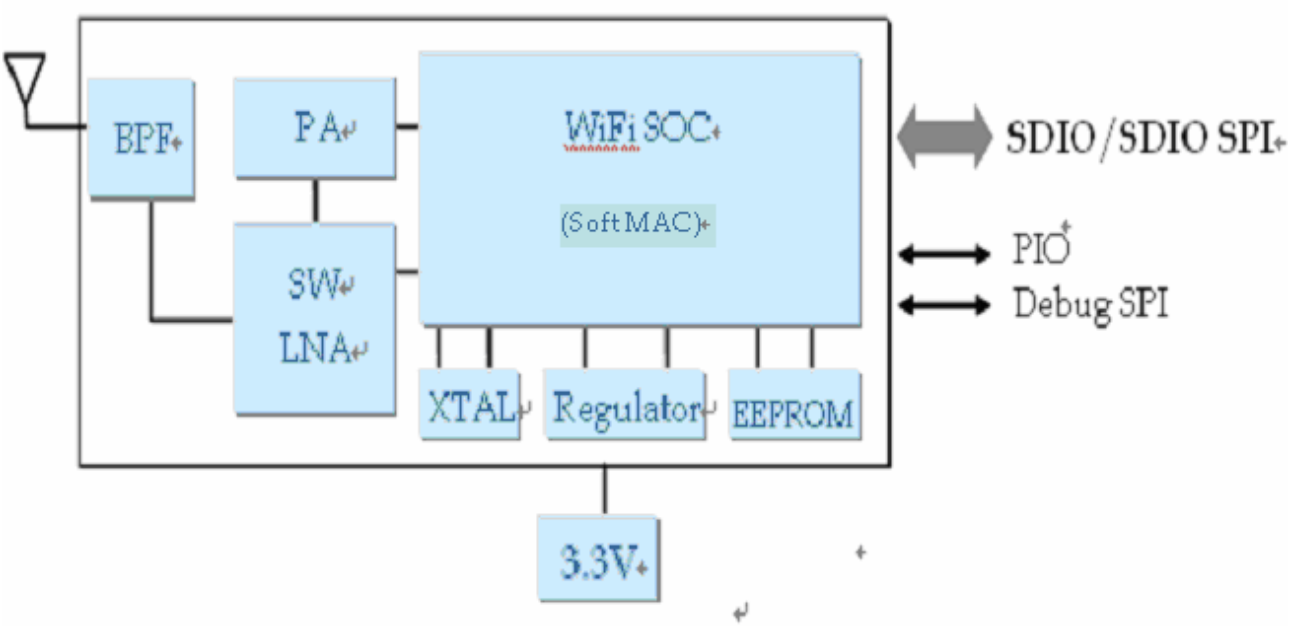
1 HARDWARE SPECIFICATION

1-1 General Specification

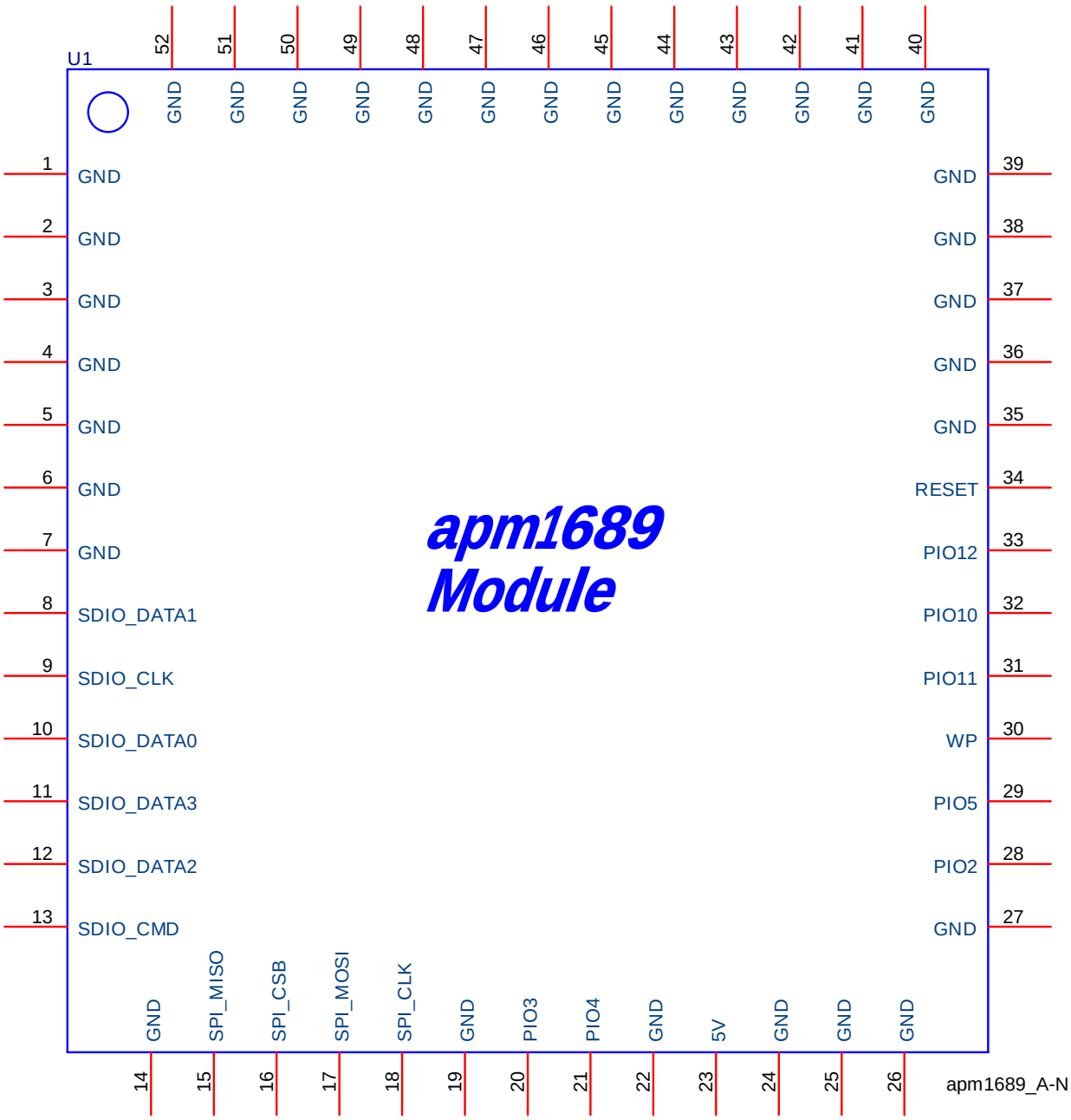
WiFi part:	
Network Standard	IEEE 802.11b/g/n Compliant
Host Interface	SDIO v2.0: SDIO 1-bit, SDIO 4-bit, SDIO SPI
Frequency Band	Channel 1 to 13 (Channel 14 at 11b only)
Data Transfer Mode	OFDM & DSSS
Modulation	64QAM (MCS0-7, 400/800ns 72.2, 65, 58.5, 57.8, 52, 43.3, 39, 28.9, 26, 21.7, 19.5, 14.4, 13, 7.2, 6.5Mbps), 64QAM (54, 48Mbps), 16QAM (36, 24Mbps), QPSK (18, 12Mbps), BPSK (9, 6Mbps); CCK (11, 5.5 Mbps), DQPSK (2 Mbps), DBPSK (1Mbps). STBC reception for MCS0-7
Access Method	Ad hoc mode, Infrastructure mode, Soft Access point (Hot spot), Wifi direct
Media Access Protocol	CSMA/ CA (Carrier Sense Multiple Access with Collision Avoidance)
Antenna	External single antenna support. The output impedance is 50Ω.

1-2 Block Diagram



1-3 Pinout

1-3-1 Pin Assignment



1-3-2 Pin Description

* I/O: Digital Input/Output, I: Digital Input, O: Digital Output, A: Analog, PU: Pull-up, PD: Pull-down

#	Name	I/O	Pin Status on Reset	Supply Domain	Description
1	GND	GND	-	-	Ground
2	GND	GND	-	-	Ground
3	GND	GND	-	-	Ground
4	GND	GND	-	-	Ground
5	GND	GND	-	-	Ground
6	GND	GND	-	-	Ground
7	GND	GND	-	-	Ground
8	WL_SD_DAT[1]	I/O	PU	WL_VSDIO	SDIO 4-bit mode: Data line [bit 1] or interrupt SDIO 1-bit mode: Interrupt CSPI mode : Interrupt
9	WL_SD_CLK	I	PU	WL_VSDIO	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock CSPI mode : Clock
10	WL_SD_DAT[0]	I/O	PU	WL_VSDIO	LSB data bit for SDIO interface. SDIO 4-bit mode: Data line [bit 0] SDIO 1-bit mode: Data line CSPI mode: Data output
11	WL_SD_DAT[3]	I/O	PU	WL_VSDIO	SDIO 4-bit mode: Data line [bit 3] SDIO 1-bit mode: Reserved CSPI mode: Card Select
12	WL_SD_DAT[2]	I/O	PU	WL_VSDIO	SDIO 4-bit mode: Data line [bit 2] or Read wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPI mode: Reserved
13	WL_SD_CMD	I	PU	WL_VSDIO	SDIO 4-bit mode: Command/Response SDIO 1-bit mode: Command/Response CSPI mode: Data input
14	GND	GND	-	-	Ground
15	WL_SPI_MISO	O	PD	WL_VDD_PADS_0_7	Debug SPI data output
16	WL_SPI_CSn	I	PU	WL_VDD_PADS_0_7	Debug SPI chip select, active low
17	WL_SPI_MOSI	I	PD	WL_VDD_PADS_0_7	Debug SPI data input
18	WL_SPI_CLK	I	PD	WL_VDD_PADS_0_7	Debug SPI clock

#	Name	I/O	Pin Status on Reset	Supply Domain	Description
19	GND	GND	-	-	Ground
20	WL_PIO[3]	I/O	PD	WL_3V3	Programmable input/output
21	WL_PIO[4]	I/O	PD	WL_3V3	Programmable input/output
22	GND	GND	-	-	Ground
23	WL_3V3	Power	-	-	Positive supply for AIO[0]-AIO[3] , PIO[8]-PIO[15], and FEM
24	GND	GND	-	-	Ground
25	GND	GND	-	-	Ground
26	GND	GND	-	-	Ground
27	GND	GND	-	-	Ground
28	WL_PIO[2]	I/O	PD	WL_3V3	Programmable input/output
29	WL_PIO[5]	I/O	PD	WL_3V3	Programmable input/output
30	WL_WP	I		-	Write protection for internal EEPROM
31	WL_PIO[10]	I/O	PD	WL_3V3	Programmable input/output
32	WL_PIO[11]	I/O	PD	WL_3V3	Programmable input/output
33	WL_PIO[12]	I/O	PD	WL_3V3	Programmable input/output
34	WL_RESETn	I	PU	WL_RESETB	Reset, active low
35	GND	GND	-	-	Ground
36	GND	GND	-	-	Ground
37	GND	GND	-	-	Ground
38	GND	GND	-	-	Ground
39	GND	GND	-	-	Ground
40	GND	GND	-	-	Ground
41	GND	GND	-	-	Ground
42	GND	GND	-	-	Ground
43	GND	GND	-	-	Ground
44	GND	GND	-	-	Ground
45	GND	GND	-	-	Ground
46	GND	GND	-	-	Ground
47	GND	GND	-	-	Ground
48	GND	GND	-	-	Ground
49	GND	GND	-	-	Ground
50	GND	GND	-	-	Ground

#	Name	I/O	Pin Status on Reset	Supply Domain	Description
51	GND	GND	-	-	Ground
52	GND	GND	-	-	Ground

All the big pads on the bottom of the module should be tied to ground.

1-4 WiFi Pins

1-4-1 SDIO Pins

apm1689 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access apm1689.

The SDIO bus has weak internal pull up resistors on chip.

SDIO Bus Name	Pin #	Pin Name	Description
DAT3	11	WL_SD_DAT[3]	SDIO 4-bit mode: CD- Data line [bit 3] or card detect SDIO 1-bit mode: CD- Card detect
DAT2	12	WL_SD_DAT[2]	SDIO 4-bit mode: RW- Data line [bit 2] or read wait(optional) SDIO 1-bit mode: RW- Read Wait (optional)
DAT1	8	WL_SD_DAT[1]	SDIO 4-bit mode: IRQ#- Data line [bit 1] or interrupt (optional) SDIO 1-bit mode: IRQ#- Interrupt
DAT0	10	WL_SD_DAT[0]	LSB data bit for SDIO interface. SDIO 4-bit mode: Data line [bit 0] SDIO 1-bit mode: Data line
CMD	13	WL_SD_CMD	SDIO 4-bit mode: Command/Response SDIO 1-bit mode: Command/Response
CLK	9	WL_SD_CLK	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock

1-4-2 CSPI Pins

While SDIO port is not available on host platform, apm1689 supports a SD-SPI device interface that connects to Synchronous Serial Port (SSP) pins on Marvell PXA platform or the similar interfaces on other host platforms.

The SD-SPI bus has weak internal pull up resistors on chip.

SD-SPI Name	Pin #	Pin Name	Description
CS	11	WL_SD_DAT[3]	Card Select
IRQ	8	WL_SD_DAT[1]	Interrupt
DO	10	WL_SD_DAT[0]	Data output
DI	13	WL_SD_CMD	Data input
SCLK	9	WL_SD_CLK	Clock

1-4-3 Debug SPI Pins

apm1689 has a SPI interface for test and debugging purposes. The lab tools, such as UniTest and UniPSUtil, can communicate with apm1689 WiFi part using the SPI protocol over a connection to an LPT port.

Debug SPI Name	Pin #	Pin Name	Description
MISO	15	WL_SPI_MISO	Debug SPI data output
MOSI	17	WL_SPI_MOSI	Debug SPI data input
CLK	18	WL_SPI_CLK	Debug SPI clock
CSn	16	WL_SPI_CSn	Debug SPI chip select, active low

1-4-4 PIO Pins

The PIO pins are used to implement user defined input and output signals to and from the module such as external interrupts and other user-defined I/Os. Each PIO can be independently controlled.

- WL_PIO[12]: Host wakeup.
- WL_PIO[2:3:4:5]: BT Co-existence
- Other PIOs: Reserved

1-4-5 WP Pin

WL_WP is write protection for internal EEPROM. The internal EEPROM stores calibration table, MAC address, etc. for WiFi part. When the pin is pulled high, it protects the EEPROM content. If tied to VSS, normal memory read/write operation is enabled.

The WiFi firmware does not incorporate any support for writing to the EEPROM during normal operation. This significantly reduces the risk of spurious writes corrupting the contents of the EEPROM, and means it is not possible to repair any damage that may occur. Hence, it is suggested that keep the pin, WL_WP, permanently pulled high to minimize the risk of data corruption.

1-5 External Voltage Source

The external supply rails to apm1689 should have less than 10mV rms noise levels between 0 to 10 MHz. Single tone frequencies are also to be avoided. Transient response of external regulators used should be <= 5us.

Supply voltage range

3.3V	3.3V +/-5% (ripple Vpp<10mV rms)

1-5-1 WiFi Reset

WL_RESETn is an active low reset input that is internally filtered using the internal low frequency clock oscillator to avoid spurious resets. A reset occurs after the signal has been asserted for between 250 and 375us. This pin may be tied to WL_VDD_PADS_0_7 if unused; otherwise it should be asserted for at least 1ms to force a reset.

The power supply supervisor monitors WL_VDD_CORE (internal module voltage) to trigger a power-on-reset. This occurs when the supply falls below 1.05V (typical) in normal operation or 0.825V (typical) in deep sleep, and ends when the supply exceeds 1.10V (typical). Glitches of up to 30mV and 2.5us duration, which could be caused by large load steps, will not trigger a reset.

Each of the internal processors has its own independent watchdog timer to detect and recover from erroneous software operation. These are typically configured with a timeout of 1.5s, but this may be increased up to a maximum of 64s for reduced power consumption. The watchdogs are enabled at power-on and continue operating while WiFi is in deep sleep.

During all forms of reset most digital I/O pins (including both bidirectional pins and dedicated inputs or outputs) default to high impedance with weak internal pull-downs. The only exceptions are WL_RESETn and WL_SPI_CS which both have pull-ups, and the SDIO/CSPI bus which is on an independent reset domain. The SDIO/CSPI host interface is only fully reset by the WL_RESETn pin or the power supply supervisor; other forms of reset leave the host interface initialized but simply clear the I/O Enable bit for function 1.

Following a reset, WiFi automatically generates safe clocks for internal use. If an external reference clock is connected to WL_CLK then this is assumed to be at the maximum supported frequency, otherwise the PLL free runs at a nominal frequency. In either case the generated clock will be slower than in normal operation, but this is sufficient for safely booting and configuring the IC.

Power-on Reset	Min	Typ	Max	Units
Reset release on WL_VDD_DIG rising (HI)	1.05	-	1.15	V
Reset assert on WL_VDD_DIG falling (LO)	HI-0.060	-	HI-0.045	V
Reset assert on WL_VDD_DIG falling (Sleep mode)	0.80	0.825	0.85	V

1-6 Electrical Specifications

1-6-1 Absolute Maximum Rating

Symbol	Description	Min.	Max.	Units
T_{ST}	Storage temperature	-40	+85	°C
WL_3V3	Positive supply for AIO[0]-AIO[3] , PIO[8]-PIO[15], and FEM	-0.3	+3.6	V

*Absolute maximum ratings indicate limits beyond which damage to the device may occur.

1-6-2 Recommended Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Units
T_{OP}	Operating temperature	-40	+25	+85	°C
WL_3V3	Positive supply for AIO[0]-AIO[3] , PIO[8]-PIO[15], and FEM	+3.2	+3.3	+3.6	V

1-7 Current Consumption

Conditions: WL_3V3= +3.3 V, T_{OP}= 25°C

Parameter	Test conditions	Units	Min.	Typ.	Max.
802.11b Current Consumption					
11Mbps transmit@+17dBm	Continuous packet, PSDU length of 1024 Bytes (958us), packet interval 50µs	mA	-	213/ 3V3	-
11Mbps receive	-85dBm.Continuous packet, PSDU length of 1024 Bytes, packet interval 50µs	mA	-	77/ 3V3	-

Parameter	Test conditions	Units	Min.	Typ.	Max.
802.11g Current Consumption					
54Mbps transmit@+13dBm	Continuous packet, PSDU length of 1024 Bytes (179us), packet interval 117μs	mA	-	133/ 3V3	-
54Mbps receive	-70dBm. Continuous packet, PSDU length of 1024 Bytes, packet interval 50μs	mA	-	82/ 3V3	-
802.11n Current Consumption					
MCS7 transmit@+12dBm	Continuous packet, PSDU length of 4096 Bytes	mA	-	122/ 3V3	-
MCS7 receive	-68dBm. Continuous packet, PSDU length of 4096 Bytes	mA	-	82/ 3V3	-
Listen	Receive but no OFDM/CCK packet in air	mA	-	10/3V3	-
Sleep Current Consumption					
Deep sleep		uA	-	290/3V3	-

1-8 RF Specification

Conditions: WL_3V3= +3.3 V, T_{OP}= 25°C

Parameter	Test conditions	Units	Min.	Typ.	Max.
802.11b Transmit					
Operating frequency range		-	Ch 1	-	Ch 13
Transmit output power	1/2/5.5/11Mbps	dBm	-	+17	-
Center frequency tolerance		ppm	-	+5	-
ACPR: 1st side lobe power	Pout=+17.0dBm, 1/2/5.5/11Mbps	dBc	-	-42	-
ACPR: 2nd side lobe power	Pout=+17.0dBm, 1/2/5.5/11Mbps	dBc	-	-58	-
Transmit EVM	11Mbps, Channel 1~13	%	-	8	-
Transmit ramp-up time	10% ~ 90%	μs	-	0.8	-
Transmit ramp-down time	10% ~ 90%	μs	-	1	-
802.11b Receive					
Minimum input level sensitivity	11Mbps CCK, FER<8% at PSDU length of 1024 bytes	dBm	-	-85	-

Parameter	Test conditions	Units	Min.	Typ.	Max.
Maximum input level capability	11Mbps CCK, FER<8% at PSDU length of 1024 bytes	dBm	-	+5	-
802.11g Transmit					
Operating frequency range		-	Ch 1	-	Ch 13
Transmit output power	54Mbps OFDM	dBm	-	+13	-
Center frequency tolerance	54Mbps OFDM	ppm	-	+5	-
Symbol clock freq. tolerance	54Mbps OFDM	ppm	-	+4	-
Transmit EVM	54Mbps OFDM, Channel 1~13	dB	-25	-	-
Transmit ramp-up time	10% ~ 90%	μs	-	0.8	-
Transmit ramp-down time	10% ~ 90%	μs	-	1	-
802.11g Receive					
Receive minimum input level sensitivity	54Mbps OFDM, FER<10% at PSDU length of 1024 bytes	dBm	-	-70	-
Receive maximum input level capability	54Mbps OFDM, FER<10% at PSDU length of 1024 bytes	dBm	-	-13	-
802.11n 20MHz Transmit					
Operating frequency range		-	Ch 1	-	Ch 13
Transmit output power	MCS6	dBm	-	+12	-
Transmit modulation accuracy	MCS6	dB	-	-25	-
Symbol clock frequency tolerance	MSC6	ppm	-	+5	-
Transmit center frequency tolerance	MCS6	ppm	-	+2	-
Spectrum Mask	f < fc-30, fc+30 <f	dBr	-	-49	-
	fc-30 <f <fc-20, fc+20 <f <fc+30	dBr		-42	
	fc-20 <f <fc-11, fc+11 <f <fc+20	dBr	-	-31	-
	fc-11 <f <fc-9, fc+9 <f <fc+11	dBr	-	-15	-
802.11n 20MHz Receive					
Receive minimum input level sensitivity	MCS7 (FER<10% at PSDU length of 1024 bytes)	dBm	-	-68	-
Receive maximum input level capability	MSC7 (FER<10% at PSDU length of 1024 bytes)	dBm	-	-17	-

2 Software Specification

2-1 OS Support & Available Drivers

- SDIO 1 bit or 4-bit
  - Linux 2.6.24 and above
  - Android
  - RTOS

2-2 Security Features Supported

- Support for IEEE 802.11i security enhancements
  - WEP
  - TKIP
  - AES
  - WPA
  - WPA2

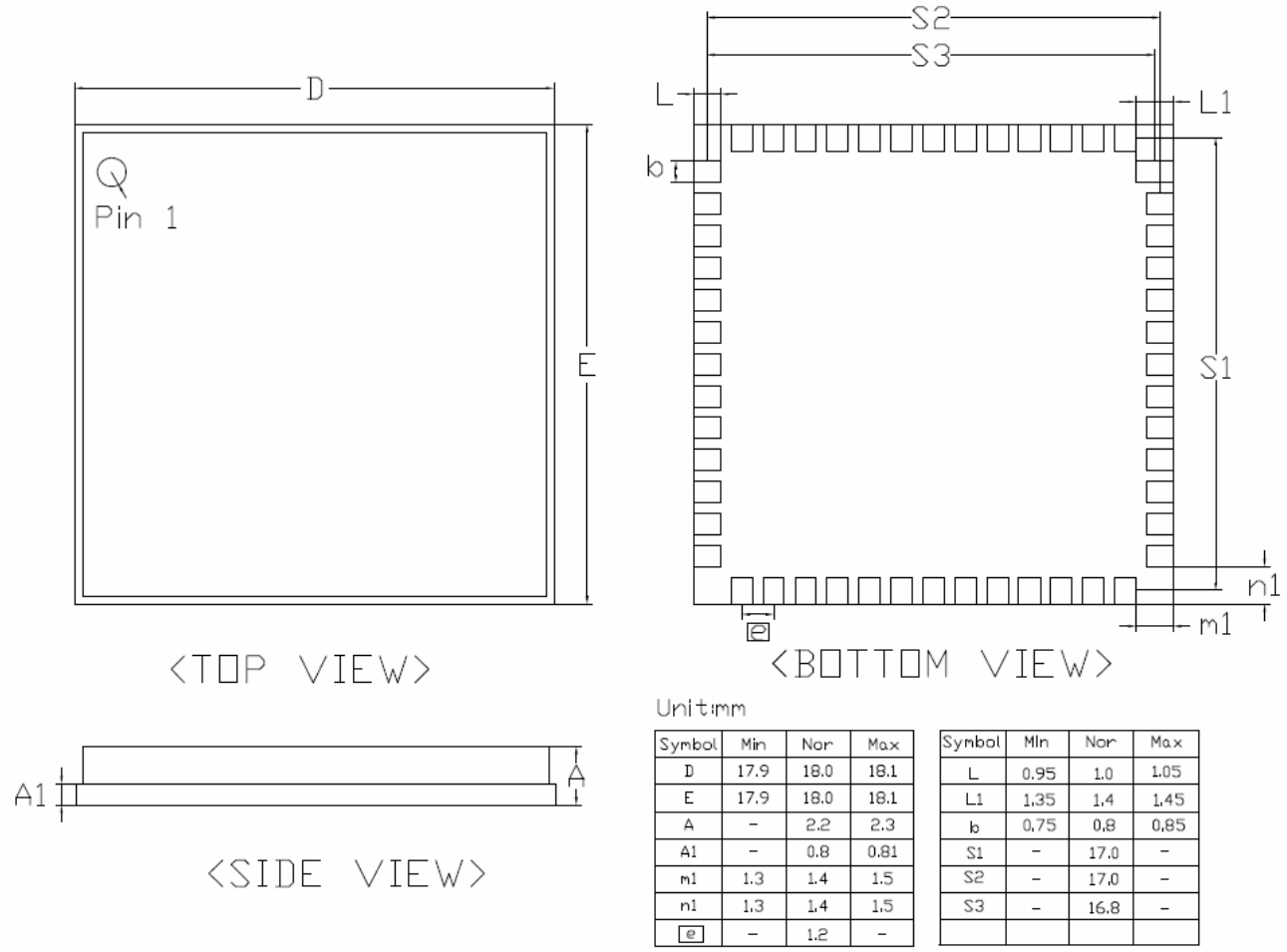
2-3 Other Features

- Support for IEEE 802.11d transmit power control (Regulatory Domain Support for New Countries)
- Support for IEEE 802.11e (Quality of Service): WMM and WMM Power Save
- Host wakeup signaling

3 Mechanical Specification

Dimension	18×18×2.2 mm (max. height)
Pinout	52
Weight	1.343g

3-1 Package Outline



Unit:mm

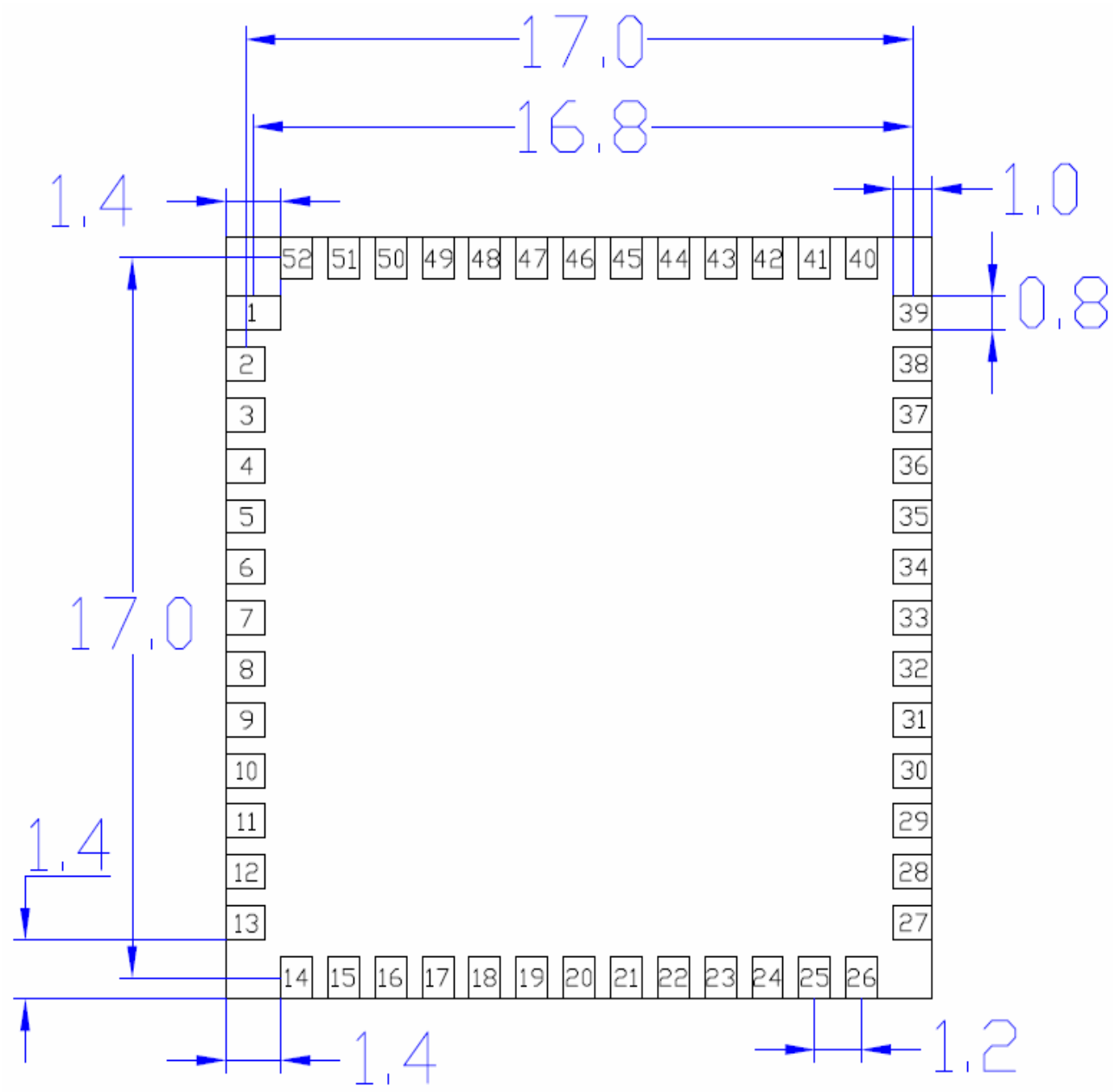
Symbol	Min	Nor	Max
D	17.9	18.0	18.1
E	17.9	18.0	18.1
A	-	2.2	2.3
A1	-	0.8	0.81
m1	1.3	1.4	1.5
n1	1.3	1.4	1.5
e	-	1.2	-

Symbol	Min	Nor	Max
L	0.95	1.0	1.05
L1	1.35	1.4	1.45
b	0.75	0.8	0.85
S1	-	17.0	-
S2	-	17.0	-
S3	-	16.8	-

4 Assembly Guideline

4-1 Recommended Mounting Pad Design (Top View)

The following figure illustrates the recommended mounting pad design for apm1689.



TOP VIEW (mm)

4-2 Recommendation for Stencil Aperture in SMT Process

Please follow general QFN stencil design guideline. Some rules of thumb are highlighted below.

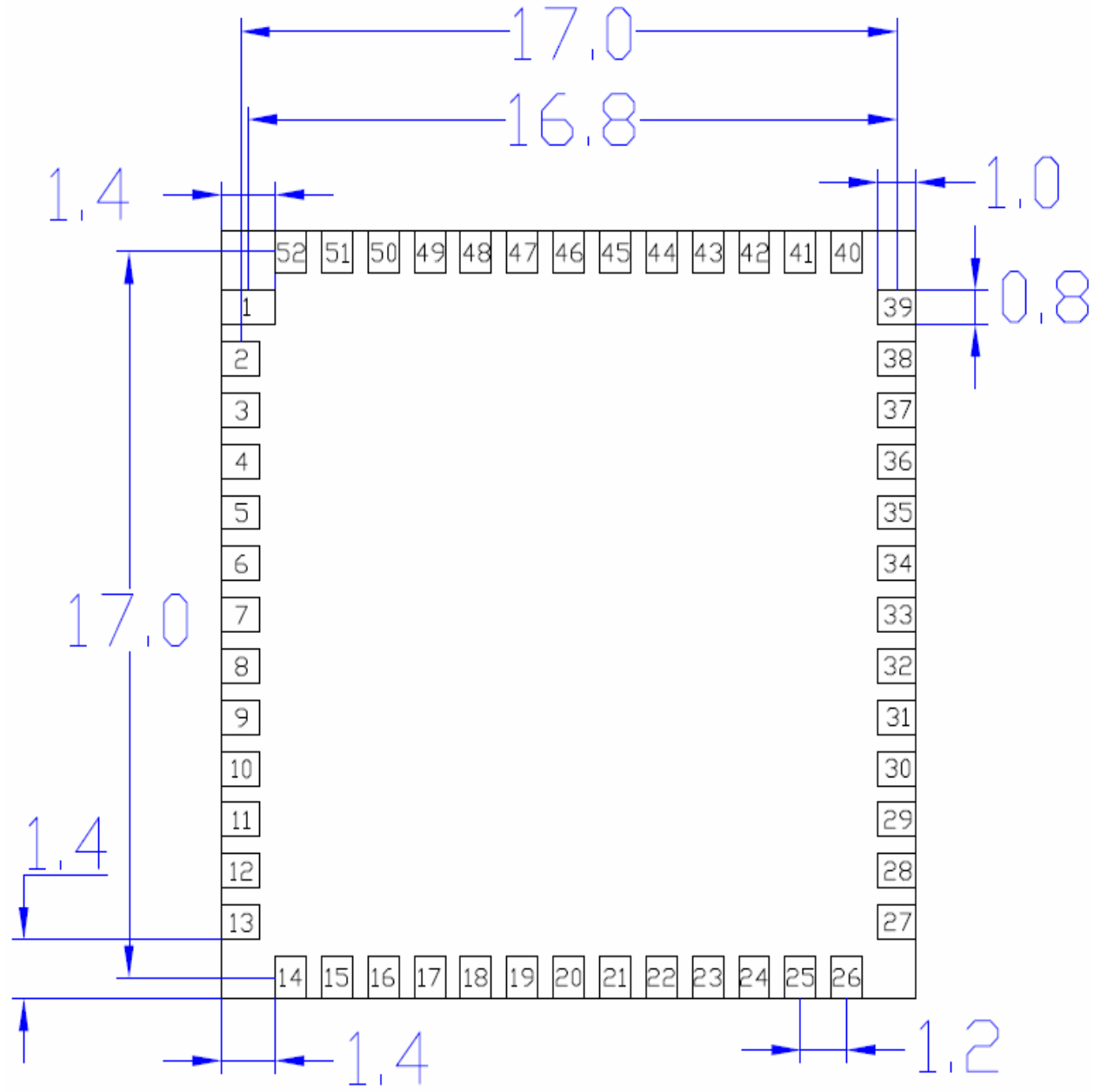
• The LGA pads should NOT be flooded over with copper, they should be connected into the plane with a track width of approx 50% of the pad width, this will mean more heat will be available at the joint. Track lengths should obviously be minimized, we would generally use about 0.3mm on external layers.

• The solder paste pattern for the internal Tab pads could be split into 4 smaller segments for the 2 large pads, and 2 smaller segments for the smaller pads, this should have the effect of preventing the paste from pooling into one area, and hence minimize the likelihood of the pads being held away from each other. We use a rule of thumb of 50% solder paste area in relation to Tab copper area (this only applies to tab pads under the device – not the signal pads).

• The thickness of the solder paste stencil has implications on solder joint quality as well, we do not have the knowledge on what stencil should be specified.

• Ensure they are using a good appropriate flux, and the correct reflow profile for unleaded (basically +20C above leaded) which is also uniform in nature.

Violating the basic rules might cause problems. For example, if the stencil apertures of the internal ground planes are improperly big, they would hold more solders in SMT process and may cause the module peripheral pads un-contacted to the main board. To improve this situation, apmcomm suggests the stencil opening shown as follows.



Stencil Aperture (Top View)

4-3 Baking condition recommendation before IR reflow

Baking condition for apm1689 module:

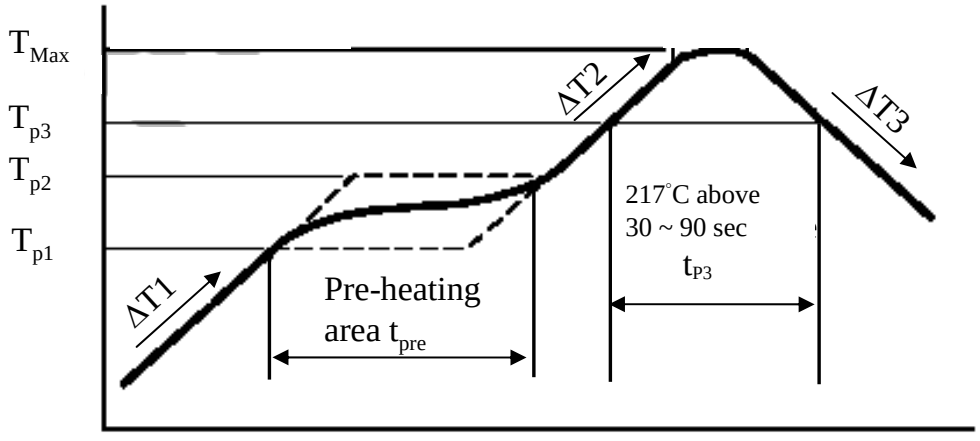
I: 125°C/4 hrs baking is necessary for apm1689 module before SMT process. After baking treatment the modules can be stored in the environment under 30°C and 60% RH for 168 hrs. If the storage time is over 168 hrs, the modules need to be re-baked using the same condition again.

II: In the event that the sealed bag is damaged on receipt of the modules, the baking condition should be changed to 125°C/8 hrs.

4-4 Recommendation for Reflow Profile

Maximum reflow temperature is 250°C.

Preheat ramp-up rate	125°C to 180°C 1 to 3°C /sec.
Peak temperature	250°C max.
Temperature maintained above 217°C	30 ~ 90 sec.
Cooling ramp-down rate	<2°C/sec.
Maximum number of reflow cycles	≤3



Heating/Cooling Speed			Pre-Heating		Heating	
ΔT1	ΔT2	ΔT3	T_{p1}–T_{p2}	t_{pre}	T_{Max}	t_{P3}
1 to 3°C /sec.	1 to 3°C /sec.	< 2°C /sec.	125 ~ 180°C	30 ~ 90 sec.	250°C max.	30 ~ 90 sec.