apm8142 BT2.0+EDR HCI Module

DESCRIPTION

With the on- chip CSR Bluetooth software stack it provides a fully compliant Bluetooth system to v2.0+EDR of the specification for data and voice communications. The device incorporates auto -calibration and built in self test (BIST) routines to simplify development, type approval and production test. The pre-tested module eliminates the need to create custom designs, resulting in greatly reduced development risk, costs and time-to-market.

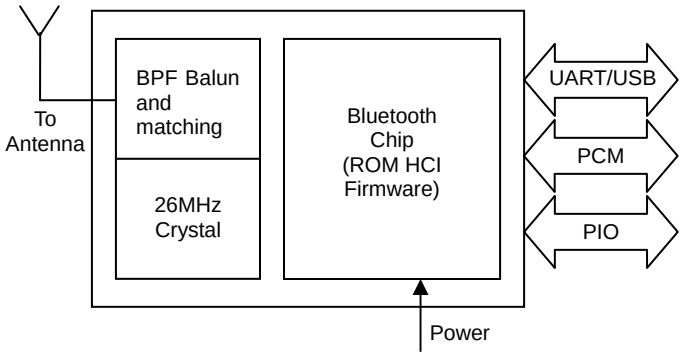
FEATURES

- Enhanced Data Rate(EDR) compliant with v2.0 of specification for both 2Mbps and 3Mbps modulation modes
- Fully Qualified Bluetooth v2.0+EDR system
- Small footprint: 6.8×6×1.35mm LGA package
- Full Speed Bluetooth Operation with Full Pico-net Support
- Scatter-net Support
- Ultra low power consumption
- Excellent Compatibility with Cellular Telephones
- USB and UART Port to 3Mbits/s
- Support for 802.11 two wire & three wire co-existence

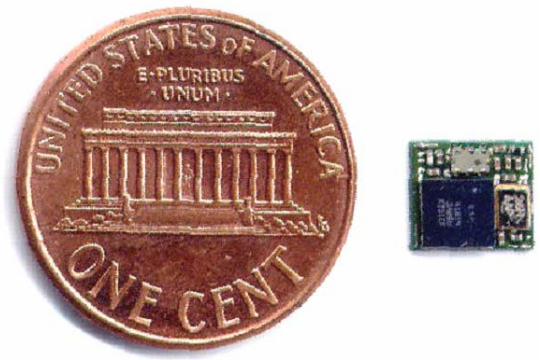
APPLICATIONS

- Headsets
- Automotive Hands-Free Kits
- Smartphone / PDA / PDA phone / WiFi Phone / DSC / DVC with Bluetooth connectivity

FUNCTIONAL BLOCK DIAGRAM



APPEARANCE



REVISION HISTORY

Date	Release	Author	Description
2006-Nov-20	1.0	Yushin/Baron	Initial release
2006-Nov-26	1.1	Yushin/Baron	Package change
2007-Nov-30	1.2	Winter/Wang	Document format revise.
2008-Feb-18	1.3	Winter	Combine and reorganize section 5, 6, 7, 8
2008-Mar-04	1.4	KungHua	Updated all sections
2008-Aug-01	1.5	Winter/Vedam	Updated Appearance Updated Pinout in section 1 Updated RF Specification in section 3-1 Updated Host Interface Selection in section 4 Updated Assembly Guideline in section 6
2008-Aug-04	1.6	Winter/Vedam	Updated Features
2008-Aug-05	1.7	Winter/Vedam	Updated ”Package Outline” in section 5-1 Updated “Assembly Guideline” in section 6
2008-Dec-09	1.8	Winter	Updated ”Picture” in Appearance Updated ”Baking condition” in section 6-3
2010-May-24	1.9	KungHua	Updated “Package Outline” in section 5-1 Updated ”Baking condition” in section 6-3
2010-May-28	2.0	KungHua	Updated Features

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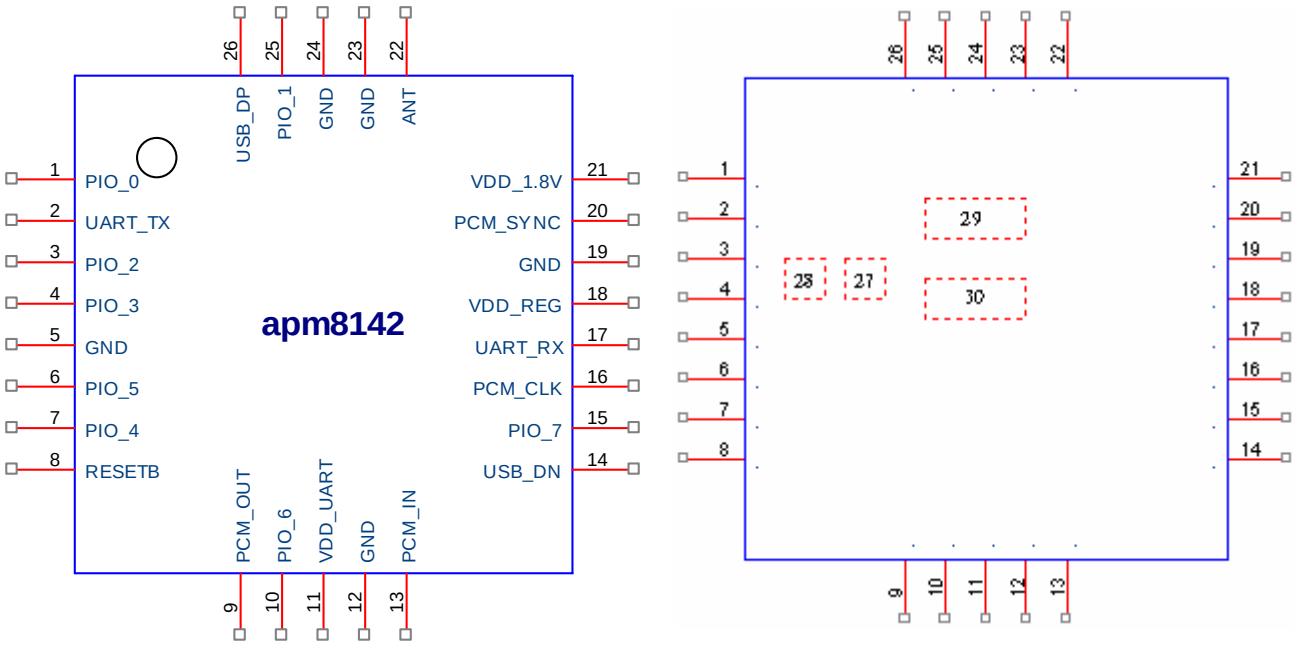
1 Pinout

1-1 Pin Assignment (Top View)



1-2 Pin Description

* I/O: Digital Input/Output, I: Digital Input, O: Digital Output, A: Analog, PU: Pull-up, PD: Pull-down

#	Name	I/O	Internal Resistor	Description
1	PIO_0	I/O	-	Programmable input/output
2	UART_TX	O	PU	UART data output active high
3	PIO_2	I/O	-	Programmable input/output
4	PIO_3	I/O	-	Programmable input/output
5	GND	GND	-	Ground
6	PIO_5	I/O	-	Programmable input/output
7	PIO_4	I/O	-	Programmable input/output
8	RESETB	I	PU	Reset, active low. Input de-bounced so must be low for >5ms to cause a reset.
9	PCM_OUT	I/O	PD	Synchronous data output
10	PIO_6	I/O	-	Programmable input/output

#	Name	I/O	Internal Resistor	Description
11	VDD_UART	Power	-	Host interface digital I/O power supply
12	GND	GND	-	Ground
13	PCM_IN	I/O	PD	Synchronous data input
14	USB_DN	I/O	-	USB data minus
15	PIO_7	I/O	-	Programmable input/output
16	PCM_CLK	I/O	PD	Synchronous data clock
17	UART_RX	I	PD	UART data input active high
18	VDD_REG	Power	-	Regulator input
19	GND	GND	-	Ground
20	PCM_SYNC	I/O	PD	Synchronous data sync
21	VDD_1.8V	Power	-	Regulator output, recommend floating
22	ANT	A	-	RF input/output
23	GND	GND	-	Ground
24	GND	GND	-	Ground
25	PIO_1	I/O	-	Programmable input/output
26	USB_DP	I/O	-	USB data plus with selectable 1.5k pull-up resister
27	PIO_8	I/O	-	Programmable input/output
28	PIO_9	I/O	-	Programmable input/output
29	GND	GND	-	Ground
30	GND	GND	-	Ground

Pin 27~ Pin30 are the pads on the bottom of the module. Please see the details in section 5-1 and 6-1.

2 Absolute Maximum Rating

Symbol	Description	Min.	Typ.	Max.	Units
-	Storage temperature	-40	-	+105	°C
VDD_REG	Supply Voltage	-0.4	-	+5.6	Volts
VDD_1.8V	Supply Voltage	-0.4	-	+2.2	Volts
VDD_UART	Supply Voltage	-.0.4	-	+3.7	Volts

*Absolute maximum ratings indicate limits beyond which damage to the device may occur.

2-1 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Units
-	Operating temperature	-20	-	+70	°C
VDD_REG	Supply Voltage	+2.2	-	+4.2	Volts
VDD_1.8V	Supply Voltage	+1.7	+1.8	+1.9	Volts
VDD_UART	Supply Voltage	+1.7	-	+3.6	Volts

*The device will operate without damage with VDD_REG as high as +5.6V. However the RF performance is not guaranteed above the +4.2V.

3 RF Specification

Condition: VDD_REG= +3.3V, VDD_UART= +3.3V, T_{OP}= 25°C

Parameter	Test conditions	Min.	Typ.	Max.	Units
Transmit – Basic Data Rate					
Maximum RF transmit power		-	+3	-	dBm
Lowest emission frequency below the operation frequency		2.40	-	-	GHz
Highest emission frequency below the operation frequency		-	-	2.478	GHz
20dB bandwidth for modulated carrier		-	800	-	kHz
Adjacent channel power F=F_0 + 2MHz(6)		-	-40	-20	dBm
Adjacent channel power F=F_0 > + 3MHz(6)		-	-45	-40	dBm
Modulation index: Δf1avg		+140	+163	+175	kHz
Modulation index: Δf2max		+115	+150	-	kHz
Modulation index: Δf2avg / Δf1avg		0.8	0.99	-	NA
Initial carrier frequency accuracy		-	+5	+25	kHz
Carrier frequency drift rate		-	+8	+20	kHz/50us
Carrier frequency drift	One slot packet	-	+7	+20	kHz
	Three slot packet	-	+8	+25	kHz
	Five slot packet	-	+8	+25	kHz
Receive – Basic Data Rate					
Sensitivity at 0.1% BER	Single slot packets	-	-82	-80	dBm
	Multi-slot packets	-	-82	-80	dBm
Co-channel Interference, C/$I_{co\text{-}channel}$ Ratio		-	+5	+11	dB
Adjacent (1MHz) Interference, C/I_{1MHz} Ratio		-	-7	0	dB
Adjacent (2MHz) Interference, C/I_{2MHz} Ratio		-	-43	0	dB
Adjacent (>3MHz) Interference, C/$I_{>3MHz}$ Ratio		-	-47	-40	-dB
Block Performance: 30MHz~2000MHz		-10	12	-	dBm
Block Performance: 2000MHz~2400MHz		-27	-6	-	dBm
Block Performance: 2500MHz~3000MHz		-27	-11	-	dBm
Block Performance: 3000MHz~12.75GHz		-10	-6	-	dBm

Parameter	Test conditions	Min.	Typ.	Max.	Units
Intermodulation performance		-39	-28	-	dBm
Maximum usable signal		-20	-10	-	dBm
Transmit – Enhanced Data Rate					
Maximum RF transmit power		-	+1	-	dBm
Relative Transmit Power		-4	-1.5	1	dB
π/4-DQPSK max carrier frequency stability ω_o		-10	+2	+10	kHz
π/4-DQPSK max carrier frequency stability ω_i		-75	+3	+75	kHz
π/4-DQPSK max carrier frequency stability $\lvert \omega_o+\omega_i \rvert$		-75	+5	+75	kHz
8DPSK max carrier frequency stability ω_o		-10	+3	+10	kHz
8DPSK max carrier frequency stability ω_i		-75	+3	+75	kHz
8DPSK max carrier frequency stability $\lvert \omega_o+\omega_i \rvert$		-75	+6	+75	kHz
π/4 DQPSK differential Phase Encoding		-	100	-	%
8DPSK differential phase encoding		-	100	-	%
π/4-DQPSK Modulation Accuracy	RMS DEVM	-	8	20	%
	Peak DEVM	-	20	35	%
8DPSK Modulation Accuracy	RMS DEVM	-	8	13	%
	Peak DEVM	-	20	25	%
Receive – Enhanced Data Rate					
Sensitivity at 0.01% BER	π/4-DQPSK	-	-84	-81	dBm
	8DPSK	-	-77	-74	dBm
Maximum usable signal π/4 DQPSK		-20	-10	-	dBm
Maximum usable signal 8DPSK		-20	-10	-	dBm
Current Consumption					
Inquiry mode		-	2.2	-	mA
Deep sleep mode		-	35	-	uA
ACL DH1 continuous packets		-	35.0	-	mA
ACL DH3 continuous packets		-	45.0	-	mA
ACL DH5 continuous packets		-	48.2	-	mA
ACL 2-DH1 continuous packets		-	35.4	-	mA
ACL 2-DH3 continuous packets		-	44.1	-	mA

Parameter	Test conditions	Min.	Typ.	Max.	Units
ACL 2-DH5 continuous packets		-	47.0	-	mA
ACL 3-DH1 continuous packets		-	35.4	-	mA
ACL 3-DH3 continuous packets		-	44.1	-	mA
ACL 3-DH5 continuous packets		-	47.1	-	mA
SCO connection HV1		-	35.0	-	mA
SCO connection HV2		-	35.0	-	mA
SCO connection HV3		-	35.0	-	mA
eSCO connection EV3		-	35.0	-	mA
eSCO connection EV4		-	35.0	-	mA
eSCO connection EV5		-	35.0	-	mA
eSCO connection 2 EV3		-	35.8	-	mA
eSCO connection 2-EV5		-	43.8	-	mA
eSCO connection 3-EV3		-	35.8	-	mA
eSCO connection 3-EV5		-	43.8	-	mA

4 Host Interface Selection

apm8142 Bluetooth (CSR BC4 ROM) boot setup (host interface etc) can be configured by using BT_PIO[0], [1] & [4]. To set a configuration bit to 0, leave the appropriate pin floating. Pull the appropriate pin high to set a configuration bit to 1.

BT_PIO[0]	BT_PIO[1]	BT_PIO[4]	Host Transport	Features	
				Auto system Clock Adaptation	Auto Band Rate Adaptation
0	0	0	BCSP(default)	Available(*1)	Available(*2)
0	0	1	BCSP with UART configured to use 2 stop bits and no parity	Available(*1)	Available(*2)
0	1	1	USB, 26MHz crystal	Not available	Not appropriate
1	0	0	Three-wire UART	Available(*1)	Available(*2)
1	0	1	Undefined	---	---
1	1	0	UART(H4)	Available(*1)	Available(*2)
1	1	1	Undefined	---	---

(*1) If a UART-based host transport is selected and the firmware does not know its clock frequency (because PSKEY_ANA_FREQ contains no value), then the firmware attempts to lock on to the available system clock signal. Use of this mechanism implies booting the firmware twice, as described in [AUTOBAUD]. PSKEY_ANA_FREQ has no default value.

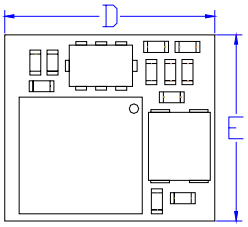
(*2) If a UART-based host transport is selected and the baud rate defined in PSKEY_UART_BAUDRATE is zero (the default value), then the baud rate adaptation process is invoked, as described in [AUTOBAUD].

If the PS Key contains a non-zero baud rate then the UART is configured with this value. If the system clock adaptation mechanism is used, it may result in the processor running slower than normal, so the consequent (measured) baud rate will also be affected.

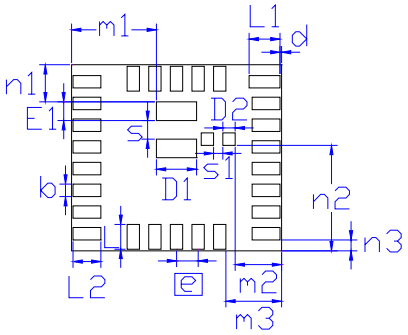
5 Mechanical Specification

Dimension	6.8×6×1.35 mm
Weight	0.1375 gram
Pinout	30
Antenna	External antenna support (Pin 22)

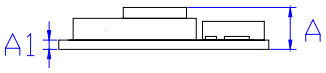
5-1 Package Outline



<TOP VIEW>



<BOTTOM VIEW>



<SIDE VIEW>

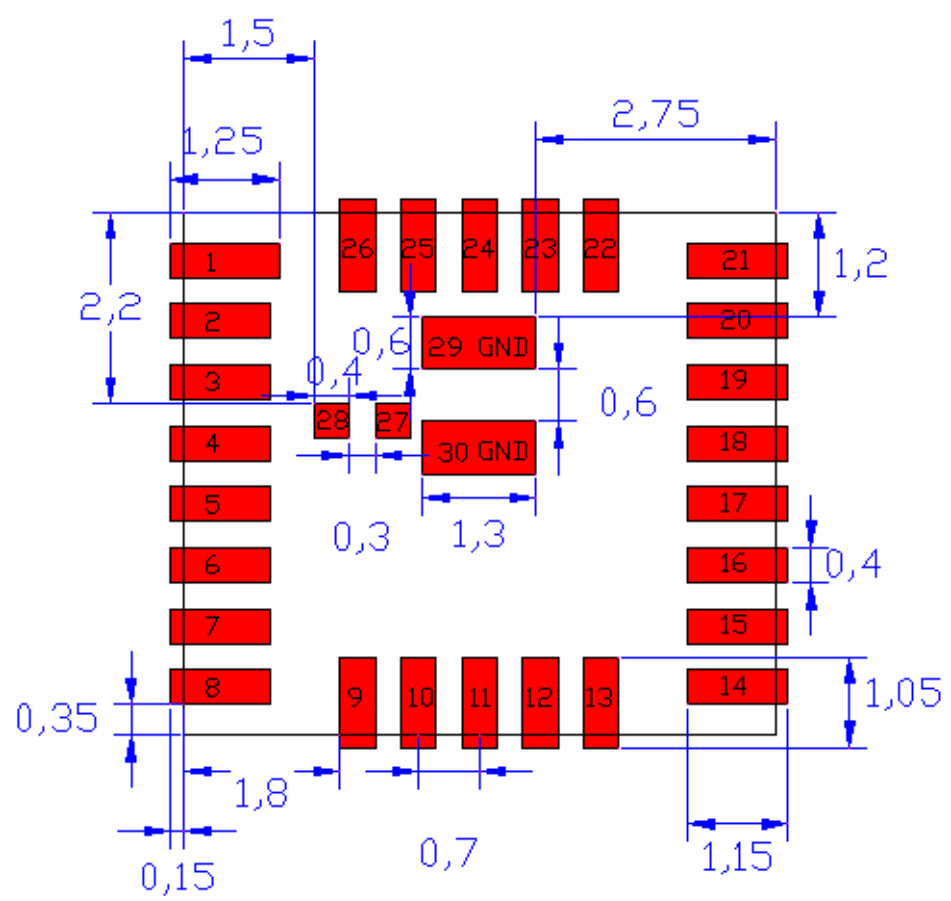
Unit:mm

Symbol	Min	Nor	Max
D	6.7	6.8	6.9
E	5.9	6.0	6.1
A	-	-	1.35
A1	-	-	0.3
m1	2.65	2.75	2.85
n1	1.1	1.2	1.3
m2	1.4	1.5	1.6
n2	3.3	3.4	3.5
m3	1.7	1.8	1.9
n3	0.25	0.35	0.45
s	0.5	0.6	0.7
s1	0.2	0.3	0.4

Symbol	Min	Nor	Max
D1	1.25	1.3	1.35
E1	0.55	0.6	0.65
D2	0.35	0.4	0.45
L	0.75	0.8	0.85
L1	0.95	1.0	1.05
L2	0.85	0.9	0.95
b	0.35	0.4	0.45
e	-	0.7	-
d	-	0.05	-

6 Assembly Guideline

6-1 Recommended Mounting Pad Design (Top View)



Unit: mm

PCB METAL LAND (TOP VIEW)

6-2 Recommendation for Stencil Aperture in SMT Process

Please follow general QFN stencil design guideline. Some rules of thumb are highlighted below.

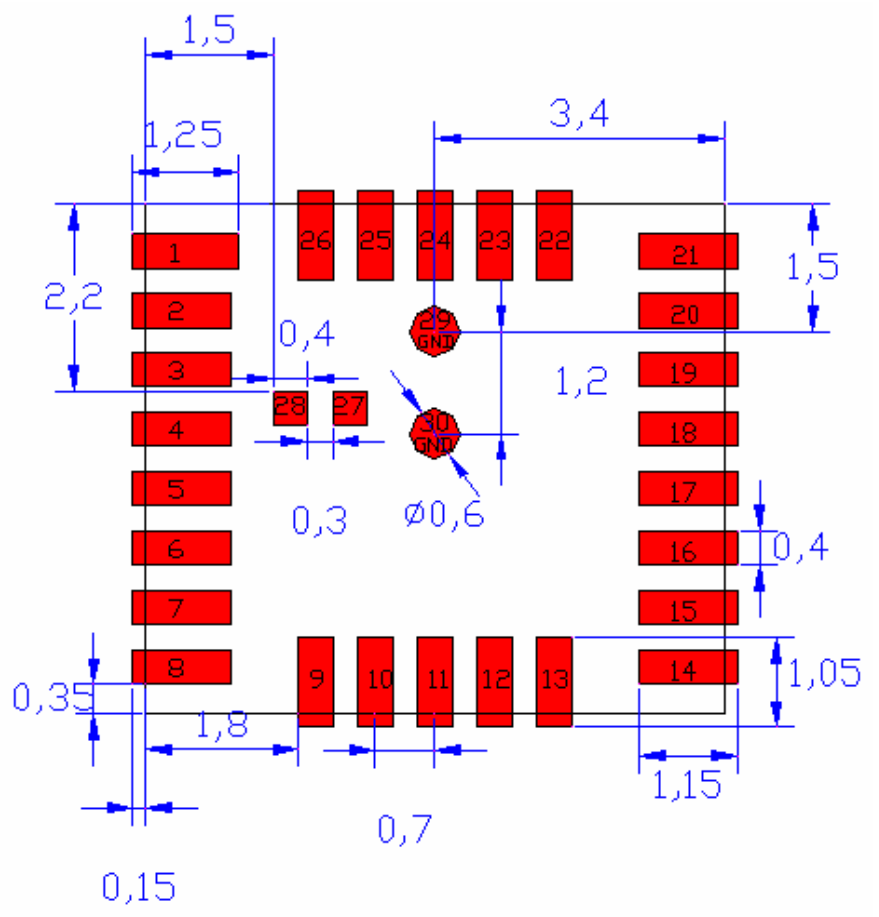
- The LGA pads should NOT be flooded over with copper, they should be connected into the plane with a track width of approx 50% of the pad width, this will mean more heat will be available at the joint. Track lengths should obviously be minimized, we would generally use about 0.3mm on external layers.

- The solder paste pattern for the internal Tab pads could be split into 4 smaller segments for the 2 large pads, and 2 smaller segments for the smaller pads, this should have the effect of preventing the paste from pooling into one

area, and hence minimize the likelihood of the pads being held away from each other. We use a rule of thumb of 50% solder paste area in relation to Tab copper area (this only applies to tab pads under the device – not the signal pads).

- The thickness of the solder paste stencil has implications on solder joint quality as well, we do not have the knowledge on what stencil should be specified.
- Ensure they are using a good appropriate flux, and the correct reflow profile for unleaded (basically +20C above leaded) which is also uniform in nature.

Violating the basic rules might cause problems. For example, if the stencil apertures of the internal ground planes are improperly big, they would hold more solders in SMT process and may cause the module peripheral pads un-contacted to the main board. To improve this situation, apm suggests the stencil opening shown as follows.



Unit: mm

STENCIL APETURE (TOP VIEW)

6-3 Baking condition recommendation before IR reflow

Baking condition for apm8142 module:

I: 125°C /4 hrs baking is necessary for apm8142 module before SMT process. After baking treatment the modules can be stored in the environment under 30°C and 60% RH for 48 hrs. If the storage time is over 48 hrs, the modules need to be re-baked using the same condition again.

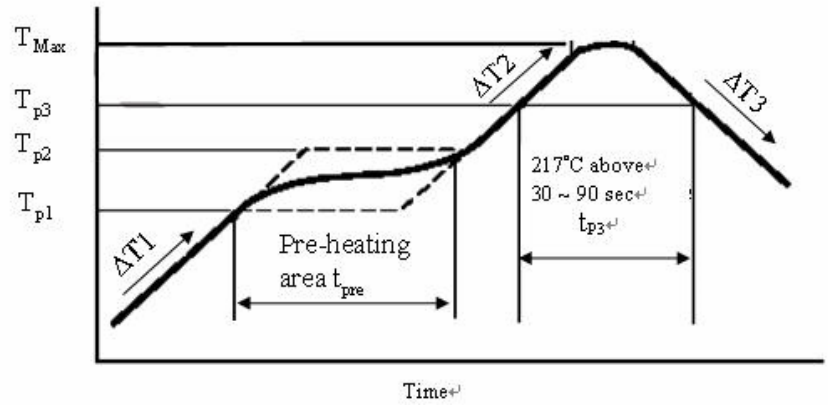
II: In the event that the sealed bag is damaged on receipt of the modules, the baking condition should be changed to 125°C /8 hrs.

6-4 Recommended Temperature Reflow Profile

The solder profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow.

Maximum reflow temperature is 250°C

Preheat ramp-up rate	125°C to 180°C 1 to 3°C / sec.
Peak temperature	250°C, Max.
Temperature maintained above 217°C	30 ~ 90 sec.
Cooling ramp-down rate	<2°C / sec.
Maximum number of reflow cycles	≤3



Typical Lead-Free Re-flow Solder Profile

Heating/Cooling Speed			Pre-Heating		Heating	
ΔT1	ΔT2	ΔT3	T_{p1}–T_{p2}	t_{pre}	T_{Max}	t_{P3}
1 to 3°C / sec	1 to 3°C / sec	< 2°C / sec	125 ~ 180°C	30 ~ 90 sec.	250°C max.	30 ~ 90 sec.