apm8282 / apm8262 Bluetooth Audio Module

DESCRIPTION

apm8282 / apm8262 are fully compliant Bluetooth v2.1+EDR system module for data and voice communication. It integrated BC5-MM, RF matching circuit, crystal and Flash memory into a surface mount module with a compact size of 11 × 13 × 1.9 mm.

The specified profiles and firmware are pre-loaded into the built-in flash memory of apm8282 / apm8262 for Bluetooth audio transmission and receiving. It can be easily embedded into portable multimedia and audio systems for Bluetooth wireless communication. The pre-tested module reduces the customer development risk and cost greatly.

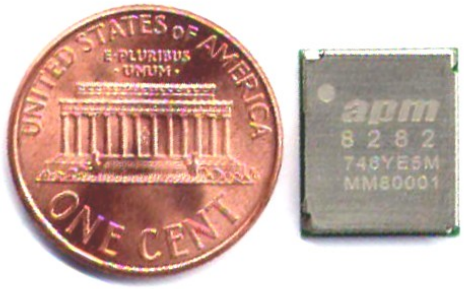
GENERAL FEATURES

- Compact size module: 64-pin surface mount module with a size of 11×13×1.9mm
- Integrate Bluetooth chip, RF matching circuit, crystal and Flash memory on a single module.
- Fully compliant with Bluetooth V2.1+EDR spec.
- Support up to 18 (16 digital and 2 analogue) programmable I/O terminals.
- Internal16-bit stereo audio CODEC with -90dB SNR for DAC
- Support PCM/I^2S/SPDIF interface
- USB and UART with Dual Port Bypass Mode to 4Mbits/s
- Support firmware upgrade.
- Class2 RF output power: < +4 dBm
- Receiver sensitivity: -88 dBm @0.1%BER

APPLICATIONS

- High Quality Stereo Wireless Headsets
- High Quality Mono Headsets
- Hands-Free Car kits
- Wireless Speaker
- VOIP Handsets
- Analogue and USB Multimedia Dongles
- Bluetooth-Enabled Automotive Wireless Gateway

APPEARANCE



REVISION HISTORY

Date	Release	Author	Description
31-Jul-07	1.0	Winter/Wang	Initial Release
19-Oct-07	1.1	Winter/Wang	Update the stencil, baking and IR reflow information in section 6, section 7 and section 8.
14-Nov-07	1.2	Winter/Wang	Updated the apm8282 photograph
20-Nov-07	1.3	Winter/Wang	Errata Correction
12-Feb-08	1.4	Winter	Reorganized Section 5 and Section 2
14-Feb-08	1.5	Winter	Reorganized Section 3 and Section 5
04-Mar-08	1.6	Winter	Reorganized all Sections.
08-May-08	1.7	Winter	Added ordering information in Section 6.
18-Jun-08	1.8	Winter	Updated the Bluetooth Specification v2.1 + EDR.
30-July-08	1.9	Winter	Updated the Section 1-3-2 and Section 1-4 RF Spec.
21-Nov-08	2.0	Winter	Updated the value of maximum RF transmit power, π/4DQPSK sensitivity in Section 1-4 and baking condition in Section 5-3.
09-Dec-08	2.1	Winter	Updated the baking condition in Section 5-3.
26-Jan-11	2.2	KungHua	Updated pin definition in section 3-2.

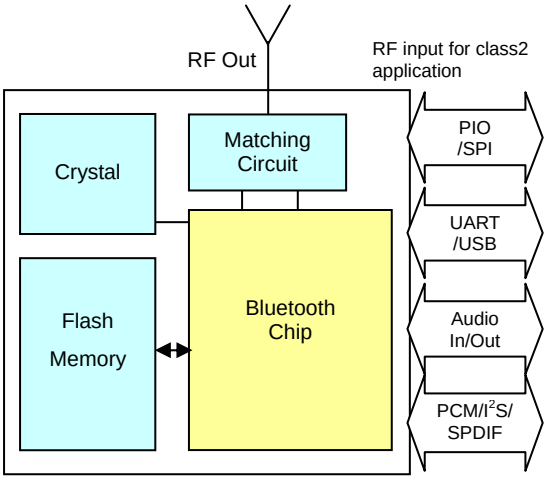
TABLE OF CONTENTS

1 Hardware Specification

1-1 General Specification

Bluetooth Specification	Bluetooth Specification v2.1 + Class 2 (all mandatory and optional features)
Interface	USB,UART,SPI and audio PCM interface
Frequency Band	2.402 to 2.480GHz (79 channels)
Modulation	GFSK, DQPSK (2Mbps), and 8DPSK (3Mbps)
Antenna	External single antenna support. The output impedance is 50Ω.

1-2 Block Diagram



1-3 Electrical Specifications

1-3-1 Absolute Maximum Rating

Description		Min.	Typ.	Max.	Units
Storage Temperature		-40	-	+85	°C
Supply Voltage: AUDIO_1V5, VDD_1V5		-0.4	-	1.65	Volts
Supply Voltage: VDD_PADS, VDD_PIO,VDD_MEM and VDD_USB		-0.4	-	3.6	Volts
Supply Voltage:	VDD_1V8	-0.4	-	2.7	Volts
	VREGENABLE	-0.4	-	5.6	Volts
	VDD_BAT,LED[0],LED[1]	-0.4	-	4.4	Volts
	VDD_CHG	-0.4	-	6.5	Volts

* Absolute maximum ratings indicate limits beyond which damage to the device may occur.

1-3-2 Recommended Operating Conditions

Description	Min.	Typ.	Max.	Units
Operating temperature	-20	-	+70	°C
Supply Voltage: VDD_1V5	1.42	-	1.57	Volts
Supply Voltage: VDD_1V8	1.7	-	1.95	Volts
Supply Voltage: VDD_PADS, VDD_PIO , and VDD_USB	1.7	3.3	3.6	Volts
VDD_MEM	2.7	3.3	3.6	Volts
VDD_USB for correct USB operation	3.1	-	3.6	

1-4 Bluetooth RF Specification

Operation Temp= +25°C, VDD_1V8= VDD_1V5= NC, VDD_PADS= VDD_PIO= VDD_USB= +3.3V

Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Transmit						
Maximum RF transmit power		1.5	3	6	-6 to +4	dBm
Lowest emission frequency below the operating frequency		2.4	-	-	≥ 2.4	GHz
Highest emission frequency above the operating frequency		-	-	2.4835	≤ 2.4835	GHz
20dB bandwidth for modulated carrier		-	870	1000	≤ 1000	kHz
Adjacent channel power F=F_0 ± 2MHz		-	-51	-20	≤-20	dBm
Adjacent channel power F=F_0 ≥ ± 3MHz		-	-58	-40	≤-40	
Modulation index: Δf1avg		140	164.2	175	140 ≤ Δf1avg ≤ 175	kHz
Modulation index: Δf2max		115	140	-	≥ 115	kHz
Modulation index: Δf2avg / Δf1avg		0.8	0.93	-	≥ 0.8	NA
Initial carrier frequency accuracy		-	10	35	± 75	kHz
Carrier frequency drift rate		-	10.5	20	≤ 20	kHz/50us
Carrier frequency drift: one slot packet		-	19	20	± 25	kHz
Carrier frequency drift: three slot packet		-	16	20	± 40	kHz
Carrier frequency drift: five slot packet		-	18	25	± 40	kHz
Emissions	**Frequency(GHz)**	**Min**	**Typ**	**Max**	**Bluetooth Spec.**	**Unit**
Emitted power in cellular bands measured at chip	0.925 ~ 0.960	-	-135.2	-133	Integrated in 200kH bandwidth	dBm/Hz

Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
terminals (Output power ≤4dBm)	1.570 ~ 1.580	-	-134.4	-132.6	Integrated in 1MHz bandwidth	
	1.805 ~ 1.880	-	-134.5	-131.9	Integrated in 200kHz bandwidth	
	1.980 ~ 1.990	-	-135.1	-133.4	Integrated in 30kHz bandwidth	
	1.930 ~ 1.990	-	-134.6	-132.8	Integrated in 200kHz bandwidth	
	1.930 ~ 1.990	-	-135.1	-133.4	Integrated in 1.2MHz bandwidth	
	2.110 ~ 2.170	-	-135	-133.4	Integrated in 1.2MHz bandwidth	
	2.110 ~ 2.170	-	-133.3	-127	Integrated in 5MHz bandwidth	
Relative transmit power (EDR)		-4	-1	1	-4 to +1	dB
π /4 DQPSK max carrier frequency stability ωo (EDR)		-10	3.2	10	± 10	kHz
π /4 DQPSK max carrier frequency stability ωi (EDR)		-75	10	75	± 75	kHz
π /4 DQPSK max carrier frequency stability ωo+ ωi (EDR)		-75	13	75	± 75	kHz
8DPSK max carrier frequency stability ω o (EDR)		-10	3	10	± 10	kHz
8DPSK max carrier frequency stability ω i (EDR)		-75	11	75	± 75	kHz
8DPSK max carrier frequency stability ωo+ ωi (EDR)		-75	14	75	± 75	kHz
π /4 DQPSK modulation accuracy (EDR)	RMS DEVM	-	0.1	-	≤ 0.2	-
	Peak DEVM	-	0.2	-	≤ 0.35	-
8DPSK modulation accuracy (EDR)	RMS DEVM	-	0.09	-	≤ 0.13	-
	Peak DEVM	-	0.22	-	≤0.25	-
Receiver						
Sensitivity at 0.1%BER for all packet types	2402	-	-88	-86	≤ -70	dBm
	2441	-	-88	-86		dBm
	2480	-	-88	-86		
Sensitivity at 0.01% BER (EDR)	π /4 DQPSK	-	-89	-87	≤ -70	dBm
	8DPSK	-	-81	-78	≤ -70	dBm
Maximum usable signal (EDR)	π /4 DQPSK	-20	-0	-	≥ -20	dBm
	8DPSK	-20	0	-	≥ -20	dBm

Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Co-channel Interference, $C/I_{co\text{-}channel}$ Ratio		-	5	11	≤ 11	dB
Co-channel Interference, $C/I_{co\text{-}channel}$ Ratio		-	5	11	≤ 11	dB
Adjacent (1MHz) Interference, C/I_{1MHz} Ratio		-	-7	0	≤ 0	dB
Adjacent (2MHz) Interference, C/I_{2MHz} Ratio		-	-37	-30	≤ -30	dB
Adjacent (≥3MHz) Interference, $C/I_{\geq 3MHz}$ Ratio		-	-47	-	≤ -40	dB
Blocking	**Frequency (GHz)**	**Min**	**Typ**	**Max**	**Modulation**	**Units**
Block Performance(for Bluetooth sensitivity of -67 dBm with 0.1% BER)	0.824 ~ 0.849	-2	16	-	GSM	dBm
	0.880 ~ 0.915	5	16	-	GSM	dBm
	1.710 ~ 1.785	3	10	-	GSM	dBm
	1.850 ~ 1.910	1	9	-	GSM	dBm
	1.920 ~ 1.980	-8	8	-	WCDMA	dBm
Block Performance(for Bluetooth sensitivity of -72 dBm with 0.1% BER)	0.824 ~ 0.849	-10	15	-	GSM	dBm
	0.880 ~ 0.915	-8	15	-	GSM	dBm
	1.710 ~ 1.785	-7	3	-	GSM	dBm
	1.850 ~ 1.910	-11	2	-	GSM	dBm
	1.920 ~ 1.980	-18	0	-	WCDMA	dBm
Inter-modulation Performance		-	-30	-39	≥ -39	dBm
Maximum usable signal		-	0	-	≥ -20	dBm

Current Consumption	Average	Units
Standby mode	125	uA
ACL connection (No Traffic)	8.2	mA
Headphone stereo audio streaming	26.0	mA
Mono SCO connection	24.0	mA
ACL DH1 data transfer	19.7	mA
ACL DH3 data transfer	19.6	mA
ACL DH5 data transfer	19.4	mA
SCO HV1 data transfer	18.5	mA
SCO HV2 data transfer	18.6	mA
SCO HV3 data transfer	18.5	mA

2 Software Specification

2-1 Bluetooth Software Stacks

apm8282 / apm8262 are supplied with Bluetooth v2.1+EDR compliant stack firmware, which runs on internal RISC microcontroller.

2-2 HCI Stack

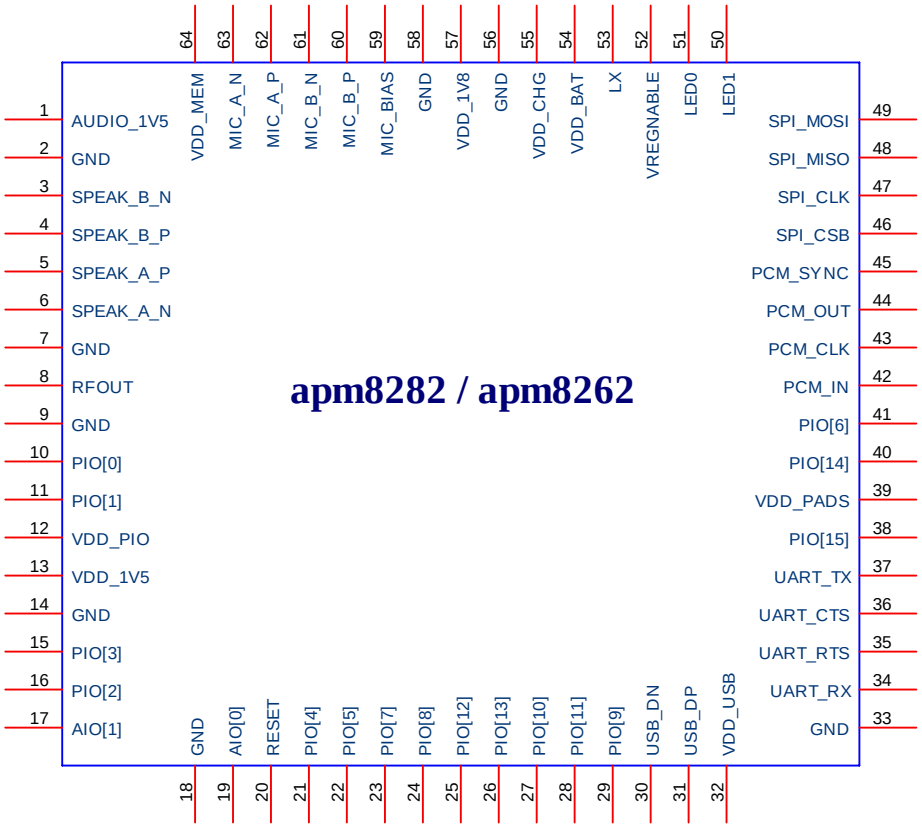
All Bluetooth v2.1+EDR mandatory and optional features are supported. The firmware also extends the standard Bluetooth functionality with numerous features. Please contact apmcomm FAE for details.

2-3 Host Software

BlueCore Embedded Host Software (BCHS) and the Windows CE Profile Pack (WPP) are supported to implement Bluetooth functionality into embedded products quickly and with low risk. Please contact apmcomm FAE for details.

3 Pin Descriptions

3-1 Pin Assignment



3-2 Pin Definition

Pin #	Pin Name	Type	Supply Domain	Description
1	AUDIO_1V5	VDD	-	1.5V regulated output for audio circuit
2	GND	GND	-	Ground
3	AUDIO_OUT_N_RIGHT	Analogue	AUDIO_1V5	Speaker output negative (right)
4	AUDIO_OUT_P_RIGHT	Analogue	AUDIO_1V5	Speaker output positive (right)
5	AUDIO_OUT_P_LEFT	Analogue	AUDIO_1V5	Speaker output positive (left)
6	AUDIO_OUT_N_LEFT	Analogue	AUDIO_1V5	Speaker output negative (left)
7	GND	GND	-	Ground
8	RF_OUT	RF	-	Transmitter output/switched receiver input
9	GND	GND	-	Ground
10	PIO[0]	Bi-directional with	VDD_PIO	Programmable input/output line

Pin #	Pin Name	Type	Supply Domain	Description
		programmable strength internal pull-up/down		
11	PIO[1]	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
12	VDD_PIO	VDD	-	Positive supply for PIO and AUX_DAC
13	VDD_1V5	VDD	-	1.5V regulated output for analogue circuit
14	GND	GND	-	Ground
15	PIO[3]	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
16	PIO[2]	Bi-directional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line
17	AIO[1]	Bi-directional	VDD_1V5	Analogue programmable input/output line
18	GND	GND	-	Ground
19	AIO[0]	Bi-directional	VDD_1V5	Analogue programmable input/output line
20	RESET	CMOS input with weak internal pull-up	-	Reset if low. Input debounced so must be low for >5ms to cause a reset.
21	PIO[4]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
22	PIO[5]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
23	PIO[7]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
24	PIO[8]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
25	PIO[12]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
26	PIO[13]	Bi-directional with programmable strength internal pull-up/down n	VDD_PADS	Programmable input/output line
27	PIO[10]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
28	PIO[11]	Bi-directional with programmable strength internal pull-up/down n	VDD_PADS	Programmable input/output line
29	PIO[9]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
30	USB_DN	Bi-directional	VDD_USB	USB data plus with selectable internal 1.5Kohm pull-up resistor

Pin #	Pin Name	Type	Supply Domain	Description
31	USB_DP	Bi-directional	VDD_USB	USB data minus
32	VDD_USB	VDD	-	Positive supply for UART/USB ports
33	GND	GND	-	Ground
34	UART_RX	CMOS input with weak internal pull-down	VDD_USB	UART data input
35	UART_RTS	Bi-directional CMOS output, tri-state, with weak internal pull-up	VDD_USB	UART request to send active low
36	UART_CTS	CMOS input with weak internal pull-down	VDD_USB	UART clear to send active low
37	UART_TX	Bi-directional CMOS output, tri-state, with weak internal pull-up	VDD_USB	UART data output
38	PIO15	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
39	VDD_PADS	VDD	-	Positive supply for all other digital input/output ports.
40	PIO[14]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
41	PIO[6]	Bi-directional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
42	PCM_IN	CMOS input, with weak internal pull down	VDD_PADS	Synchronous data input
43	PCM_CLK	Bi-directional with weak internal pull-up/down	VDD_PADS	Synchronous data clock
44	PCM_OUT	CMOS output, tri-state, with weak internal pull down	VDD_PADS	Synchronous data output
45	PCM_SYNC	Bi-directional with weak internal pull down	VDD_PADS	Synchronous data sync
46	SPI_CSB	Input with weak internal pull-up	VDD_PADS	Chip select for Serial Peripheral interface(SPI), active low
47	SPI_CLK	Input with weak internal pull-down	VDD_PADS	SPI clock
48	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	VDD_PADS	SPI data output
49	SPI_MOSI	CMOS input, with weak internal pull-down	VDD_PADS	SPI data input
50	LED1	Open drain output	-	LED driver
51	LED0	Open drain output	-	LED driver
52	VREGENABLE	Analogue	-	Take high to enable high-voltage linear regulator and switch-mode regulator
53	LX	Switch-mode power regulator output	-	Switch-mode power regulator output
54	VDD_BAT	Battery terminal	-	Lithium ion/polymer battery positive terminal. Battery charge output and input to switch-mode regulator.

Pin #	Pin Name	Type	Supply Domain	Description
55	VDD_CHG	Charge input	Charge input	Lithium ion/polymer battery charger input
56	GND	GND	-	Ground
57	VDD_1V8	VDD	-	1.8V regulated output for analogue /digital circuit
58	GND	GND	-	Ground
59	MIC_BIAS	Analogue	AUDIO_1V5	Microphone bias
60	AUDIO_IN_P_RIGHT	Analogue	AUDIO_1V5	Microphone input positive, right
61	AUDIO_IN_N_RIGHT	Analogue	AUDIO_1V5	Microphone input negative, right
62	AUDIO_IN_P_LEFT	Analogue	AUDIO_1V5	Microphone input positive, left
63	AUDIO_IN_N_LEFT	Analogue	AUDIO_1V5	Microphone input negative, left
64	VDD_MEM	VDD	-	Positive supply for flash pads

All the big pads on the bottom of the module should be tied to ground.

3-3 Bluetooth Pins

3-3-1 Debug SPI Pins

apm8282 / apm8262 have SPI interface for debug primarily. The lab tools, PSTOOL, can communicate with apm8282 / apm8262 BT part using the SPI protocol over a connection to an LPT port.

Debug SPI Name	Pin #	Pin Name	Description
CS#	46	SPI_CSB	Debug SPI chip select, active low
CLK	47	SPI_CLK	Debug SPI clock
MISO	48	SPI_MISO	Debug SPI data output
MOSI	49	SPI_MOSI	Debug SPI data input

3-3-2 UART Pins

apm8282 / apm8262 supports a Universal Asynchronous Receiver Transmitter (UART) interface with programmable baud rate up to 3Mbps. BlueCore Serial Protocol (BCSP), a proprietary alternative to the standard Bluetooth UART Host Transport, is also supported.

UART Bus Name	Pin #	Pin Name	Description
RX	34	UART_RX	UART data input active high
RTS	35	UART_RTS	UART request to send active low
CTS	36	UART_CTS	UART clear to send active low
TX	37	UART_TX	UART data output active high

3-3-3 PCM Pins

apm8282 / apm8262 audio Pulse Code Modulation (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth. The Digital Audio Interface (I2S) shares the same pins as the PCM interface.

Bus Name	Pin #	Pin Name	Description
IN	42	PCM_IN	PCM: PCM2 Synchronous data input I2S: I2S_IN
CLK	43	PCM_CLK	PCM: PCM2 Synchronous data clock I2S: I2S_SCK
OUT	44	PCM_OUT	PCM: PCM2 Synchronous data output I2S: I2S_OUT
SYNC	45	PCM_SYNC	PCM: PCM2 Synchronous data sync I2S: I2S_WS

PCM/I2S/SPDIF interface mapping

3-3-4 USB Pins

This is a full speed (12Mbps) Universal Serial Bus (USB) interface for communicating with other compatible digital devices. apm8282 / apm8262 acts as a USB peripheral, responding to requests from a master host controller.

Please be noted that VDD_USB should be from +3.1V to +3.6V for correct USB operation.

Bus Name	Pin #	Pin Name	Description
DN	30	USB_DN	USB data minus
DP	31	USB_DP	USB data plus

3-3-5 Power Pins

The following list shows the pins referenced to VDD_1V5

Pin #	Pin name		Pin #	Pin name		Pin #	Pin name
3	AUDIO_OUT_N_RIGHT		4	AUDIO_OUT_P_RIGHT		5	AUDIO_OUT_P_LEFT
6	AUDIO_OUT_N_LEFT		17	AIO[1]		19	AIO[0]
60	AUDIO_IN_P_RIGHT		61	AUDIO_IN_N_RIGHT		62	AUDIO_IN_P_LEFT
63	AUDIO_IN_N_LEFT						

The following list shows the pins referenced to VDD_PIO.

Pin #	Pin name		Pin #	Pin name		Pin #	Pin name
10	PIO[0]		11	PIO[1]		15	PIO[3]
16	PIO[2]						

The following list shows the pins referenced to VDD_PADS.

Pin #	Pin name		Pin #	Pin name		Pin #	Pin name
21	PIO[4]		22	PIO[5]		23	PIO[7]
24	PIO[8]		25	PIO[12]		26	PIO[13]
27	PIO[10]		28	PIO[11]		29	PIO[9]
38	PIO[15]		40	PIO[14]		41	PIO[6]
42	PCM_IN		43	PCM_CLK		44	PCM_OUT
45	PCM_SYNC		46	SPI_CSB		47	SPI_CLK
48	SPI_MISO		49	SPI_MOSI			

The following list shows the pins referenced to VDD_USB.

Pin #	Pin name		Pin #	Pin name		Pin #	Pin name
30	USB_DN		31	USB_DP		34	UART_RX
35	UART_RTS		36	UART_CTS		37	UART_TX

3-3-6 I/O Parallel Ports

Sixteen lines of programmable bi-directional input/output (I/O) are provided. PIO[15:4] are powered from VDD_PADS. PIO[3:0] are powered from VDD_PIO. AIO[1:0] are powered from VDD_1V5.

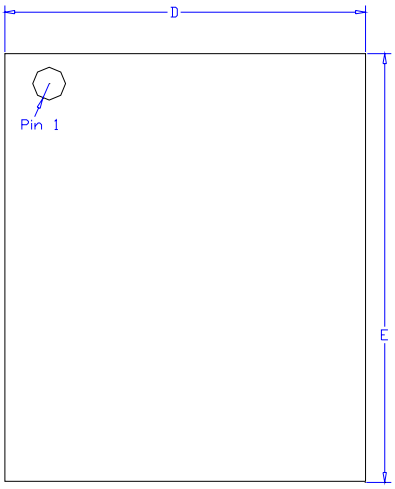
The GPIO pins are used to implement user defined input and output signals to and from the module such as external interrupts, LED controlled outputs, and other user-defined I/Os. Each GPIO can be independently controlled

- PIO0: For class1 application control pin.
- PIO1: For class1 application control pin
- PIO5: a single BT_ Priority output of 2-wire scheme
- PIO7: a single WLAN_ active input of 2-wire scheme
- Other PIOs: reserved

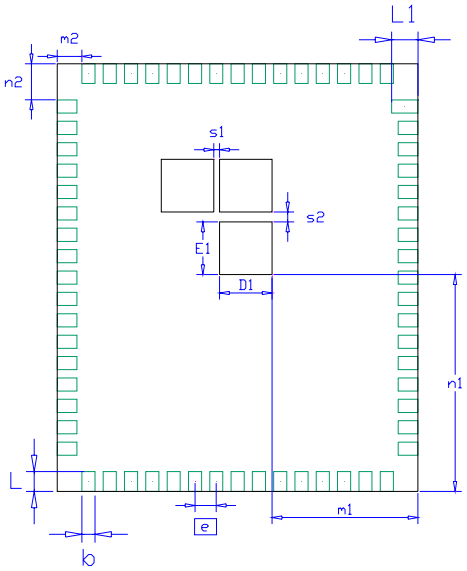
4 Mechanical Specification

Dimension	11×13×1.9mm
Weight	0.621g
Pinout	64pin
Antenna	External single antenna support (Pin 8)

4-1 Package Outline



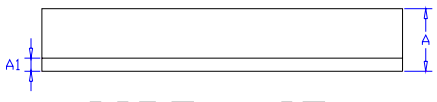
<TOP VIEW>



<BOTTOM VIEW>

Unit:mm

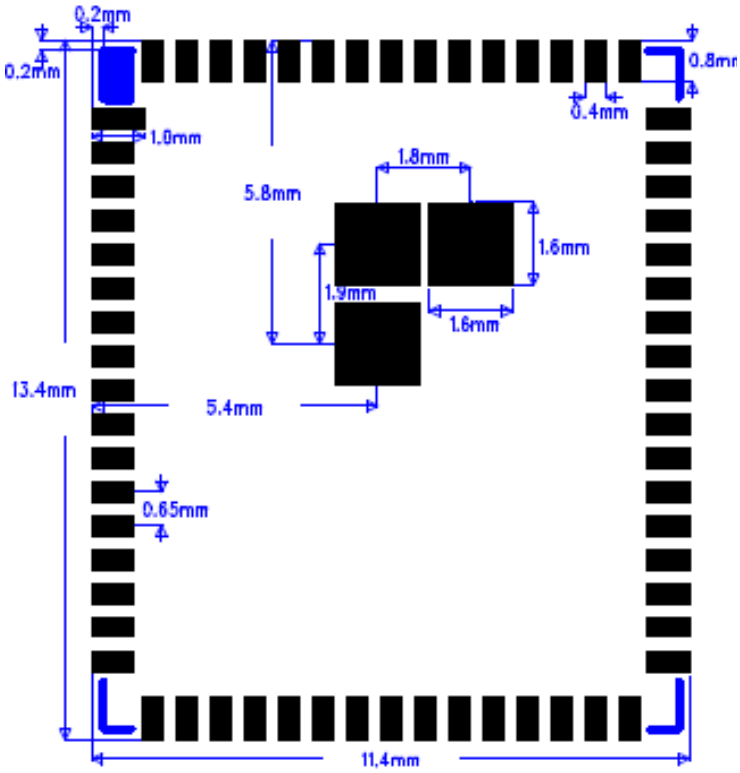
Symbol	Min	Nor	Max
D	10.9	11.0	11.1
E	12.9	13.0	13.1
D1	1.5	1.6	1.7
E1	1.5	1.6	1.7
m1	4.35	4.45	4,55
n1	6.49	6.59	6.69
m2	0.7	0.75	0.8
n2	1.04	1.09	1.14
e	-	0.65	-
L	0.55	0.6	0.65
L1	0.75	0.8	0.85
b	0.35	0.4	0.45
s1	0.13	0.18	0.23
s2	0.25	0.3	0.35
A	-	-	1.9
A1	-	-	0.4



<SIDE VIEW>

5 Assembly Guideline

5-1 Recommended Mounting Pad Design (Top View)



Unit: mm

PCB METAL LAND (TOP VIEW)

5-2 Recommendation for Stencil Aperture in SMT Process

Please follow general QFN stencil design guideline. Some rules of thumb are highlighted below.

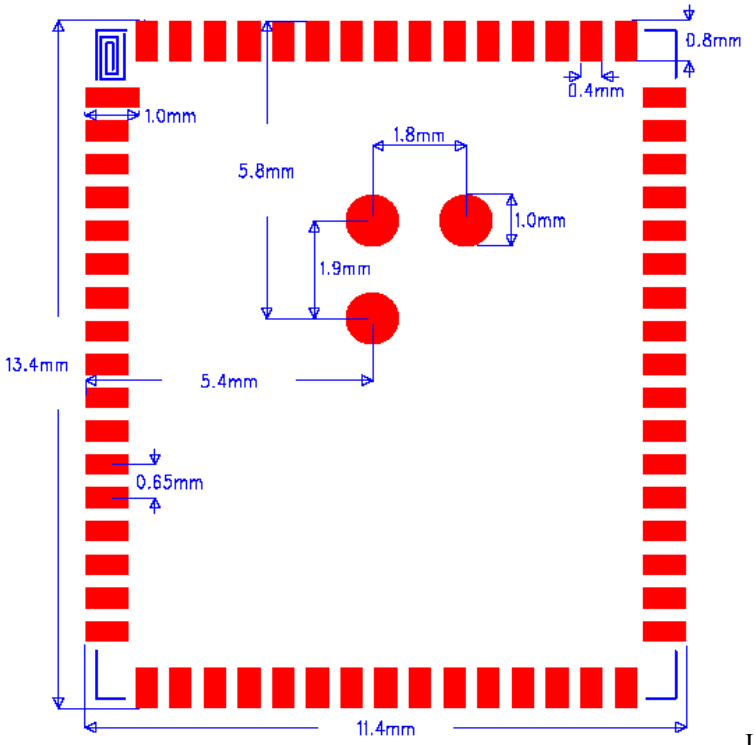
• The LGA pads should NOT be flooded over with copper, they should be connected into the plane with a track width of approx 50% of the pad width, this will mean more heat will be available at the joint. Track lengths should obviously be minimized, we would generally use about 0.3mm on external layers.

• The solder paste pattern for the internal Tab pads could be split into 4 smaller segments for the 2 large pads, and 2 smaller segments for the smaller pads, this should have the effect of preventing the paste from pooling into one area, and hence minimize the likelihood of the pads being held away from each other. We use a rule of thumb of 50% solder paste area in relation to Tab copper area (this only applies to tab pads under the device – not the signal pads).

• The thickness of the solder paste stencil has implications on solder joint quality as well, we do not have the knowledge on what stencil should be specified.

• Ensure they are using a good appropriate flux, and the correct reflow profile for unleaded (basically +20C above leaded) which is also uniform in nature.

Violating the basic rules might cause problems. For example, if the stencil apertures of the internal ground planes are improperly big, they would hold more solders in SMT process and may cause the module peripheral pads un-contacted to the main board. To improve this situation, apm suggests the stencil opening shown as follows.



Unit: mm

STENCIL APETURE (TOP VIEW)

5-3 Baking condition recommendation before IR reflow

Baking condition for apm8282 / apm8262 module:

I: 125℃/4 hrs baking is necessary for apm8282 / apm8262 module before SMT process. After baking treatment the modules can be stored in the environment under 30℃ and 60% RH for 168 hrs. If the storage time is over 168 hrs, the modules need to be re-baked using the same condition again.

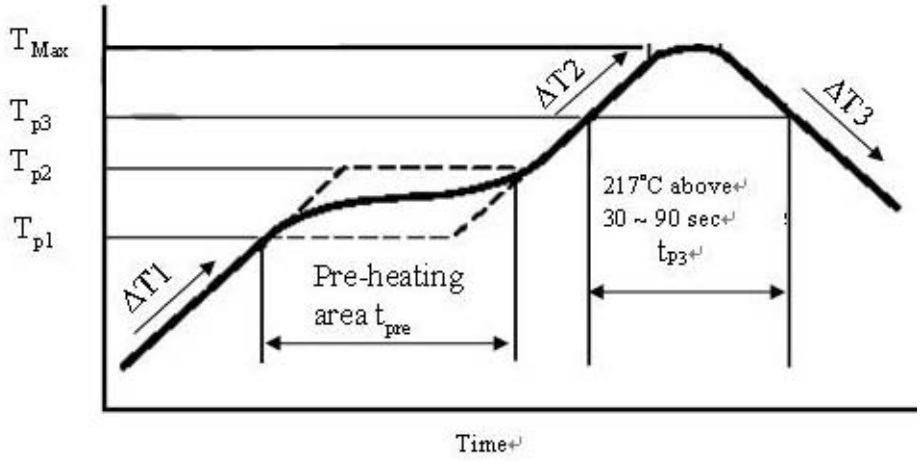
II: In the event that the sealed bag is damaged on receipt of the modules, the baking condition should be changed to 125℃/8 hrs.

5-4 Recommended Temperature Reflow Profile

The solder profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow.

Maximum reflow temperature is 250℃

Preheat ramp-up rate	125℃ to 180℃ 1 to 3℃/ sec.
Peak temperature	250℃, Max.
Temperature maintained above 217℃	30 ~ 90 sec.
Cooling ramp-down rate	<2℃/ sec.
Maximum number of reflow cycles	≤3



Heating/Cooling Speed			Pre-Heating		Heating	
ΔT1	ΔT2	ΔT3	T_{p1}–T_{p2}	t_{pre}	T_{Max}	t_{P3}
1 to 3℃/sec.	1 to 3℃/sec.	< 2℃/sec.	125 ~ 180℃	30 ~ 90 sec.	250℃, Max.	30 ~ 90 sec.

6 Order Information

Order Number	Package Size	Description
apm8282	11 × 13 × 1.9 mm	8Mbit Flash memory embedded
apm8262	11 × 13 × 1.9 mm	16Mbit Flash memory embedded