

## Integrated Backup Unit

### Features

- Power monitoring, backup supply, and switching for 3V battery-backup applications
- Write-protect control
- Input decoder for control of up to 2 banks of SRAM
- 3-volt backup power output
- Internal 130mAh lithium-coin cell
- Reset output for system power-on reset
- Less than 10ns chip-enable propagation delay
- 5% or 10% supply operation

### General Description

The CMOS bq2502 Integrated Backup Unit provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V VCC input for an out-of-tolerance condition. When out of tolerance is detected, the two conditioned chip-enable outputs are forced inactive to write-protect both banks of SRAM.

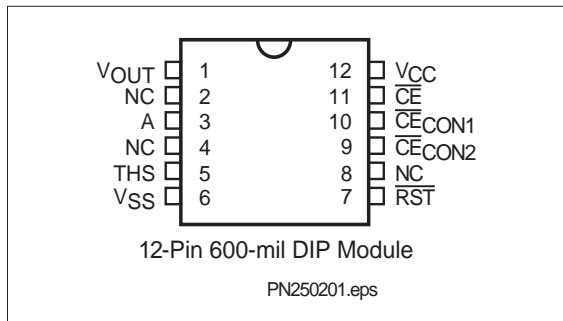
Power for the external SRAMs is switched from the VCC supply to the internal battery-backup supply as VCC decays. On a subsequent power-up, the VOUT supply is automatically switched from the internal lithium supply to the VCC supply.

The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

The internal lithium cell is initially electrically isolated, protecting the battery from accidental discharge. Connection to the battery is made only after the first application of VCC.

### Pin Connections



### Pin Names

V <sub>OUT</sub>	Supply output
R <sub>ST</sub>	Reset output
THS	Threshold select input
CE	chip-enable active low input
CE <sub>CON1</sub> , CE <sub>CON2</sub>	Conditioned chip-enable outputs
A	Bank select input
NC	No connect
V <sub>CC</sub>	5-volt supply input
V <sub>SS</sub>	Ground

### Functional Description

Two banks of CMOS static RAM can be battery-backed using the V<sub>OUT</sub> and conditioned chip-enable output pins from the bq2502. As the voltage input V<sub>CC</sub> slews down during a power failure, the two conditioned chip-enable outputs, CE<sub>CON1</sub> and CE<sub>CON2</sub>, are forced inactive independent of the chip-enable input CE.

This activity unconditionally write-protects external SRAM as V<sub>CC</sub> falls to an out-of-tolerance threshold V<sub>PFD</sub>. V<sub>PFD</sub> is selected by the threshold-select input pin, THS. If THS is tied to V<sub>SS</sub>, the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to V<sub>OUT</sub>, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V<sub>SS</sub> or V<sub>OUT</sub> for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t<sub>WPT</sub> (150μs maximum), the two chip-enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

## bq2502

As the supply continues to fall past  $V_{PFD}$ , an internal switching device forces  $V_{OUT}$  to the internal backup energy source.  $\overline{CECON1}$  and  $\overline{CECON2}$  are held high by the  $V_{OUT}$  energy source.

During power-up,  $V_{OUT}$  is switched back to the 5V supply as  $V_{CC}$  rises above the backup cell input voltage sourcing  $V_{OUT}$ . Outputs  $\overline{CECON1}$  and  $\overline{CECON2}$  are held inactive for time  $t_{CER}$  (120ms maximum) after the power supply has reached  $V_{PFD}$ , independent of the  $\overline{CE}$  input, to allow for processor stabilization.

The reset output ( $\overline{RST}$ ) goes active within  $t_R$  (150 $\mu$ s maximum) after  $V_{PFD}$ , and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The  $\overline{RST}$  output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when  $\overline{RST}$  returns inactive.

During power-valid operation, the  $\overline{CE}$  input is passed through to one of the two  $\overline{CECON}$  outputs with a propagation delay of less than 10ns. The  $\overline{CE}$  input is output on one of the two  $\overline{CECON}$  output pins depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup, as shown in Figure 1.

The internal lithium cell is capable of supplying 3V on  $V_{OUT}$  for an extended period. The cumulative length of time that the external SRAMs retain data in the absence of power is a function of the data-retention current of the SRAMs used. The initial capacity of the internal lithium cell is 130mAh. Typically, if the data-retention currents for two external SRAMs are 1 $\mu$ A per SRAM at room temperature, nonvolatility is calculated to be for more than 7 years. If only one external SRAM is used, the data-retention time increases to more than 13 years.

The bq2502 battery life is a function of the time spent in battery-backed mode and the data-retention current of the external SRAM. For example, office equipment is generally powered on for 8 hours and powered off for 16 hours. Under these conditions, a single bq2502 provides SRAMs drawing 2 $\mu$ A total data-retention current with more than 10 years of nonvolatility.

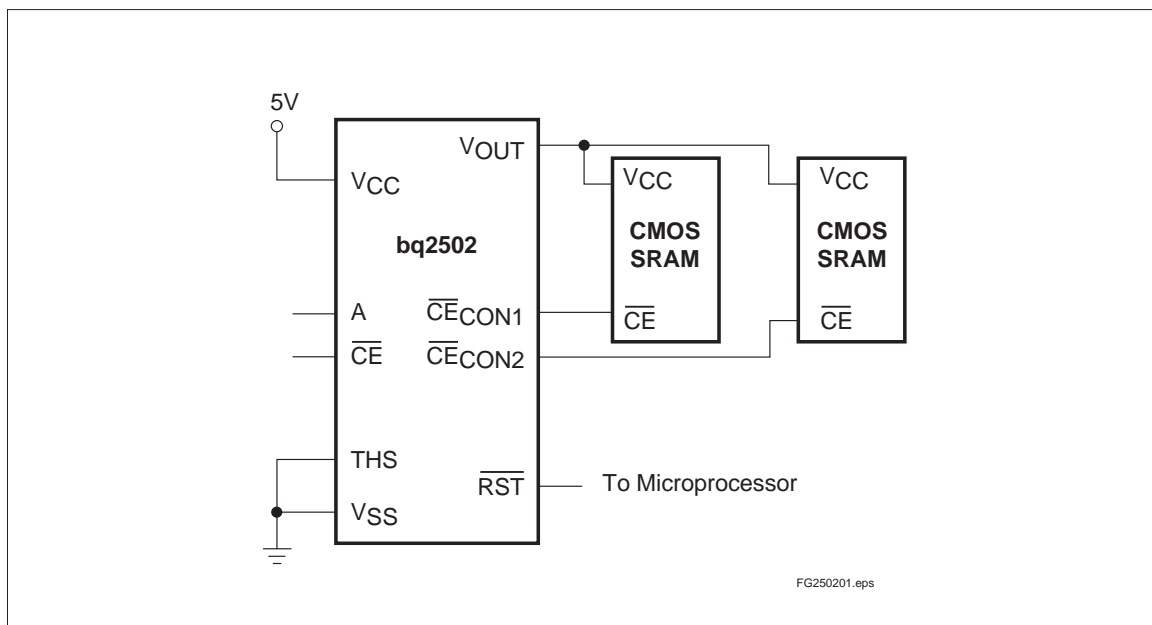


Figure 1. Hardware Hookup (5% Supply Operation)

As shipped from Benchmark, the internal lithium cell is electrically isolated from  $V_{OUT}$ ,  $\overline{CE}_{CON1}$ , and  $\overline{CE}_{CON2}$ . Self-discharge in this condition is less than 0.5% per year at 20°C.

**Note:** Following the first application of  $V_{CC}$ , this isolation is broken, and the backup cell provides power to  $V_{OUT}$ ,  $\overline{CE}_{CON1}$ , and  $\overline{CE}_{CON2}$  for the external SRAM.

**Caution:**

Take care to avoid inadvertent discharge through  $V_{OUT}$ ,  $\overline{CE}_{CON1}$ , and  $\overline{CE}_{CON2}$  after battery isolation has been broken.

This isolation can be reestablished by applying a valid isolation signal to the bq2502. See Figure 2. This signal requires  $\overline{CE}$  low as  $V_{CC}$  crosses both  $V_{PFD}$  and  $V_{SO}$  during a power-down. Between these two points in time,  $\overline{CE}$  must be brought to  $(0.48 \text{ to } 0.52) * V_{CC}$  and held for at least 700ns. The isolation signal is invalid if  $\overline{CE}$  exceeds  $0.54 * V_{CC}$  at any point between  $V_{CC}$  crossing  $V_{PFD}$  and  $V_{SO}$ .

The battery is connected to  $V_{OUT}$  immediately on subsequent application and removal of  $V_{CC}$ .

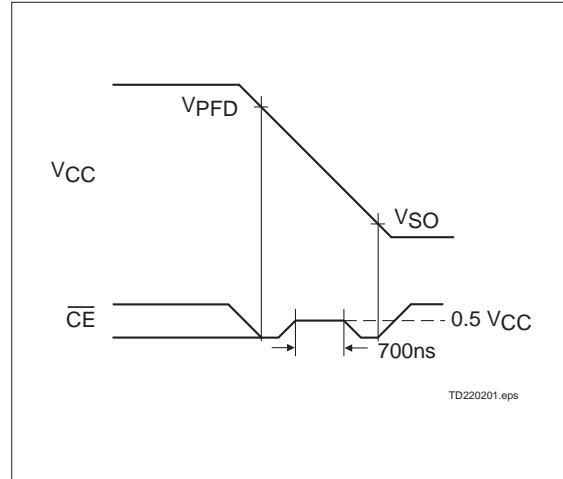


Figure 2. Battery Isolation Signal

**Truth Table**

Input		Output	
$\overline{CE}$	A	$\overline{CE}_{CON1}$	$\overline{CE}_{CON2}$
H	X	H	H
L	L	L	H
L	H	H	L

## bq2502

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### Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V <sub>CC</sub>	DC voltage applied on V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to +7.0	V	
V <sub>T</sub>	DC voltage applied on any pin excluding V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to +7.0	V	V <sub>T</sub> ≤ V <sub>CC</sub> + 0.3
T <sub>OPR</sub>	Operating temperature	0 to 70	°C	
T <sub>STG</sub>	Storage temperature	-40 to +70	°C	
T <sub>BIAS</sub>	Temperature under bias	-10 to +70	°C	
T <sub>SOLDER</sub>	Soldering temperature	260	°C	For 10 seconds
I <sub>OUT</sub>	V <sub>OUT</sub> current	200	mA	

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

### Recommended DC Operating Conditions (T<sub>A</sub> = 0 to 70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V <sub>CC</sub>	Supply voltage	4.75	5.0	5.5	V	THS = V <sub>SS</sub>
		4.50	5.0	5.5	V	THS = V <sub>OUT</sub>
V <sub>SS</sub>	Supply voltage	0	0	0	V	
V <sub>IL</sub>	Input low voltage	-0.3	-	0.8	V	
V <sub>IH</sub>	Input high voltage	2.2	-	V <sub>CC</sub> + 0.3	V	
THS	Threshold select	-0.3	-	V <sub>CC</sub> + 0.3	V	

**Note:** Typical values indicate operation at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V or V<sub>BAT</sub>.

**DC Electrical Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
C	Battery capacity	-	130	-	mAhr	Refer to graphs in Typical Battery Characteristics section.
I <sub>LI</sub>	Input leakage current	-	-	± 1	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
V <sub>OH</sub>	Output high voltage	2.4	-	-	V	I <sub>OH</sub> = -2.0mA
V <sub>OH(B)</sub>	V <sub>OH</sub> , backup supply	V <sub>BAT</sub> - 0.3	-	-	V	V <sub>BAT</sub> > V <sub>CC</sub> , I <sub>OH</sub> = -10μA
V <sub>OL</sub>	Output low voltage	-	-	0.4	V	I <sub>OL</sub> = 4.0mA
V <sub>BAT</sub>	Internal battery voltage	-	2.9	-	V	Refer to graphs in Typical Battery Characteristics section.
I <sub>CC</sub>	Operating supply current	-	3	6	mA	No load on V <sub>OUT</sub> , $\overline{CE}_{CON1}$ , $\overline{CE}_{CON2}$ , and RST.
V <sub>PF(D)</sub>	Power-fail detect voltage	4.55	4.62	4.75	V	THS = V <sub>SS</sub>
		4.30	4.37	4.50	V	THS = V <sub>OUT</sub>
V <sub>SO</sub>	Supply switch-over voltage	-	2.9	-	V	
I <sub>CC(D)</sub>	Data-retention mode current from internal battery	-	-	100	nA	No load on V <sub>OUT</sub> , $\overline{CE}_{CON1}$ , $\overline{CE}_{CON2}$ , and RST.
V <sub>OUT1</sub>	V <sub>OUT</sub> voltage	V <sub>CC</sub> - 0.2	-	-	V	V <sub>CC</sub> > V <sub>BAT</sub> , I <sub>OUT</sub> = 100mA
		V <sub>CC</sub> - 0.3	-	-	V	V <sub>CC</sub> > V <sub>BAT</sub> , I <sub>OUT</sub> = 160mA
V <sub>OUT2</sub>	V <sub>OUT</sub> voltage from internal battery	V <sub>BAT</sub> - 0.2	-	-	V	V <sub>CC</sub> < V <sub>BAT</sub> , I <sub>OUT</sub> = 100μA, from internal battery
I <sub>OUT1</sub>	V <sub>OUT</sub> current	-	-	160	mA	V <sub>OUT</sub> ≥ V <sub>CC</sub> - 0.3V

**Note:** Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  or  $V_{BAT}$ .

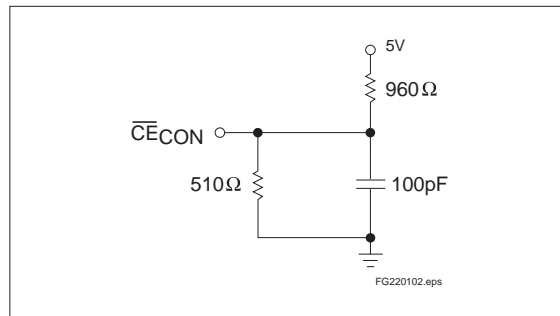
**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $F = 1\text{MHz}$ ,  $V_{CC} = 5.0\text{V}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C <sub>IN</sub>	Input capacitance	-	-	8	pF	Input voltage = 0V
C <sub>OUT</sub>	Output capacitance	-	-	10	pF	Output voltage = 0V

**Note:** This parameter is sampled and not 100% tested.

**AC Test Conditions**

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See Figure 3



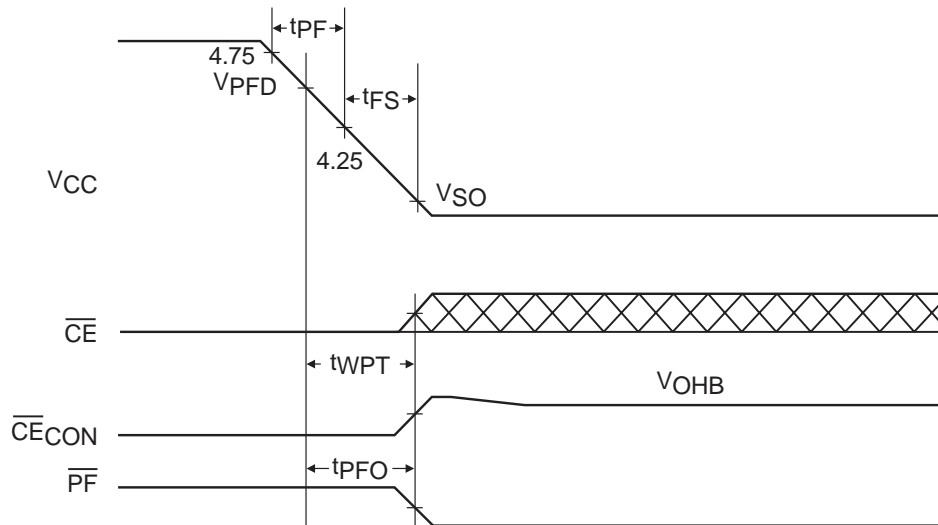
**Figure 3. Output Load**

**Power-Fail Control** ( $T_A = 0$  to  $70^\circ\text{C}$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{PF}$	$V_{CC}$ slew 4.75 to 4.25V	300	-	-	$\mu\text{s}$	
$t_{FS}$	$V_{CC}$ slew 4.25V to $V_{SO}$	10	-	-	$\mu\text{s}$	
$t_{PU}$	$V_{CC}$ slew 4.25 to 4.75V	0	-	-	$\mu\text{s}$	
$t_{CED}$	Chip-enable propagation delay	-	7	10	ns	
$t_{CER}$	Chip-enable recovery time	$t_{RR}$	-	$t_{RR}$	ms	Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up
$t_{RR}$	$V_{PFD}$ to $\overline{RST}$ inactive	40	80	120	ms	Time, after $V_{CC}$ becomes valid, before $\overline{RST}$ is cleared
$t_{AS}$	Input A set up to $\overline{CE}$	0	-	-	ns	
$t_{WPT}$	Write-protect time	$t_R$	-	$t_R$	$\mu\text{s}$	Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is write-protected
$t_R$	$V_{PFD}$ to $\overline{RST}$ active	40	100	150	$\mu\text{s}$	Delay after $V_{CC}$ slews down past $V_{PFD}$ before $\overline{RST}$ is active

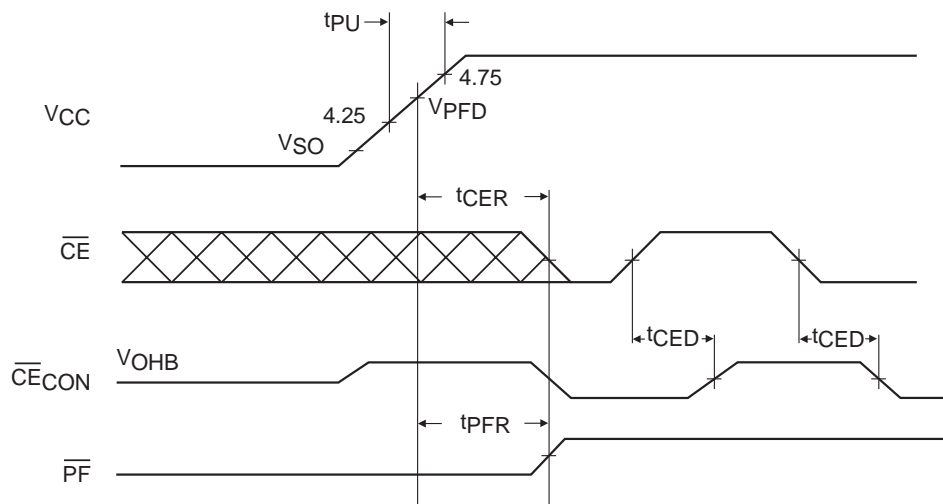
**Note:** Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .

**Power-Down Timing**



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**Power-Up Timing**

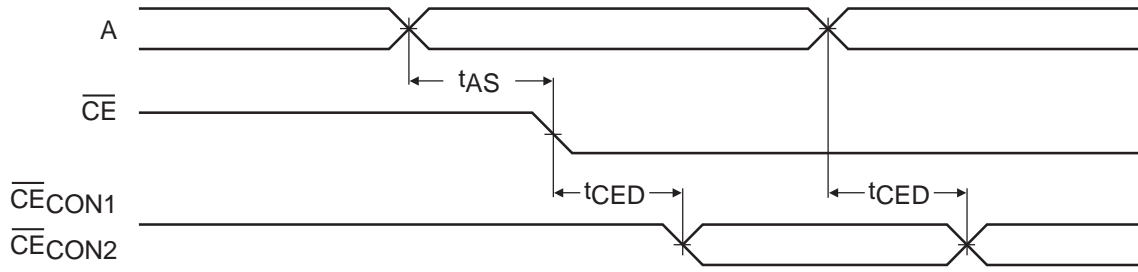


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## Address-Decode Timing

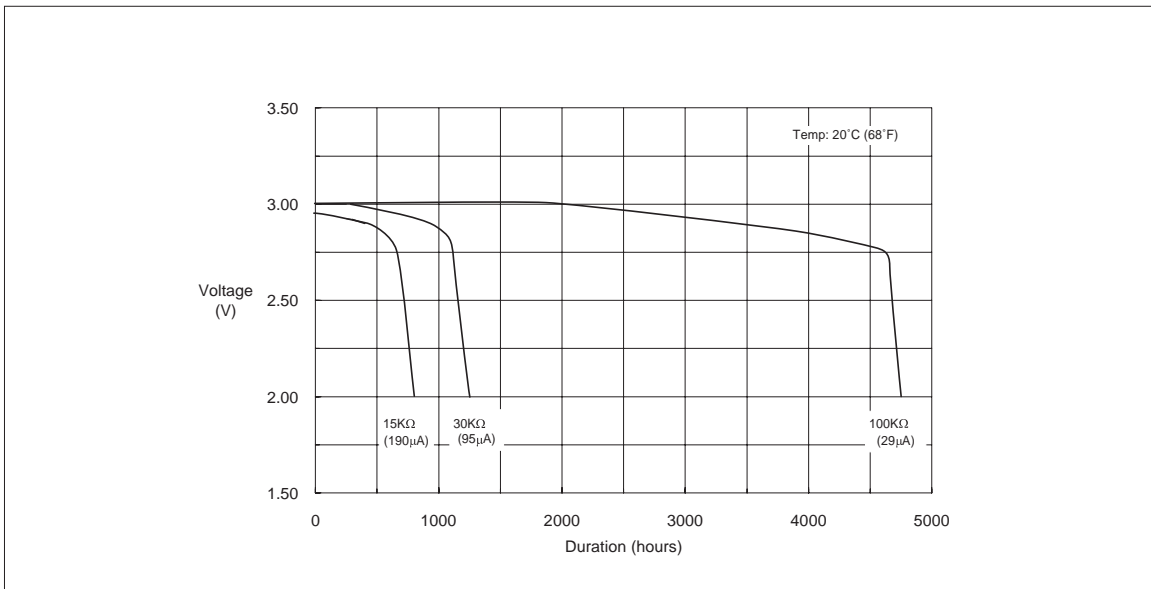


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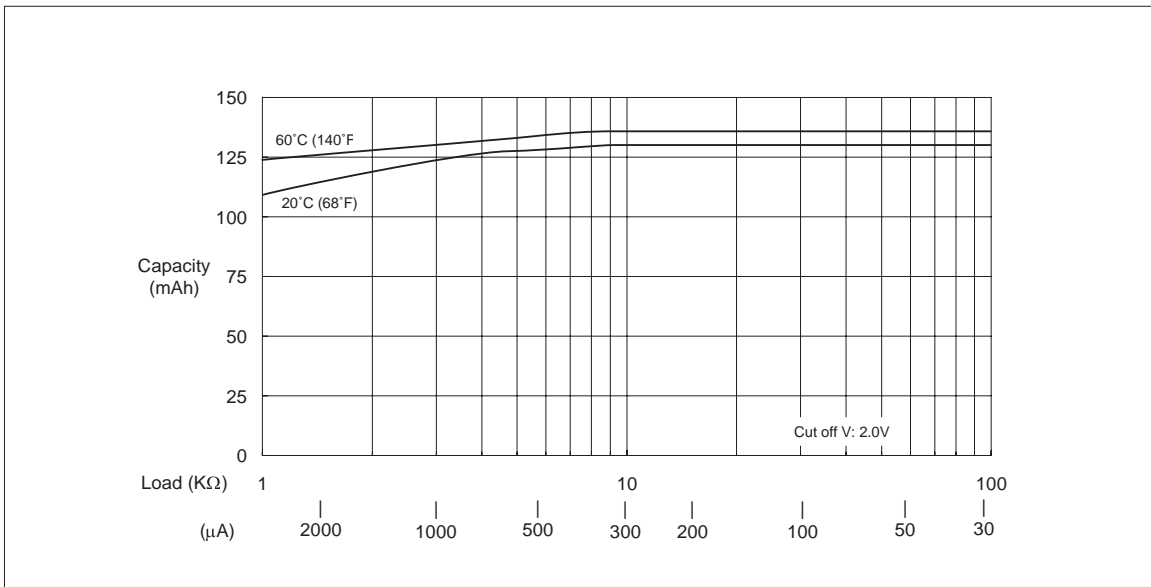


Typical Battery Characteristics (source = Panasonic)

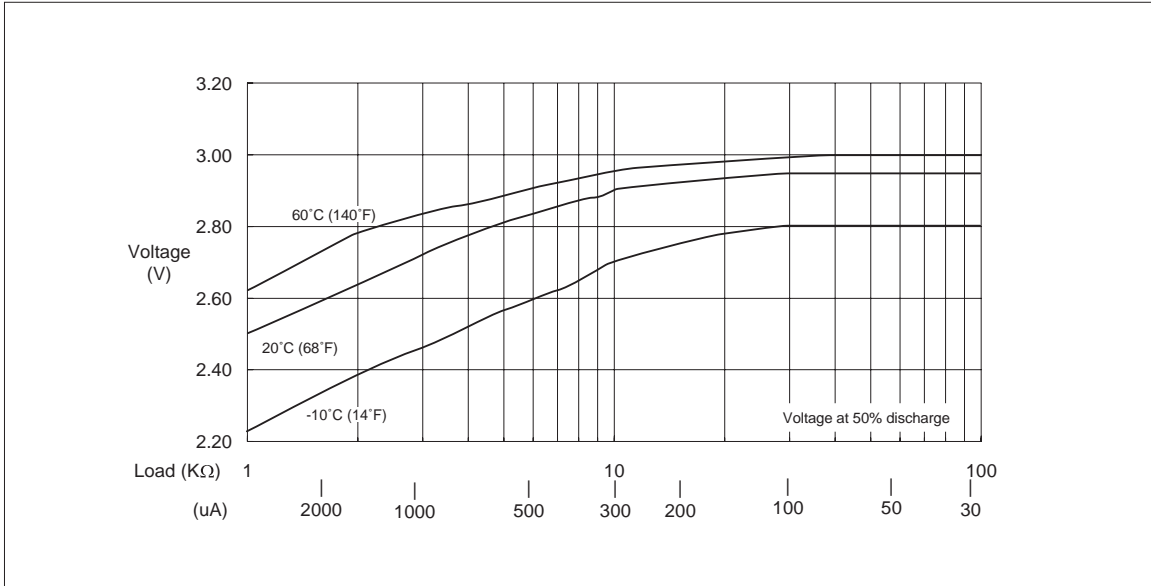
CR1632 Load Characteristics



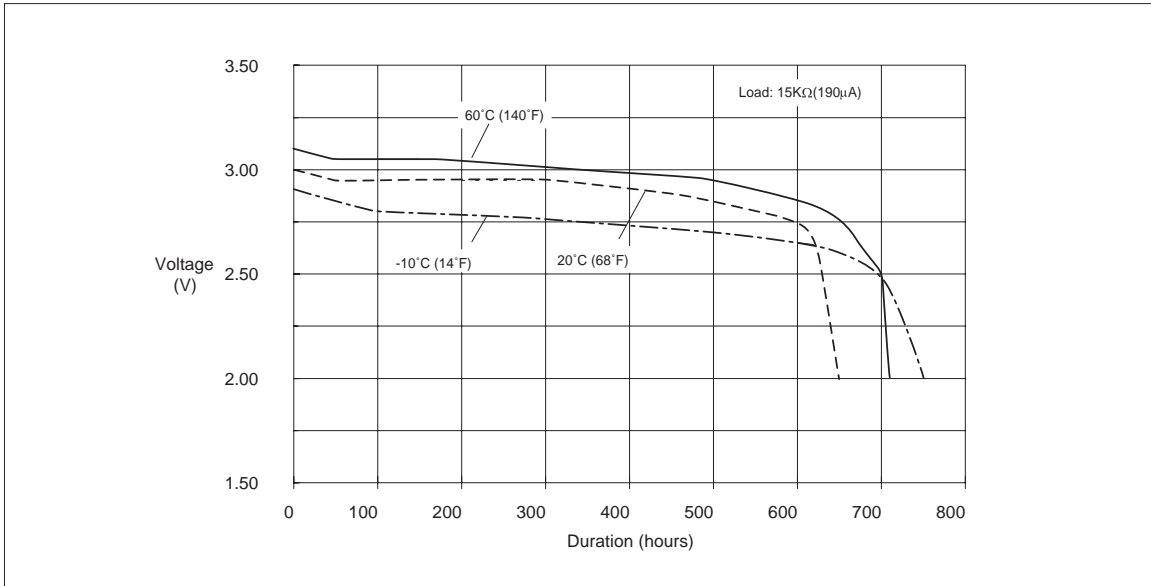
CR1632 Capacity vs. Load Resistance



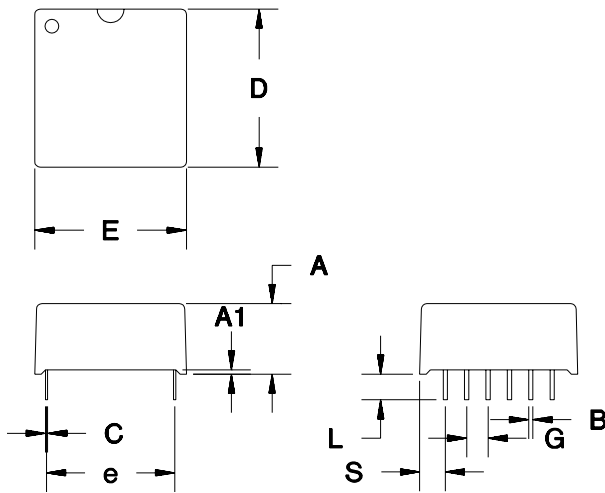
### CR1632 Operating Voltage vs. Load Resistance



### CR1632 Temperature Characteristics



12-Pin Module

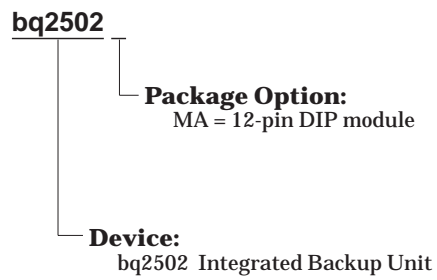


12-Pin Module (MA)

Dimension	Minimum	Maximum
A	0.365	0.375
A1	0.015	-
B	0.017	0.023
C	0.008	0.013
D	0.710	0.740
E	0.710	0.740
e	0.590	0.630
G	0.090	0.110
L	0.120	0.150
S	0.105	0.130

All dimensions are in inches.

Ordering Information



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