eSLS Series

16 Bits DSP
Sound Processor

Product Specification

DOC. VERSION 1.7

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
1.0	1. Modified the Pin description in Section 6 2. Modified the Operating Temperature Range in Section 7.2	2006/10/31
1.1	1. Modified the Application Circuits diagram in Section 7 2. Modified the Selection Table in Section 4 3. Modified the Boot SPI in Section 5 4. Modified Application Circuit in Section 8 5. Modified the Sampleing Rate Range in Section 4 6. Added the IOVDD, IOVSS, AVDD, AVSS in Section 6.1	2007/04/13
1.2	1. Modified the Temperature Range in Section 7.2 2. Added algorithm support such as speech control and pitch control in Section 2 and 4	2007/08/10
1.3	1. Added package information 2. Modified Application Circuit in Section 8	2007/11/10
1.4	1. Modified PWM current in Section 6.3	2008/01/10
1.5	1. Modified Application Circuit in Section 8 2. Modified Algorithm support in Section 2 and 4	2008/10/15
1.6	1. Added Algorithm-relative section in Section 5	2009/04/15
1.7	1. Modified Application Circuit in Section 9	2009/12/01

1 General Description

The ELAN eSLS Series IC is a 16-bit DSP Sound Processor with multi-channel speech and instrument playback. It is based on ELAN 16-bit DSP platform. The series has a powerful 16-bit DSP architecture that handles most of the speech/ melody functions. Speech and melody can be played back simultaneously. The speech synthesis is implemented by software and supports a wide range of compression bit rates and various volume levels. The ELAN eSLS Series provides real instrument waveform to obtain good quality melody. The ELAN eSLS peripheral includes RTC, Timer, WDT, DAC, PWM, etc.

The ELAN eSLS Series IC's offer Fast mode, Sleep mode, Green mode, and Slow mode of operation. The use of Green/Slow mode will further reduce the power consumption. Green mode also provides RTC function for wake-up purposes.

The ELAN eSLS Series enhanced features make it suitable for versatile voice and sound effect product applications. These enhanced versatile features allow users to create products with a wide variety of new fancy ideas.

The ELAN eSLS Series have extreme high performance in speech application based on powerful DSP architecture and good algorithm in audio compression.

2 Features

- MCU
  - 16-bit RISC CPU architecture
  - CPU clock**:** 20 MHz @ 3.3V
  - Programmable PLL
  - Four CPU operation modes: fast, slow, green, sleep
  - Powerful DSP Instruction Set supports multiplication, division, repeat, loop and soft interrupt instructions
  - Saturation mode is supported for multimedia applications
  - Eight general purpose registers (GPR)
  - 18 interrupt sources with 2-level priority
- Memory
  - 32K-word program memory
  - 2K-word data RAM
  - 128/256/512K-word data ROM
- Peripherals
  - Real Time Clock (RTC) with wake-up function
  - Four 8-bit timers, two general purpose timers, two multiple-function timers
  - 8-bit Watchdog Timer (WDT) with general purpose timer capability
  - 24 GPIO
  - 12-bit current-steering Digital to Analog Converter (DAC)
  - 10-bit resolution Pulse Width Modulation (PWM)

3 Block Diagram

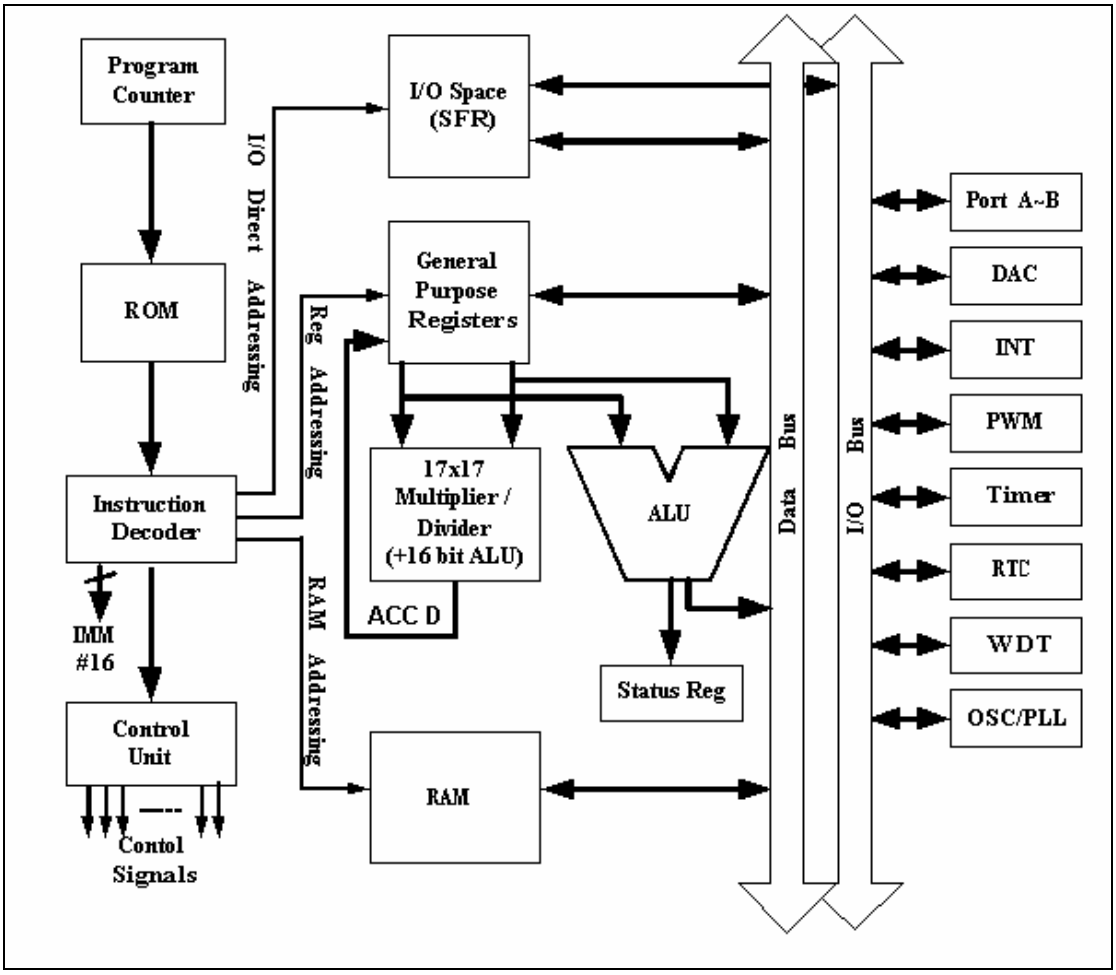


Figure 3-1 ELAN eSLS System Block Diagram

4 Selection Table

The ELAN eSLS Series integrates an extensive range of features, most of which are common to all devices, except for some distinctive features like Data ROM and Coding Type. For user convenience in the choice of the most suitable product for their application, the following table is provided, which enumerates the main features of each device.

Product No.	eSL128S	eSL256S	eSL512S
Pin Count	45		
Program ROM	32K × 16		
Data RAM	2K ×16		
Data ROM	128K×16	256K×16	512K×16
Timer	4 × 8-bit timers		
Watchdog	Yes		
PWM	10-bit		
Current D/A	12-bit		
I/O	24 I/O ports		

Product No.	eSL128SA*	eSL256SA*	eSL512SA*
Pin Count	45		
Program ROM	32K × 16		
Data RAM	2K ×16		
Data ROM	128K×16	256K×16	512K×16
Timer	4 × 8-bit timers		
Watchdog	Yes		
PWM	10-bit		
Current D/A	12-bit		
I/O	24 I/O ports		

* The product number “A” means advanced audio algorithm supported.

5 Algorithm Selection Table

The ELAN eSLS Series algorithm feature:

- Built-in software voice synthesizer (0.8K ~ 96Kbps@8kHz)
- Multiple flash with volume level option
- Directly controls port output value by waveform (waveform control port)
- Supports mark number in waveform with ROM optimized configuration
- Up to 2-channel speech with different channel sample rate or 1-channel speech + 8-channel melody
- Support speed control to adjust playback speed
- Support pitch control to change voice pitch

Product No.	eSL128S	eSL256S	eSL512S
Audio**	Up to 2-channel speech with different channel sample rate or 1-channel speech + 8-channel melody		
Coding Type**	12K/16K/20K/24K/32K/40K bps @ 8KHz		
Sampling Rate Range**	6kHz ~ 48KHz		

Product No.	eSL128SA*	eSL256SA*	eSL512SA*
Audio**	Up to 2-channel speech with different channel sample rate or 1-channel speech + 8-channel melody		
Coding Type**	0.8K~96K bps @ 8KHz		
Sampling Rate Range**	6kHz ~ 48KHz		
Speech Speed/Pitch Control	Yes		

* The product number “A” means advanced algorithm supported. A series support vocal high compress application.

** For more detailed information, refer to the Assembler Reference Manual, C Macro Reference Manual and related Application note.

6 eSLS and eSL Series Comparison

Product No.	eSLZ000	eSL	eSLS
JTAG ICE	Yes	No	No
Boot SPI	Yes	No	No
Total I/O number	48 I/O	48 I/O	24 I/0 (Port A + Port B0~7)
Large Current I/O number	8+4	8+4	4 (Port A 12~15)
Wake-up Pin	16+5	16+5	8+4
SPI	Yes	Yes	No
MIC Front-end AGC	Yes	Yes	No
ADC	Yes	Yes	No

7 Pin Description

7.1 Power Supply

Name	Type	Supply Voltage	Description
VDD_CPU	P	3V	Positive power supply for CPU, digital peripheral and DRAM
VDD_PM	P	3V	Positive power supply for PROM, DROM and POR
VDD_OSC	P	3V	Positive power supply for Oscillator system and PLL
IOVDD_PWM	P	3V, 5V	Positive power supply for PWM I/O pad
IOVDD_PB	P	3V, 5V	Positive power supply for Port A.2~15 and Port B I/O pad
IOVDD*	P	3V, 5V	Positive power supply
VSS_CPU	P	GND	Negative power supply for CPU, digital peripheral and DRAM
VSS_PM	P	GND	Negative power supply for PROM, DROM and POR
VSS_OSC	P	GND	Negative power supply for Oscillator system and PLL
IOVSS_PWM	P	GND	Negative power supply for PWM I/O pad
IOVSS_PB	P	GND	Negative power supply for Port A.2~15 and Port B I/O pad
IOVSS*	P	GND	Negative power supply
AVDD_DA	P	3V	Positive power supply for D/A
AVDD**	P	3V	Positive power supply
AVSS_DA	P	GND	Negative power supply for D/A
AVSS**	P	GND	Negative power supply
RVIN	P	5V	Regulator voltage input
RVOUT	P	3V	Regulator voltage output 3.0V

* These power pins must connect to the same VDD and VSS as IOVDD_PB and IOVSS_PB

** These power pins must connect to the same VDD and VSS as AVDD_DA and AVSS_DA

7.2 System Control

Name	Type	Description
RSTB	I	RSTB is the low active global reset input *
TEST	I	Test mode select pin (High active). Internal pull down. For chip internal test only. Normally connect to VSS.
OSCI	I	Crystal or RC oscillator connecting pin RC or Crystal selection is by OSCS pin
OSCO	O	Crystal oscillator connecting pin
OSCS	I	RC or Crystal selection: **0** = RC **1** = Crystal
PLLC	I	PLL loop filter capacitor **

* This pin has an internal pull-up 150KΩ resistor, refer to the Application Circuit.

** This pin must connect a 47nF capacitor to ground, refer to the Application Circuit.

7.3 DAC Output

Name	Type	Description
DACO	O	Current D/A output pin

7.4 I/O Port

- Port A Attributes and Definitions

Name	Function	Type	Description
PA[0]	GPIO	I/O	General-purpose I/O function
	PWM0	O	PWM Output 0
PA[1]	GPIO	I/O	General-purpose I/O function
	PWM1	O	PWM Output 1
PA[2]	GPIO	I/O	General-purpose I/O function
PA[3]	GPIO	I/O	General-purpose I/O function
PA[4]	GPIO	I/O	General-purpose I/O function
	TEX12	I	External Timer 2 clock input
PA[5]	GPIO	I/O	General-purpose I/O function
	TEX13	I	External Timer 3 clock input
PA [6]	GPIO	I/O	General-purpose I/O function
PA [7]	GPIO	I/O	General-purpose I/O function
PA [8]	GPIO	I/O	General-purpose I/O function
	TCCP2	I/O	Timer 2 capture input or compare output
PA [9]	GPIO	I/O	General-purpose I/O function
	TCCP3	I/O	Timer 3 capture input or compare output
PA [10]	GPIO	I/O	General-purpose I/O function
	EXINT0	I	External Interrupt 0 input
PA [11]	GPIO	I/O	General-purpose I/O function
	EXINT1	I	External Interrupt 1 input
PA [12]	GPIO	I/O	General-purpose I/O function with programmable high current
PA [13]	GPIO	I/O	General-purpose I/O function with programmable high current
PA [14]	GPIO	I/O	General-purpose I/O function with programmable high current
PA [15]	GPIO	I/O	General-purpose I/O function with programmable high current

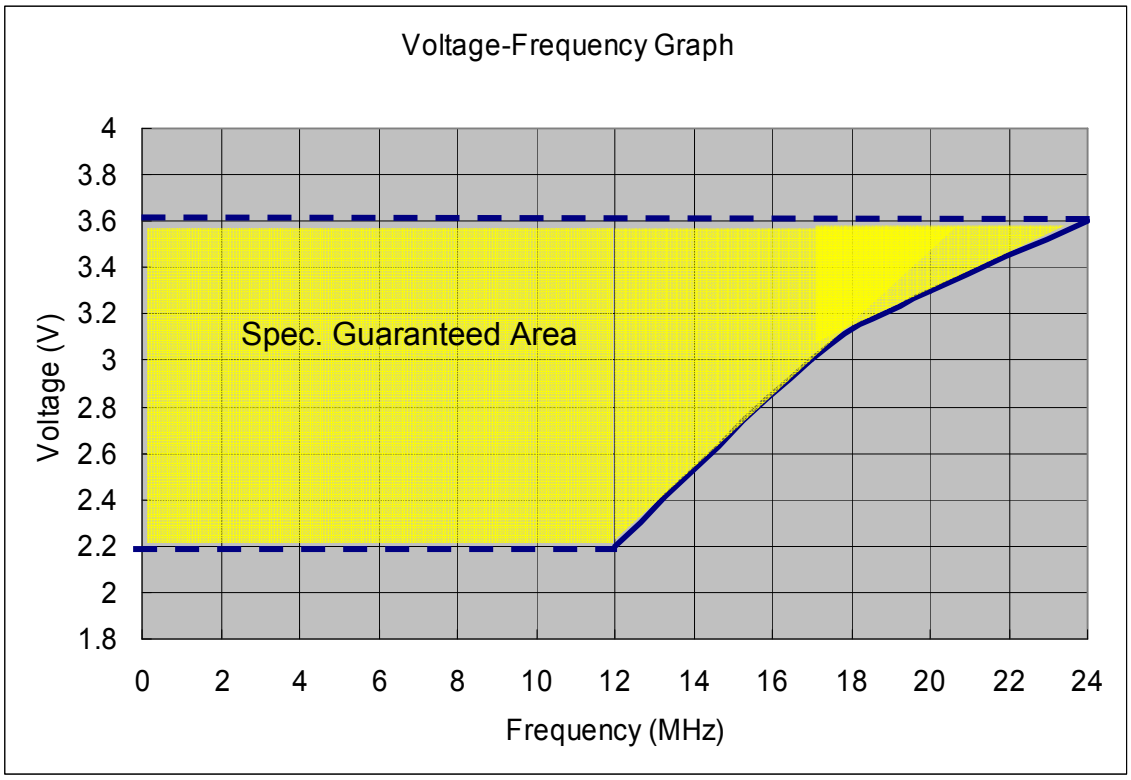
- Port B Attributes and Definitions

Name	Function	Type	Description
PB [7:0]	GPIO	I/O	General-purpose I/O function
		I	Wake-up function with programmable pull-up resistor

8 Electrical Characteristics

8.1 CPU Voltage – Frequency Graph

The speed of a MOS device depends on voltage, temperature, and process variation. Performance analysis is based on a combination of these three factors. The central operating condition is characterized at 3.3V, 25°C, and typical process parameters.



8.2 Absolute Maximum Ratings

Parameter	Pins	Symbol	Condition	Rated Value	Unit
Power supply voltage	VDD	V_{DD}	T_A=25°C	-0.3 to +6.0	V
Input voltage	All Input	V_{IN}	T_A=25°C	-0.3 to VDD+0.3	
Operating temperature range	—	T_A	—	-40 to +85	°C
Storage temperature range	—	T_{STR}	—	-65 to +150	

8.3 DC Characteristics

Standard operation conditions: VDD = 3V, GND=0V, T_A = 25°C

Parameter	Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	VDD[1]	V_{DD}	2 batteries	2.2	3.0	3.6	V
			3 batteries	3.6	4.5	5.5	
Input voltage	—	V_{IN1}	—	VDD×0.7	—	VDD	
	—	VI_{N2}	—	0	—	VDD×0.3	
Input threshold voltage (Schmitt Trigger)	—	—	—	0.5×VDD	—	0.75×VDD	
	—	—	—	0.2×VDD	—	0.4×VDD	
Pull-up resistor	/RESET	V_{PU1L}	Vin=GND	500	1000	1500	kΩ
	/RESET	V_{PU1H}	Vin=2V	80	100	120	
Pull-down resistor	TEST	R_{PD}	Vin=1V	80	100	120	

[1]Refer to the User Manual Voltage Regulator section for details.

Parameter	Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Ports A, B output high current	IOH0	I_{OH0}	VDD=3V VOH=2.4V	-2	-3	—	mA
Ports A, B output low current	IOL0	I_{OL0}	VDD=3V VOL=0.4V	2	3	—	
Port A [12:15] high current (HD enabled)	IOH2	I_{OH2}	VDD=3V VOH=2.4V	TBD	TBD	—	
Port A [12:15] low current (HD enabled)	IOL2	I_{OL2}	VDD=3V VOL=0.4V	TBD	TBD	—	
PWM output high current	PWM0 PWM1	I_{PWMH}	VDD=3V VOH=VDD/2 Max. volume	-140	-150	—	
PWM output low current	PWM0 PWM1	I_{PWML}	VDD=3V VOL=VDD/2 Max. volume	140	150	—	
DAC output current	DACO	I_{DAC}	VDD = 2.2 ~ 3.3V	2.5	3	—	
Regulator output high current	RVOUT	I_{OUTH}	RVIN = 4.5V RVOUT = 3.0V Fast, Slow mode	70	—	—	
Regulator output low current	RVOUT	I_{OUTL}	RVIN = 4.5V RVOUT = 3.0V Green, Sleep mode	7	—	—	
Fast mode current consumption increment per MHz	—	I_{FAST}	VDD=3V No load DAC off	—	700	800	µA
Slow mode current consumption	—	I_{SLOW}	VDD=3V No load DAC off	—	70	80	
Green mode current consumption	—	I_{GREEN}	VDD=3V	—	8	10	
Sleep mode current consumption	—	I_{SLEEP}	VDD=3V Regulator on	—	2	—	
			VDD = 3V Regulator off	—	1	1.2	
CPU operation frequency	—	F_{sys}	VDD = 3V	14	16	—	MHz

9 Application Circuits

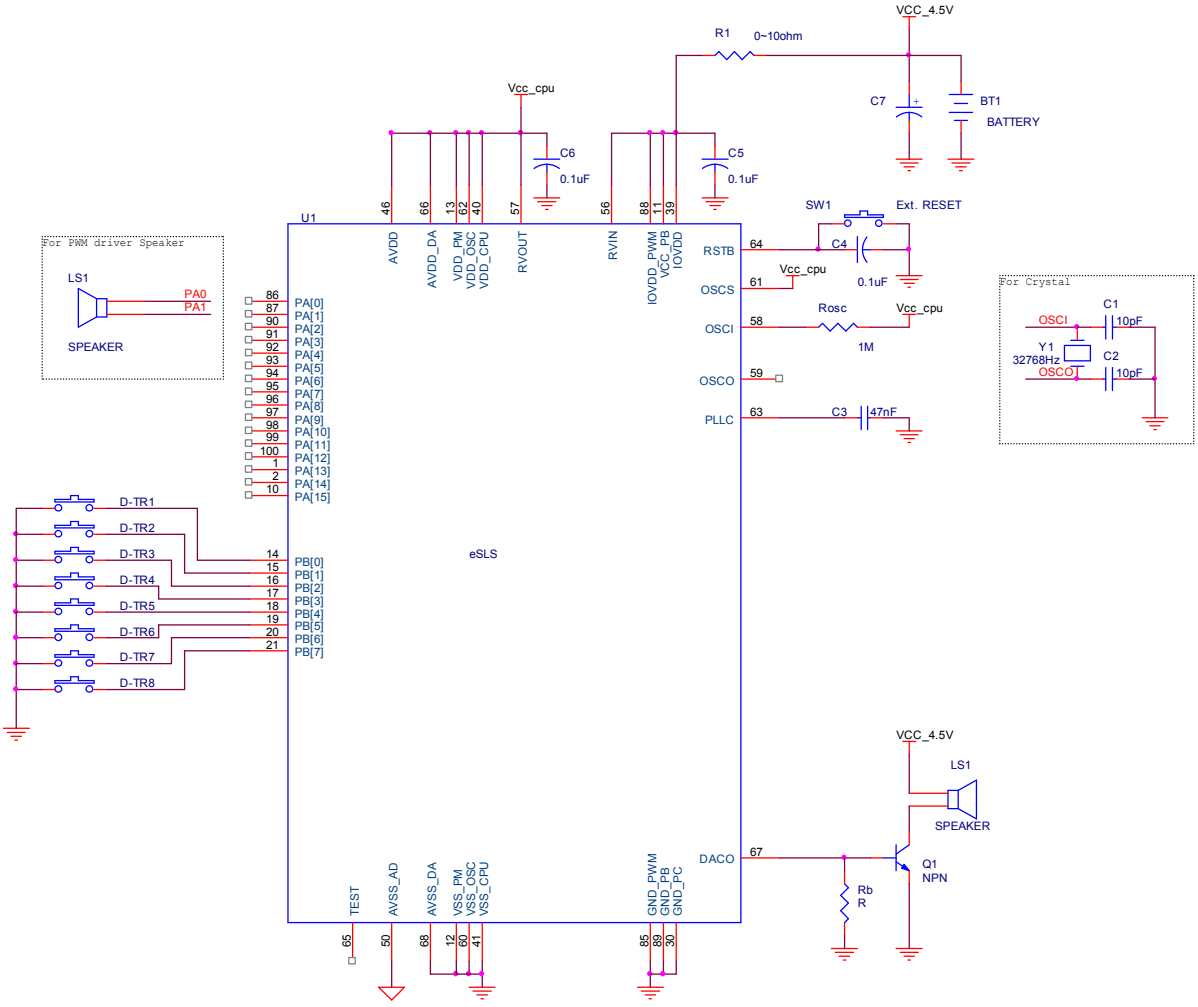


Figure 9-1 ELAN eSLS Series Application Circuit Diagram with D/A using BJT, RC OSC OR Crystal OSC, and PWM for 3V/4.5V Support

NOTE

For different package type, the system characteristic issue such as power consumption due to IO pad floating must controlled by software. For example, if user don't bonding IO pad, you must set IO pad type is input with pull-up resister or output to prevent power consumption.