ft2725

2X11W Stereo Class-D Audio Power Amplifier with ALC & DRC

GENERAL DESCRIPTION

The ft2725 is a highly efficient 2X11W stereo Class-D audio power amplifier with automatic level control (ALC) and dynamic range compression (DRC). It operates with a wide range of supply voltages from 3.7V to 9V. When powered with 9V supply voltage, the ft2725 is capable of delivering 11W per channel into a pair of 4Ω speakers in a bridge-tied-load (BTL) configuration, or 15W into a single 3Ω speaker in parallel BTL (PBTL) configuration, with 10% THD+N.

The ft2725 features ALC with an adjustable threshold for dynamic range control (DRC). The ALC constantly monitors and safeguards the audio outputs against a user-defined threshold voltage, preventing output clipping distortion, excessive power dissipation, or hazardous speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifiers proportionally to eliminate output clipping while maintaining a maximally-allowed dynamic range of the audio outputs. The threshold voltage of the ALC can be set at either the supply voltage or an externally defined value.

As a filterless Class-D audio amplifier, the ft2725 features high efficiency (up to 89%), high PSRR (76dB at 1kHz), and low EMI emissions, which reduce design and manufacturing complexities, lower system cost and PCB space.

In ft2725, comprehensive protection features against various operating faults ensure its safe and reliable operation.

FEATURES

- Wide supply voltage range from 3.7V to 9V
- Automatic level control with adjustable threshold
- High efficiency up to 89%
- Maximum output power in Non-ALC mode
  (VDD=9V, VALC≥0.8*GVDD, 10% THD+N)
  6W/Ch (8Ω load)
  11W/Ch (4Ω load)
  15W (3Ω load in PBTL configuration)
- ALC output power in ALC Mode
  (VDD=9V, VALC=0V, 0.3% THD+N)
  4.5W/Ch (8Ω load)
  8.5W/Ch (4Ω load)
  11.5W (3Ω load in PBTL configuration)
- Low THD+N: 0.06%
  (VDD=9V, f=1kHz, 4Ω load, Po=5W)
- High PSRR: 76dB @ 1kHz
- Wide ALC dynamic range: 10dB
- Maximum voltage gain: 32.4dB
- Volume fade-in and fade-out
- Optional spread-spectrum (SS) audio outputs to suppress EMI
- Optional mono mode for PBTL configuration with low-impedance audio speakers
- Auto-recovering over-current & short-circuit protection
- Available in TSSOP-24L package

APPLICATIONS

- Blue Tooth Speakers
- Performance Audio Speakers
- TV/Monitors

APPLICATION CIRCUIT

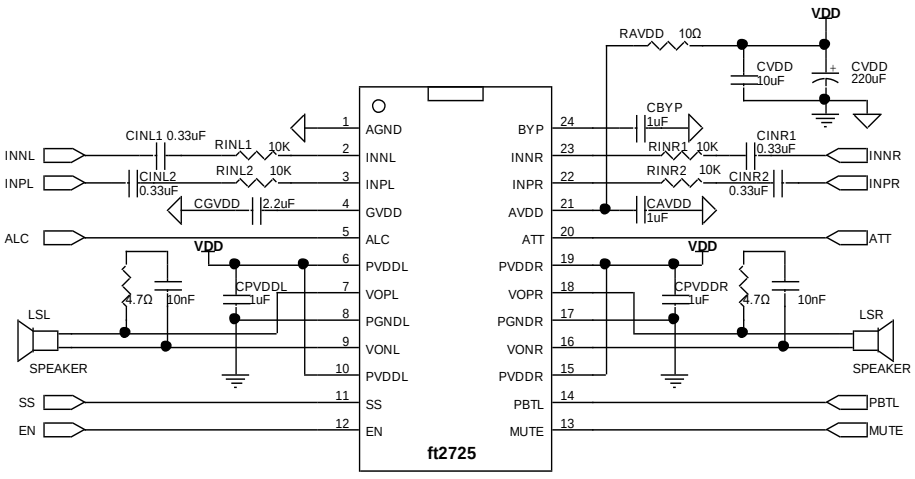
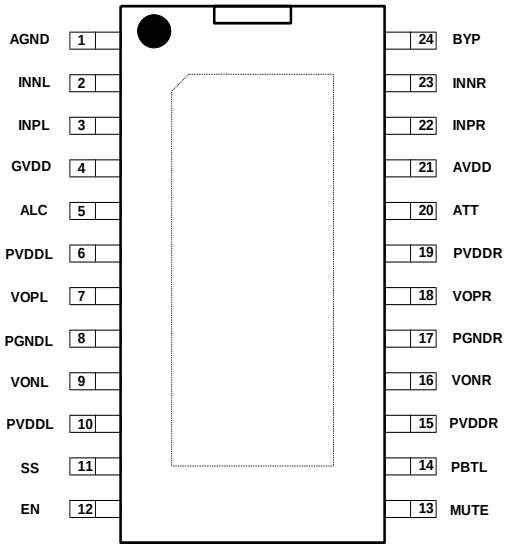


Figure 1: Typical Audio Power Amplifier Application Circuit

PIN CONFIGURATION AND DESCRIPTION



ft2725P (TOP VIEW)

NAME	PIN #	TYPE	DESCRIPTION
AGND	1	G	Analog ground. Connect to the system ground GND.
INNL	2	AI	Left-channel inverting audio input terminal.
INPL	3	AI	Left-channel non-inverting audio input terminal.
GVDD	4	AO	Internally generated voltage supply. Connect to a 2.2µF capacitor for decoupling.
ALC	5	AI	**ALC and Dynamic Range Control**. Connect to a 0.1µF capacitor for decoupling.
PVDDL	6, 10	P	Power supply for the left-channel power amplifier's output stage. Connect directly to the system power supply VDD and add a 1µF capacitor for decoupling.
VOPL	7	AO	Left-channel non-inverting audio output terminal.
PGNDL	8	G	Power ground for the output stage of the left-channel power amplifier. Connect to the system ground GND.
VONL	9	AO	Left-channel inverting audio output terminal.
SS	11	DI	**Spread-Spectrum Select** (Active High) with a 300kΩ internal pulldown resister.
EN	12	DI	**Chip Enable** (Active High) with a 300kΩ internal pulldown resister to ground.
MUTE	13	DI	**Mute Control** (Active High) with a 300kΩ internal pulldown resistor to ground.
PBTL	14	DI	**PBTL Select** (Active High) with a 300kΩ internal pulldown resistor to ground.
PVDDR	15, 19	P	Power supply for the right-channel power amplifier's output stage. Connect directly to the system power supply VDD and add a 1µF capacitor for decoupling.
VONR	16	AO	Right-channel inverting audio output terminal.
PGNDR	17	G	Power ground for the output stage of the right-channel power amplifier. Connect to the system ground GND.
VOPR	18	AO	Right-channel non-inverting audio output terminal.
ATT	20	DI	**ALC Attack Time Select** with a 300kΩ internal pulldown resistor to ground.
AVDD	21	P	Power supply for internal analog circuitry. Connect to the system power supply through a small decoupling resistor (10Ω). Also, add a 1µF capacitor for decoupling.
INPR	22	AI	Right-channel non-inverting audio input terminal.
INNR	23	AI	Right-channel inverting audio input terminal.
BYP	24	AO	Common-mode bias for audio inputs. Connect to a 1µF capacitor for decoupling.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ft2725P	-40°C to +85°C	TSSOP-24L

REVISION HISTORY

Initial Release 1.0 (Jan., 2015)

Changed from Initial 1.0 (January, 2015) to Revision 1.1 (January, 2017)

1. Deleted the package option of QFN5x5-28L.
2. Changed input capacitors (C_{INL1}, C_{INL2}, C_{INR1}, and C_{INR2}) from 1.0μF to 0.33μF in Typical Application Circuits.
3. Revised Table 4, Typical Voltage Gain Settings & Input Resistor Values for Various Input Levels.
4. Added snubber circuits across audio outputs VOPL/R and VONL/R in Figure 1, 33, 34, 35, and 36.

Changed from Revision 1.1 (June, 2017) to Revision 1.2 (November, 2017)

1. Changed $C_{PVDDL/R}$ from 10μF to 1μF.
2. Added C_{VDD} of 10μF//220μF onto the system power supply.
3. Updated Figure 1, Typical Application Circuit, on Page 1.
4. Updated Figure 33 and 34 on Page 24; Figure 35 and 36 on Page 25.

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE
Supply voltage, AVDD, PVDDL/R	-0.3V to 9.2V
All other Pins	-0.3V to VDD+0.3V
Storage Temperature	-65°C to +150°C
ESD Ratings-Human Body Model (HBM)	2000V
Junction Temperature	150°C
Maximum Soldering Temperature (@10 second duration)	260°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may damage the device or affect device reliability.

POWER DISSIPATION RATINGS (Note 2, 3)

PACKAGE	$T_A \leq +25°C$	$T_A = +70°C$	$T_A = +85°C$	Θ_{JA}
TSSOP-24L	3.1W	2.0W	1.7W	40°C/W

Note 2: The thermal pad of the package must be directly soldered onto a grounded metal island (as a thermal sink) on the system board.
Note 3: The power dissipation ratings are for a two-side, two-plane printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

Parameter	Conditions	MIN	TYP	MAX	UNIT
Supply Voltage，V_{DD} (Note 4)	AVDD, PVDDL/R	3.7		9.0	V
Operating Free-Air Temperature, T_A		-40		85	°C
Minimum Load Resistance, R_L		3.0			Ω

Note 4: The peak supply voltage including its tolerance over various operating conditions must not exceed its absolute-maximum-rated value (9.2v). Exposure to absolute-maximum-rated supply voltage may damage the device or affect device reliability permantly. For applications where the system supply voltage might momentarily exceed the rating, it is strongly suggested to add an external Schottky diode in series from the system power supply to ensure the peak suppy voltage not exceeding the absolute maximum rating.

IMPORTANT APPLICATION NOTES

1. For best noise performance, it is recommended to use differential inputs from the audio source for ft2725. In a single-ended input application, the unused input of ft2725 should be AC-grounded at the audio source. The impedance seen at the two differential inputs should be the same.
2. The ft2725 requires adequate power supply decoupling to ensure its optimum operation and performance in output power, efficiency, distortion, and EMI emissions. Place respective decoupling capacitors individually as close as possible to the device's AVDD, GVDD, BYP, and PVDDL/R pins.
3. The ft2725 is a high performance, high power, stereo Class-D audio amplifier with an exposed thermal pad on the underside of the device. The thermal pad should be directly soldered onto a ground plane, where AGND and PGNDL/R pins are directly connected, as a thermal sink for proper power dissipation. Failure to do so may result in the device prematurely going into thermal overload protection.
4. It is strongly recommended to employ power (PVDD) and ground (GND) planes for ft2725 on the system board. Also, place a small decoupling resistor (10Ω) between AVDD and PVDD to prevent high frequency Class-D transient spikes from interfering with the on-chip linear amplifiers.
5. Use a simple ferrite bead filter for further EMI suppression, as shown in Figure 31. Choose a ferrite bead with a rated current no less than 3A or greater for applications with a load resistance less than 4Ω. Also, place respective ferrite beard filters as individually close to VOPL/R and VONL/R pins as possible
6. To enhance long-term reliability, it is strongly recommended to add an RC snubber circuit, as shown in Figure 32, between the two output pins of each individual channel, VOPL/R and VONL/R, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition.
7. Do not short audio outputs (VOPL/R and VONL/R) directly to ground (AGND, PGNDL/R) or the supply voltage (AVDD, PVDDL/R) as this might damage the device permanently, particularly when the supply voltage is higher than 8.4V.

FUNCTIONAL BLOCK DIAGRAM

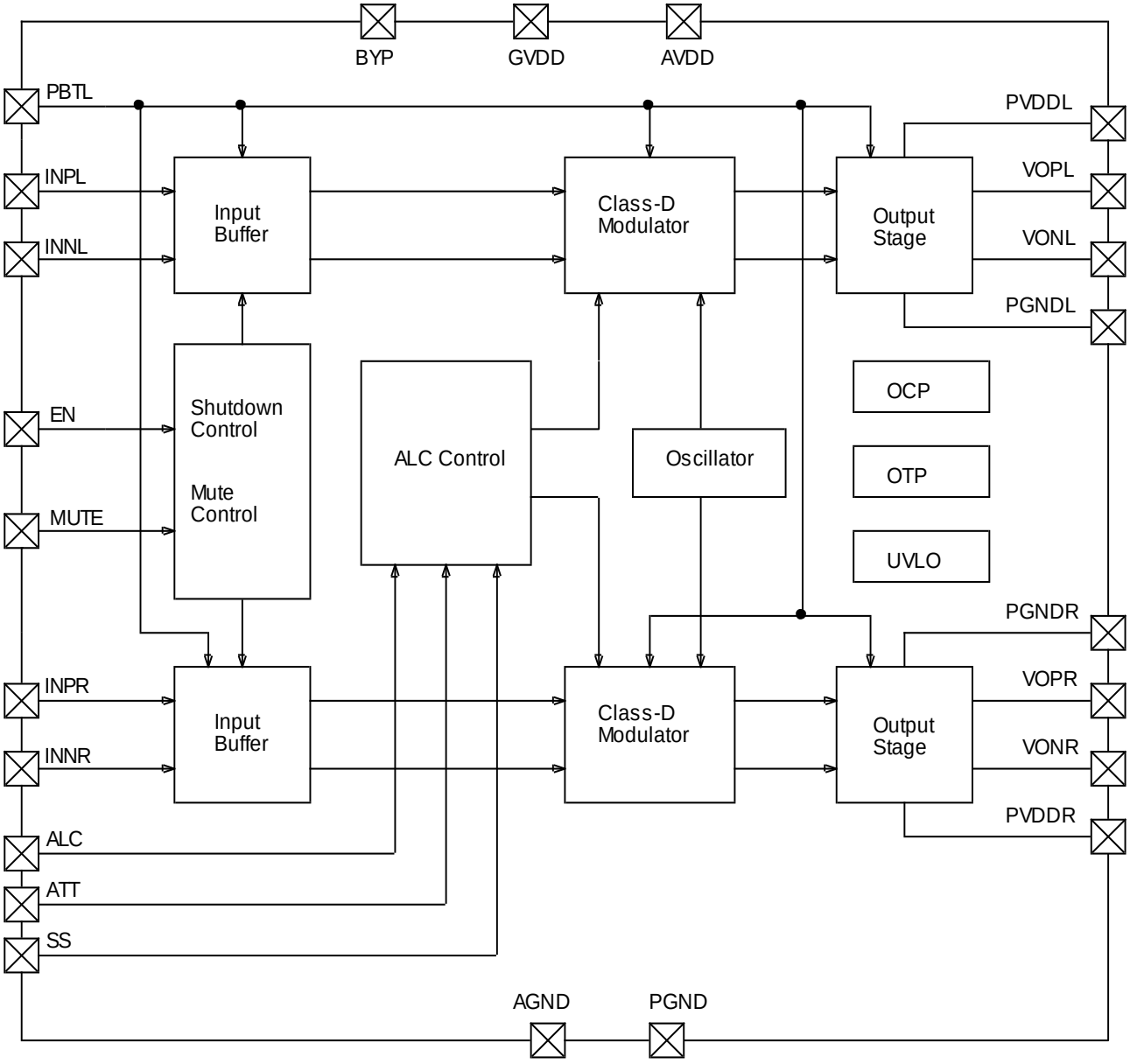


Figure 2: Simplified Functional Block Diagram of ft2725

ELECTRICAL CHARACTERISTICS

V_{DD}=9V, C_{IN}=0.33μF, R_{IN}=10kΩ, MUTE=Low, PBTL=Low, SS=Low, ATT=High, C_{BYP}=1μF, C_{GVDD}=2.2μF, C_{AVDD}=1μF, $C_{PVDDL/R}$=1μF, f=1kHz, Load=4Ω+33μH, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	AVDD, PVDDL/R	3.7		9.0	V
V_{UVLOUP}	Power-Up Threshold Voltage	VDD from Low to High		3.2		V
V_{UVLODN}	Power-Off Threshold Voltage	VDD from High to Low		2.9		V
GVDD	Regulator Output Voltage	VDD=9V	5.8	6.2	6.6	V
BYP	Common-Mode Bias Voltage	VDD=9V	2.8	3.1	3.4	V
I_{VDD} (Normal Mode)	Supply Quiescent Current Inputs AC-Grounded MUTE=Low, No Load	VDD=9V, PBTL=Low	13	18	23	mA
		VDD=9V, PBTL=High				mA
I_{VDD_MUTE} (Mute Mode)	Mute Current Inputs AC-Grounded Mute=High, No Load	VDD=9V, PBTL=Low	4	6	8	mA
		VDD=9V, PBTL=High				mA
I_{SD}	Shutdown Current	EN Low		10		μA
V_{IH}	Digital High Level Input Voltage	EN, MUTE, SS, PBTL, ATT	1.2			V
V_{IL}	Digital Low Level Input Voltage	EN, MUTE, SS, PBTL, ATT			0.4	V
R_{DOWN}	Pulldown Resistor to Ground	EN, MUTE, SS, PBTL, ATT		300		kΩ
CLASS-D AMPLIFIER						
$P_{O, MAX}$ (VDD=9V)	THD+N=10%, VALC≥0.8*GVDD (Non-ALC Mode)	R_L=4Ω		11		W/Ch
		R_L=3Ω in Mono Mode		15		W
	THD+N=1% VALC≥0.8*GVDD (Non-ALC Mode)	R_L=4Ω		9.0		W/Ch
		R_L=3Ω in Mono Mode		12		W
$P_{O, ALC}$ (VDD=9V)	V_{IN}=0.36V_{RMS} VALC≤0.4V (ALC Mode)	R_L=4Ω		8.5		W/Ch
		R_L=3Ω in Mono Mode		11.5		W
$P_{O, DRC}$ (VDD=9V)	V_{IN}=0.40V_{RMS} VALC=2.7V (DRC Mode)	R_L=4Ω		8.8		W/Ch
		R_L=3Ω in Mono Mode		11.5		W
	V_{IN}=0.40V_{RMS} VALC=1.8V (DRC Mode)	R_L=4Ω		4.9		W/Ch
		R_L=3Ω in Mono Mode		6.5		W
$P_{O, MAX}$ (VDD=7.2V)	THD+N=10%, VALC≥0.8*GVDD (Non-ALC Mode)	R_L=4Ω		7.0		W/Ch
		R_L=3Ω in Mono Mode		9.6		W
	THD+N=1% VALC≥0.8*GVDD (Non-ALC Mode)	R_L=4Ω		5.6		W/Ch
		R_L=3Ω in Mono Mode		7.7		W
$P_{O, ALC}$ (VDD=7.2V)	V_{IN}=0.36V_{RMS} VALC≤0.4V (ALC Mode)	R_L=4Ω		5.4		W/Ch
		R_L=3Ω in Mono Mode		7.5		W
$P_{O, DRC}$ (VDD=7.2V)	V_{IN}=0.40V_{RMS} VALC=2.16V (DRC Mode)	R_L=4Ω		6.0		W/Ch
		R_L=3Ω in Mono Mode		8.0		W
	V_{IN}=0.40V_{RMS} VALC=1.44V (DRC Mode)	R_L=4Ω		3.8		W/Ch
		R_L=3Ω in Mono Mode		5.0		W
$P_{O, MAX}$ (VDD=6.5V)	THD+N=10%, VALC≥0.8*GVDD (Non-ALC Mode)	R_L=4Ω		5.8		W/Ch
		R_L=3Ω in Mono Mode		8.0		W
	THD+N=1% VALC≥0.8*GVDD (Non-ALC Mode)	R_L=4Ω		4.6		W/Ch
		R_L=3Ω in Mono Mode		6.4		W
$P_{O, ALC}$ (VDD=6.5V)	V_{IN}=0.36V_{RMS} VALC≤0.4V (ALC Mode)	R_L=4Ω		4.5		W/Ch
		R_L=3Ω in Mono Mode		6.2		W
$P_{O, DRC}$ (VDD=6.5V)	V_{IN}=0.40V_{RMS} VALC=1.95V (DRC Mode)	R_L=4Ω		5.0		W/Ch
		R_L=3Ω in Mono Mode		6.6		W
	V_{IN}=0.40V_{RMS} VALC=1.3V (DRC Mode)	R_L=4Ω		3.4		W/Ch
		R_L=3Ω in Mono Mode		4.5		W

ELECTRICAL CHARACTERISTICS (Cont'd)

V_{DD}=9V, C_{IN}=0.33μF, R_{IN}=10kΩ, MUTE=Low, PBTL=Low, SS=Low, ATT=High, C_{BYP}=1μF, C_{GVDD}=2.2μF, C_{AVDD}=1μF, $C_{PVDDL/R}$=1μF, f=1kHz, Load=4Ω+33μH, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CLASS-D AMPLIFIER (Cont'd)						
THD+N	Total Harmonic Distortion+Noise VALC≥0.8*GVDD (Non-ALC Mode)	R_L=4Ω, Po=5W		0.06		%
	Total Harmonic Distortion+Noise VALC≤0.4V (ALC Mode) V_{IN}=0.36V_{RMS}	R_L=4Ω, Po=8.5W		0.3		%
		R_L=3Ω, Po=11.5W		0.4		%
	Total Harmonic Distortion+Noise VALC=2.7V (DRC Mode) V_{IN}=0.40V_{RMS}	R_L=4Ω, Po=8.8W		0.6		%
		R_L=3Ω, Po=11.5W		0.6		%
	Total Harmonic Distortion+Noise VALC=1.8V (DRC Mode) V_{IN}=0.40V_{RMS}	R_L=4Ω, Po=4.9W		0.3		%
		R_L=3Ω, Po=6.5W		0.4		%
A_V	Overall Voltage Gain	R_{IN}=10kΩ		28		dB
R_{IN}	Input Resistance	@ INNL/R, INPL/R		15		kΩ
R_{OUT-SD}	Output Resistance in Shutdown	@ VOPL/R, VONL/R, EN=Low		2.5		kΩ
V_{OS}	Output Offset Voltage	No Load		±10		mV
V_N	Idle-Channel Noise	AV=28dB, Inputs AC-Grounded A-weighted		150		μV_{RMS}
η	Power Efficiency	V_{DD}=9V, Po=8W, R_L=4Ω		89		%
PSRR	Power Supply Rejection Ratio	f=1kHz		76		dB
CMRR	Common Mode Rejection Ratio	f=1kHz		70		dB
SNR	Signal-to-Noise Ratio	Maximum Output (6V_{RMS}) with THD+N<1%, R_L=4Ω, AV=20dB, A-weighted		92		dB
Crosstalk	Channel Separation	Po=5W, f=1kHz		80		dB
T_{STUP}	Startup Time			160		ms
T_{SD}	Shutdown Mode Settling Time			20		ms
f_{SW}	PWM Output Carrier Frequency			360		kHz
I_{LIMIT}	Over-Current Limit	V_{DD}=9V, Stereo Mode		3.2		A/Ch
		V_{DD}=7.2V, Mono Mode		2.7		A/Ch
		V_{DD}=9V, Stereo Mode		4.2		A
		V_{DD}=7.2V, Mono Mode		3.6		A
T_{OCP}	Over-Current Recovery Time			40		ms
T_{OTP}	Over-Temperature Threshold			160		°C
T_{HYS}	Over-Temperature Hysteresis			20		°C
AUTOMATIC LEVEL CONTROL (ALC)						
A_{MAX}	Maximum ALC Attenuation			10		dB
T_{ATTACK}	ALC Attack Time	ATT=Low		2		ms
		ATT=High		50		ms
$T_{RELEASE}$	ALC Release Time			500		ms
V_{ALC}	Operating Mode Threshold	ALC Mode			0.4	V
		DRC Mode	0.6		0.5*GVD	V
		Non-ALC Mode	0.8*GVDD			V
FADE-IN & FADE-OUT						
T_{FADEIN}	Fade-In Time			20		ms
$T_{FADEOUT}$	Fade-Out Time			10		ms

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=9V, C_{IN}=0.33μF, R_{IN}=10kΩ, MUTE=Low, PBTL=Low, SS=Low, ATT=High, C_{BYP}=1μF, C_{GVDD}=2.2μF, C_{AVDD}=1μF, $C_{PVDDL/R}$=1μF, f=1kHz, Load=4Ω+33μH, T_A=25°C, unless otherwise specified.

DESCRIPTION	CONDITIONS	FIGURE #
Output Power vs. Supply Voltage	R_L=8Ω+33μH, Vin=0.3V_{RMS}, ALC & Non-ALC Modes, PBTL=Low	3
	R_L=4Ω+33μH Vin=0.3V_{RMS}, ALC & Non-ALC Modes, PBTL=Low	4
	R_L=3Ω+33μH, Vin=0.3V_{RMS}, ALC & Non-ALC Modes, PBTL=High	5
Output Power vs. V_{ALC}	R_L=4Ω+33μH, Vin=0.4V_{RMS}, DRC Mode V_{DD}=8.8V & 7.2V & 6.5V	6
Output Power vs. Input Voltage	R_L=4Ω+33μH, DRC (V_{ALC}=2.7V) Non-ALC, ALC, DRC Modes	7
	R_L=4Ω+33μH, DRC Mode V_{ALC}=1.8V, 2.2V, 2.7V	8
Efficiency vs. Output Power	V_{DD}=8.8V, R_L=4Ω+33μH, Non-ALC Mode	9
THD+N vs. Output Power	R_L=4Ω+33μH, Non-ALC Mode	10
THD+N vs. Input Voltage	R_L=4Ω+33μH, ALC & Non-ALC Modes	11
	R_L=4Ω+33μH, DRC Mode V_{ALC}=1.8V, 2.2V, 2.7V	12
THD+N vs. Input Frequency	R_L=4Ω+33μH, ALC Mode, Po=5W	13
PSRR vs. Frequency	R_L=4Ω+33μH, Inputs AC-Grounded	14
Crosstalk vs. Input Frequency	R_L=4Ω+33μH, Vo=2.0V_{RMS}, R-CH to L-CH	15
Quiescent Current vs. Supply Voltage	Input AC-Grounded, No Load, ALC Mode	16
ALC Attack & Release Time	Vin=0.2V_{RMS} ~ 0.63V_{RMS}, R_L=4Ω+33μH V_{ALC}=0V (ALC Mode), ATT=Low	17
ALC Attack & Release Time	Vin=0.2V_{RMS} ~ 0.63V_{RMS}, R_L=4Ω+33μH V_{ALC}=2.7V (DRC Mode), ATT=Low	18
(VOP-VON) Startup Waveforms	R_L=4Ω+33μH, Vin=0.1V_{RMS}, ALC Mode	19
(VOP-VON) Shutdown Waveforms	R_L=4Ω+33μH, Vin=0.1V_{RMS}, ALC Mode	20
Broadband Output Spectrum	R_L=4Ω+33μH, Vin=0.2V_{RMS}, SS=Low	21
	R_L=4Ω+33μH, Vin=0.2V_{RMS}, SS=High	22

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

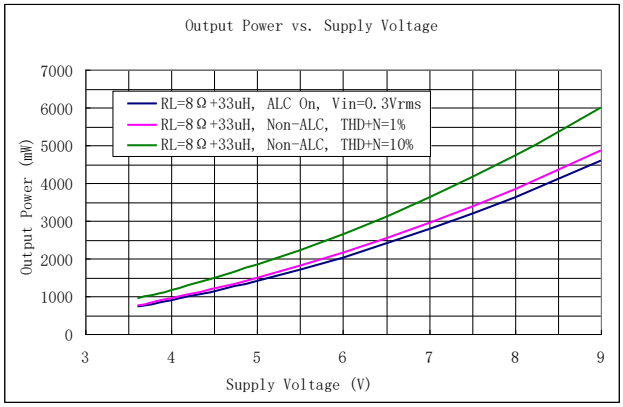


Figure 3: Output Power vs. Supply Voltage

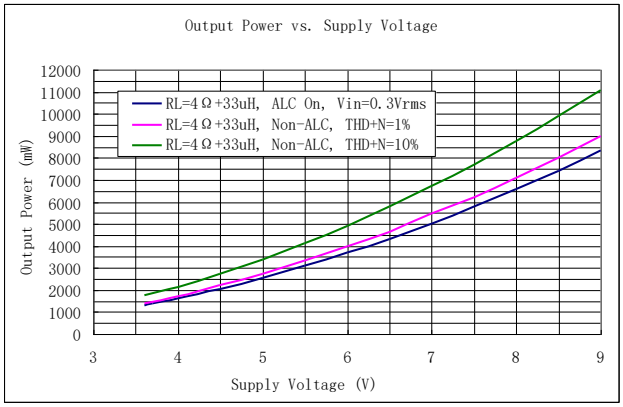


Figure 4: Output Power vs. Supply Voltage

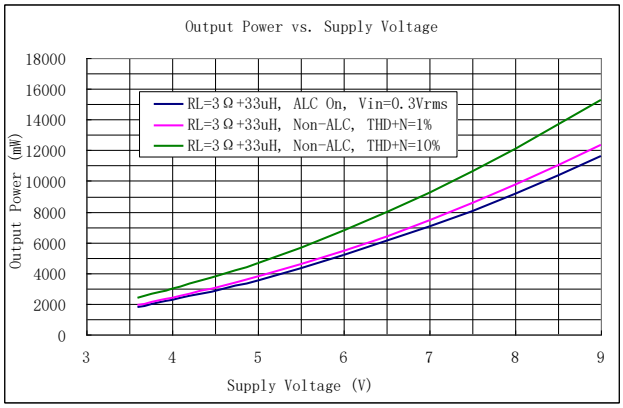


Figure 5: Output Power vs. Supply Voltage

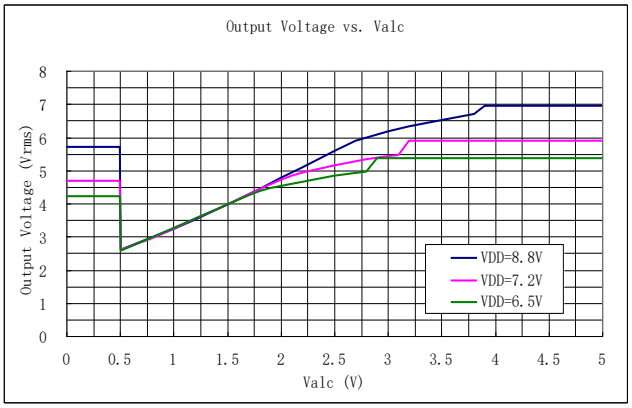


Figure 6: Output Power vs. VALC (DRC Mode)

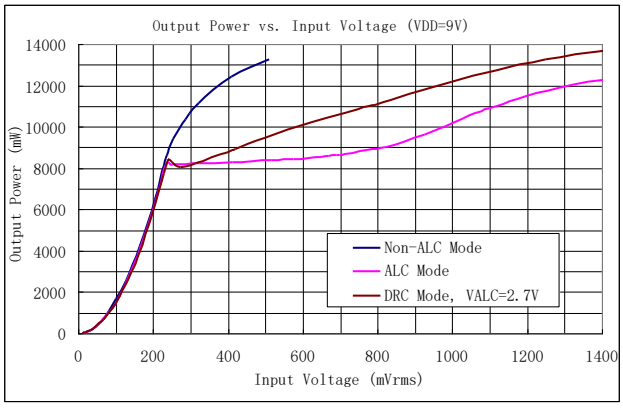


Figure 7: Output Power vs. Input Voltage

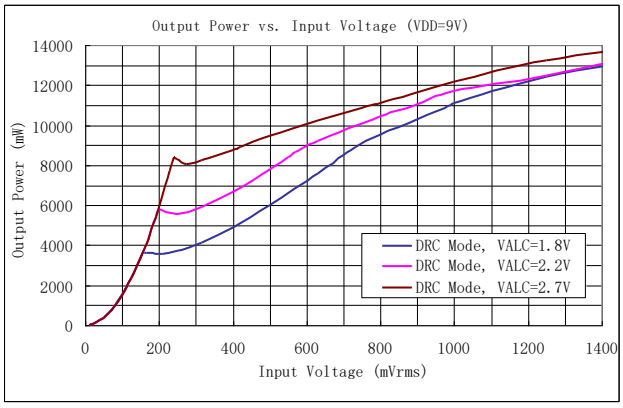


Figure 8: Output Power vs. Input Voltage (DRC Mode)

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

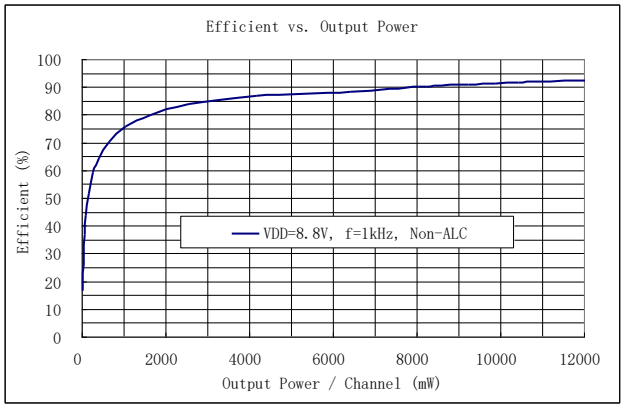


Figure 9: Efficiency vs. Output Power

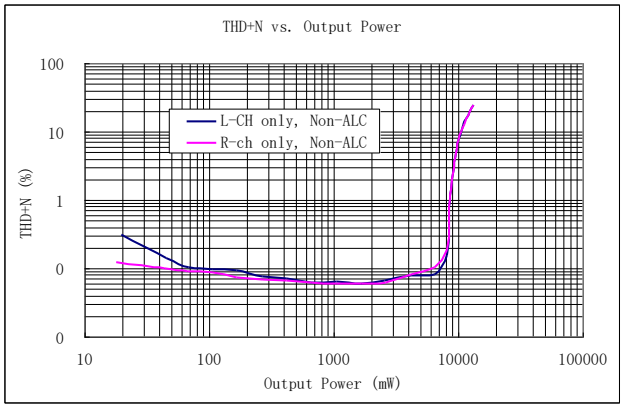


Figure 10: THD+N vs. Output Power

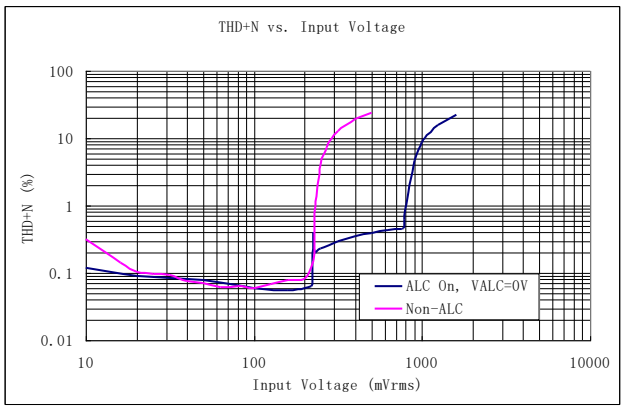


Figure 11: THD+N vs. Input Voltage

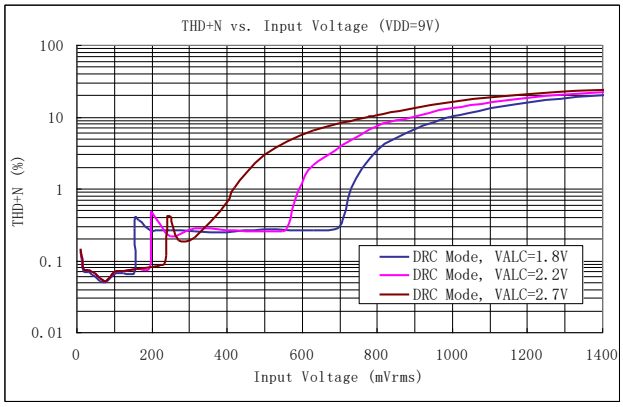


Figure 12: THD+N vs. Input Voltage (DRC Mode)

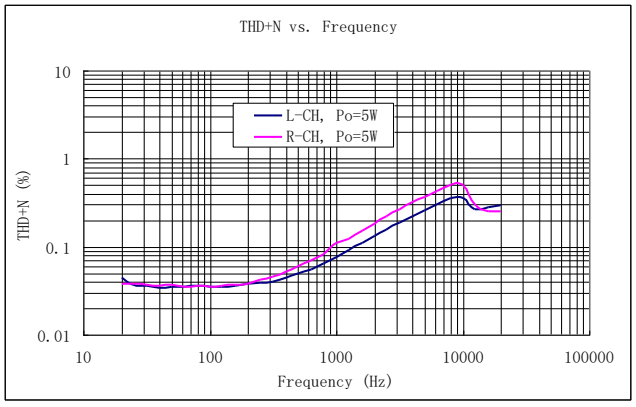


Figure 13: THD+N vs. Frequency

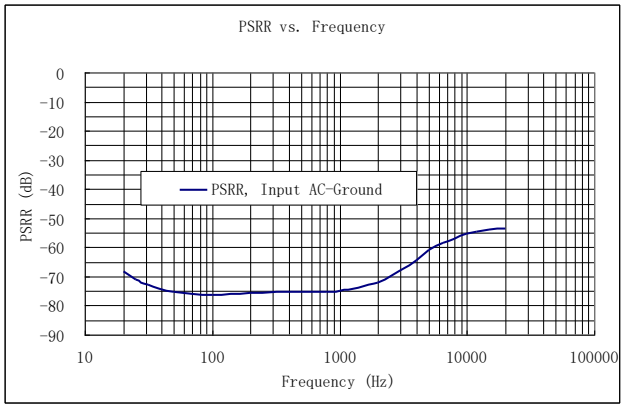


Figure 14: PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

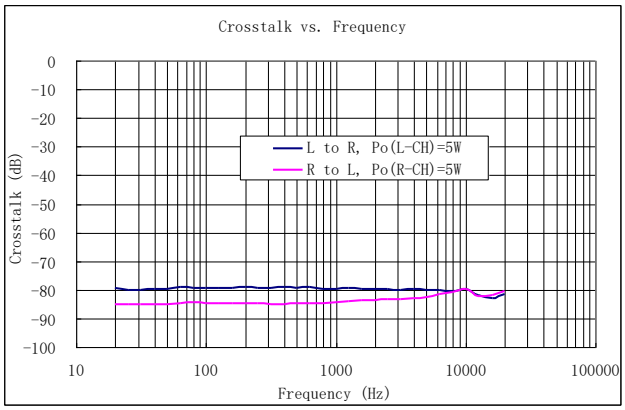


Figure 15: Crosstalk vs. Frequency

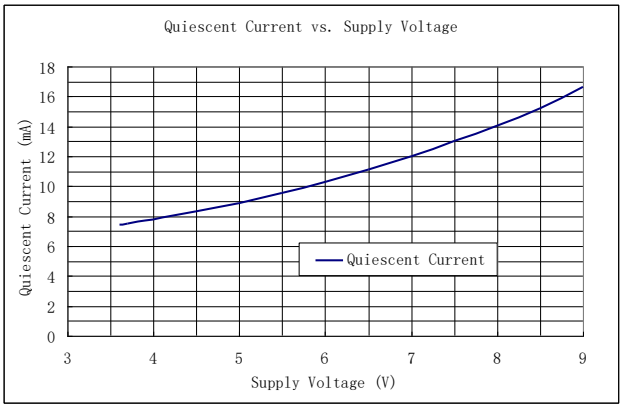


Figure 16: Quiescent Current vs. Supply Voltage

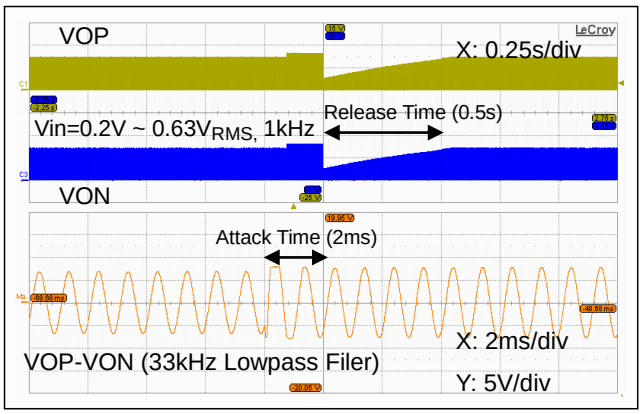


Figure 17: ALC Attack & Release Time (ALC Mode)

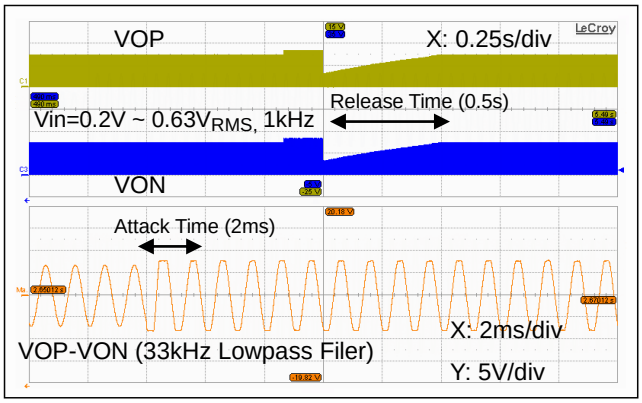


Figure 18: ALC Attack & Release Time (DRC Mode)

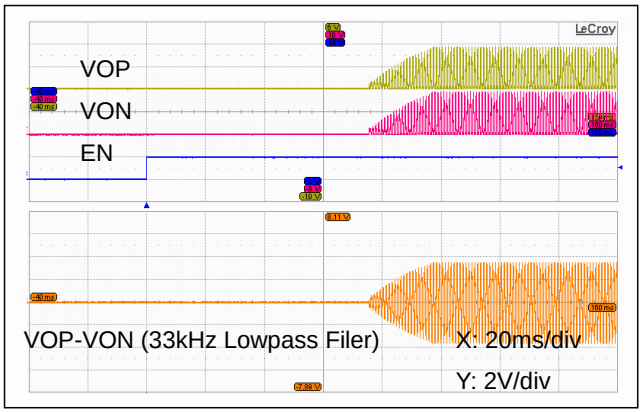


Figure 19: (VOP-VON) Startup Waveforms

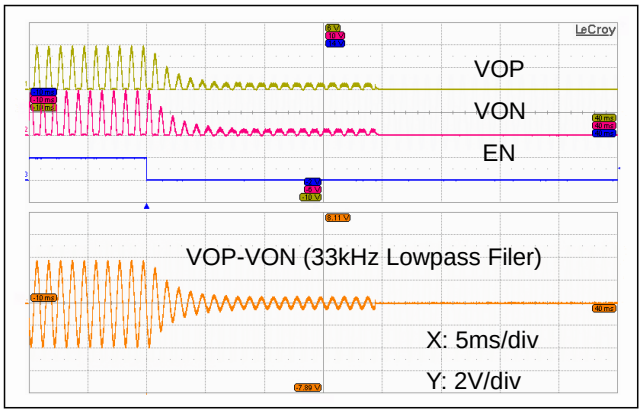


Figure 20: (VOP-VON) Shutdown Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

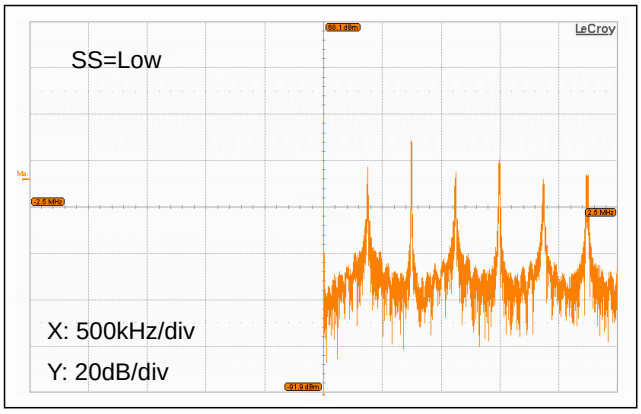


Figure 21: Broadband Output Spectrum

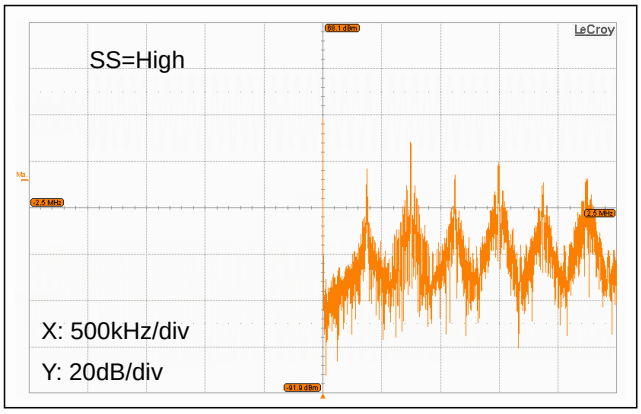


Figure 22: Broadband Output Spectrum

APPLICATION INFORMATION

The ft2725 is a highly efficient 2X11W stereo Class-D audio power amplifier with automatic level control (ALC) and dynamic range compression (DRC). It operates with a wide range of supply voltages from 3.7V to 9V. When powered with 9V supply voltage, the ft2725 is capable of delivering 11W per channel into a pair of 4Ω speakers in a bridge-tied-load (BTL) configuration, or 15W into a single 3Ω speaker in parallel BTL (PBTL) configuration, with 10% THD+N.

The ft2725 features ALC with an adjustable threshold for dynamic range control (DRC). The ALC constantly monitors and safeguards the audio outputs against a user-defined threshold voltage, preventing output clipping distortion, excessive power dissipation, or hazardous speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of the audio amplifiers proportionally to eliminate output clipping while maintaining for a maximally-allowed dynamic range of the audio outputs. The threshold voltage of the ALC can be set at either the supply voltage or an externally defined value.

In ft2725, three operating modes, i.e., ALC, DRC, and Non-ALC, are available that can be selected via the ALC pin. The Non-ALC mode configures the device in a conventional Class-D operation, where the output power is maximized without ALC operation. In ALC mode, the output limiting voltage is set at the supply voltage. In DRC mode, the threshold voltage for dynamic range compression is adjustable and set at a user-defined value that is linearly proportional to the voltage applied onto the ALC pin.

As a filterless Class-D audio amplifier, the ft2725 features high efficiency (up to 89%), high PSRR (76dB at 1kHz), and low EMI emissions, which reduce design and manufacturing complexities, lower system cost and PCB space. These features make ft2725 an ideal audio solution for portable and plug-in consumer electronic devices.

As specifically designed for portable applications, the ft2725 incorporates a shutdown mode to minimize the power consumption by holding the EN pin to ground. It also includes comprehensive protection features against various operating faults such as over-current, short-circuit, over-temperature, or under-voltage for a safe and reliable operation.

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the audio output signals for a maximum voltage swing without distortion when an excessive input that may cause output clipping is applied. With the ALC function, the ft2725 lowers the gain of the amplifier to an appropriate value such that the clipping at the outputs is substantially eliminated. It also eliminates the clipping of the output signal due to the reduction of the power-supply voltage.

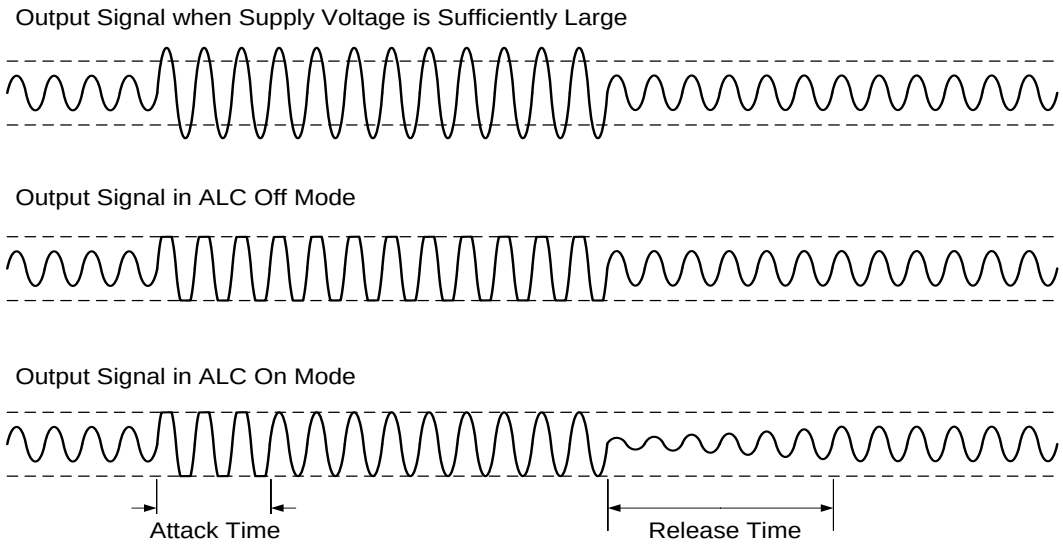


Figure 23: Automatic Level Control Diagram

The attack time and release time of the ALC are shown in Table 1. The attack time is defined as the time interval required for the gain to fall to its steady-state gain less 3dB approximately, assumed that a sufficiently large input signal is applied. The release time is the time interval required for the amplifier to exit out of the present mode of operation.

ATT Logic Level	Attack Time (ms)	Release Time (ms)
Low	2	500
High	50	500

Table 1: Attack Time & Release Time

OPERATING MODE CONTROL

As described in Table 2, depending upon the voltage applied onto the ALC pin, the ft2725 can be configured in one of the three operating modes: ALC (automatic level control with a fixed threshold voltage at VDD), DRC (automatic level control with an adjustable threshold voltage defined by the voltage at the ALC pin), and Non-ALC. If the voltage at the ALC pin is set less than 0.4V, the ft2725 operates in ALC mode, where the threshold voltage of ALC is set at the supply voltage, VDD. In this case, the output peak voltage is limited to a value that is substantially close to the supply voltage VDD. If the voltage at the ALC pin is set in the range from 0.6V to 0.5*GVDD, the ft2725 operates in DRC mode, where audio compression will be performed for the audio outputs exceeding the defined threshold voltage. In this case, the threshold voltage of DRC is linearly proportional to the voltage at the ALC pin. If the voltage at the ALC pin is set higher than 0.8*GVDD, the ft2725 operates in Non-ALC mode, where the ft2725 operates as a conventional Class-D amplifier without ALC or DRC function. In this case, the output voltage will clip when the output peak voltage reaches beyond VDD.

Voltage at ALC	Mode of Operation
$V_{ALC} \leq 0.4V$	ALC (with fixed threshold voltage at VDD)
$0.6V \leq V_{ALC} \leq 0.5*GVDD$	DRC (with adjustable threshold voltage)
$V_{ALC} \geq 0.8*GVDD$	Non-ALC

Table 2: Operating Mode Control

VOLTAGE GAIN SETTING

In ft2725, the voltage gain of the audio amplifier can be externally adjusted by inserting external input resistors, R_{IN}, in series with the input capacitors, as depicted in Figure 24 and 25. In both figures, it is required that C_{IN} = C_{INL1} = C_{INL2} = C_{INR1} = C_{INR2}, R_{IN} = R_{INL1} = R_{INL2} = R_{INR1} = R_{INR2}.

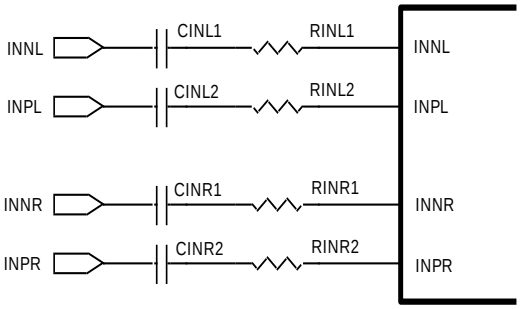


Figure 24: Gain Setting (Differential Inputs)

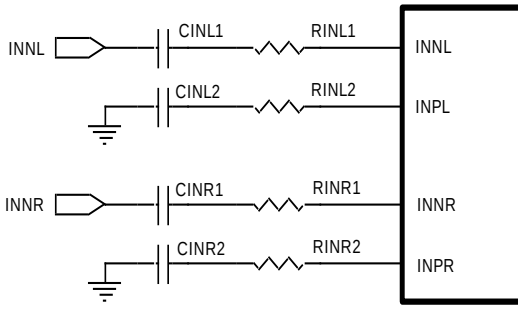


Figure 25: Gain Setting (Single-Ended Input)

The value of R_{IN} (in kΩ) for a given voltage gain can be calculated by Equation 1, where A_V is the voltage gain of the audio amplifier.

$$A_V = \frac{625}{R_{IN} + 15} \qquad (1)$$

Table 3 shows suitable resistor values of RIN that can be used for various voltage gains.

RIN (kΩ)	10	16	20	24	30	36	39	47	56	62
AV (dB)	28	26	25	24	23	22	21	20	19	18

Table 3: External Input Resistor Values Required for Various Voltage Gains

The choice of the voltage gain will strongly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause audio outputs to be severely clipped for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quite) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for well balanced audio quality.

The voltage gain is chosen based upon various system-level considerations including the supply voltage, the dynamic range of audio sources and speaker loads, and the desired sound effects. As a general guideline, the voltage gain can be simply expressed in Equation 2. In the equation, $V_{IN, MAX}$ (in V_{RMS}) is the maximum input level from the audio source, PVDD (in volts) is the supply voltage, and α is the design parameter, which ranges from 0.65 to 2.2. The higher α is, the higher the average output power (louder) is, with some degree of compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN, MAX}} \qquad (2)$$

As an example, Table 4 shows the voltage gains for various input levels and PVDD settings with α at about 1.2. In the table, RIN is the external input resistor in series with the input capacitor.

PVDD (V)	VIN, MAX (VRMS)	RIN (kΩ)	AV (V/V)	AV (dB)	PO, ALC (W) with 4Ω+33μH Load
9.0	0.3	10	25	28	8.5
	0.5	20	18	25	
	0.7	36	12	22	
	1.0	62	8	18	
7.2	0.3	16	20	26	5.2
	0.5	33	13	22	
	0.7	47	10	20	
6.5	0.3	20	18	25	4.2
	0.5	36	12	22	
	0.7	56	9	19	

Table 4: Typical Voltage Gain Settings & Input Resistor Values for Various Input Levels

GVDD SUPPLY

The GVDD is an internally generated supply voltage for internal circuitry. It can also be used as the supply voltage for the resistor divider to set the voltage at the ALC pin. It is recommended to decouple GVDD with a 2.2μF ceramic capacitor to ground for stable operation. Note that the current drawn from GVDD by external circuitry, including the resistor divider at the ALC pin, must be kept less than 0.5mA.

ADJUSTABLE DRC THRESHOLD VOLTAGE

In conventional Class-D audio amplifiers with ALC operation, the output peak voltage is limited with respect to the supply voltage applied to the device. The ft2725 features a DRC mode whose threshold (knee) voltage can be externally set via the ALC pin. The threshold voltage (V_{KNEE}) is linearly proportional to the voltage at the ALC pin, as described by Equation 3.

$$V_{KNEE} = 3 \times V_{ALC} \quad (3)$$

In Equation 3, V_{ALC} is the voltage at the ALC pin and can be set by a resistor divider from GVDD (an internally generated reference voltage) to ground, as shown in Figure 26. It is strongly recommended to add a 0.1µF capacitor from the ALC pin to ground for a stable operation. For best accuracy, the parallel combination of the resistor divider should be close to 100kΩ.

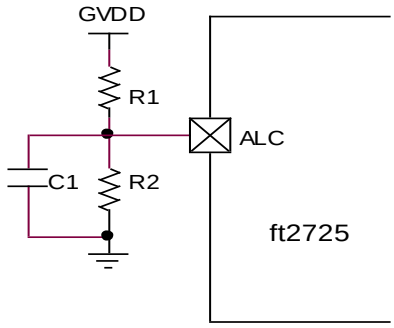


Figure 26: Typical Circuit Setting V_{ALC}

Table 5 shows typical values of R1 and R2 that can be used to derive various V_{ALC}. In the table, the corresponding DRC threshold voltage and the output power where DRC commences for each individual setting are also shown.

R1 (kΩ)	R2 (kΩ)	R2/(R1+R2)	GVDD (V)	VALC (V)	VKNEE (V)	Po (W) @ 4Ω
200	82	0.29	6.2	1.8	5.4	3.6
170	82	0.32	6.2	2.0	6.0	4.5
180	100	0.36	6.2	2.2	6.6	5.4
150	100	0.40	6.2	2.5	7.5	7.0
130	100	0.43	6.2	2.7	8.1	8.2

Table 5: Typical Resistor Values of R1 & R2 (VDD=9V) for Various DRC Threshold Voltages

In DRC mode, the ALC lowers the voltage gain for high-level (loud) audio outputs that are above the threshold, while maintaining a constant and relatively high voltage gain for low-level (quiet) audio outputs. In this manner, relatively quite sounds become louder while louder sounds remain unclipped. The net effect of DRC is to keep the audio volume fairly constant over a range from medium to high level sounds while allowing relatively quiet sounds of the music much more audible. For most applications, it is recommended to set the voltage gain at its highest value (A_V=32.4dB), if possible, for the device operating in DRC mode.

For most applications, V_{ALC} can be set in the range from 0.3*GVDD (or 0.2*VDD) to 0.45*GVDD (or 0.3*VDD). A lower V_{ALC} allows audio compression commencing at a lower audio output with a lower compression ratio. On the contrary, a higher V_{ALC} makes audio compression commencing at a higher audio output with a higher compression ratio. Note that the ALC mode ($V_{ALC} \leq 0.4V$) is one of the exceptional cases of DRC where the DRC threshold is set at a value substantially close to the supply voltage with a fairly large compression ratio.

Figure 27 illustrates the transfer (gain) function of the output (in dBVrms) with respect to the input (in dBVrms) for ft2725 operating with V_{DD}=9V and A_V=32.4dB in DRC mode for three different values of V_{ALC}. As shown in the figure, the voltage gain is constant at 32.4dB for low-level audio output (less than the threshold) while the voltage gain for high-level audio output (more than the threshold) is gradually lowered as the audio output grows larger. In a sense, the audio output is compressed as the audio output is larger than the threshold.

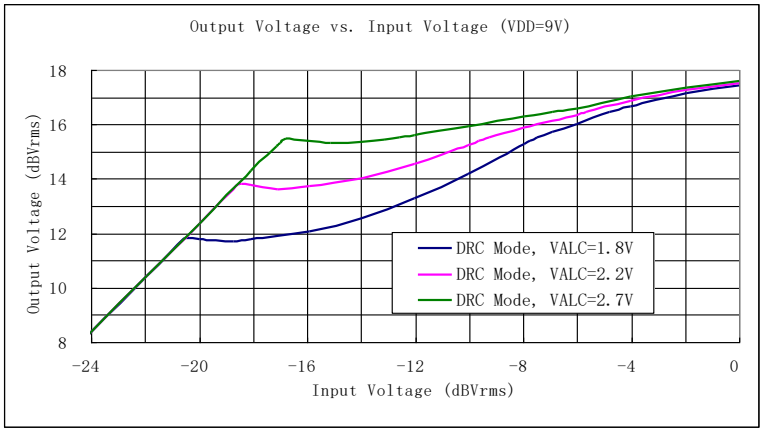


Figure 27: Output Voltage vs. Input Voltage (in dBVrms)

MONO MODE

The ft2725 features an optional mono mode that allows the left and right channels to operate in parallel BTL configuration, delivering up to 15W into a single 3Ω speaker. Apply a logic-high to PBTL pin to enable mono mode. In mono mode, as shown in Figure 28, an audio input signal applied to the left channel is routed to the H-bridge of both channels. The ft2725 operates in stereo mode by driving a logic-low to PBTL pin or leave the pin unconnected. Driving PBTL low or leaving it unconnected while the audio outputs VOPL/R and VONL/R are wired together in PBTL configuration can trigger the over-current or thermal overload protection or both. The mono mode of ft2725 is configured by:

- Connect PBTL to logic-high to set the device in mono mode.
- Connect INPR and INNR pins (pin 22 and 23) directly to BYP.
- Audio input signals are applied to INPL and INNL pins (pin 2 and 3).
- Connect VOPL to VONL and VOPR to VONR using heavy PCB traces as close as possible to the device.
- Place the speaker between the left and right-channel outputs.

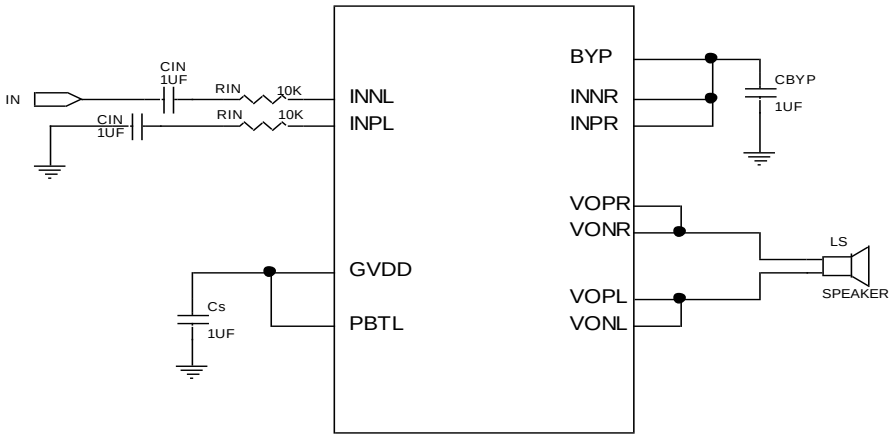


Figure 28: Application Circuit of Mono Mode in PBTL Configuration

VOLUME FADE-IN & FADE-OUT

The volume fade-in/out function operates when toggled EN or MUTE state. This function is used to reduce intermittent sound considerably and eliminate uncomfortable feeling.

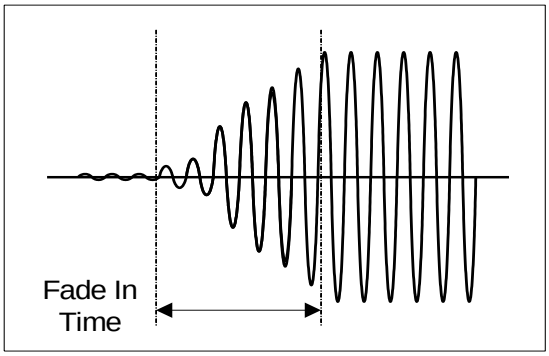


Figure 29: Fade-In Waveform

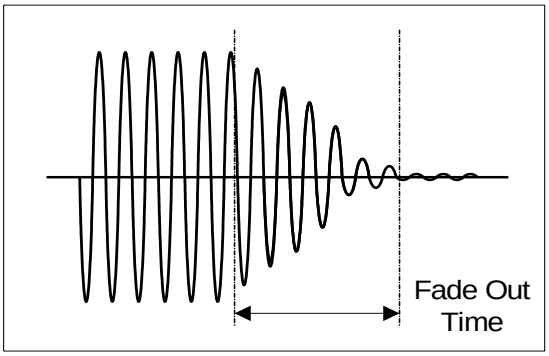


Figure 30 Fade-Out Waveform

SHUTDOWN AND STARTUP

The ft2725 employs the EN pin to minimize power consumption while it is not in use. When the EN pin is pulled to ground, the ft2725 is forced into shutdown mode, where all the analog circuitry is de-biased and the supply current is thus reduced to less than 10μA, and the differential outputs are shorted to ground through an internal resistor (2.5kΩ) individually. Once in shutdown mode, the EN pin must remains low for at least 20ms (T_{SD}), the shutdown settling time, before it can be brought high again. When the EN pin is asserted high, the device exits out of the shutdown mode and enters into the normal mode of operation after the startup time (T_{STUP}) of 160ms.

Note that an internal pulldown resistor of 300kΩ is implemented onto the EN pin. Furthermore, the shutdown mode is the state when the power supply is first applied to the device. Whenever possible, it is recommended to assert EN high to exit the device out of the shutdown mode only after the device is properly started up. Also, place the amplifiers in the shutdown mode prior to removing the power supply voltage for best power-off pop performance.

MUTE CONTROL

In ft2725, the MUTE pin is used to control the operation of the output stages of both channels. When playing music, the MUTE pin is pulled low and the output stages of audio amplifiers are enabled. When the MUTE pin is asserted high, the output stages of audio amplifiers are de-biased while the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors individually.

CLICK-AND-POP SUPPRESSION

The ft2725 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential audio outputs VOPL/R and VONL/R ramp down to ground quickly and simultaneously.

PSRR ENHANCEMENT

With a dedicated pin for the common-mode voltage bias and an external holding capacitor onto the pin, the ft2725 achieves a PSRR, 76dB at 1kHz.

PROTECTION MODES

The ft2725 incorporates various protection functions against possible operating faults for a safe operation. It includes Under-voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

Under-Voltage Lockout (UVLO)

The ft2725 incorporates a circuitry to detect a low supply voltage for a safe and reliable operation. When the supply voltage is first applied, the ft2725 will remain inactive until the supply voltage exceeds 3.2V (V_{UVLU}). When the supply voltage is removed and drops below 2.9V (V_{UVLD}), the ft2725 enters into shutdown mode immediately.

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a preset threshold, the device enters into the over-temperature shutdown mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors individually. The device will resume normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

Over-Current Protection (OCP)

During operation, the output of Class-D amplifier constantly monitors for any over-current and/or short-circuit conditions. When a short-circuit condition between two differential outputs, differential output to AVDD, PVDDL, PVDDR or ground is detected, the output stage of the amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft2725 then enters into the shutdown mode and remains in this mode for about 40ms (T_{OCP}), the over-current recovery time. When the shutdown mode times out, the ft2725 will initiate another start-up sequence and then check if the short-circuit condition has been removed. If the fault condition is still present, the ft2725 will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is so-called the hiccup mode of operation. Once the fault condition is removed, the ft2725 automatically restores to its normal mode of operation.

Although the output stages of the Class-D audio amplifiers can withstand a short between VOPL/R and VONL/R pins, do not short audio output pins (VOPL/R and VONL/R) directly to ground pins (AGND, PGNDL/R) or the supply voltage pins (AVDD, PVDDL/R) as this might damage the device permanently, particularly when the supply voltage is higher than 8.4V.

LOW-EMI FILTERLESS OUTPUT STAGE

Traditional Class-D amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft2725 applies an edge-rate control circuitry to reduce EMI emission, while maintaining high power efficiency. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

EMI REDUCTION

The ft2725 does not require an LC output filter for short connections from the amplifier to the speakers. However, additional EMI suppressions can be made by use of a ferrite bead in conjunction with a capacitor, as shown in Figure 31. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 330Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current value no less than 4A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance. Place the ferrite and capacitor as close to the output terminals (VOPL/R and VONL/R) as possible for the best EMI performance. Also, the capacitors should be grounded to power ground (PGNDL/R).

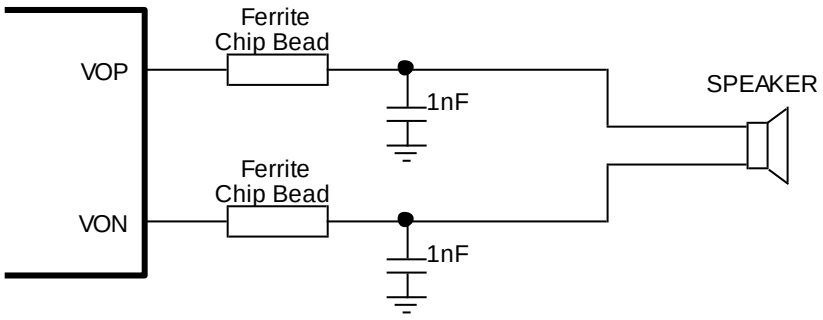


Figure 31: Ferrite Bead Filter to Reduce EMI

RC SNUBBER CIRCUIT

For applications where the power supply is rated more than 7.2V or the load resistance less than 4Ω, it may become necessary to add an RC snubber circuit between the two output pins of each individual channel, VOPL/R and VONL/R, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition. Note that the snubber circuit at the audio outputs also lowers the EMI emissions of the Class-D audio amplifiers.

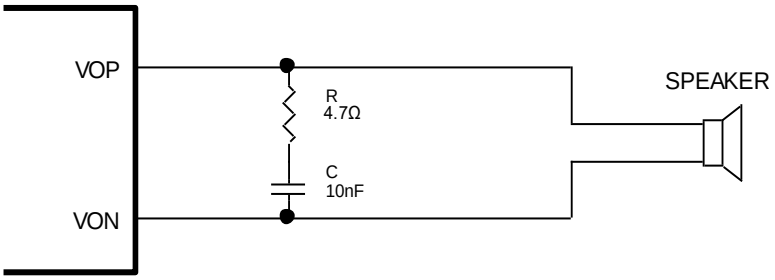


Figure 32: RC Snubber Circuit of Class-D Amplifiers' Outputs

SPREAD-SPECTRUM AUDIO OUTPUTs

The Class-D audio amplifiers in ft2725 can be operated at a fixed or jittered PWM frequency via the SS pin. By asserting the SS pin high, the Class-D audio amplifiers operate in a jittered PWM frequency, which results in further reduction of EMI emissions, with negligible penalty on THD+D, of the Class-D audio amplifiers. On the other hand (the SS pin is left open or shorted to ground), the Class-D audio amplifiers operate at a fixed frequency.

SS Logic Level	PWM Frequency
Low	Fixed
High	Jittered

Table 6: Spread-Spectrum Select

SUPPLY DECOUPLING CAPACITOR (C_{AVDD}, C_{PVDDL}, C_{PVDDR})

The ft2725 as a high-performance stereo audio power amplifier requires sufficient decoupling of the power supply to ensure its high efficiency operation with low total harmonic distortion. Sufficient power supply coupling also prevents oscillations for long lead lengths between the amplifier and the speakers. In light of power efficiency and EMI, it is strongly recommended to use power and ground planes to reduce parasitic resistance and inductance.

Place a low equivalent-series-resistance (ESR) ceramic capacitor (X7R or X5R), 1μF or greater, as close to AVDD pin as possible. Also, a small decoupling resistor, typically 10Ω, can be placed between AVDD and the system power supply to keep high frequency transient spikes from entering the on-chip linear amplifiers.

For best audio quality and reliability, place a 1μF low-ESR ceramic capacitor ($C_{PVDDL/R}$) individually close to PVDDL/R pins. In tandem with each 1μF capacitor, add a small, good quality, low-ESR ceramic capacitor of 0.047μF, within 2mm of the PVDDL/R pins, for high-frequency filtering and EMI reduction.

INPUT CAPACITOR (C_{INL1}, C_{INL2}, C_{INR1}, C_{INR2})

The input DC decoupling capacitors are recommended to bias the incoming audio inputs to a proper DC level. The input capacitor C_{IN}, in conjunction with the amplifier input resistance (including both internal 15kΩ and external resistor R_{IN}, if any) forms a highpass filter that removes the DC bias of the audio inputs. The corner frequency, f_C, of the highpass filter is given by Equation 4.

$$f_C = 1 / [2 \times \pi \times (R_{IN} + 15k\Omega) \times C_{IN}] \quad (4)$$

where $C_{IN} = C_{INL1}$, C_{INL2}, C_{INR1}, or C_{INR2}

R_{IN} is the external input resistance for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally. Thus choose input resistors with a tolerance of 5% or better.

Choose C_{IN} such that f_C is well below the lowest frequency of interest. Setting it too high affects the amplifiers' low-frequency response. Consider an example where the specification calls for A_V=28dB and a flat frequency response down to 20Hz. In this example, R_{IN}=10kΩ and C_{IN} is calculated to be about 0.32μF; thus 0.33μF, as a common choice of capacitance, can be chosen for C_{IN}.

Note that any mismatch in capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Choose input capacitors with a tolerance of ±5% or better.

Furthermore, the type of the input capacitor is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies. Other factors, including the constraints of the overall system such as the physical size of the speakers, are to be considered when designing the input filter.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

Decoupling capacitors - C_{AVDD} should be placed as close as possible to AVDD pin. $C_{PVDDL/R}$ should be placed as individually close as possible to PVDDL/R pins. Large (100μF or greater) bulk power supply decoupling capacitors should be placed close to ft2725.

Grounding - The AVDD decoupling capacitor should be grounded to analog ground AGND. The PVDD decoupling capacitors should be grounded to power ground PGND. Analog ground and power ground should be connected to a central ground in a star manner or a ground plan.

EMI - The ferrite EMI filter as shown in Figure 31 should be placed as close to the output terminals as possible for the best EMI performance. Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.

TYPICAL APPLICATION CIRCUITS

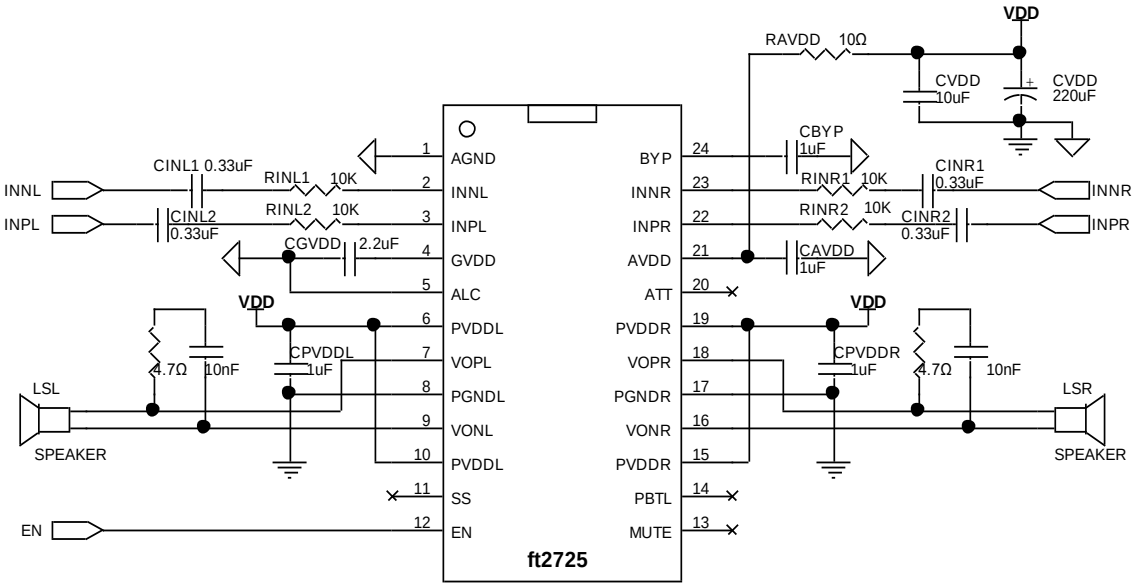


Figure 33: Differential Inputs in ALC Mode with Fast ALC Attack

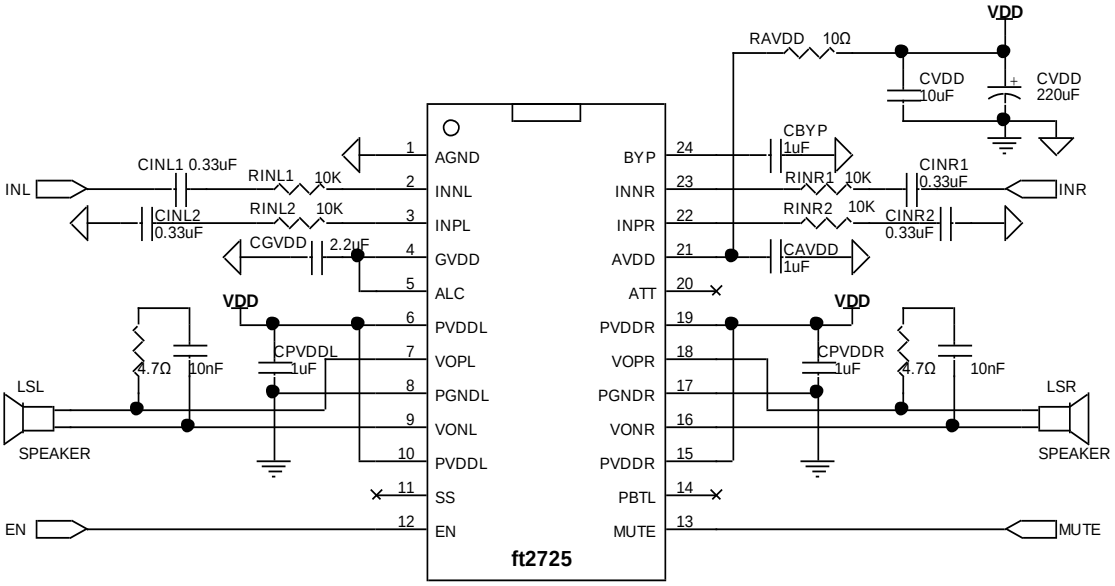


Figure 34: Single-Ended Inputs in Non-ALC Mode

TYPICAL APPLICATION CIRCUITS (Cont'd)

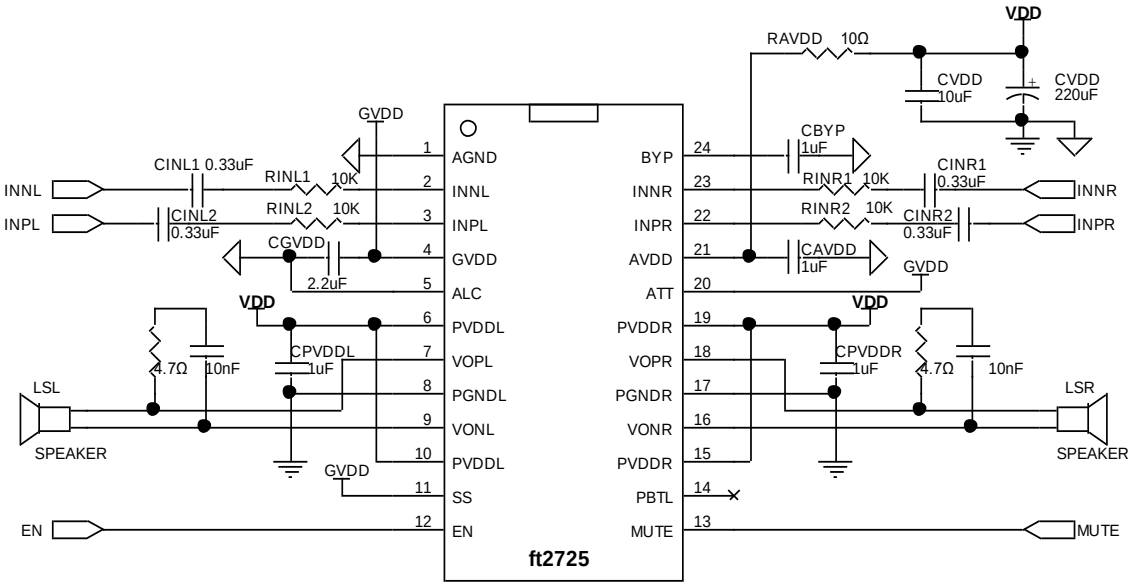


Figure 35: Differential Inputs in ALC Mode with Slow ALC Attack & Spread–Spectrum Audio Outputs

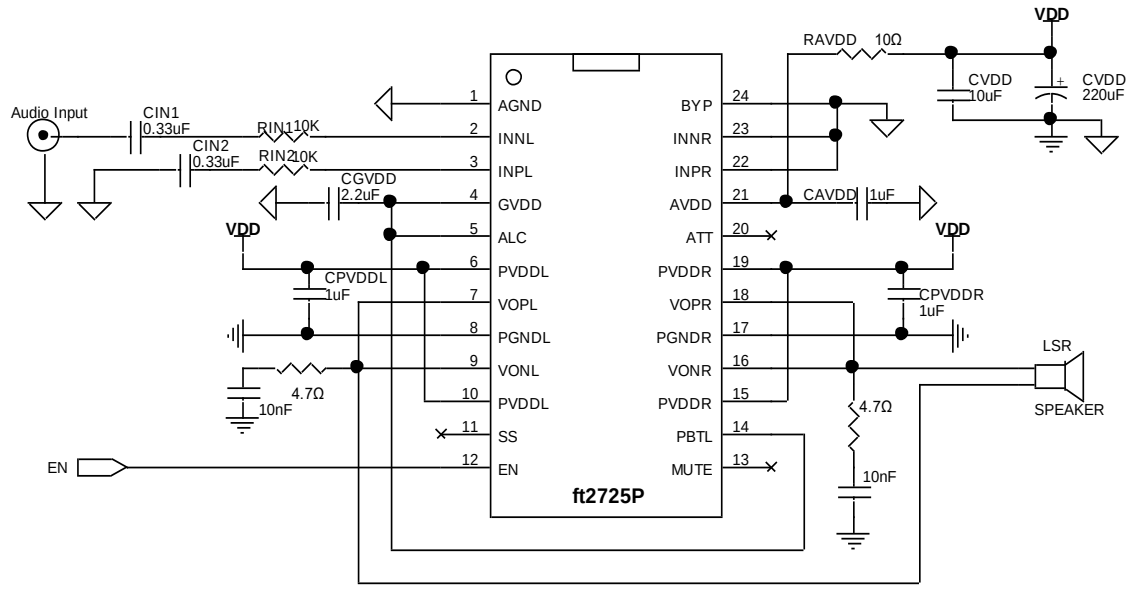
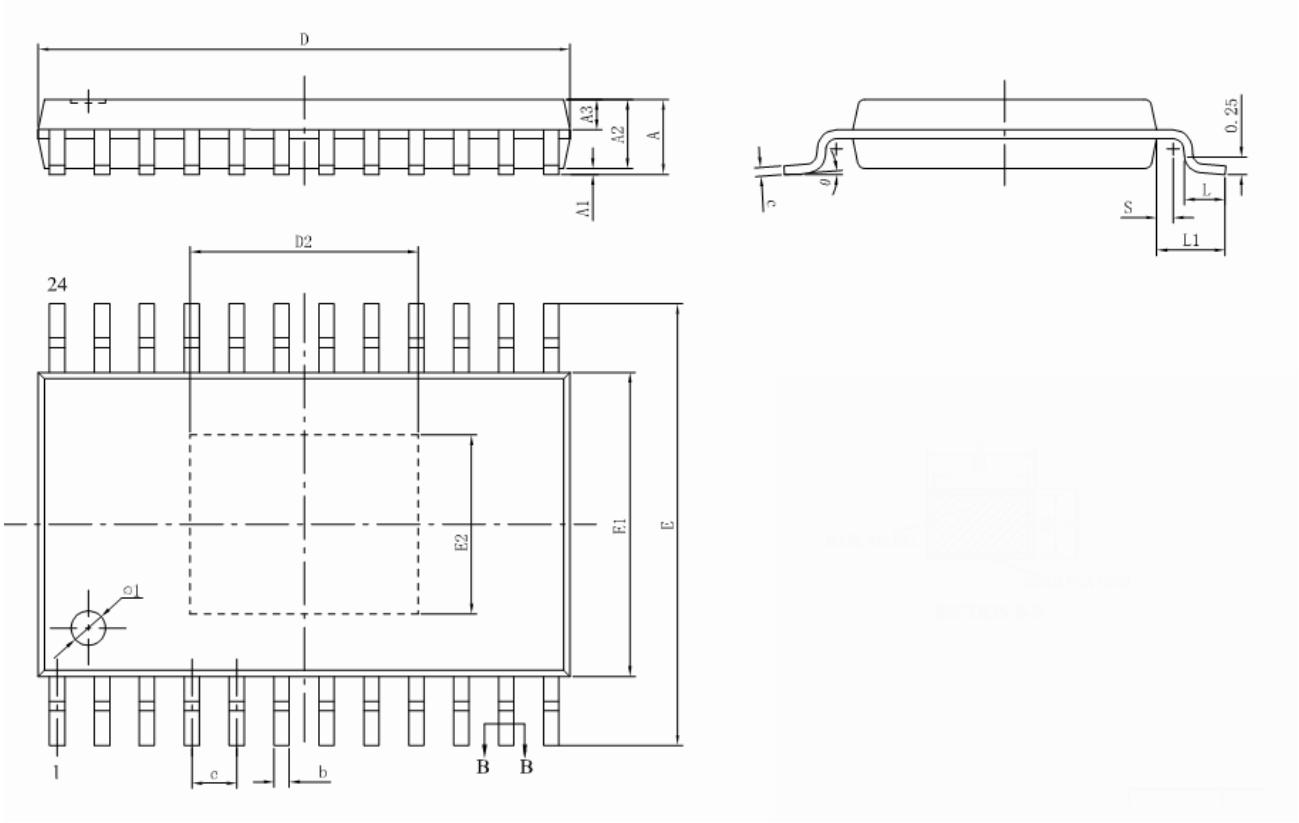


Figure 36: Single-Ended Input in Non-ALC Mode in PBTL Configuration

PHYSICAL DIMENSIONS

TSSOP-24L PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
S	0.20	—	—
Ø1	Ø0.8X0.05~0.10DP		
θ	0	—	8°

Unit: mm

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