ft3128

High Power Stereo Class-D Audio Power Amplifier with Adjustable Power Limit & Automatic Level Control

GENERAL DESCRIPTION

The ft3128 is a high power, high efficiency, stereo Class-D audio power amplifier with adjustable power limit (APL) and automatic level control (ALC). It operates with a wide range of supply voltages from 5.5V to 20V. With 15V supply voltage, it can deliver into a pair of 4Ω speakers an output power of 22W per channel with 1% THD+N, or an ALC output power of 20W per channel with 0.5% THD+N.

The high efficiency (up to 90%) of ft3128 extends battery life in playing music and allows it to deliver an output power of 2X20W without the need for a bulky heat sink on a two-layer system board. The high PSRR (75dB @ 1kHz in SSM) and low EMI emission of ft3128 reduce system design and manufacturing complexities and lower system cost.

The ft3128 features APL and ALC. The APL limits peak audio outputs to a user-defined value to protect audio speakers from excessive power dissipation and over-load. The ALC adjusts the voltage gain of the audio amplifiers in response to over-limit audio inputs, eliminating output clipping distortion while maintaining a maximally allowed dynamic range of audio outputs. The limiting voltage of APL and ALC can be either a user-defined value or the supply voltage.

The ft3128 facilitates two PWM modulation schemes for the Class-D audio amplifiers: Dual-Side-Modulation (DSM) and Single-Side-Modulation (SSM).

The ft3128 can be configured into driving either a pair of speakers in BTL for stereo applications or a single speaker in Parallel BTL (PBTL) for mono applications.

In ft3128, comprehensive protection modes against various operating faults ensure its safe and reliable operation.

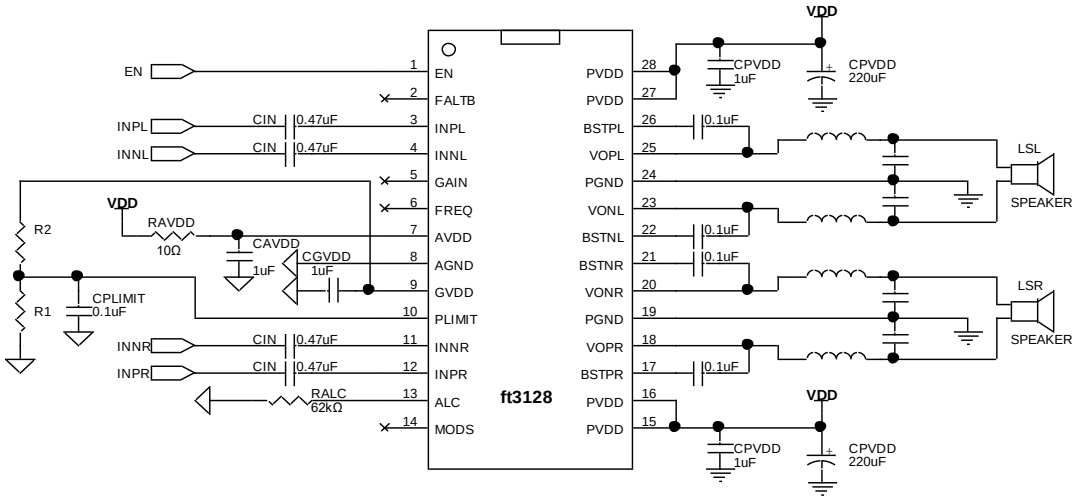
FEATURES

- Wide range of supply voltages from 5.5V to 20V
- Adjustable power limit to safeguard audio speakers
- Automatic level control to eliminate output clipping
- Four selectable gain settings: 20/26/30/34dB
- Three selectable ALC dynamic characteristics
- Two selectable PWM frequencies with optional spread-spectrum: 360/500kHz
- Two modulation schemes: SSM, DSM
- Optional PBTL configuration for mono applications
- Maximum output power (THD+N=1%) in Non-ALC
  32W/Ch (V_{DD}=18V, 4Ω+33μH, BTL)
  18W/Ch (V_{DD}=18V, 8Ω+33μH, BTL)
  45W (V_{DD}=18V, 3Ω+15μH, PBTL)
- ALC output power (THD+N≤0.5%) in ALC
  30W/Ch (V_{DD}=18V, 4Ω+33μH, BTL)
  15W/Ch (V_{DD}=18V, 8Ω+33μH, BTL)
  40W (V_{DD}=18V, 3Ω+15μH, PBTL)
- Wide ALC dynamic range: 12dB (V_{DD}=12V)
- Low THD+N: 0.1% (V_{DD}=15V, 4Ω+33μH, P_O=15W/Ch)
- High PSRR: 75dB @ 1kHz in SSM
- High efficiency up to 90%
- Protection modes against various operating faults including under-voltage, over-voltage, over-current, over-temperature, and DC-detect
- Thermal-enhanced package: TSSOP-28L

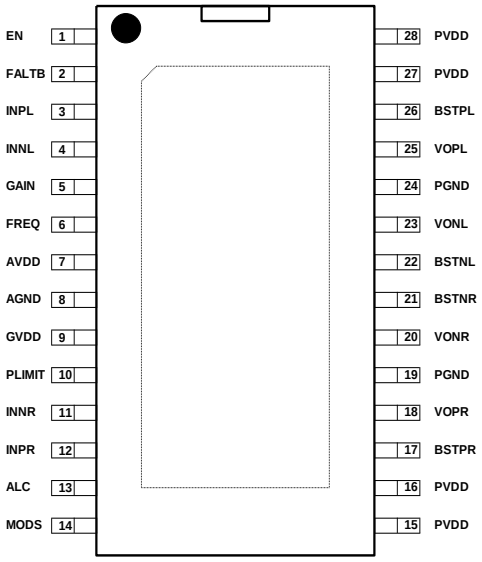
APPLICATIONS

- Blue Tooth Speakers
- Performance Audio Speakers
- Soundbars

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION



ft3128P (TOP VIEW)

FUNCTIONAL BLOCK DIAGRAM

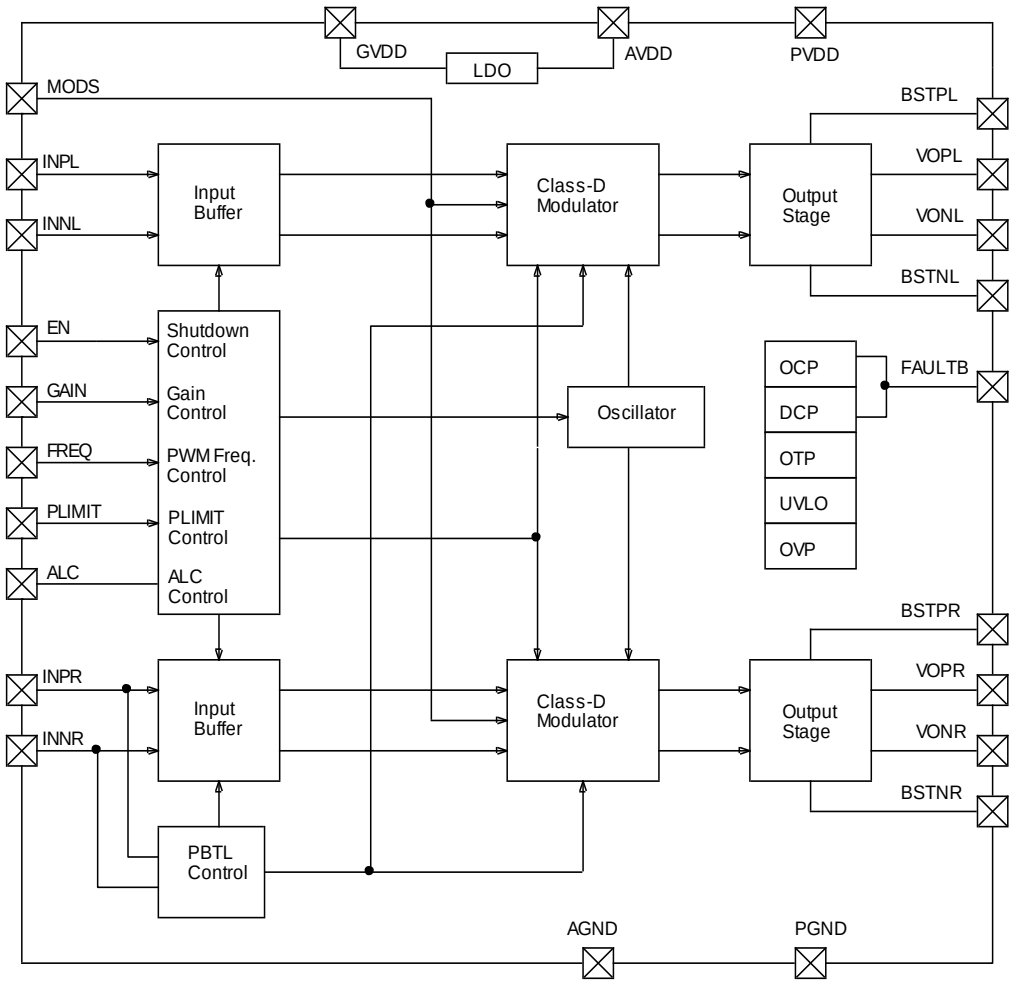


Figure 1: Simplified Functional Block Diagram of ft3128

PIN ASSIGNMENT & DESCRIPTION

NAME	PIN #	TYPE	DESCRIPTION
EN	1	DI	**Chip Enable** (Active High) with an on-chip 250kΩ pulldown resistor to ground. A TTL logic input in compliance with AVDD.
FAULTB	2	DO	Open-drain output indicating operational faults of OCP or DCP. Both faults can be set for auto-recovery by externally connecting FAULTB to EN. Otherwise, both OCP and DCP faults must be reset by cycling EN. A TTL logic output in compliance with AVDD.
INPL	3	AI	Left-channel non-inverting audio input biased at one half of GVDD.
INNL	4	AI	Left-channel inverting audio input biased at one half of GVDD.
GAIN	5	AO	**Voltage Gain Select** with an on-chip 250kΩ pulldown resistor to ground. Connect to a resistor to ground to set the voltage gain of the audio amplifiers.
FREQ	6	AO	**PWM Frequency Select** with an on-chip 250kΩ pulldown resistor to ground. Connect to a resistor to ground to set the PWM frequency with optional spread-spectrum.
AVDD	7	P	Analog supply. Connect to a 1µF capacitor for decoupling. Also, add a decoupling resistor of 10Ω between this pin and the system power supply for high-frequency filtering.
AGND	8	G	Analog ground. Connect to the system ground GND.
GVDD	9	AO	Internally generated reference voltage at 5.6V. Connect to a 1µF capacitor for decoupling.
PLIMIT	10	AI	Adjustable Power Limit. Connect to a resistor divider from GVDD to AGND to set the output voltage limit. Add a 0.1µF capacitor for decoupling.
INNR	11	AI	Right-channel inverting audio input biased at one half of GVDD. Connect to ground (without decoupling capacitor) for mono mode in PBTL configuration.
INPR	12	AI	Right-channel non-inverting audio input biased at one half of GVDD. Connect to ground (without decoupling capacitor) for mono mode in PBTL configuration.
ALC	13	AO	**ALC Mode Select** with an on-chip 250kΩ pulldown resistor to ground. Connect to a resistor to ground to set ALC dynamic characteristic.
MODS	14	DI	**PWM Modulation Select** with an on-chip 250kΩ pulldown resistor to ground. A TTL logic input in compliance with GVDD.
PVDD	15, 16	P	Power supply inputs for right-channel H-bridge. Connect to a 1µF capacitor for decoupling. The power supplies for right-channel and left-channel H-bridges are internally shorted.
BSTPR	17	AO	Connection to a bootstrap holding capacitor for right-channel non-inverting output, VOPR. Place a 0.1µF ceramic capacitor between this pin and VOPR.
VOPR	18	AO	Right-channel non-inverting audio output terminal.
PGND	19	G	Power ground for right-channel H-bridge. Connect to the system ground GND. The power ground for right-channel and left-channel H-bridges are internally shorted.
VONR	20	AO	Right-channel inverting audio output terminal.
BSTNR	21	AO	Connection to a bootstrap holding capacitor for right-channel inverting output, VONR. Place a 0.1µF ceramic capacitor between this pin and VONR.
BSTNL	22	AO	Connection to a bootstrap holding capacitor for left-channel inverting output, VONL. Place a 0.1µF ceramic capacitor between this pin and VONL.
VONL	23	AO	Left-channel inverting audio output terminal.
PGND	24	G	Power ground for left-channel H-bridge. Connect to the system ground GND. The power ground for right-channel and left-channel H-bridges are internally shorted.
VOPL	25	AO	Left-channel non-inverting audio output terminal.
BSTPL	26	AO	Connection to a bootstrap holding capacitor for left-channel non-inverting output, VOPL. Place a 0.1µF ceramic capacitor between this pin and VOPL.
PVDD	27, 28	P	Power supply inputs for left-channel H-bridge. Connect to a 1µF capacitor for decoupling. The power supplies for right-channel and left-channel H-bridges are internally shorted.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ft3128P	0°C to +85°C	TSSOP-28L

REVISION HISTORY

Initial Release 1.0 (December 2017)

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER		VALUE
Supply Voltage Pins	AVDD, PVDD	-0.3V to 26V
Digital I/O Pins	EN, FAULTB	-0.3V to V_{DD}+0.3V
	MODS	-0.3V to V_{GVDD}+0.3V
Analog Output Pins	GVDD	-0.3V to 7V
	ALC, GAIN, FREQ	-0.3V to V_{GVDD}+0.3V
Analog Input Pins	INPL/R, INNL/R, PLIMIT	-0.3V to V_{GVDD}+0.3V
All other Pins		-0.3V to V_{DD}+0.3V
ESD Ratings-Human Body Model (HBM)		3000V
Operating Junction Temperature		0°C to +150°C
Storage Temperature		-65°C to +150°C
Maximum Soldering Temperature (@10 second duration)		260°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may damage the device or affect device reliability.

POWER DISSIPATION RATINGS (Note 2, 3)

PACKAGE	$T_A \leq$ +25°C	T_A = +70°C	T_A = +85°C	Θ_{JA}
TSSOP-28L	4.5W	2.9W	2.3W	28°C/W

Note 2: The thermal pad of the package must be directly soldered onto a grounded metal island, as a thermal sink, on the system board.
Note 3: The power dissipation ratings are for a two-side, two-plane printed circuit board.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (Note 4,5)	V_{DD}	PVDD, AVDD	5.5		20	V
Operating Ambient Temperature	T_A		0		85	°C
Minimum Load Impedance (Note 5, 6)	R_L	BTL Configuration (Stereo)	3.2	4		Ω
		PBTL Configuration (Mono)	1.6	3		Ω
Analog Input Level	V_{INNR} V_{INPR}	PBTL Configuration (Mono)	0		0.3	V
Audio Input Capacitor	C_{IN}	@ INPL/R, INNL/R	0.1	0.47		μF
Bootstrap Holding Capacitor	$C_{BSTPL/R}$ $C_{BSTNL/R}$	@ BSTPL/R, BSTNL/R	0.047	0.1	0.22	μF
PLIMIT Voltage	V_{PLIMIT}	PLIMIT	0		V_{GVDD}	V
Digital “High” Input Voltage	V_{IH}	EN	2		V_{DD}	V
		MODS	2		V_{GVDD}	V
Digital “Low” Input Voltage	V_{IL}	EN, MODS			0.8	V
Maximum Load Current from GVDD	I_{LOAD}	GVDD		2	5	mA
Modulation Scheme Select	MODS	Single-Side-Modulation (SSM)	Low or Open			
		Double-Side-Modulation (DSM)	High			
Voltage Gain Select	GAIN	26dB	Open			
		30dB	Short to GND			
		34dB	68kΩ to GND			
		20dB	220kΩ to GND			
ALC Mode Select	ALC	Non-ALC	Open			
		ALC-1	Short to GND			
		ALC-2	68kΩ to GND			
		ALC-3	220kΩ to GND			
PWM Frequency Select	FREQ	360kHz	Open			
		360kHz with Spread-Spectrum	Short to GND			
		500kHz	68kΩ to GND			
		500kHz with Spread-Spectrum	220kΩ to GND			

Note 4: The peak supply voltage including its tolerance over various operating conditions must not exceed its absolute-maximum-rated value (26V). Exposure to absolute-maximum-rated supply voltage may damage the device or affect device reliability permantly.

Note 5: For high power applications, the maximum power supply V_{DD} that can be applied to the ft3128 is largely limited by the thermal dissipation capability of the package and the system board layout.

Note 6: The ft3128 is specfied with an 8Ω resistive load in series with 33μH inductive load or with a 4Ω resistive load in series with 33μH inductive load or with a 3Ω resistive load in series with 15μH inductive load (in PBTL configuration). Without inductive loads, the maximum continous output power will severely suffer from efficiency and thermal degradation.

IMPORTANT APPLICATION NOTES

Output Power Considerations

1. The maximum output power of ft3128 is determined primarily by the power supply (output voltage and current) and speaker impedance. As a high power audio amplifier, the maximum output power of ft3128 can be severely limited by the thermal dissipation capability of the system board layout.
2. The ft3128 is packaged with an exposed thermal pad on the underside of the device. Solder the thermal pad directly onto a large grounded metal island (GND) underneath the package, as a thermal sink for proper thermal dissipation. On the grounded metal island, place several rows of solid, equally-spaced vias connecting to the bottom layer of the system board. Failure to do so can severely limit its thermal dissipation capability. It might even cause the device going into over-temperature shutdown occasionally.
3. Use wide open areas around the ft3128 on the top and bottom layers of the system board as the ground plane GND. Place lots of solid vias connecting the top and bottom layers of GND. Furthermore, for proper thermal dissipation, reserve wide and uninterrupted GND areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow in the proximity of the device.
4. The power ground pins, PGND, are directly shorted to the ground plane GND, which serves as a central “star” ground for the ft3128. Use a single point of connection between the analog ground AGND and the ground plane GND to minimize the coupling of high-current switching noise onto audio signals.
5. The power supply pins, PVDD, for the audio amplifiers’ output stages are directly connected together with short and wide metal traces.
6. Use direct and low-impedance traces from the audio outputs (VOPL/R and VONL/R) to their individual output filters and speakers.

Output Filter Considerations

7. For most applications, the ft3128 does not require a LC output filter when speaker wires are less than 10cm.
8. A ferrite bead filter constructed from a ferrite bead and a ceramic capacitor can be used to suppress EMI. Choose a ferrite bead with a rated current no less than 3A for 8Ω loads, 5A for 4Ω loads, and 7A for 3Ω or less loads (in PBTL configuration). Place the filter tightly together and as close as possible to the audio amplifier’s output pins. A ferrite bead filter can also reduce high-frequency interference.
9. For applications where EMC requirements are extremely stringent or speaker wires are long, use a second-order LC lowpass filter. Place the filter tightly together and as close as possible to the audio amplifier’s output pins. The LC output filter must be designed specifically for the speaker load since the load impedance affects the quality factor of the filter.

General Considerations

10. The ft3128 requires adequate power supply decoupling to ensure its peak output power, high efficiency, low distortion, and low EMI emissions. Place each supply decoupling capacitor as individually close as possible to AVDD and PVDD pins.
11. Place a small decoupling resistor (10Ω) between the system power supply and AVDD to prevent high frequency Class-D transient spikes from interfering with the on-chip linear amplifiers.
12. For best noise performance, use differential inputs from the audio source for ft3128. In single-ended input applications, the unused inputs of ft3128 must be AC-grounded at the audio source. Also, take care to match the impedances seen at two differential inputs closely.
13. The maximum input signal dictates the required voltage gain to achieve the desired maximum output power. For best noise performance, consider a voltage gain as low as possible.
14. Do not alter the logic state of the MODS pin while the device is in operation. To change the setting of the pin, the device must be first brought into shutdown mode by pulling the EN pin low for at least 5 milliseconds before it can be restored to its normal operation.

TEST SETUP FOR ELECTRICAL & PERFORMANCE CHARACTERISTICS

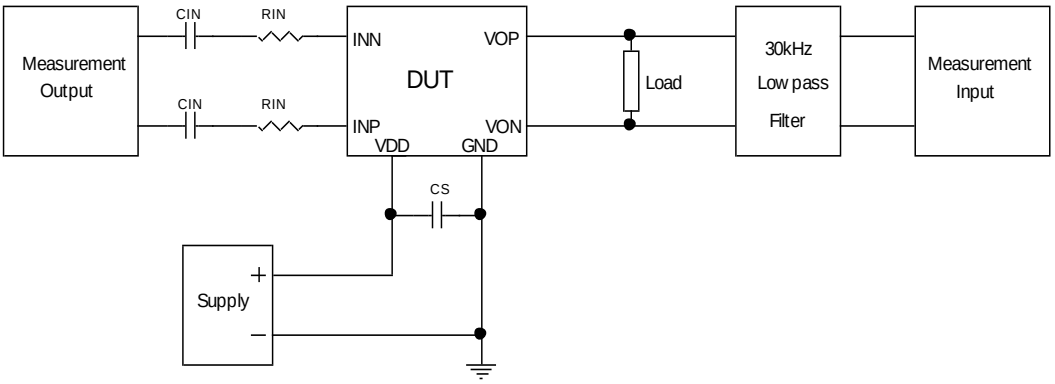


Figure 2: Test Setup Diagram for ft3128

All parameters specified in Electrical and Typical Performance Characteristics sections are measured according to the conditions:

1. The two differential inputs are shorted for common-mode input voltage measurement. All other parameters are taken with input resistors R_{IN}=0kΩ and input capacitors C_{IN}=0.47μF, unless otherwise specified.
2. The supply decoupling capacitors C_{PVDD}=1μF//220μF are placed close to the device.
3. A 33μH inductor was placed in series with the load resistor to emulate a speaker load for all AC and dynamic parameters.
4. The 33kHz lowpass filter is added even if the analyzer has an internal lowpass filter. An RC lowpass filter (100Ω, 47nF) is used on each output for the data sheet graphs.

ELECTRICAL CHARACTERISTICS

V_{DD}=12V, f=1kHz, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=0kΩ, GAIN=NC (A_V=26dB), FREQ=NC (f_{PWN}=360kHz), MODS=NC (SSM), ALC=68kΩ to GND (ALC-2), V_{PLIMIT}=V_{GVDD}, C_{PVDD}=1μF//220μF, C_{AVDD}=1μF, C_{GVDD}=1μF, C_{PLIMIT}=0.1μF, C_{BPL}=C_{BNL}=C_{BPR}=C_{BNR}=0.1μF, both channels driven, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage	PVDD, AVDD		5.5		20	V
I_{VDD}	Supply Quiescent Current	Inputs AC-grounded No Load	SSM	7	10	15	mA
			DSM	10	14	20	mA
I_{MUTE}	Mute Current	PLIMIT shorted to GND		5	8	12	mA
I_{SD}	Shutdown Current	EN=Low	SSM		30	50	μA
			DSM		50	80	μA
V_{UVLOUP}	Supply Voltage UVLO Detection	V_{DD} Rising			4.6		V
V_{UVLODN}	Supply Voltage UVLO Release	V_{DD} Falling			4.3		V
V_{OVPUP}	Supply Voltage OVP Detection	V_{DD} Rising			24		V
V_{OVPDN}	Supply Voltage OVP Release	V_{DD} Rising			23		V
V_{GVDD}	Voltage Regulator Output	No Load		5.2	5.6	6.0	V
V_{COMM}	Input Common-Mode Bias	INPL/R, INNL/R		2.6	2.8	3.0	V
V_{IH}	Digital “High” Input Voltage	EN		2.0		V_{DD}	V
		MODS		2.0		V_{GVDD}	V
V_{IL}	Digital “Low” Input Voltage	EN, MODS				0.8	V
V_{OL}	Digital “Low” Output Voltage	FAULTB R_{PULLUP}=100kΩ, V_{DD}=18V				0.4	V
R_{DOWN}	Pulldown Resistor to Ground	EN, MODS, ALC, GAIN, FREQ			250		kΩ
R_{OUT-SD}	Output Resistance in Shutdown	@ VOPL/R, VONL/R, EN=Low			3		kΩ
V_{GAIN} V_{FREQ} V_{ALC}	Voltage Level @ GAIN, FREQ, ALC pins	Open		1.85	3.0		V
		Shorted to GND			0	0.20	V
		68kΩ to GND		0.40	0.55	0.75	V
		220kΩ to GND		1.05	1.30	1.60	V
R_{IN}	Input Resistance @ INPL/R, INNL/R pins	Open			30		kΩ
		R_{GAIN}=0kΩ			20		kΩ
		R_{GAIN}=68kΩ			12		kΩ
		R_{GAIN}=220kΩ			60		kΩ
A_V	Voltage Gain	Open			26		dB
		R_{GAIN}=0kΩ			30		dB
		R_{GAIN}=68kΩ			34		dB
		R_{GAIN}=220kΩ			20		dB
f_{SW}	PWM Frequency	Open or R_{FREQ}=0kΩ			360		kHz
		R_{FREQ}=68kΩ or R_{FREQ}=220kΩ			500		kHz
T_{OTSD}	Over-Temperature Threshold				160		°C
T_{HYS}	Over-Temperature Hysteresis				20		°C

ELECTRICAL CHARACTERISTICS

V_{DD}=12V, f=1kHz, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=0kΩ, GAIN=NC (A_V=26dB), FREQ=NC (f_{PWN}=360kHz), MODS=NC (SSM), ALC=68kΩ to GND (ALC-2), V_{PLIMIT}=V_{GVDD}, C_{PVDD}=1μF//220μF, C_{AVDD}=1μF, C_{GVDD}=1μF, C_{PLIMIT}=0.1μF, C_{BPL}=C_{BNL}=C_{BPR}=C_{BNR}=0.1μF, both channels driven, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CLASS-D AMPLIFIER (V_{DD}=12V, R_L=4Ω+33μH, Both Channels Driven)						
$P_{O, MAX}$	Maximum Output Power	THD+N=1%		15		W/Ch
$P_{O, ALC}$	ALC Output Power	V_{IN}=0.50V_{RMS}		13		W/Ch
THD+N	Total Harmonic Distortion+Noise	Po=10W/Ch, Non-ALC Mode		0.1		%
		V_{IN}=0.50V_{RMS}, ALC Mode		0.3		%
η	Power Efficiency	Po=10W/Ch, Non-ALC Mode		87		%
		V_{IN}=0.50V_{RMS}, ALC Mode		88		%
V_{OS}	Output Offset Voltage	No Load		±5	±15	mV
V_N	Idle-Channel Noise	Inputs AC-Grounded, A-weighted		140		μV_{RMS}
SNR	Signal-to-Noise Ratio	Maximum Output (7V_{RMS}) A-weighted		94		dB
PSRR	Power Supply Rejection Ratio	f=217Hz		80		dB
		f=1kHz		75		dB
CMRR	Common Mode Rejection Ratio	f=1kHz, V_{IN}=0.2V_{RMS}		60		dB
Crosstalk	Channel Separation	Po=10W/Ch, f=1kHz		75		dB
A_{MAX}	Maximum ALC Attenuation	V_{DD}=12V		12		dB
		V_{DD}=15V		10		dB
		V_{DD}=18V		9		dB
$T_{STARTUP}$	Startup Time	Including Fade-In Time		50		ms
T_{SD}	Shutdown Settling Time	Including Fade-Out Time		5		ms
ADJUSTABLE POWER LIMIT (APL)						
V_{PLIMIT}	Mute Mode				0.3	V
	APL with Adjustable Limiting	V_{GVDD}=5.6V, V_{DD}=18V	0.7		3.4	V
	ALC with Adjustable Limiting	V_{GVDD}=5.6V, V_{DD}=18V	0.7		3.0	V
	APL Disabled	V_{GVDD}=5.6V	4.5		V_{GVDD}	V
	ALC with V_{DD} Limiting	V_{GVDD}=5.6V	4.5		V_{GVDD}	V
V_{LIMIT}	Output Limit Voltage	V_{PLIMIT}=1.5V	7.5	8.7	9.6	V
DC CURRENT PROTECTION (DCP)						
V_{DCP}	DC Detect Threshold	V_{DD}=12V		2.1		V
		V_{DD}=15V		2.7		V
		V_{DD}=18V		3.5		V
FADE-IN & FADE-OUT						
T_{FADEIN}	Fade-In Time			10		ms
$T_{FADEOUT}$	Fade-Out Time			3		ms

ELECTRICAL CHARACTERISTICS

V_{DD}=15V, Load=4Ω+33μH (BTL), both channels driven, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
$P_{O, MAX}$	Maximum Output Power	THD+N=1%	V_{DD}=15V		22		W/Ch
			V_{DD}=16.8V		27		W/Ch
			V_{DD}=18V		32		W/Ch
$P_{O, ALC}$	ALC Output Power	V_{DD}=15V, V_{IN}=0.60V_{RMS}			20		W/Ch
		V_{DD}=16.8V, V_{IN}=0.65V_{RMS}			25		W/Ch
		V_{DD}=18V, V_{IN}=0.70V_{RMS}			30		W/Ch
THD+N	Total Harmonic Distortion+Noise	Po=15W/Ch, Non-ALC Mode			0.1		%
		V_{IN}=0.60V_{RMS}, ALC Mode			0.5		%
η	Power Efficiency	Po=15W/Ch, Non-ALC Mode			86		%
		V_{IN}=0.60V_{RMS}, ALC Mode			87		%
V_N	Idle-Channel Noise	Inputs AC-Grounded, A-weighted			140		μV_{RMS}
SNR	Signal-to-Noise Ratio	Maximum Output (10V_{RMS}) A-weighted			97		dB

V_{DD}=18V, Load=8Ω+33μH (BTL), both channels driven, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$P_{O, MAX}$	Maximum Output Power	THD+N=1%		18		W/Ch
$P_{O, ALC}$	ALC Output Power	V_{IN}=0.70V_{RMS}		15		W/Ch
THD+N	Total Harmonic Distortion+Noise	Po=10W/Ch, Non-ALC Mode		0.1		%
		V_{IN}=0.70V_{RMS}, ALC Mode		0.4		%
η	Power Efficiency	Po=10W/Ch, Non-ALC Mode		88		%
		V_{IN}=0.70V_{RMS}, ALC Mode		91		%
V_N	Idle-Channel Noise	Inputs AC-Grounded, A-weighted		150		μV_{RMS}
SNR	Signal-to-Noise Ratio	Maximum Output (12V_{RMS}) A-weighted		98		dB

V_{DD}=18V, Load=3Ω+15μH (PBTL), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
$P_{O, MAX}$	Maximum Output Power	THD+N=1%	Load=3Ω+15μH		45		W
			Load=2Ω+15μH		66		W
$P_{O, ALC}$	ALC Output Power	V_{IN}=0.70V_{RMS}	Load=3Ω+15μH		40		W
			Load=2Ω+15μH		60		W
THD+N	Total Harmonic Distortion+Noise	Po=30W, Non-ALC Mode			0.1		%
		V_{IN}=0.70V_{RMS}, ALC Mode			0.4		%
η	Power Efficiency	Po=30W, Non-ALC Mode			82		%
		V_{IN}=0.70V_{RMS}, ALC Mode			82		%
V_N	Idle-Channel Noise	Inputs AC-Grounded, A-weighted			160		μV_{RMS}
SNR	Signal-to-Noise Ratio	Maximum Output (12V_{RMS}) A-weighted			97		dB

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=12V, f=1kHz, Load=4Ω+33μH, C_{IN}=0.47μF, R_{IN}=0kΩ, GAIN=NC (A_V=26dB), FREQ=NC (f_{PWN}=360kHz), MODS=NC (SSM), ALC=68kΩ to GND (ALC-2), V_{PLIMIT}=V_{GVDD}, C_{PVDD}=1μF//220μF, C_{AVDD}=1μF, C_{GVDD}=1μF, C_{PLIMIT}=0.1μF, C_{BPL}=C_{BNL}=C_{BPR}=C_{BNR}=0.1μF, both channels driven, T_A=25°C, unless otherwise specified.

DESCRIPTION	CONDITIONS	FIGURE #
Maximum Output Power vs. Supply Voltage	R_L=8Ω+33μH (BTL), Non-ALC Mode, 10% & 1% THD+N	3
	R_L=4Ω+33μH (BTL), Non-ALC Mode, 10% & 1% THD+N	4
	R_L=3Ω+15μH (PBTL), Non-ALC Mode, 10% & 1% THD+N	5
ALC Output Power vs. Supply Voltage	R_L=8Ω+33μH (BTL), ALC-2 Mode, V_{IN}=0.70V_{RMS}	6
	R_L=4Ω+33μH (BTL), ALC-2 Mode, V_{IN}=0.70V_{RMS}	7
	R_L=3Ω+15μH (PBTL), ALC-2 Mode, V_{IN}=0.70V_{RMS}	8
Output Power vs. Input Voltage	V_{DD}=18V, R_L=8Ω+33μH (BTL), Non-ALC & ALC-2 Modes	9
	V_{DD}=12V, R_L=4Ω+33μH (BTL), Non-ALC & ALC-2 Modes	10
	V_{DD}=12V, R_L=3Ω+15μH (PBTL), Non-ALC & ALC-2 Modes	11
Output Power vs. V_{PLIMIT}	V_{DD}=18V, R_L=8Ω+33μH (BTL), V_{IN}=0.70V_{RMS}, APL & ALC-2 Modes	12
	V_{DD}=12V, R_L=4Ω+33μH (BTL), V_{IN}=0.50V_{RMS}, APL & ALC-2 Modes	13
	V_{DD}=12V, R_L=3Ω+15μH (PBTL), V_{IN}=0.50V_{RMS}, APL & ALC-2 Modes	14
THD+N vs. Output Power	V_{DD}=18V, R_L=8Ω+33μH (BTL), Non-ALC Mode	15
	V_{DD}=12V, R_L=4Ω+33μH (BTL), Non-ALC Mode	
	V_{DD}=12V, R_L=3Ω+15μH (PBTL), Non-ALC Mode	
THD+N vs. Input Voltage	V_{DD}=18V, R_L=8Ω+33μH (BTL), Non-ALC Mode	16
	V_{DD}=12V, R_L=4Ω+33μH (BTL), Non-ALC Mode	
	V_{DD}=12V, R_L=3Ω+15μH (PBTL), Non-ALC Mode	
THD+N vs. Input Frequency	V_{DD}=18V, R_L=8Ω+33μH (BTL), Po=5W/Ch, Non-ALC Mode	17
	V_{DD}=12V, R_L=4Ω+33μH (BTL), Po=5W/Ch, Non-ALC Mode	
	V_{DD}=12V, R_L=3Ω+15μH (PBTL), Po=10W, Non-ALC Mode	
Efficiency vs. Output Power	V_{DD}=18V, R_L=8Ω+33μH (BTL), Non-ALC Mode	18
	V_{DD}=12V, R_L=4Ω+33μH (BTL), Non-ALC Mode	
	V_{DD}=12V, R_L=3Ω+15μH (PBTL), Non-ALC Mode	
PSRR vs. Input Frequency	V_{DD}=12V, R_L=4Ω+33μH, Inputs AC-Grounded	19
Crosstalk vs. Input Frequency	V_{DD}=12V, R_L=4Ω+33μH	20
Quiescent Current vs. Supply Voltage	V_{DD}=12V, Inputs AC-Grounded, No Load, SSM & DSM	21
Output Voltage Limit vs. V_{PLIMIT}	V_{DD}=18V, No Load & R_L=8Ω+33μH & R_L=4Ω+33μH, APL Mode	22
Audio Outputs during ALC Attack	V_{IN}=0.34V_{RMS} → 1.0V_{RMS}, R_L=4Ω+33μH, ALC-2 Mode	23
Audio Outputs during ALC Release	V_{IN}=1.0V_{RMS} → 0.34V_{RMS}, R_L=4Ω+33μH, ALC-2 Mode	24
Audio Outputs during Startup	V_{DD}=12V, R_L=4Ω+33μH, V_{IN}=0.50V_{RMS}, ALC-2 Mode	25
Audio Outputs during Shutdown	V_{DD}=12V, R_L=4Ω+33μH, V_{IN}=0.50V_{RMS}, ALC-2 Mode	26

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

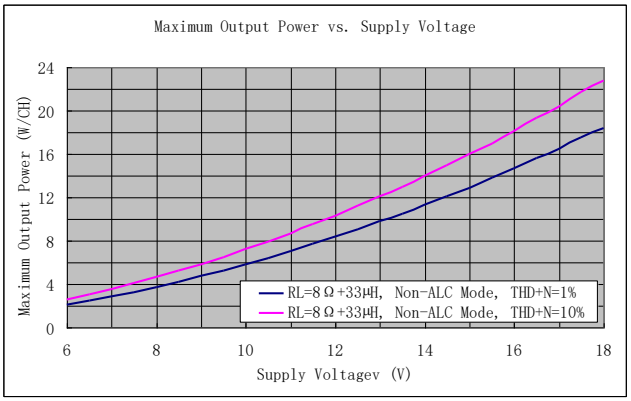


Figure 3: Maximum Output Power (BTL) vs. V_{DD}

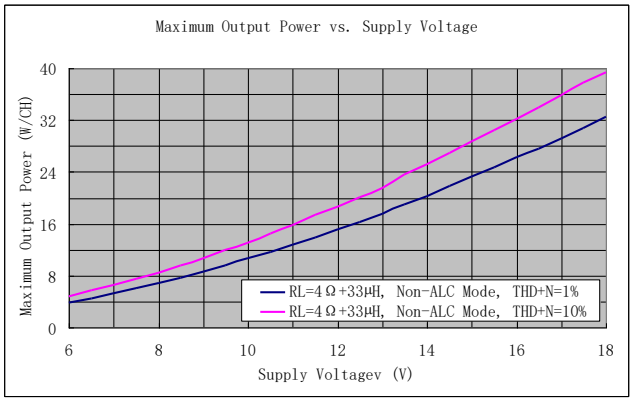


Figure 4: Maximum Output Power (BTL) vs. V_{DD}

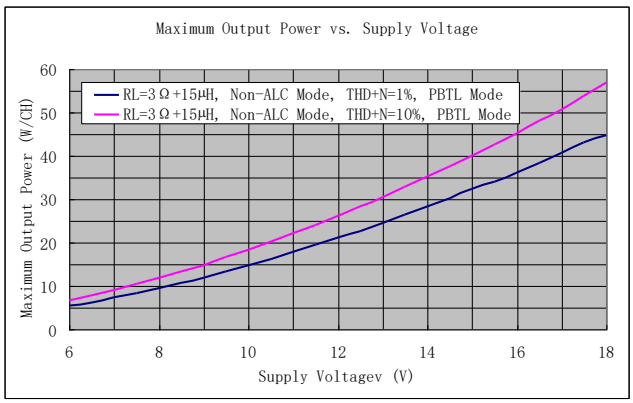


Figure 5: Maximum Output Power (PBTL) vs. V_{DD}

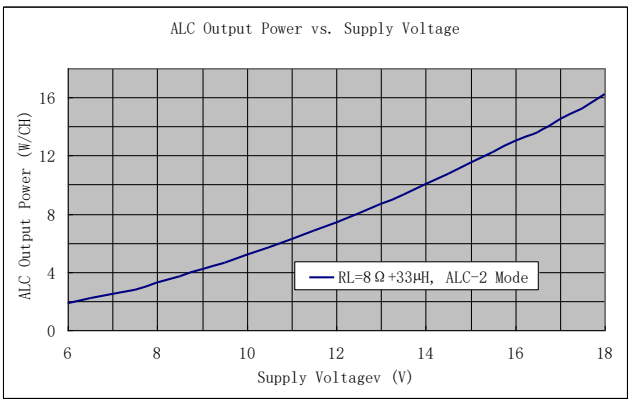


Figure 6: ALC Output Power (BTL) vs. V_{DD}

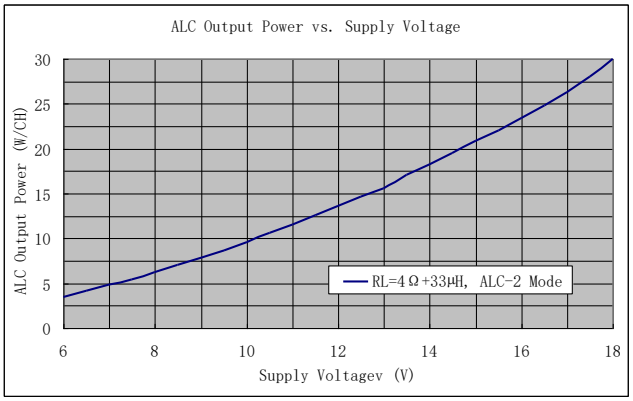


Figure 5: ALC Output Power (BTL) vs. V_{DD}

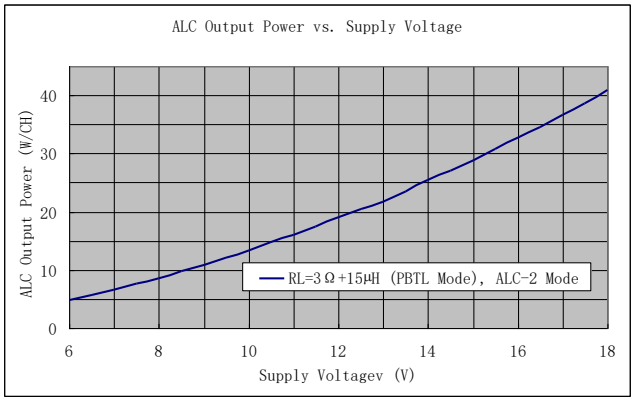


Figure 6: ALC Output Power (PBTL) vs. V_{DD}

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

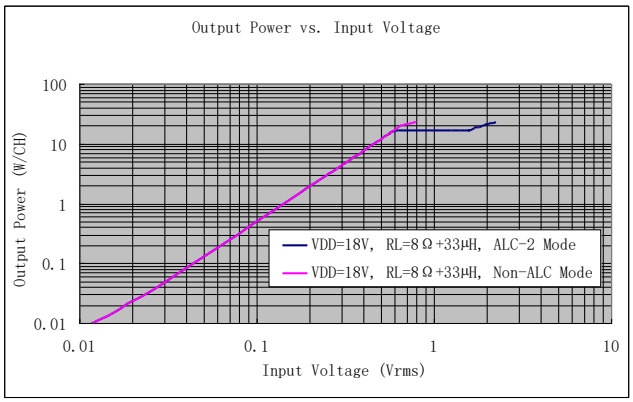


Figure 9: Output Power (BTL) vs. Input Voltage

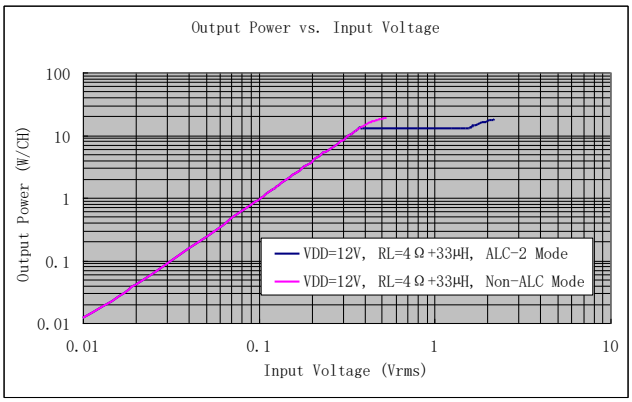


Figure 10: Output Power (BTL) vs. Input Voltage

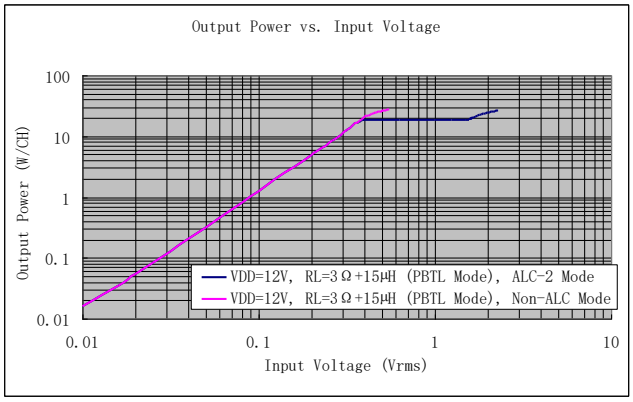


Figure 11: Output Power (PBTL) vs. Input Voltage

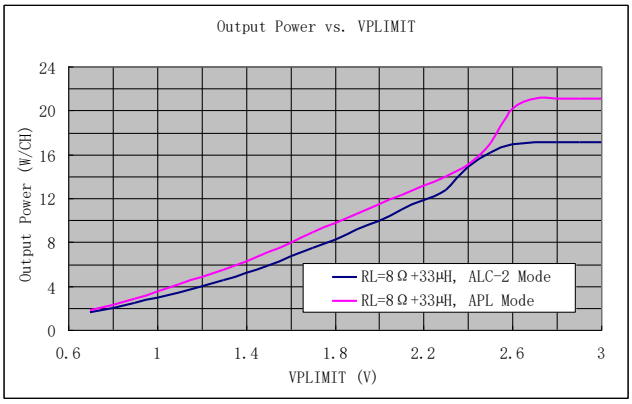


Figure 12: Output Power (BTL) vs. V_{PLIMIT}

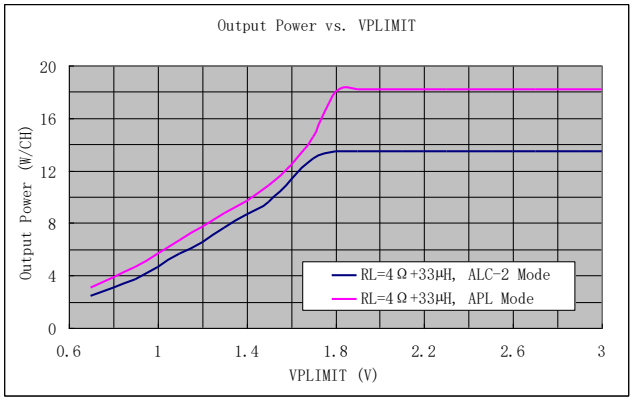


Figure 13: Output Power (BTL) vs. V_{PLIMIT}

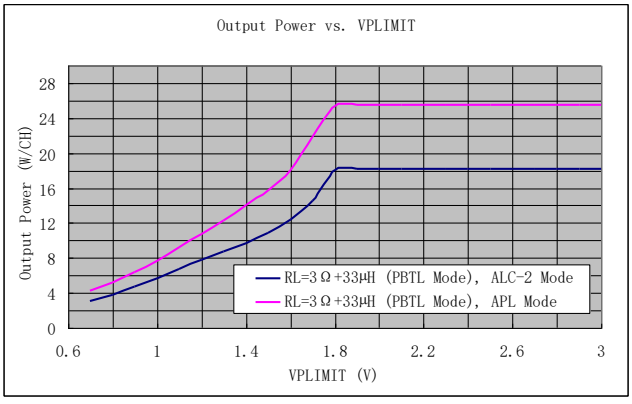


Figure 14: Output Power (PBTL) vs. V_{PLIMIT}

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

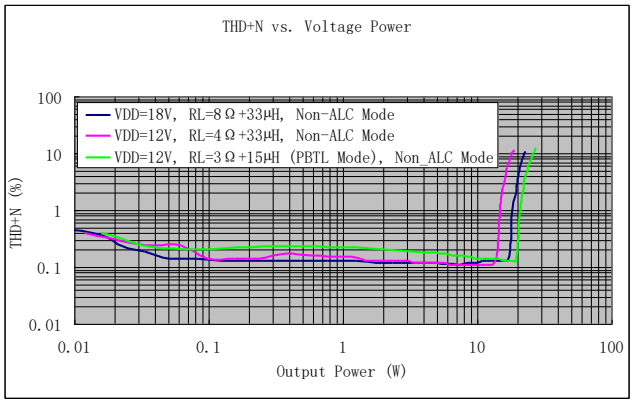


Figure 15: THD+N vs. Output Power

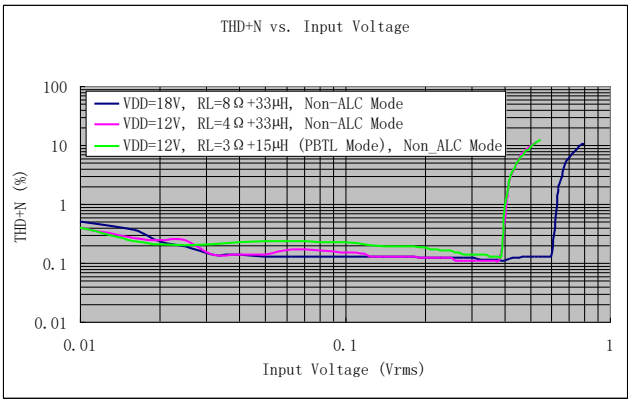


Figure 16: THD+N vs. Input Voltage

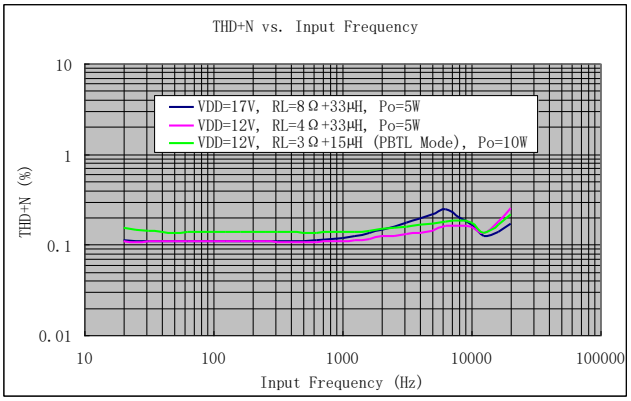


Figure 17: THD+N vs. Input Frequency

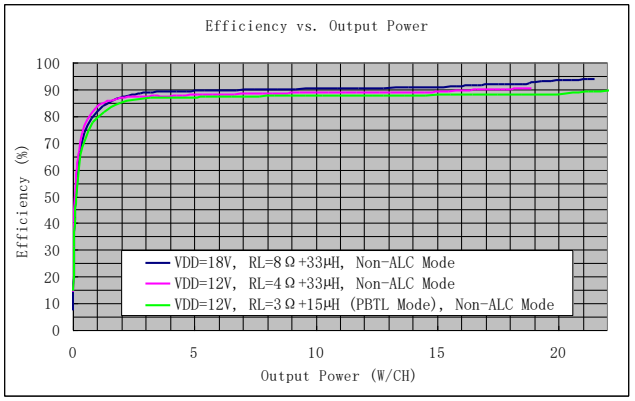


Figure 18: Efficiency vs. Output Power

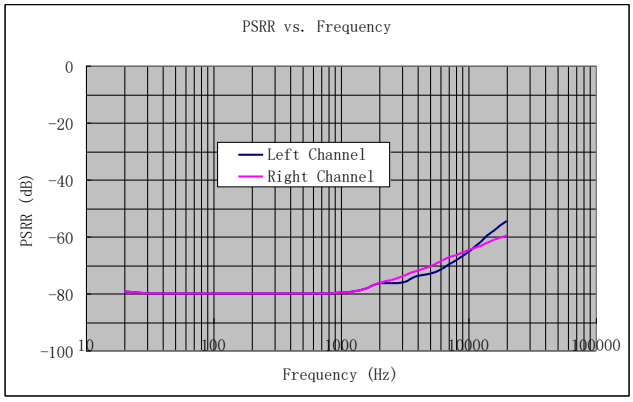


Figure 19: PSRR vs. Input Frequency

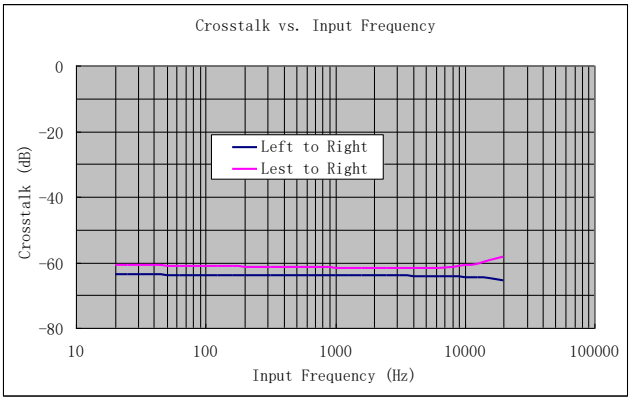


Figure 20: Crosstalk vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

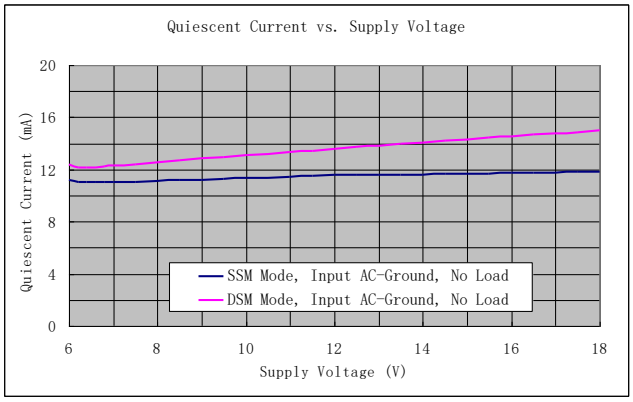


Figure 21: Quiescent Current vs. V_{DD}

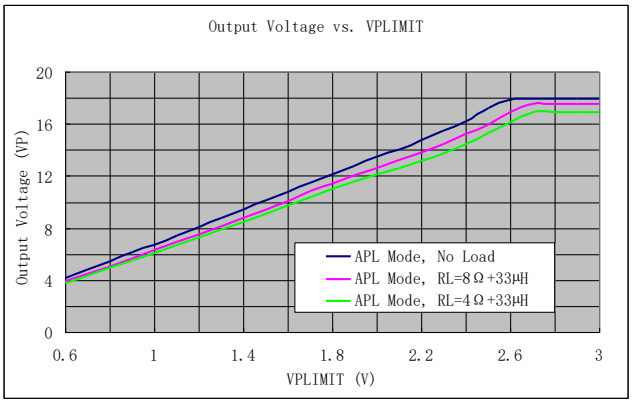


Figure 22: Output Voltage Limit vs. V_{PLIMIT}

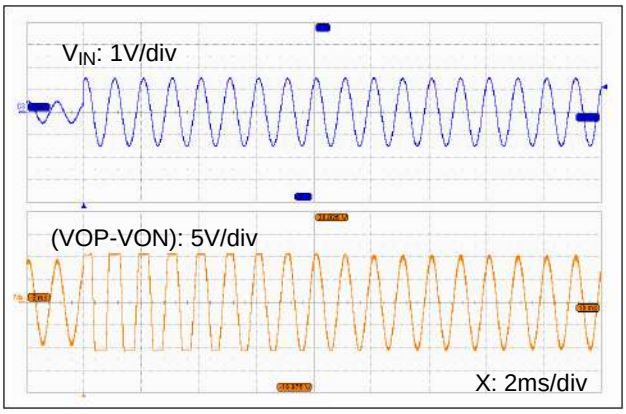


Figure 23: Audio Outputs during ALC Attack

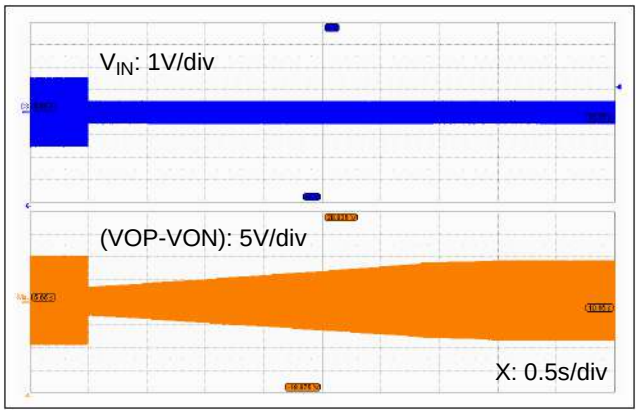


Figure 24: Audio Outputs during ALC Release

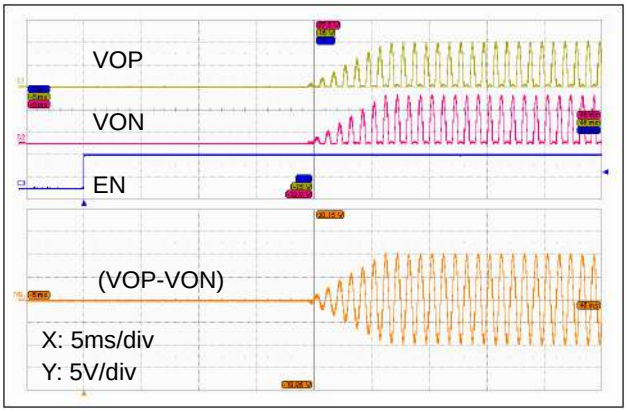


Figure 25: Audio Outputs during Startup

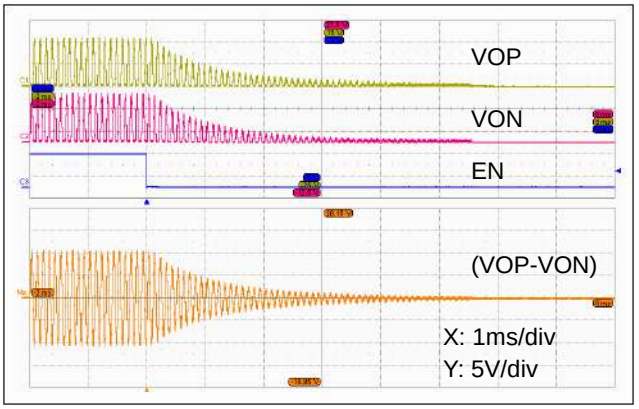


Figure 26: Audio Outputs during Shutdown

APPLICATION INFORMATION

The ft3128 is a high power, high efficiency, stereo Class-D audio power amplifier with adjustable power limit (APL) and automatic level control (ALC). It operates with a wide range of supply voltages from 5.5V to 20V. With 15V supply voltage, it can deliver into a pair of 4Ω speakers, an output power of 22W per channel with 1% THD+N, or an ALC output power of 20W per channel with 0.5% THD+N. With 18V supply voltage, it can deliver into a pair of 8Ω speakers, an output power of 18W per channel with 1% THD+N, or an ALC output power of 15W per channel with 0.4% THD+N.

The high efficiency (up to 90%) of ft3128 extends battery life in playing music and allows it to deliver an output power of 2X20W without the need for a bulky heat sink on a two-layer system board. The high PSRR (75dB @ 1kHz in SSM) and low EMI emission of ft3128 reduce system design and manufacturing complexities and lower system cost.

The ft3128 features APL and ALC. The APL limits peak audio outputs to a user-defined value to protect audio speakers from excessive power dissipation and over-load. The ALC adjusts the voltage gain of the audio amplifiers in response to over-limit audio inputs, eliminating output clipping distortion while maintaining a maximally allowed dynamic range of audio outputs. The limiting voltage of APL and ALC can be either the supply voltage or a user-defined value.

The ft3128 facilitates two PWM modulation schemes for the Class-D audio amplifiers: Dual-Side-Modulation (DSM) and Single-Side-Modulation (SSM).

The ft3128 can be configured into driving either a pair of speakers in BTL configuration for stereo applications or a single speaker in Parallel BTL (PBTL) configuration for mono applications.

The ft3128 includes comprehensive protection modes against various operating faults including under-voltage, over-voltage, over-current, over-temperature, and DC-detect for safe and reliable operation.

OPERATING MODE CONTROL

The ft3128 features APL and ALC modes of operation. In APL mode, peak audio outputs are clamped (hard-limited) to a voltage level defined by the PLIMIT pin, protecting audio speakers from excessive power dissipation and over-load. In ALC mode, not only peak audio outputs are limited to a value defined by the PLIMIT pin, but also the voltage gain of the audio amplifiers is lowered proportionally to eliminate output clipping distortion while maintaining a maximally allowed dynamic range of audio outputs.

As described in Table 1, depending upon the pin voltage at PLIMIT and the pin configuration at ALC, the ft3128 can be configured into one of four operating modes: Mute, APL, ALC, and Traditional. In ft3128, the pin voltage at PLIMIT, V_{PLIMIT}, defines the limiting voltage of audio outputs for both APL and ALC modes while the pin configuration at ALC controls the activation and dynamic characteristics of the automatic gain control (AGC).

V_{PLIMIT}	R_{ALC}	Mode	Description
$V_{PLIMIT} \leq 0.3V$	X	Mute	Audio outputs shorted to GND
$0.7V \leq V_{PLIMIT} \leq 3.4V$	Open	APL	Audio outputs limited to a value defined by V_{PLIMIT}
$V_{PLIMIT} \geq 4.5V$		Traditional	No APL and No ALC
$0.7V \leq V_{PLIMIT} \leq 3.0V$	0kΩ, 68kΩ, 220kΩ to GND	ALC	Audio outputs limited to a value defined by V_{PLIMIT}
$V_{PLIMIT} \geq 4.5V$			Audio outputs limited to the supply voltage PVDD

Table 1: Operating Mode Control

If V_{PLIMIT} is set less than 0.3V, the device operates in mute mode regardless of the pin configuration at ALC. If V_{PLIMIT} is set in the range from 0.7V to 3.4V with the ALC pin unconnected, the device operates in APL mode, where the audio outputs are clamped to a value approximately equal to (5.8 x V_{PLIMIT}). If V_{PLIMIT} is set higher than 4.5V with the ALC pin unconnected, the device operates in a traditional Class-D mode without APL or ALC. In this mode, the output clipping distortion will occur as peak output voltages reach to the supply voltage PVDD.

If V_{PLIMIT} is set in the range from 0.7V to 3.0V with the ALC pin connected to ground through an external resistor of 0kΩ, or 68kΩ, or 220kΩ, the device operates in ALC mode. In a similar manner as APL mode, audio outputs in ALC mode are limited to a value approximately equal to (5.8 x V_{PLIMIT}). However the output limiting is facilitated by dynamically adjusting the voltage gain of the audio amplifiers in response to excessive audio inputs. In ALC mode, if V_{PLIMIT} is set higher than 4.5V, the limiting voltage of audio outputs is internally set at the supply voltage. Thus, the peak voltage of audio outputs is limited to a value that is substantially close to PVDD.

Figure 27 depicts large audio outputs in different operating modes when excessive inputs are applied to cause peak outputs higher than either the supply voltage or a user-defined voltage limit lower than the supply voltage.

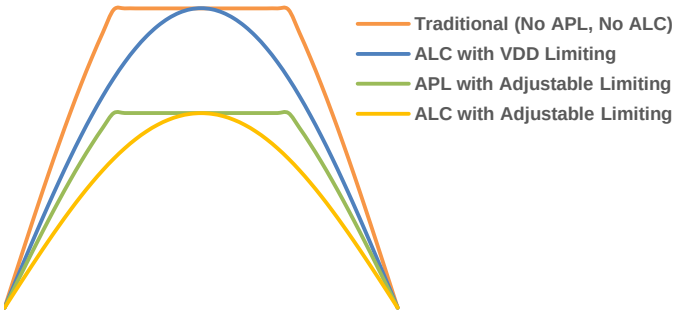


Figure 27: Large Audio Outputs in Different Operating Modes

ADJUSTABLE POWER LIMIT (APL)

The ft3128 features APL to limit audio output voltages below a value defined by the PLIMIT pin. The user-defined limit applies to both left and right channels together. The output limiting voltage $V_{O,LIMIT}$ is linearly proportional to the voltage at the PLIMIT pin as given by Equation 1.

$$V_{O,LIMIT} = 5.8 \times V_{PLIMIT} \quad (1)$$

In Equation 1, V_{PLIMIT} is the voltage at the PLIMIT pin. Typically, as shown in Figure 28, V_{PLIMIT} is set by a resistor divider (R_1 and R_2) from GVDD (an internally generated reference voltage at 5.6V) to AGND. Add a 0.1μF ceramic capacitor from PLIMIT to AGND for stable limiter operation. To limit the current drawn from the GVDD pin, it is recommended to use a resistor divider of 100kΩ or more. An external voltage reference can also be applied onto the PLIMIT pin directly if tighter tolerance of the power limit is required.

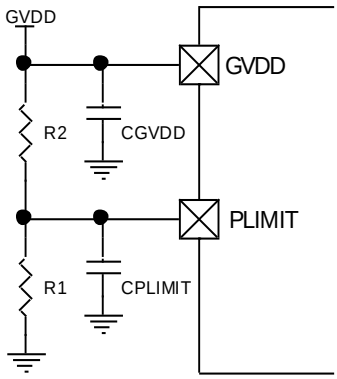


Figure 28: Typical Circuit Diagram at PLIMIT

The output limiting voltage, $V_{O,LIMIT}$, can be used to calculate the maximum output power of an unclipped output (approximately 1% THD+N) for a given speaker load as described by Equation 2.

$$P_O = \frac{\left[V_{O,LIMIT} \times \left(\frac{R_L}{R_L + 2 \times R_S} \right) \right]^2}{2 \times R_L} \quad (2)$$

In the equation, R_S is the total series resistance including R_{DSON} of on-chip power devices and any resistances in the output filter, R_L is the speaker impedance.

In either APL or ALC mode, the voltage at the PLIMIT pin defines the limiting voltage of audio outputs. In this manner, the output power can be regulated and limited to a value, as described by Equation 2, presumed that the $V_{O,\ LIMIT}$ is set lower than the supply voltage PVDD. If the $V_{O,\ LIMIT}$ is set higher than the supply voltage, the output voltage will still be clipped at the supply voltage but with higher THD+N. Thus a limiting voltage higher than PVDD can be used for applications where greater audio loudness is desirable at the expense of some level of output clipping distortion. It is important to note that Equation 2 for the output power no longer holds true in this case. The output power will increase slightly with accelerated degradation on the output clipping distortion. For example, 4% THD+N will be resulted if $V_{O,\ LIMIT}$ is set at 10% higher than the supply voltage PVDD.

Table 2 shows example values of R_1 and R_2 to set the output power limit for 4Ω and 8Ω speakers, respectively.

GVDD (V)	R_1 (kΩ)	R_2 (kΩ)	V_{PLIMIT} (V)	$V_{O,\ LIMIT}$ (V)	Po (W/Ch)	
					Non-ALC (1% THD+N)	ALC
V_{DD}=12V, R_L=4Ω+33μH						
5.6	100	Open	0	0	Mute	
5.6	30	100	1.29	7.5	7	6
5.6	33	100	1.39	8.1	8	7
5.6	36	100	1.48	8.6	9	8
5.6	39	100	1.57	9.1	10	9
5.6	43	100	1.68	9.8	12	11
5.6	Open	100	V_{GVDD}	V_{DD}	15	13
V_{DD}=18V, R_L=8Ω+33μH						
5.6	100	Open	0	0	Mute	
5.6	43	100	1.68	10	6	5.5
5.6	68	130	1.92	11	8	7.5
5.6	75	120	2.15	12.5	10	9.5
5.6	82	110	2.39	14	12	11
5.6	100	120	2.55	15	14	13
5.6	150	140	2.90	16.8	16	14
5.6	Open	100	V_{GVDD}	V_{DD}	18	16

Table 2: Typical Resistor Values of R_1 & R_2

GVDD SUPPLY

The GVDD is an internally generated supply voltage for internal circuitry. It is also used as the supply voltage for the resistor divider to set the voltage at the PLIMIT pin. It is highly suggested to decouple the GVDD pin with a 1μF ceramic capacitor to ground for stable operation. Note that the current drawn from the GVDD pin by external circuitry, including all the resistor dividers at ALC, GAIN, FREQ, and PLIMIT pins, must be kept less than 5mA.

MUTE CONTROL

The ft3128 can be configured into mute mode when the PLIMIT pin is pulled low by an inverting transistor, as shown in Figure 29. In mute mode, the output stages of both audio amplifiers are in Hi-Z and the differential audio outputs (VOPL/R and VONL/R) are pulled to ground through on-chip resistors respectively. To restore to its normal operation, the output of the inverting transistor is reverted to Hi-Z state, allowing the resistor divider (from GVDD to ground) tapped at the PLIMIT pin to set the voltage limit for APL and ALC.

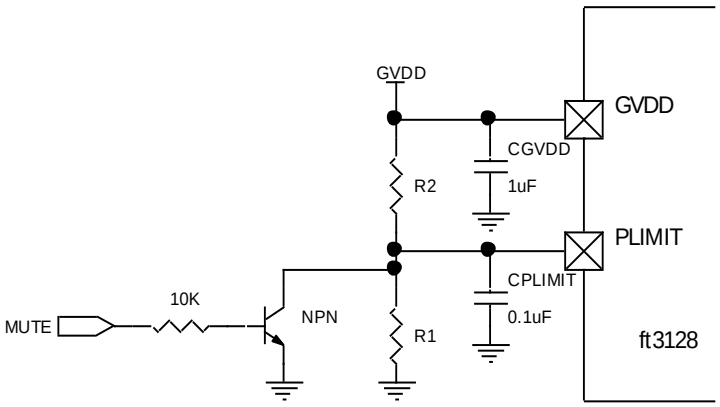


Figure 29: Example Circuit Diagram of Mute Control

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control is to maintain the audio outputs for a maximum voltage swing without clip distortion when excessive inputs that may cause output clipping are applied. With ALC, the ft3128 lowers the voltage gain of both audio amplifiers to an appropriate value such that output clipping is substantially eliminated.

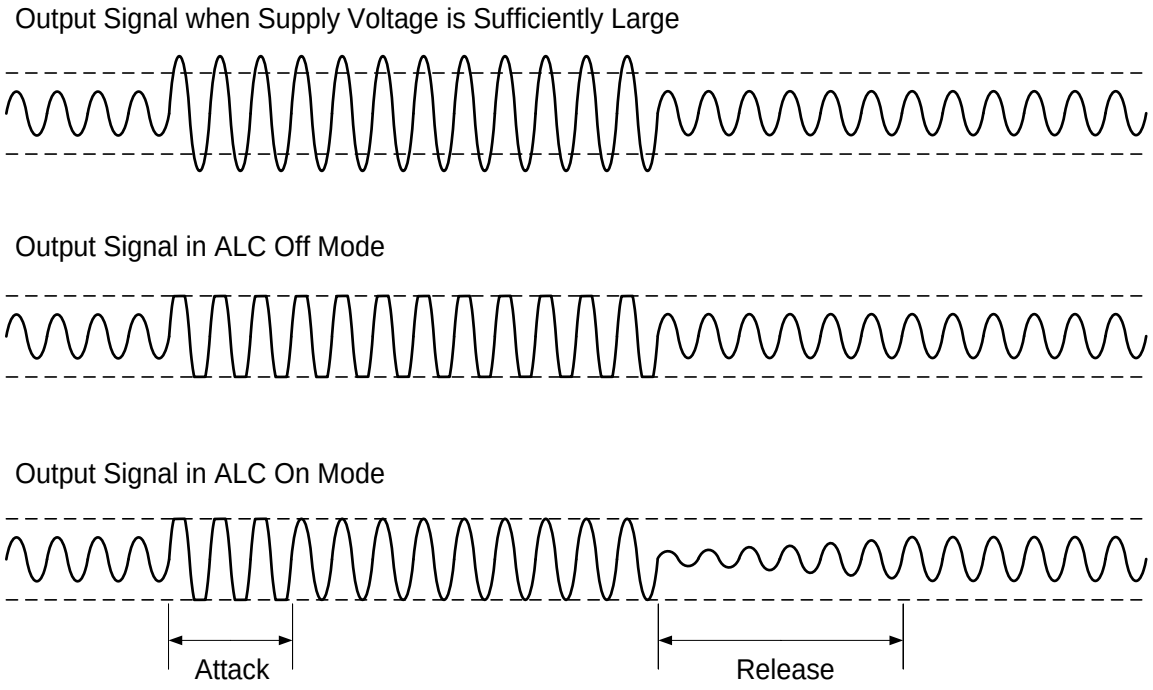


Figure 30: Automatic Level Control Diagram

In Figure 30, “Attack” is the duration where the voltage gain of the audio amplifiers decreases until output clipping is substantially eliminated. “Release” is the duration where the voltage gain of the audio amplifiers recovers (increases) until it reaches to a value that is maximally allowed without output clipping.

ALC MODE SELECT

The ft3128 can be configured into ALC or Non-ALC mode via the ALC pin, as described in Table 3. When the ALC pin is left unconnected, the ft3128 operates in Non-ALC mode. The Non-ALC mode is typically chosen for applications where maximum audio loudness is desired and the amount of output clipping distortions can be measurably controlled at the audio source. In other pin configurations, the ft3128 operates in ALC mode with three specific audio dynamic characteristics. For most applications, the ALC mode is preferred for its capability to substantially eliminate output clipping distortion, excessive power dissipation, and speaker over-load.

Three sets of ALC dynamic characteristics can be selected for specific sound effects, as described in Table 3. The ALC-1 mode (the ALC pin shorted to GND) plays music in a most mellow manner with negligible amount of clipping distortion and lower average output power. On the other hand, the ALC-3 mode (the ALC pin shorted to GND via a 220kΩ resistor) plays music in a most dynamic manner with some extent of clipping distortion and higher average output power (loudness).

ALC Pin Configuration	ALC Mode	Sound Effects	
		Loudness	Output Clipping Distortion
Open	Non-ALC	Potentially highest loudness	No control on output clipping
Short to GND	ALC-1	Most mellow sound (Lowest loudness under ALC)	Negligible output clipping
68kΩ to GND	ALC-2	Medium loudness	Slight output clipping
220kΩ to GND	ALC-3	Most dynamic sound (Highest loudness under ALC)	Acceptable output clipping
Note: The resistor tolerance of R_{ALC} should be 5% or better.			

Table 3: ALC Mode Select

VOLTAGE GAIN SETTING

To accommodate various application requirements, the ft3128 features four selectable voltage gains for audio amplifiers. An external resistor R_{GAIN} from the GAIN pin to ground sets the voltage gain, as shown in Table 4.

GAIN Pin Configuration	$R_{INTERNAL}$ (kΩ)	A_V (V/V)	A_V (dB)
Open	30	20	26
Short to GND	20	30	30
68kΩ to GND	12	50	34
220kΩ to GND	60	10	20
Note: The resistor tolerance of R_{GAIN} should be 5% or better.			

Table 4: Voltage Gain Select

Although the voltage gains as described in Table 4 vary a little (less than 2%) from parts to parts, the input impedances at the same voltage gain may vary by ±20% over parts, due to process variations in the actual resistance of the input resistors. For design purposes, the input impedance should be assumed to be 10kΩ, which is the absolute minimum input impedance of the audio amplifiers in ft3128. At lower gain settings, the input impedance could be as high as 72kΩ.

The voltage gain of the audio amplifiers can be slightly adjusted by inserting small external input resistors R_{IN}, in series with the input capacitors C_{IN}, as depicted in Figure 31 and Figure 32. In the figures, it is required that $C_{IN}=C_{INL1}=C_{INL2}=C_{INR1}=C_{INR2}$ and $R_{IN}=R_{INL1}=R_{INL2}=R_{INR1}=R_{INR2}$.

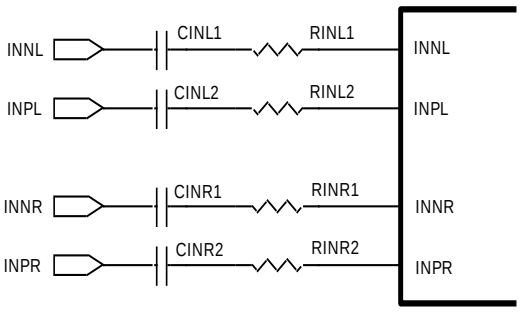


Figure 31: Gain Setting (Differential Inputs)

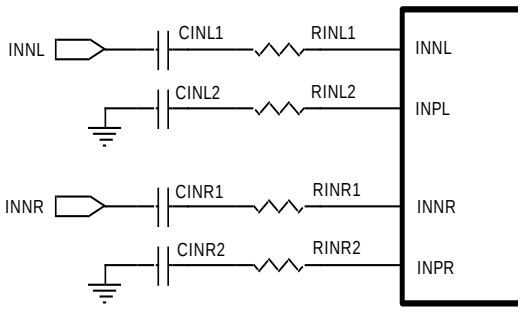


Figure 32: Gain Setting (Single-Ended Inputs)

The value of R_{IN} (in kΩ) for a given voltage gain can be calculated by Equation 3, where A_V is the voltage gain of the audio amplifier.

$$A_V = \frac{600}{R_{IN} + R_{INTERNAL}} \quad (3)$$

The choice of the voltage gain will strongly influence the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause audio outputs to be severely clipped (Non-ALC mode) or compressed (ALC mode) for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quite) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for well balanced audio quality.

The voltage gain is chosen based upon various system-level considerations including the supply voltage, the dynamic range of audio sources and speaker loads, and the desired sound effects. As a general guideline, the voltage gain can be simply expressed in Equation 4. In the equation, $V_{IN, MAX}$ (in V_{RMS}) is the maximum input level from the audio source, PVDD (in volts) is the supply voltage, and α is the design parameter, which ranges from 0.66 to 1.0. The higher α is, the higher the average output power (louder) is, with some degree of compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN, MAX}} \quad (4)$$

As an example, Table 5 shows the voltage gain for various input levels with PVDD at 12V and 18V and α at about 0.80. In the table, R_{IN} is the external input resistor in series with the input capacitor and $R_{INTERNAL}$ is the internal input resistor.

$V_{IN, MAX}$ (V_{RMS})	A_V (V/V)	A_V (dB)	R_{GAIN} to GND (kΩ)	$R_{INTERNAL}$ (kΩ)	R_{IN} (kΩ)
V_{DD}=12V					
0.5	20	26	Open	30	0
0.7	13.3	22.5	Open	30	15
1.0	10	20	220	60	0
V_{DD}=18V					
0.5	30	29.5	0	20	0
0.7	20	26	Open	30	0
1.0	13.3	22.5	Open	30	15

Table 5: Typical Voltage Gain Settings for Various V_{DD} & Audio Input Levels

PWM FREQUENCY SETTING

To accommodate various application requirements, the ft3128 features two selectable PWM frequencies with optional spread-spectrum for the Class-D audio amplifiers. An external resistor R_{FREQ} from the FREQ pin to ground sets the PWM frequency and optional spread-spectrum, as shown in Table 6.

FREQ Pin Configuration	PWM Frequency (kHz)	Spread-Spectrum
Open	360	No
Short to GND	360	Yes
68kΩ to GND	500	No
220kΩ to GND	500	Yes
Note: The resistor tolerance of R_{FREQ} should be 5% or better.		

Table 6: PWM Frequency Select with Optional Spread-Spectrum

PWM MODULATION SCHEME

To accommodate various application requirements, the ft3128 features two PWM modulation schemes, i.e., Single-Side-Modulation (SSM) and Double-Side-Modulation (DSM). In typical applications, the SSM is suggested for its lower EMI and higher efficiency. The modulation scheme is selected via the MODS pin, as described in Table 7. The PWM modulation scheme is latched during power-up and cannot be changed while the device is in operation.

MODS	Modulation Scheme
Low	SSM
High	DSM

Table 7: Modulation Scheme Select

Single-Side-Modulation (SSM)

The SSM scheme alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the selection of the filter components and type of the output filter. In SSM scheme, the outputs operate less than 5% modulation during idle conditions. When an audio signal is applied, one output will decrease and another one will increase. The decreasing output signal will quickly rail to ground where all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in SSM due to the reduction of switching losses. The THD penalty with the SSM scheme is minimized by the on-chip linear feedback loop.

Double-Side-Modulation (DSM)

The DSM scheme allows operation without classic LC reconstruction filters when the amplifier drives an inductive load with short speaker wires (less than 10cm). Each audio output switches from ground to the supply voltage. With no audio input, the VOPL/R and VONL/R outputs are at 50% duty cycle and in phase with each other, resulting in little or no current flowing through the speaker. With a positive audio input, the duty cycle of VOPL/R is greater than 50% and VONL/R is less than 50%, resulting in a positive current flowing through the speaker. With a negative audio input, the duty cycle of VOPL/R is less than 50% and VONL/R is greater than 50%, resulting in a negative current flowing through the speaker. The voltage across the speaker load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the speaker load.

VOLUME FADE-IN & FADE-OUT

The ft3128 features volume fade-in and fade-out to reduce intermittent sound and eliminate uncomfortable hearing experience during the transitions when the device enters into or exits out of normal operation. Figure 33 and Figure 34 show the audio output waveforms during fade-in and fade-out respectively.

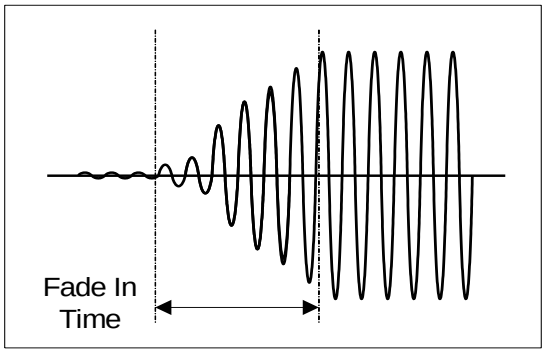


Figure 33: Fade-In Waveform

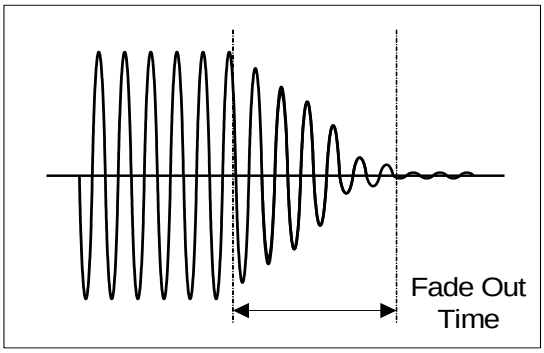


Figure 34: Fade-Out Waveform

PBTL CONFIGURATION (MONO MODE)

The ft3128 features an optional mono mode that allows the left and right channels to operate in parallel BTL configuration. To operate the ft3128 in mono mode, connect the INNR and INPR pins (pin 11 and 12) directly to ground (no decoupling capacitors). In mono mode, as shown in Figure 35, an audio input signal applied to the left channel (pin 3 and 4) is routed to the H-bridge of both channels. Note that the mono mode is intended to be configured strictly by the hardware connection. Leaving either INNR or INPR pin unconnected while the audio outputs VOPL/R and VONL/R are wired together in PBTL configuration can trigger an over-current or thermal overload protection or both. The mono mode is configured by the following arrangement:

- Connect INPR and INNR pins directly to ground (no decoupling capacitors).
- Apply an audio signal to the left-channel inputs (INPL and INNL pins).
- Connect VOPL to VONL together as one terminal of the speaker and connect VOPR to VONR together as the other terminal of the speaker. Use heavy PCB traces as close as possible to the device.
- Place the speaker between the left and right-channel outputs.

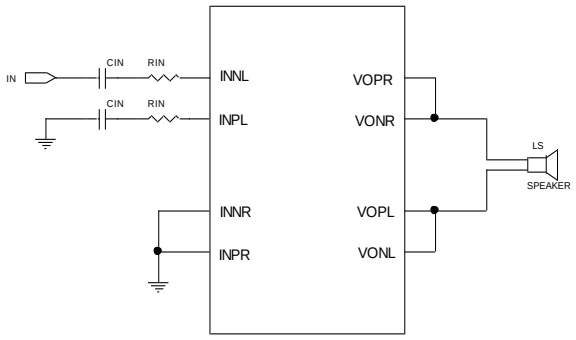


Figure 35: PBTL Configuration for Mono Applications

CLICK-AND-POP SUPPRESSION

The ft3128 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential audio outputs VOPL/R and VONL/R ramp down to ground quickly and simultaneously.

PSRR ENHANCEMENT

Without a dedicated pin for the common-mode voltage bias and an external holding capacitor onto the pin, the ft3128 achieves a PSRR, 75dB at 1kHz.

STARTUP AND SHUTDOWN

The ft3128 employs the EN pin to minimize power consumption while it is not in use. When the EN pin is pulled low, the ft3128 is forced into shutdown mode, where all the analog circuitry is de-biased and the supply current is reduced to be less than 80μA, and the differential outputs are shorted to ground through an on-chip resistor (3kΩ) individually. Once in shutdown mode, the EN pin must remains low for at least 5 milliseconds (T_{SD}), the shutdown settling time, before it can be brought high again. When the EN pin is asserted high, the device exits out of shutdown mode and enters into normal operation after the startup time (T_{STUP}) of 50 milliseconds.

An on-chip pulldown resistor of 250kΩ is included onto the EN pin. Thus, shutdown mode is the state when the power supply is first applied to the device. Whenever possible, it is strongly recommended to hold the EN pin low until the device is properly powered up and the audio signals at the inputs are stable. Also, for best power-off pop performance, place the device in shutdown mode prior to removing the power supply voltage.

Note that the setting at the MODS pin is latched during startup and cannot be changed while the device is in operation. To change the setting of the MODS pin, the device must be first brought into shutdown mode by pulling the EN pin low for at least 5 milliseconds before it can be restored to its normal operation.

PROTECTION MODES

For safe operation, the ft3128 incorporates comprehensive protection circuits against various operating faults including Under-Voltage, Over-Voltage, Over-Temperature, Over-Current, and DC-Detect, as described in Table 8. In the shutdown mode, all the analog circuitry is de-biased with differential outputs to be shorted to ground. In the mute mode, all the analog circuitry is enabled with differential outputs to be shorted to ground.

Fault	Detection Condition	FAULTB	Audio Outputs	Mode	Latched or Self-Recovery
Over-Current	Audio outputs shorted to PVDD or GND or each other	Low	3kΩ to GND	Shutdown	Latched
DC-Detect	See Table 9	Low	3kΩ to GND	Shutdown	Latched
Over-Temperature	Tj > 160 °C	-	3kΩ to GND	Mute	Self-Recovery
Under-Voltage	PVDD < 4.3V	-	3kΩ to GND	Mute	Self-Recovery
Over-Voltage	PVDD > 24V	-	3kΩ to GND	Mute	Self-Recovery

Table 8: Protection Modes of Various Operating faults

Under-Voltage Lockout (UVLO)

The ft3128 incorporates circuitry to detect a low supply voltage for safe and reliable operation. When the supply voltage is first applied, the ft3128 will remain inactive until the supply voltage exceeds 4.6V (V_{UVLOUP}). When the supply voltage is removed and drops below 4.3V (V_{UVLODN}), the ft3128 enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (3kΩ) individually.

Over-Voltage Protection (OVP)

The ft3128 features over-voltage protection. When the supply voltage exceeds 24V (V_{VOPUP}), the device enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (3kΩ) individually. The device will resume normal operation once the supply voltage returns to a value lower than 23V (V_{VOPDN}).

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds 160°C, the device enters into mute mode, where the differential audio outputs VOPL/R and VONL/R are pulled to ground through on-chip resistors (3kΩ) individually. The device will resume normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

Over-Current Protection (OCP)

In operation, the output of Class-D amplifier constantly monitors for any over-current and/or short-circuit conditions. When a short-circuit condition between two differential outputs, differential output to PVDD or ground is detected, the output stage of the amplifier is immediately forced into high impedance state. Once the fault condition persists over a prescribed period, the ft3128 then enters into the shutdown mode and remains in this mode for about 40ms (T_{OCP}), the over-current recovery time. When the shutdown mode times out, the ft3128 will initiate another start-up sequence and then check if the short-circuit condition has been removed. If the fault condition is still present, the ft3128 will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is so-called the hiccup mode of operation. Once the fault condition is removed, the ft3128 automatically restores to its normal mode of operation.

DC-Detect Protection (DCP)

The ft3128 features DCP circuit to protect the speakers from large DC current. A DC-detect fault is issued when the duty cycle of differential outputs of either channel exceeds 20% for more than 720ms at the same polarity. Note that the DCP threshold is a function of the supply voltage, as shown in Table 9. To avoid nuisance faults due to the DCP circuit, it is recommended to hold the EN pin low during startup until the audio signals at the inputs are stable. Also, take care to closely match the impedance seen at two differential inputs.

A DC-detect fault will be flagged on the FAULTB pin at a low state. It will also force the device into shutdown mode. If automatic recovery from the DCP latch is desired, connect the FAULTB pin directly to the EN pin. This allows the FAULTB pin to automatically drive the EN pin, which clears the DCP latch.

PVDD (V)	Vos, Output Offset Voltage (V)
6.5	1.3
12	2.1
15	2.7
18	3.5

Table 9: DC-Detect Threshold Voltages

CLASS-D AUDIO AMPLIFIER

The audio power amplifiers in ft3128 operate in much the same way as traditional Class-D amplifiers and similarly offer much higher power efficiency.

FULLY DIFFERENTIAL AMPLIFIER

The ft3128 includes a pair of fully differential amplifiers with differential inputs and outputs. The fully differential amplifiers ensure that the differential output voltages are equal to the differential input voltages times the amplifier gain. Although the ft3128 supports for a single-ended input, differential inputs are much preferred for applications where the environment can be noisy in order to ensure maximum SNR.

LOW-EMI FILTERLESS OUTPUT STAGE

Traditional Class-D audio amplifiers require for the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. The ft3128 applies an edge-rate control circuitry to reduce EMI emissions, while maintaining high power efficiency.

FILTERLESS DESIGN

The ft3128 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the audio outputs is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum performance, use speakers with series inductances greater than 10μH. Typical 4Ω speakers exhibit series inductances from 10μH to 47μH.

FERRITE BEAD OUTPUT FILTER

With an edge-rate control circuitry in ft3128, it is possible to design a low EMI, highly efficient class-D audio amplifier without the need for an LC output filter for the connection from the amplifier to the speaker. However, EMI suppression can be further reduced by use of a low-cost ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 36. The ferrite bead filter is applied to block radiation in the range of 30MHz and above from appearing on the speaker wires and the power supply lines. The impedance of the ferrite bead is used with a small capacitor in the range of 1nF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead filter should be less than 10MHz.

Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 330Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than their rated current values. Choose a ferrite bead with a rated current no less than 3A for 8Ω loads, 5A for 4Ω loads, and 7A for 3Ω loads (in PBTL configuration).

A high quality ceramic capacitor is needed for the ferrite bead filter. A low ESR ceramic capacitor with good temperature and voltage characteristics will be the best choice. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. It is crucial to place each ferrite bead filter tightly together and individually close to VOPL/R and VONL/R pins respectively.

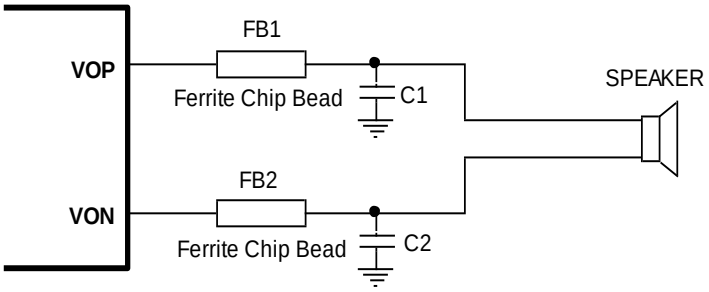


Figure 36: Ferrite Bead Filter for EMI Reduction

Additional EMI improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network are 10Ω in series with a 680pF capacitor. Note that design of the RC snubber circuit is specific to every application and must take into account the parasitic reactance of the system board to reach proper values of R and C. Evaluate and ensure that the voltage spikes (overshoots and undershoots) at VOPL/R and VONL/R on the actual system board are within their absolute maximum ratings. Pay close attention to the layout of the RC snubber circuit to be tight and individually close to VOPL/R and VONL/R pins, respectively.

LC OUTPUT FILTER

For applications where there are nearby circuits that are highly sensitive to noise or long speaker wires, it may become necessary to add a LC reconstruction filter for best EMI reduction. A classic second-order lowpass filter, as shown in Figure 37, can be used for the output filter.

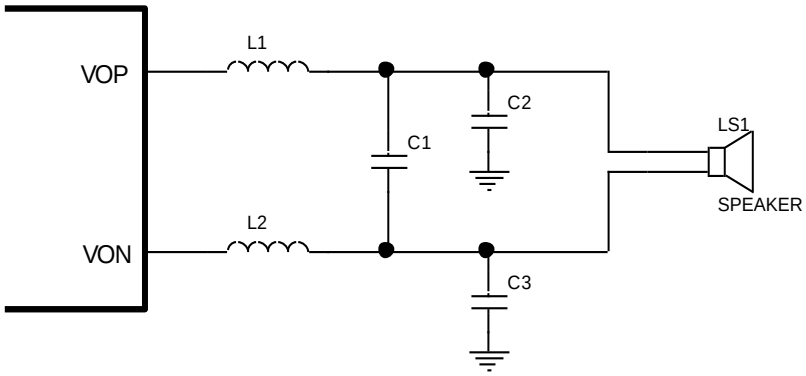


Figure 37: LC Output Filter for EMI Reduction

In Figure 37, the corner frequency of the LC lowpass filter, as given by Equation 5, must be designed to be sufficiently high to allow for high-frequency components of audio signals, yet be low enough to sufficiently attenuate high-frequency components of the audio outputs from VOPL/R and VONL/R. The corner frequency of the filter is typically set about 50kHz. In Equation 5, it is assumed that $L=L_1=L_2$, $C_G=C_2=C_3$, and $C=2 \times C_1 + C_G$.

$$f_{C,LPF} = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \quad (5)$$

The quality factor Q of the output filter is important. Lower Q increases output noise and higher Q results in passband peaking at frequencies near the corner frequency. The quality factor of the filter is typically set between 0.7 and 1.0. As shown in Equation 6, the speak load, R_{LOAD}, affects the quality factor of the filter.

$$Q = \frac{R_{LOAD}}{4 \times \pi \times f_C \times L} \quad (6)$$

Table 10 lists suggested component values of L_1, L_2, C_1, C_2, and C_3 for the second-order Butterworth lowpass filter with the speaker load at 2Ω, 3Ω, 4Ω, or 8Ω.

Speaker Load (Ω)	Modulation Scheme	L_1, L_2 (μH)	C_1 (μF)	C_2, C_3 (μF)	$f_{C, LPF}$ (kHz)	Q
8	SSM	22	0.33	0.068	40	0.73
	DSM	22	-	0.68	41	0.70
4	SSM	10	0.56	0.10	46	0.70
	DSM	10	-	1.0	50	0.63
3	SSM	6.8	0.68	0.10	50	0.70
	DSM	6.8	-	1.5	50	0.70
2	SSM	4.7	1.0	0.22	50	0.68
	DSM	4.7	-	2.2	50	0.68

Table 10: Suggested Component Values of LC Output Filter

AUDIO INPUT CAPACITORS (C_{INL1}, C_{INL2}, C_{INR1}, C_{INR2})

The input DC decoupling capacitors are recommended to bias the incoming audio inputs to a proper DC level. The input capacitor C_{IN}, in conjunction with the amplifier input resistance (including both internal resistor $R_{INTERNAL}$ and external resistor R_{IN}, if any) forms a highpass filter that removes the DC bias of the audio inputs. The corner frequency $f_{C, HPF}$ of the highpass filter is given by Equation 7. In the equation, it is assumed that $R_{IN}=R_{INL1}=R_{INL2}=R_{INR1}=R_{INR2}$ and $C_{IN}=C_{INL1}=C_{INL2}=C_{INR1}=C_{INR2}$.

$$f_{C, HPF} = \frac{1}{2 \times \pi \times (R_{IN} + R_{INTERNAL}) \times C_{IN}} \quad (7)$$

R_{IN} is the external input resistance for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally. Choose R_{IN} with a tolerance of 2% or better.

Choose C_{IN} such that $f_{C, HPF}$ is well below the lowest frequency of interest. Setting it too high affects the amplifiers' low-frequency response. Consider an example where the specification calls for A_V=26dB and a flat frequency response down to 10Hz. In this example, R_{IN}=0Ω and $R_{INTERNAL}$=30kΩ and C_{IN} is calculated to be about 0.53μF; thus 0.47μF, as a common choice of capacitance, can be chosen for C_{IN}.

Any mismatch in capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise, PSRR, CMRR performance. Choose C_{IN} with a tolerance of ±2% or better.

Furthermore, the type of the input capacitor is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

SUPPLY COUPLING CAPACITORS (C_{PVDD}, C_{AVDD}, C_{GVDD}, C_{PLIMIT})

Decouple each pair of PVDD pins respectively with a 1μF low-ESR ceramic capacitor (X7R or X5R) to GND. It is highly suggested to add an additional 10nF capacitor, in tandem with each 1μF capacitor, for high-frequency decoupling. Place the decoupling capacitors as individually close as possible to each pair of PVDD pins. Furthermore, add a large (100μF or greater) bulk power supply decoupling capacitors (electrolytic or tantalum type) on the PVDD supply in close proximity to the device. Make sure that the coupling capacitors maintain their capacitances over the supply voltage PVDD and the operating temperature of the device.

Decouple the AVDD pin with a 1µF low-ESR ceramic capacitor to GND. Place the decoupling capacitor as close as possible to the AVDD pin. Furthermore, add a small decoupling resistor (R_{AVDD}) of 10Ω between the system power supply and the AVDD pin, preventing high-frequency transients of PVDD from interfering with on-chip linear amplifiers.

Decouple the GVDD pin with a 1µF low-ESR ceramic capacitor to GND. Place the decoupling capacitor close to the GVDD pin.

Decouple the PLIMIT pin with a 0.1µF low-ESR ceramic capacitor to GND for high-frequency filtering. Place the decoupling capacitor close to the PLIMIT pin.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

As a high power, high efficiency, Class-D stereo audio power amplifier, the ft3128 requires proper PCB layout and grounding to ensure high efficiency, low distortion, and low EMI emission. Use wide traces for the power supply inputs (PVDD) and audio outputs (VOPL/R and VONL/R) to minimize losses due to parasitic trace resistances. Route all traces that carry switching transients away from the traces or components in the audio signal path.

Grounding - The power ground pins, PGND, are directly shorted to a large ground plane GND, which serves as a central “star” ground for the ft3128. Use a single point of connection between the analog ground AGND and the ground plane GND to minimize the coupling of high-current switching noise onto audio signals.

Output Filters - Place each audio output filter (Ferrite Bead or LC filter) individually close to their respective output pins, VOPL/R and VONL/R, for optimum EMI performance and operational robustness. Keep the current loop from each of the audio outputs through the output filters and back to the PGND pins as short and tight as possible.

Power Dissipation - The maximum output power of ft3128 can be severely limited by its thermal dissipation capability. To ensure the device operating properly and reliably at maximum output power without incurring over-temperature shutdown, the following guidelines are given for optimization of its thermal dissipation capability:

- Fill both top and bottom layers of the system board with solid GND metal traces.
- Solder the thermal pad directly onto a grounded metal plane.
- Place lots of equally-spaced vias underneath the thermal pad connecting the top and bottom layers of GND. The vias are connected to a solid metal plane on the bottom layer of the board.
- Reserve wide and uninterrupted areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
- Avoid using vias for traces carrying high current.

TYPICAL APPLICATION CIRCUITS

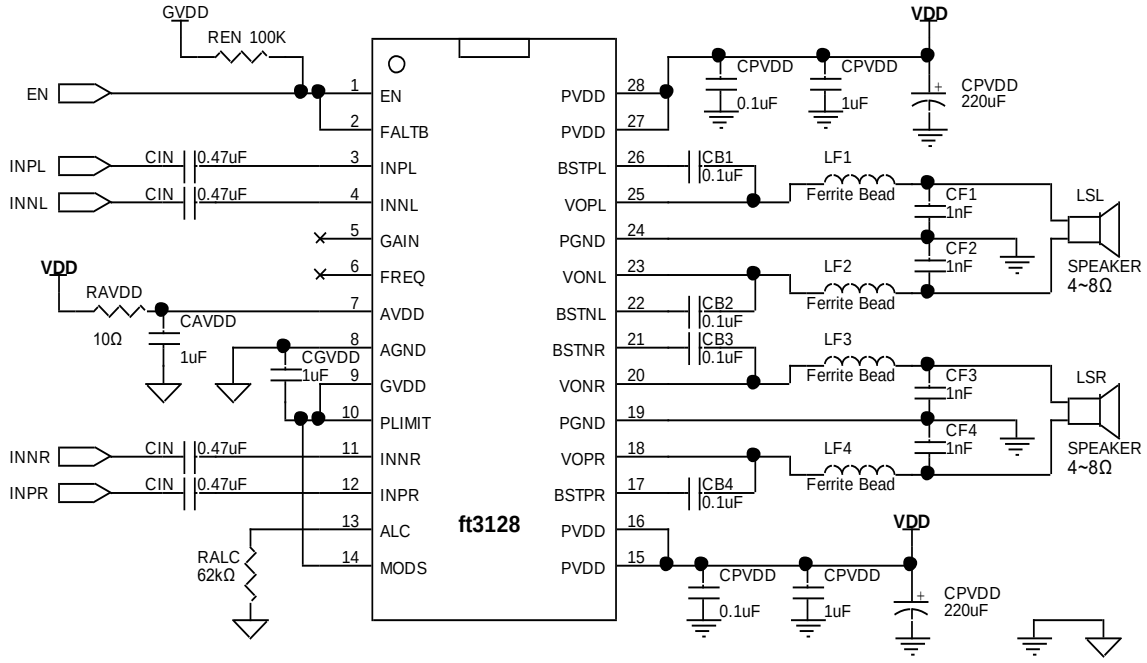


Figure 38: Differential Inputs in ALC-2 Mode with DSM

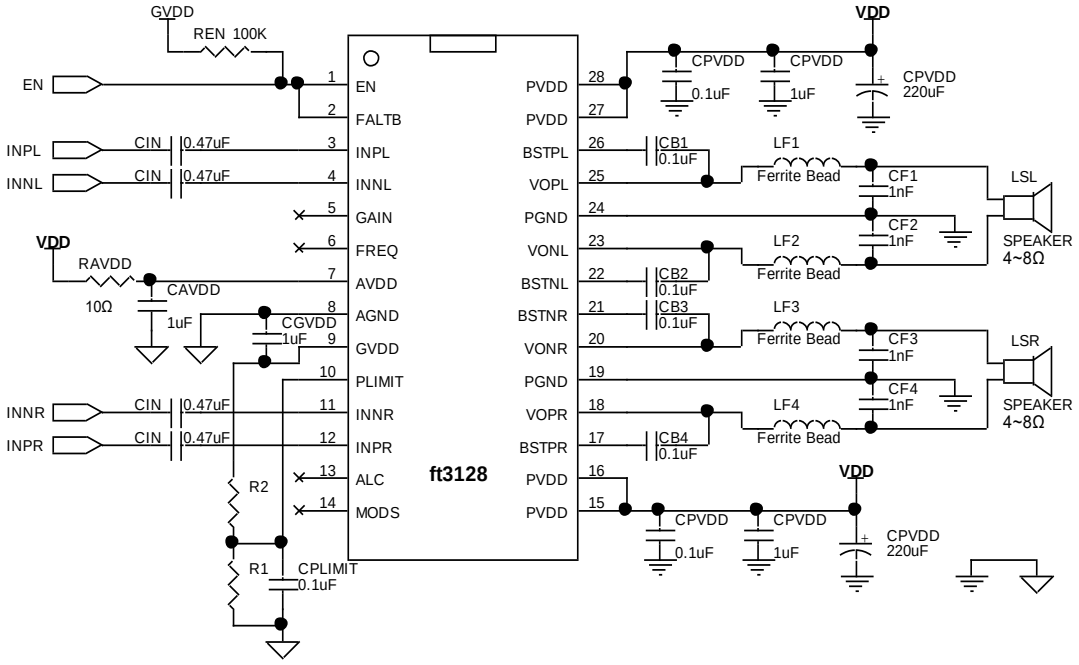


Figure 39: Differential Inputs in APL Mode with SSM

TYPICAL APPLICATION CIRCUITS (Cont'd)

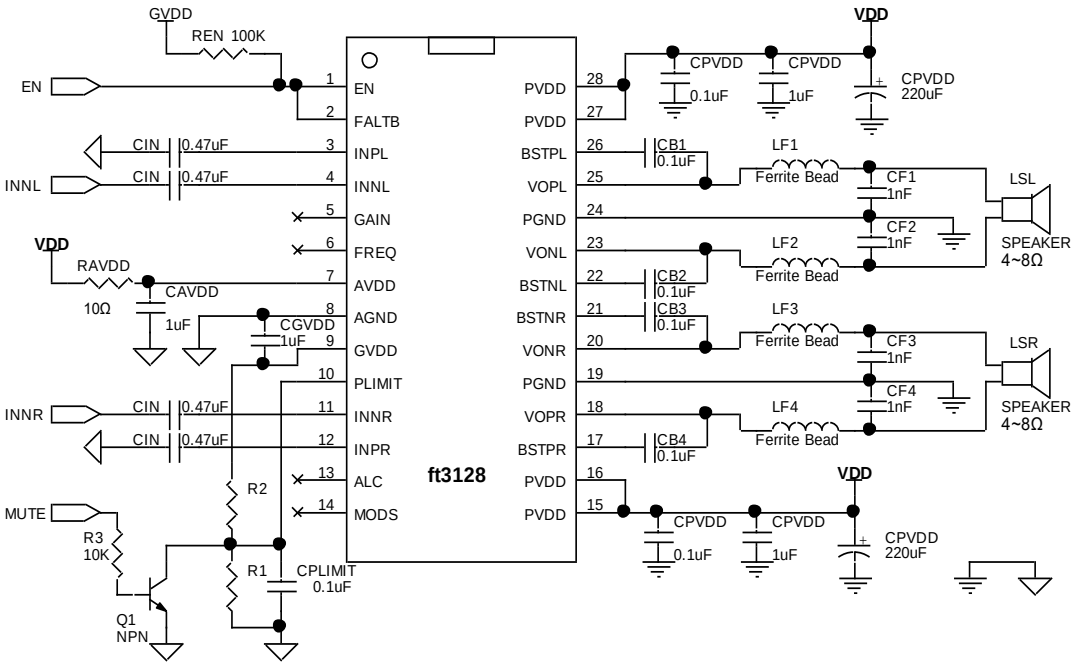


Figure 40: Single-Ended Inputs in APL Mode with Mute Control

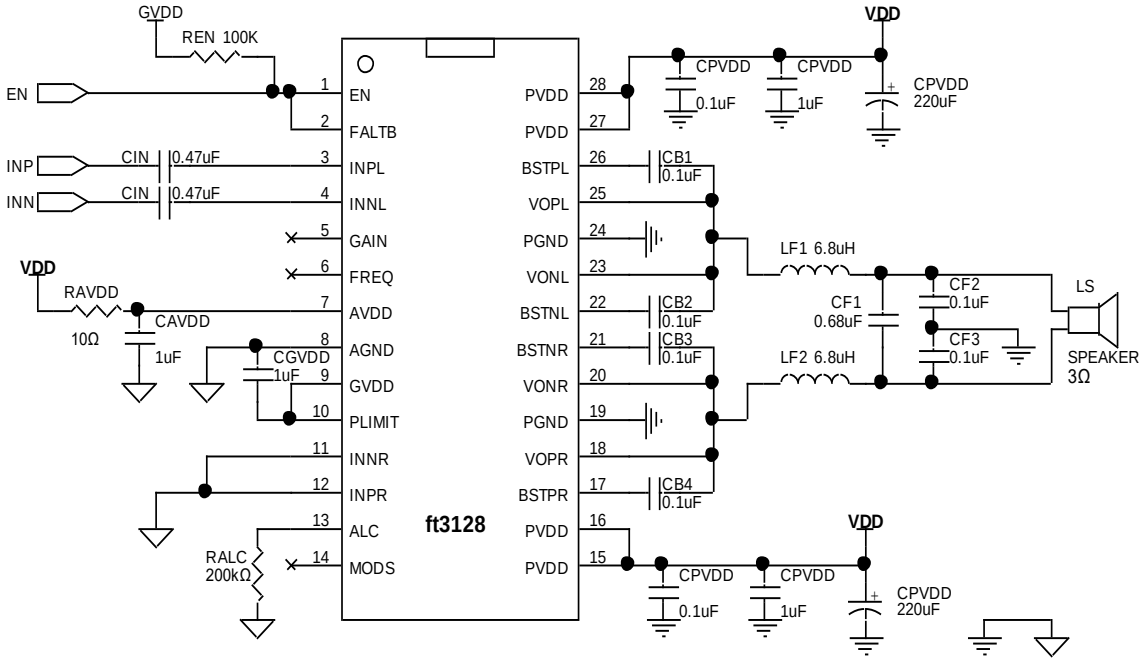
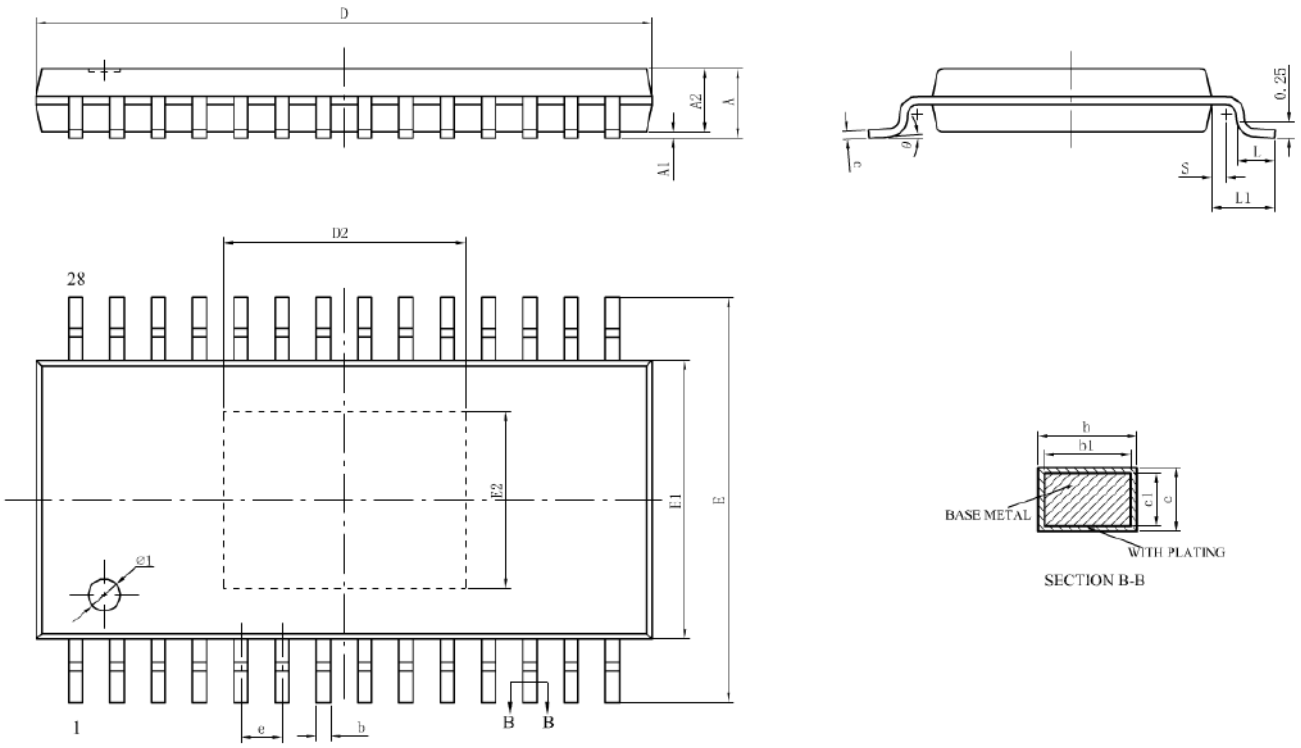


Figure 41: Differential Inputs in ALC-3 Mode with SSM in PBTL Configuration

PHYSICAL DIMENSIONS

TSSOP-28L PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0. 80	—	1. 00
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	9.60	9.70	9.80
D2	3.71	3.81	3.91

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
E2	2.69	2.79	2.89
e	0.65BSC		
L	0. 50	0. 60	0. 70
L1	1.00BSC		
S	0.20	—	—
Ø1	Ø1.0X0. 05~0. 10DP		
θ	1	—	7°

IMPORTANT NOTICE

1. Disclaimer: The information in document is intended to help you evaluate this product. Fangtek, LTD. makes no warranty, either expressed or implied, as to the product information herein listed, and reserves the right to change or discontinue work on this product without notice.

2. Life support policy: Fangtek's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president and general counsel of Fangtek Inc. As used herein

Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

3. Fangtek assumes no liability for incidental, consequential or special damages or injury that may result from misapplications or improper use or operation of its products

4. Fangtek makes no warranty or representation that its products are subject to intellectual property license from Fangtek or any third party, and Fangtek makes no warranty or representation of non-infringement with respect to its products. Fangtek specifically excludes any liability to the customer or any third party arising from or related to the products' infringement of any third party's intellectual property rights, including patents, copyright, trademark or trade secret rights of any third party.

5. The information in this document is merely to indicate the characteristics and performance of Fangtek products. Fangtek assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the document presented herein. Fangtek makes no warranty with respect to its products, express or implied, including, but not limited to the warranties of merchantability, fitness for a particular use and title.

6. Trademarks: The company and product names in this document may be the trademarks or registered trademarks of their respective manufacturers. Fangtek is trademark of Fangtek, LTD.

CONTACT INFORMATION

Fangtek Electronics (Shanghai) Co., Ltd

Room 501A, Lane 198, Zhangheng Road

Zhangjiang Hi-tech Park, Pudong District

Shanghai, China, 201204

Tel: +86-21-61631978

Fax: +86-21-61631981

Website: www.fangtek.com.cn