

**GENERAL DESCRIPTION**

The ft809 series are power supply supervisory circuits used to monitor the power supplies in microprocessors and digital systems. The ft809 series provide a reset to the microprocessors during system power-up, power-down and brown-out conditions.

The ft809 is designed to monitor the  $V_{CC}$  supply voltage and asserts a reset signal whenever the supply voltage declines below the preset threshold.

The reset signal remains asserted for at least 140ms after  $V_{CC}$  has risen above the threshold. The ft809 provides an active-low reset output.

The ft809 series are optimized to reject fast transients on the  $V_{CC}$ . Low supply current of 10 $\mu$ A makes the ft809 ideal for use in portable devices.

The ft809 series are available in SOT23-3 package.

**FEATURES**

- Precision monitoring of 2.63V/ 2.70V/ 2.93V/ 3.08V
- Fully specified over temperatures
- 140ms (minimum) power-on-reset pulse width
- 10 $\mu$ A low supply current
- Power supply transient immunity

**APPLICATIONS**

- Set top box
- ADSL
- CPU
- Portable electronic devices

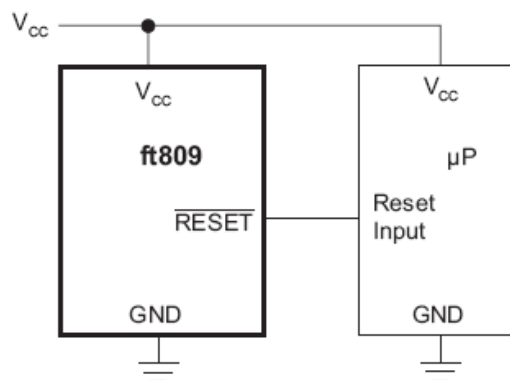
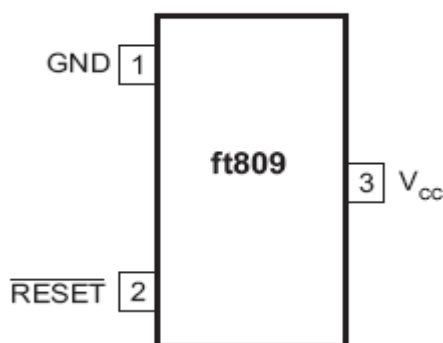
**APPLICATION CIRCUIT**

Figure 1: Typical Application Circuit

**PIN CONFIGURATION**



**PIN DESCRIPTION**

NAME	PIN #	DESCRIPTION
GND	1	Ground
$\overline{\text{RESET}}$	2	Active-Low Reset Output. It goes low when $V_{CC}$ is below the reset threshold. It remains low for at least 140ms after $V_{CC}$ rises above the reset threshold.
$V_{CC}$	3	Supply Voltage.

**ORDERING INFORMATION**

PART NUMBER	RESET THRESHOLD (V)	TEMPERATURE RANGE	PACKAGE
ft809R	2.63	-40°C to +85°C	SOT23-3
ft809V	2.70	-40°C to +85°C	SOT23-3
ft809S	2.93	-40°C to +85°C	SOT23-3
ft809T	3.08	-40°C to +85°C	SOT23-3

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply voltage, $V_{CC}$	-0.3V to +6.0 V
DC input voltage (all inputs except $V_{CC}$ and GND)	-0.3V to ( $V_{CC}+0.3V$ )
DC input current (all inputs)	20mA
DC output current (all outputs)	20mA
Junction temperature	125°C
Ambient temperature range	-40°C to +105°C
Storage temperature Range	-65°C to +160°C
Power dissipation	320mW

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$V_{CC}$  = Full Range,  $T_A$  = -40°C to +85°C, unless otherwise noted.

Typical values are at  $T_A$  = +25°C,  $V_{CC}$  = 3.3V for 2.93/3.08V version, and  $V_{CC}$  = 3V for 2.70V/2.63V version.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
	$V_{CC}$ Range	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	1.0		5.5	V
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.2		5.5	
$I_{CC}$	Supply Current	$V_{CC} < 3.6V$		10	20	$\mu\text{A}$
$V_{TH}$	Reset Threshold	ft809R $T_A = +25^\circ\text{C}$	2.55	2.63	2.70	V
		ft809V $T_A = +25^\circ\text{C}$	2.62	2.70	2.77	
		ft809S $T_A = +25^\circ\text{C}$	2.85	2.93	3.00	
		ft809T $T_A = +25^\circ\text{C}$	3.00	3.08	3.15	
	Reset Active Timeout	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	140	240	560	ms
$V_{OL}$	Reset Output Voltage Low	$V_{CC} = V_{TH \text{ min}}$ , $I_{SINK} = 1.2\text{mA}$			0.3	V
		$V_{CC} > 1.4V$ , $I_{SINK} = 50\mu\text{A}$			0.3	
$V_{OH}$	Reset Output Voltage High	$V_{CC} > V_{TH \text{ max}}$ , $I_{SOURCE} = 500\mu\text{A}$	$0.8 V_{CC}$			V

**TYPICAL PERFORMANCE CHARACTERISTICS**

**Supply Current vs. Temperature  
(No Load, 2.63/2.7/2.93/3.08)**

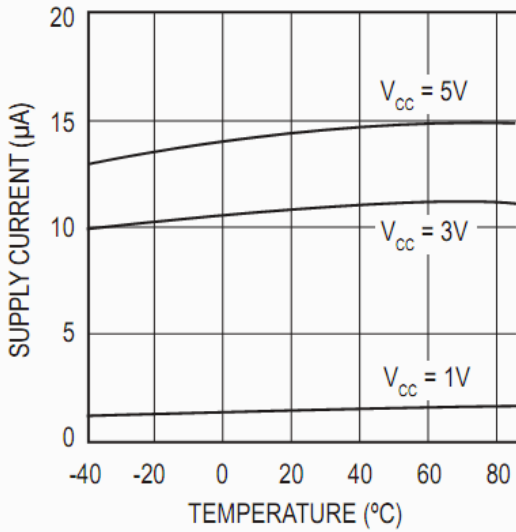


Figure 2: Supply Current vs. Temperature

**Power Up Reset Timeout vs. Temperature**

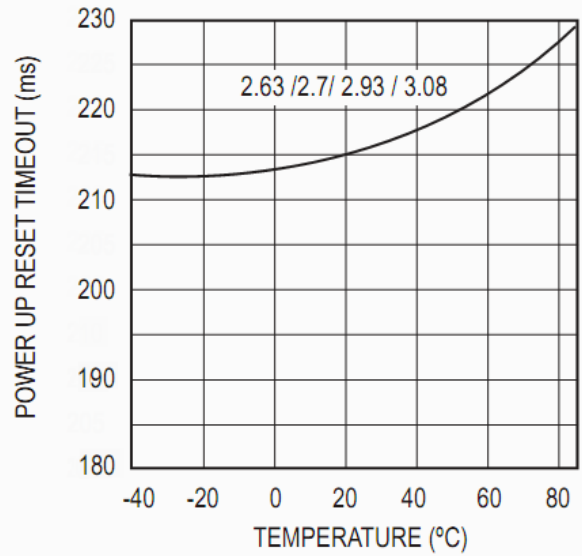


Figure 3: Power Up Reset Timeout vs. Temperature

**Power-Down Reset Delay vs. Temperature  
(2.63/2.7/2.93/3.08)**

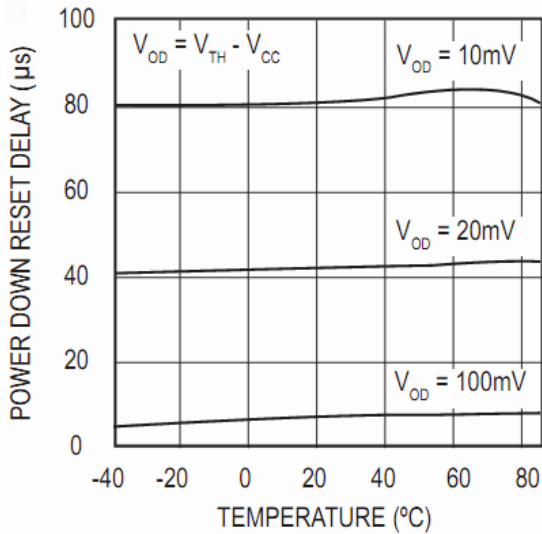


Figure 4: Power-Down Reset Delay vs. Temperature

**Normalized Reset Threshold vs. Temperature**

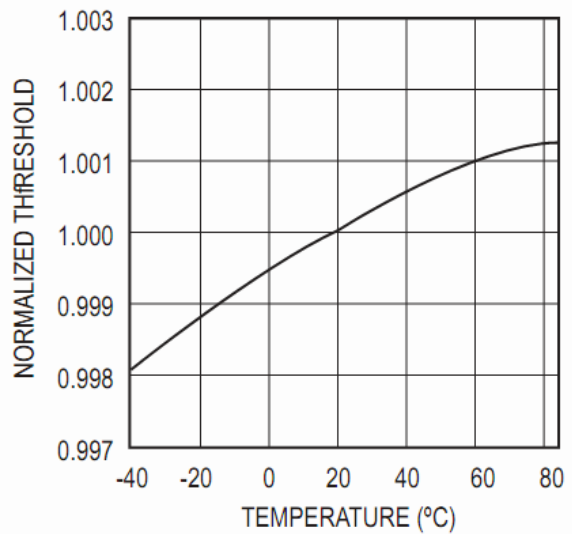


Figure 5: Threshold vs. Temperature

## APPLICATION INFORMATION

### Detailed Operation Description

The ft809 series microprocessor reset circuits are designed to monitor the power supplies in digital systems and provide a reset signal to the processor under the preset conditions. Figure 6 shows the timing diagram below. Initially consider that the input voltage ( $V_{CC}$ ) is higher than the reset threshold ( $V_{thr}$ ) for a long time, the RESET output pin of the ft809 is high. When the input voltage falls below  $V_{thr}$ , the RESET output pin will be driven low to assert reset to the microprocessor. After the power interruption,  $V_{CC}$  will rise to its nominal level above  $V_{thr}$  while the reset signal will remain asserted for a preset period. During the reset process, the ft809 internal oscillator circuitry is activated to count the signal asserting period. The reset signal will revert back to high when the preset asserting period times out.

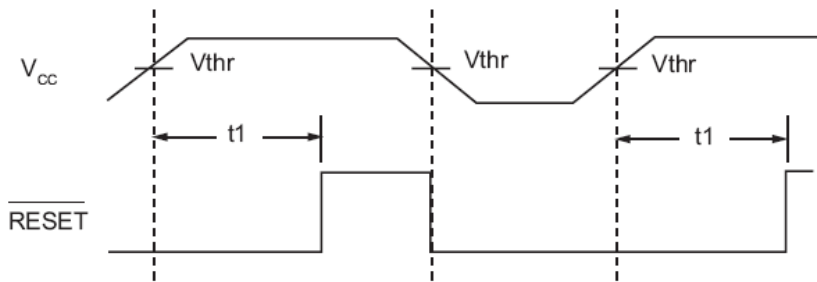


Figure 6: Reset Timing Diagram

### $V_{CC}$ Transient Rejection

While the ft809 series provide accurate power supply monitoring and issue a reset during power-up, power-down and brown-out conditions, they are relatively immune to short-duration, negative-going VCC transients. The VCC transient rejection can be best depicted in Figure 7, which shows typical transient duration for which the ft809 do not generate a reset pulse as a function of reset comparator overdrive. It indicates the maximum pulse width a negative-going VCC transient can have without causing a reset pulse. As the magnitude of the transient increases, the maximum allowable pulse width decreases. Typically, for a VCC transient that goes 100mV below the reset threshold and lasts 20 $\mu$ s or less will not cause a reset pulse. Additional transient immunity can be obtained by mounting a 0.1 $\mu$ F bypass capacitor as close as possible to the  $V_{CC}$  pin.

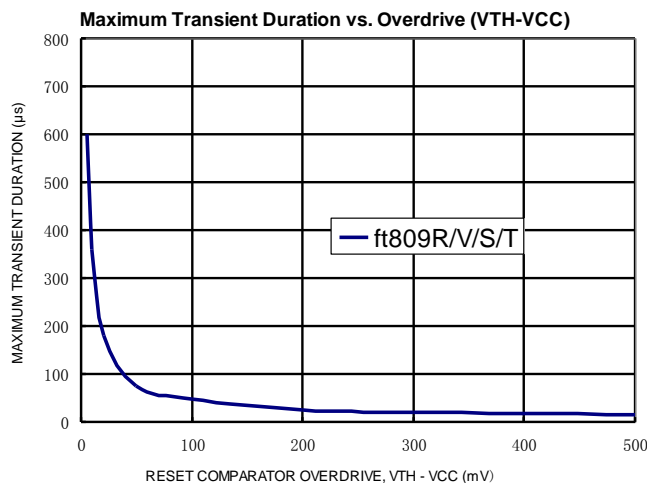


Figure 7: Maximum Transient Duration vs. Reset Comparator Overdrive

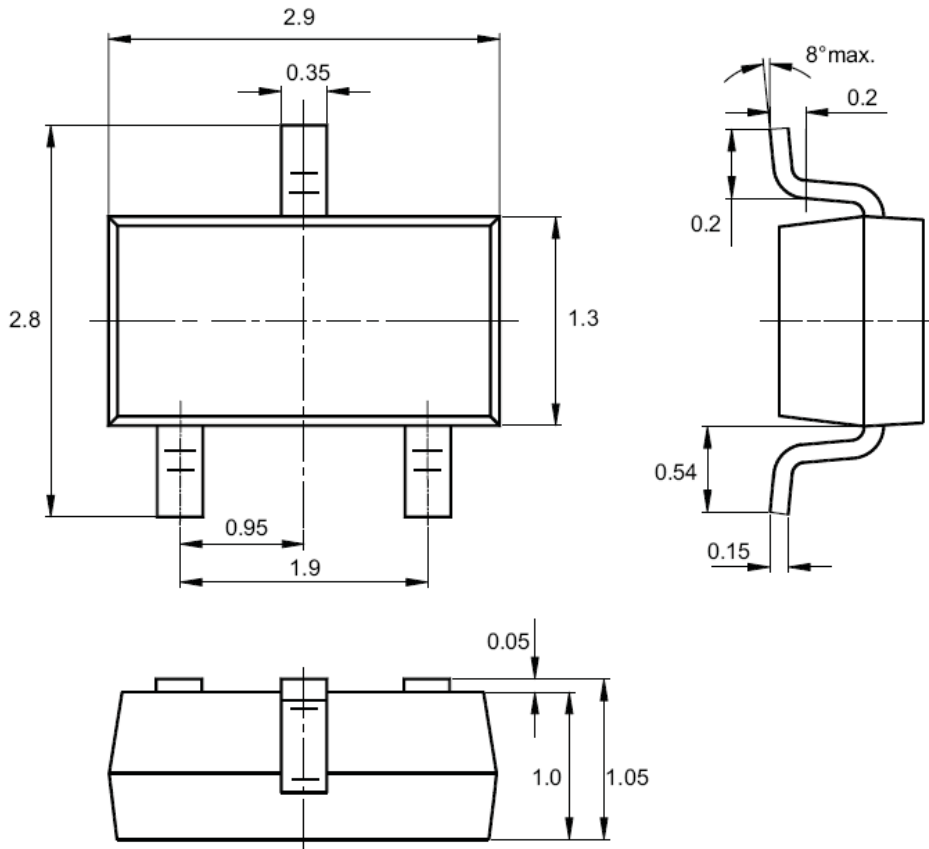
### Enable Reset during Power-down

When  $V_{CC}$  falls below 1V, the ft809  $\overline{\text{RESET}}$  output no longer sinks current. This will cause the CMOS logic inputs to the microprocessor floating at an undetermined voltage. Most digital systems are shutdown well above this voltage. However, in situations where  $\overline{\text{RESET}}$  must be maintained valid to  $V_{CC} = 0V$ , a pull-down resistor must be connected from  $\overline{\text{RESET}}$  to ground to discharge stray capacitance and hold the output low. A 100k $\Omega$  resistor will be suitable for most applications.

### Processors with Bi-directional I/O Pins

When the ft809 is to use with microprocessors with a bi-directional reset pin, logic conflict may take place and cause undermined logic level. To avoid such situation, a 4.7k $\Omega$  resistor shall be connected in series between the  $\overline{\text{RESET}}$  pin and the microprocessor reset interface. If there are other components requiring a reset signal, a buffer shall be added between the reset pin and the other system components.

**PHYSICAL DIMENSIONS**



Unit: millimeters.

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