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Genesis Microchip Inc.

2150 Gold Street, P.O. Box 2150, Alviso, CA USA 95002 Tel: (408) 262-6599 Fax: (408) 262-6365
165 Commerce Valley Dr. West, Thornhill, ON Canada L3T 7V8 Tel: (905) 889-5400 Fax: (905) 889-5422
George Thangiah Complex(E), 2nd Flr, 80 Feet Road, Jeevan Bhima Nagar, Bangalore 560 075, India, Tel 91-80-526 3878 Fax 91-80-529 6245
4F, No. 57, Sing Jung Road, NeiHu Taipei, Taiwan 114, R.O.C Tel: 886-2-2791-0118 Fax: 886-2-2791-0196
143-37 Hyundai Tower, #902, Samsung-dong, Kangnam-gu, Seoul, Korea 135-090 Tel 82-2-553-5693 Fax 82-2-552-4942
Rm2614-2618 Shenzhen Office Tower, 6007 Shennan Blvd, 518040, Shenzhen, Guandong, P.R.C., Tel (0755)386-0101, Fax (0755)386-7874
2-9-5 Higashigotanda, Shinagawa-ku, Tokyo, 141-0022, Japan, Tel 81-3-5798-2758, Fax 81-3-5798-2759
www.genesis-microchip.com / info@genesis-microchip.com

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1. OVERVIEW

The Genesis Microchip gm6015 display processor is a low-cost, high-quality video processor for progressive TV (480p), digital TV (DTV) and high definition TV (HDTV) applications. The highly integrated gm6015 includes dual digital video inputs for MAIN and PIP display, dual bi-level / tri-level sync separators, "pixel-based" motion adaptive de-interlacing, 2:2/3:2 inverse pull-down film processing, diagonal processing, arbitrary shrink/zoom scaling on both MAIN and PIP channels, , "3D" noise reduction filter, SDRAM controller, color space conversion, color controls, video look up table (VLUT) and multi-image PIP display.

1.1 Applications

- SDTV, HDTV and DTV
- Flat panel TV (LCD, PDP)
- Set-top box
- Scan converter box

1.2 System Design Example

Figure 1 below shows a XGA LCD TV system block diagram using gm6015. Designs based on gm6015 will benefit from its high integration and flexibility, which result in lower system cost and design for multi-platform approach.

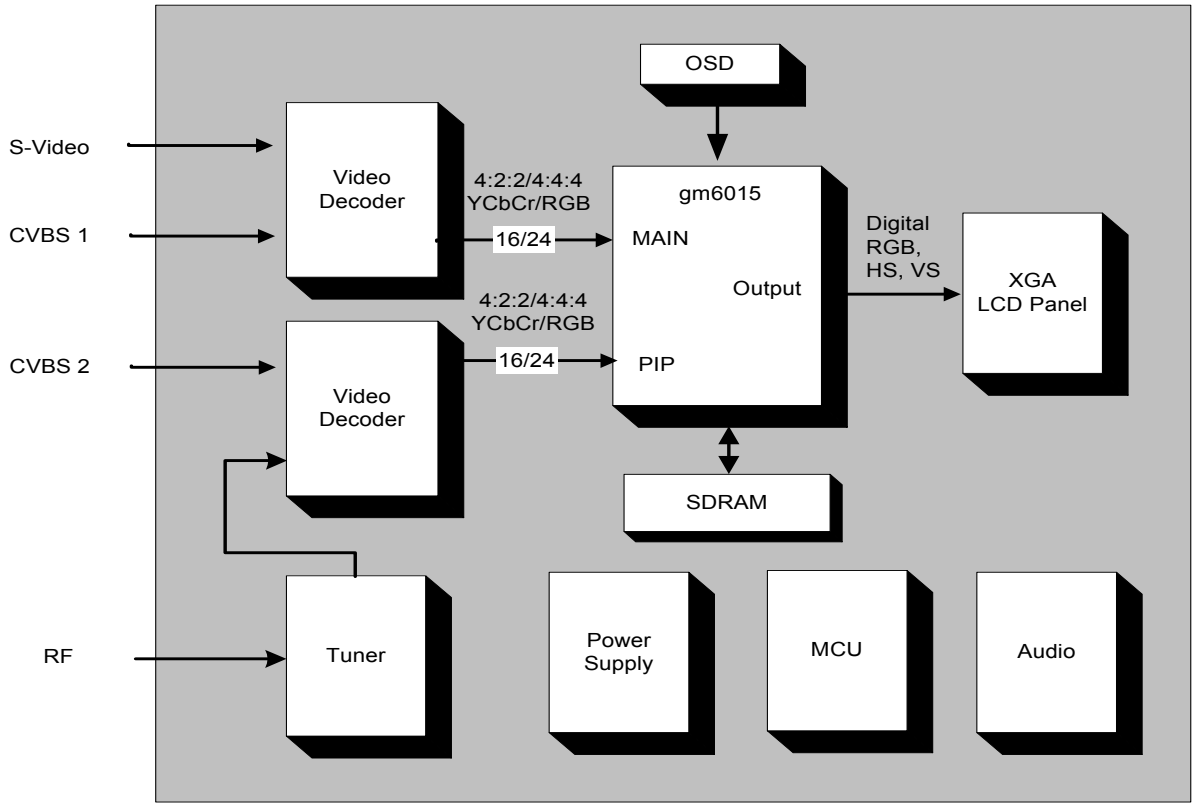


Figure 1. gm6015 System Design Example

1.3 gm6015 Features

- **Dual Digital Input Port**
  - Interface compatible with common NTSC/PAL/SECAM video decoders, YPbPr/YUV/RGB digitizers, MPEG decoders and DVI receivers.
  - Bi-level and tri-level sync strip / processing.
  - Support for 8/16/24-bit 4:2:2/4:4:4 CCIR 656/601 YCbCr and RGB inputs.
  - Programmable input capture size allows input of various SDTV / HDTV resolutions.
  - Flexible input port configuration for various video format and data bus width.
  - Clamp pulse generation for ADC interface.
  - Progressive / Interlace input supported.
  - Dual input format measurement units for input timing detection support
  - Built-in Wide Screen Signal (WSS) decoder
- **Digital Output Port**
  - Embedded (SOG) or separate syncs output.
  - Programmable Y C delay (+ / - 3 pixels)
  - 4:2:2 / 4:4:4 YCbCr / RGB output formats
  - ITU-R BT.656 output supported
  - 6 / 8 / 10 bits per channel.
  - Programmable MAIN and PIP display size for various VESA / SDTV / HDTV resolutions.
  - Bi-level / tri-level sync support
  - Progressive / Interlace output
- **Genesis Proprietary De-interlacing**
  - Auto detection of film or video source
  - 2nd generation adaptive film mode (AFM) de-interlacing.
  - Motion adaptive de-interlacing or inverse 3:2/2:2 pull-down de-interlacing on Main channel
  - Diagonal processing in MAIN channel
  - De-interlacing on PIP channel
- **Advanced Arbitrary Scaling**
  - Programmable zoom/shrink scale on MAIN channel allows aspect ratio to be converted or preserved.
  - Programmable zoom/shrink scale on PIP channel allows variable PIP size.
  - Panoramic zoom / shrink are supported in MAIN channel

- **Flexible MAIN / PIP Configuration**
  - Multiple PIPs supported. A maximum of 16 PIP windows can be displayed.
  - Programmable MAIN and PIP positions
  - Programmable MAIN background colors
  - Programmable PIP border colors.
  - Programmable blending levels of PIP display.
  - Hi-light border eases active PIP selection in multi-PIP display
  - Instantaneous MAIN / PIP swapping
- **Others**
  - Integrated triple 256x10-bit video look up table.
  - Integrated SDRAM controller. Typically only 1 2M x 32-bit SDRAM is needed.
  - Integrated DDS and PLL for clock generation. Only a single low cost 14.31818 MHz crystal is needed externally.
  - Arbitrary up/down frame rate conversion. (e.g. 50Hz to 60Hz, 50Hz to 100Hz, 60Hz to 50Hz, ….etc)
  - Input and output color space conversion (CSC)
  - Fully programmable color space coefficients and offsets in MAIN and PIP input CSC.
  - Bypass channel available
  - “3D” noise reduction filter in MAIN channel for standard definition video
  - Sharpening filter in MAIN channel with selectable coefficients.
  - Programmable interrupt
  - Chip activity monitoring circuit.
  - OSD interface
  - 2-wire or 3-wire SPI host interface

2. PINOUT DIAGRAM

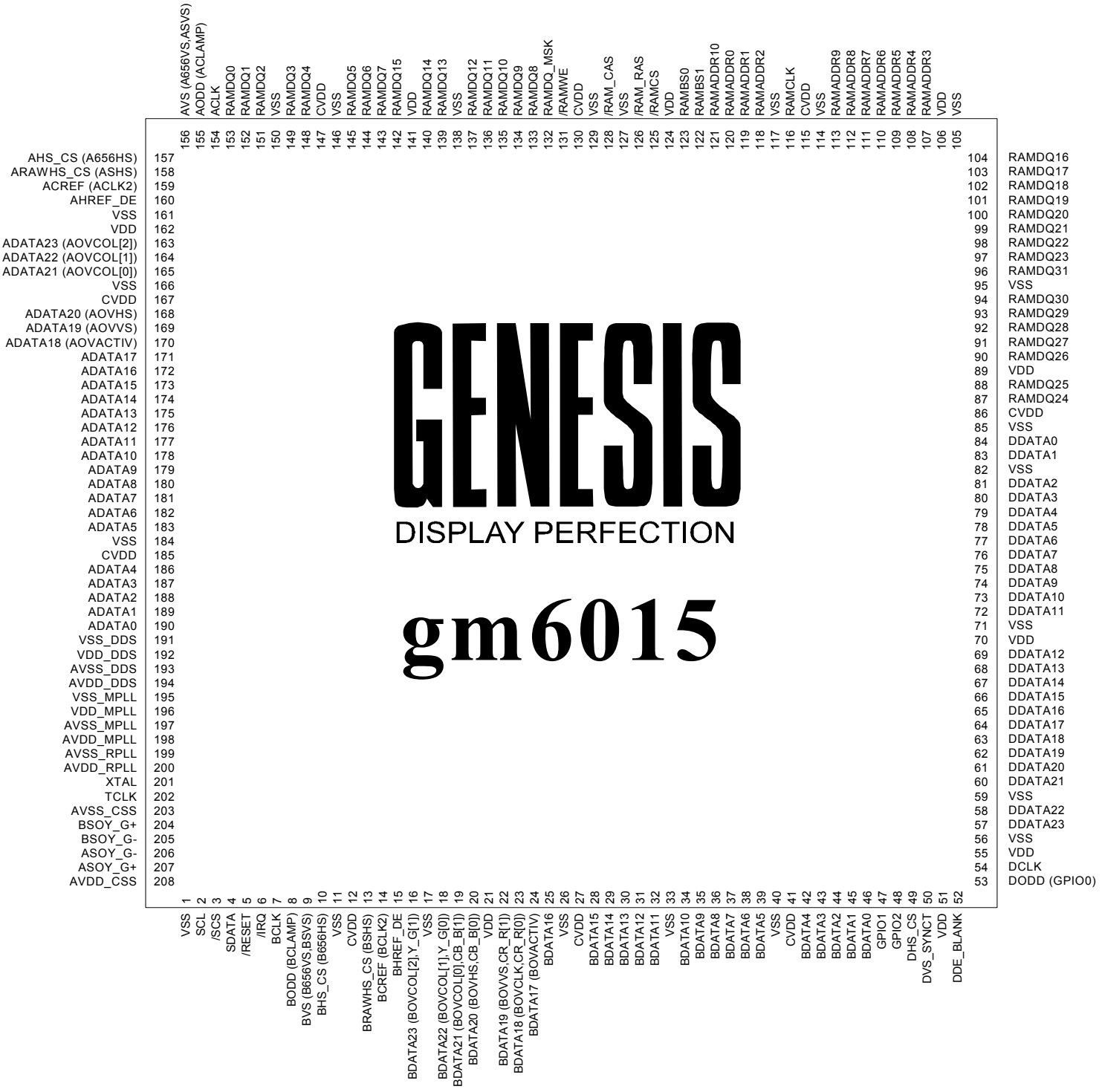


Figure 2. gm6015 Pinout Diagram

3. PIN DESCRIPTION

I/O Legend: **I** = Input **O** = Output **P** = Power **G** = Ground

Table 1. Input Port A

Name	I/O	Pin#	Description
ACLK1	I	154	Port A input clock 1
AODD	I	155	1. Port A odd/even field indicator input (Default)
(ACLAMP)	O		2. Port A clamp pulse output
AVS	I	156	1. Port A input VS (Default)
(A656VS)	O		2. Port A VS extracted from 656 data
(ASVS)	O		3. Port A VS extracted from SOG / SOY
AHS_CS	I	157	1. Port A input HS or composite sync (Default)
(A656HS)	O		2. Port A HS extracted from 656 data
ASOY_G+	I	207	Port A bi-level / tri-level sync on green / Y
ASOY_G-	I	206	Port A bi-level / tri-level sync on green / Y
ARAWHS_CS	I	158	1. Port A raw HS or composite sync (Default)
(ASHS)	O		2. Port A HS extracted from SOG / SOY
ACREF	I	159	1. Port A input clock qualifier (Default)
(ACLK2)	I		2. Port A input clock 2
AHREF_DE	I	160	Port A input HREF or DE (Data Enable) from DVI receiver
ADATA23 (AOVCOL[2])	I	163	1. Port A input data or overlay interface. Please refer to Table 11 for bus selection.
ADATA22 (AOVCOL[1])	I	164	2. Overlay interface
ADATA21 (AOVCOL[0])	I	165	
ADATA20 (AOVHS)	I (O)	168	
ADATA19 (AOVVS)	I (O)	169	
ADATA18 (AOVCLK)	I (O)	170	
ADATA17 (AOVACTIV)	I	171	
ADATA16	I	172	
ADATA15	I	173	
ADATA14	I	174	
ADATA13	I	175	
ADATA12	I	176	
ADATA11	I	177	
ADATA10	I	178	
ADATA9	I	179	
ADATA8	I	180	
ADATA7	I	181	
ADATA6	I	182	
ADATA5	I	183	
ADATA4	I	186	
ADATA3	I	187	
ADATA2	I	188	
ADATA1	I	189	
ADATA0	I	190	

Table 2. Input Port B

Name	I/O	Pin#	Description
BCLK1	I	7	Port B input clock 1
BODD (BCLAMP)	I O	8	1. Port B odd/even field indicator input (Default) 2. Port B clamp pulse output
BVS (B656VS) (BSVS)	I O O	9	1. Port B input VS (Default) 2. Port B VS extracted from 656 data 3. Port B VS extracted from SOG / SOY
BHS_CS (B656HS)	I O	10	1. Port B input HS or composite sync (Default) 2. Port B HS extracted from 656 data
BSOY_G+	I	204	Port B bi-level / tri-level sync on green / Y
BSOY_G-	I	205	Port B bi-level / tri-level sync on green / Y
BRAWHS_CS (BSHS)	I O	13	1. Port B raw HS or composite sync (Default) 2. Port B HS extracted from SOG / SOY
BCREF (BCLK2)	I I	14	1. Port B input clock qualifier (Default) 2. Port B input clock 2
BHREF_DE	I	15	Port B HREF or DE (Data Enable) from TMDS receiver
BDATA23 (BOVCOL[2], Y_G[1])	I (I, O)	16	1. Port B input data. Please refer to Table 11 for bus selection. 2. Overlay interface. 3. Output LSB bits of 10-bit per channel output data • 30-bit YCbCr 4:4:4 BDATA[23:22] = Y[1:0] BDATA[21:20] = Cb[1:0] BDATA[19:18] = Cr[1:0] • 30-bit RGB BDATA[23:22] = G[1:0] BDATA[21:20] = B[1:0] BDATA[19:18] = R[1:0]
BDATA22 (BOVCOL[1], Y_G[0])	I (I, O)	18	
BDATA21 (BOVCOL[0], CB_B[1])	I (I, O)	19	
BDATA20 (BOVHS, CB_B[0])	I (O, O)	20	
BDATA19 (BOVVS, CR_R[1])	I (O, O)	22	
BDATA18 (BOVCLK, CR_R[0])	I (O, O)	23	
BDATA17 (BOVACTIV)	I	24	
BDATA16	I	25	
BDATA15	I	28	
BDATA14	I	29	
BDATA13	I	30	
BDATA12	I	31	
BDATA11	I	32	
BDATA10	I	34	
BDATA9	I	35	
BDATA8	I	36	
BDATA7	I	37	
BDATA6	I	38	
BDATA5	I	39	
BDATA4	I	42	
BDATA3	I	43	
BDATA2	I	44	
BDATA1	I	45	
BDATA0	I	46	

Table 3. Digital Display Port

Name	I/O	Pin#	Description
DDATA[23]	O	57	Digital display data bus. Please refer to Input Port B for 10-bit RGB / YCbCr 4:4:4 LSB bits For pin assignment of various video formats please refer to Table 14.
DDATA[22]	O	58	
DDATA[21]	O	60	
DDATA[20]	O	61	
DDATA[19]	O	62	
DDATA[18]	O	63	
DDATA[17]	O	64	
DDATA[16]	O	65	
DDATA[15]	O	66	
DDATA[14]	O	67	
DDATA[13]	O	68	
DDATA[12]	O	69	
DDATA[11]	O	72	
DDATA[10]	O	73	
DDATA[9]	O	74	
DDATA[8]	O	75	
DDATA[7]	O	76	
DDATA[6]	O	77	
DDATA[5]	O	78	
DDATA[4]	O	79	
DDATA[3]	O	80	
DDATA[2]	O	81	
DDATA[1]	O	83	
DDATA[0]	O	84	

Table 4. Display Control

Name	I/O	Pin#	Description
DCLK	O	54	Display output clock
DVS (DSYNCT)	O O	50	1. Display VSYNC (Default) 2. Display tri-level sync control
DHS_CS	O	49	Display HSYNC / composite sync
DODD (GPIO 0)	O I/O	53	1. Display field indicator (Default) 2. General purpose I/O pin 0 Note: This is a GPIO pin with DODD as default function. For other GPIO functions, refer to section 4.11.
DDE_BLANK	O	52	1. Display data enable / blanking

Table 5. SDRAM Interface Signals

Name	I/O	Pin#	Description
RAMCLK	O	116	SDRAM clock
RAMBS0	O	123	SDRAM bank select 0
RAMBS1	O	122	SDRAM bank select 1
RAMCS#	O	125	SDRAM chip select
RAMDQ_MSK	O	132	SDRAM data input / output mask
RAMWE#	O	131	SDRAM write enable
RAM_RAS#	O	126	SDRAM row address strobe
RAM_CAS#	O	128	SDRAM column address strobe
RAMADDR10	O	121	SDRAM address bus
RAMADDR9	O	113	
RAMADDR8	O	112	
RAMADDR7	O	111	
RAMADDR6	O	110	
RAMADDR5	O	109	
RAMADDR4	O	108	
RAMADDR3	O	107	
RAMADDR2	O	118	
RAMADDR1	O	119	
RAMADDR0	O	120	
RAMDQ31	I/O	96	SDRAM data bus
RAMDQ30	I/O	94	
RAMDQ29	I/O	93	
RAMDQ28	I/O	92	
RAMDQ27	I/O	91	
RAMDQ26	I/O	90	
RAMDQ25	I/O	88	
RAMDQ24	I/O	87	
RAMDQ23	I/O	97	
RAMDQ22	I/O	98	
RAMDQ21	I/O	99	
RAMDQ20	I/O	100	
RAMDQ19	I/O	101	
RAMDQ18	I/O	102	
RAMDQ17	I/O	103	
RAMDQ16	I/O	104	
RAMDQ15	I/O	142	
RAMDQ14	I/O	140	
RAMDQ13	I/O	139	
RAMDQ12	I/O	137	
RAMDQ11	I/O	136	
RAMDQ10	I/O	135	
RAMDQ9	I/O	134	
RAMDQ8	I/O	133	
RAMDQ7	I/O	143	

Name	I/O	Pin#	Description
RAMDQ6	I/O	144	
RAMDQ5	I/O	145	
RAMDQ4	I/O	148	
RAMDQ3	I/O	149	
RAMDQ2	I/O	151	
RAMDQ1	I/O	152	
RAMDQ0	I/O	153	

Table 6. Host Interface

Name	I/O	Pin#	Description
/SCS	I	3	Chip select for 3-wire mode. Active low.
SCLK	I	2	Clock for host interface.
SDATA	I/O	4	Serial data.
/RESET	I	5	Reset. Active low
/IRQ	O	6	Interrupt output. Active low, open drain

Table 7. PLL / DDS

Name	I/O	Pin#	Description
TCLK	O	202	Feedback connection to 14.318 MHz crystal. If the reference clock source is a clock oscillator, this pin should be grounded through a 2.7K pulldown resistor.
XTAL	I	201	Crystal oscillator input. Connect to 14.318 MHz crystal.

Table 8. General Purpose I/O

Name	I/O	Pin#	Description
GPIO1	I/O	47	General Purpose I/O
GPIO2	I/O	48	General Purpose I/O

Table 9. Power and Ground

Name	I/O	Pin#	Description
Composite Sync Separator			
AVDD_CSS	P	208	3.3V analog power for composite sync separator
AVSS_CSS	G	203	Analog ground for composite sync separator
PLL / DDS			
AVDD_RPLL	P	200	3.3V analog power for REFCLK PLL
AVDD_MPLL	P	198	3.3V analog power for PROCCLK PLL
AVDD_DDS	P	194	3.3V Analog power for DCLK DDS
VDD_PLL	P	196	3.3V digital power for DCLK PLL
VDD_DDS	P	192	3.3V digital power for DDS
AVSS_RPLL	G	199	Analog ground for REFCLK PLL
AVSS_MPLL	G	197	Analog ground for PROCCLK PLL
AVSS_DDS	G	193	Analog ground for DCLK DDS

Name	I/O	Pin#	Description
VSS_PLL	G	195	Digital ground for DCLK PLL
VSS_DDS	G	191	Digital ground for DDS
Others			
VDD	P	21, 51, 70, 89, 106, 124, 141, 162,	3.3V Power for I/O logic
CVDD	P	12, 27, 41, 55, 86, 115, 130, 147, 167, 185	2.5V Power for core logic
VSS	G	1, 11, 17, 26, 33, 40, 56, 59, 71, 82, 85, 95, 105, 114, 117, 127, 129, 138, 146, 150, 161, 166, 184	Ground

4. FUNCTIONAL DESCRIPTION

The block diagram below illustrates the internal functional blocks of gm6015. Each block will be described in the following sections.

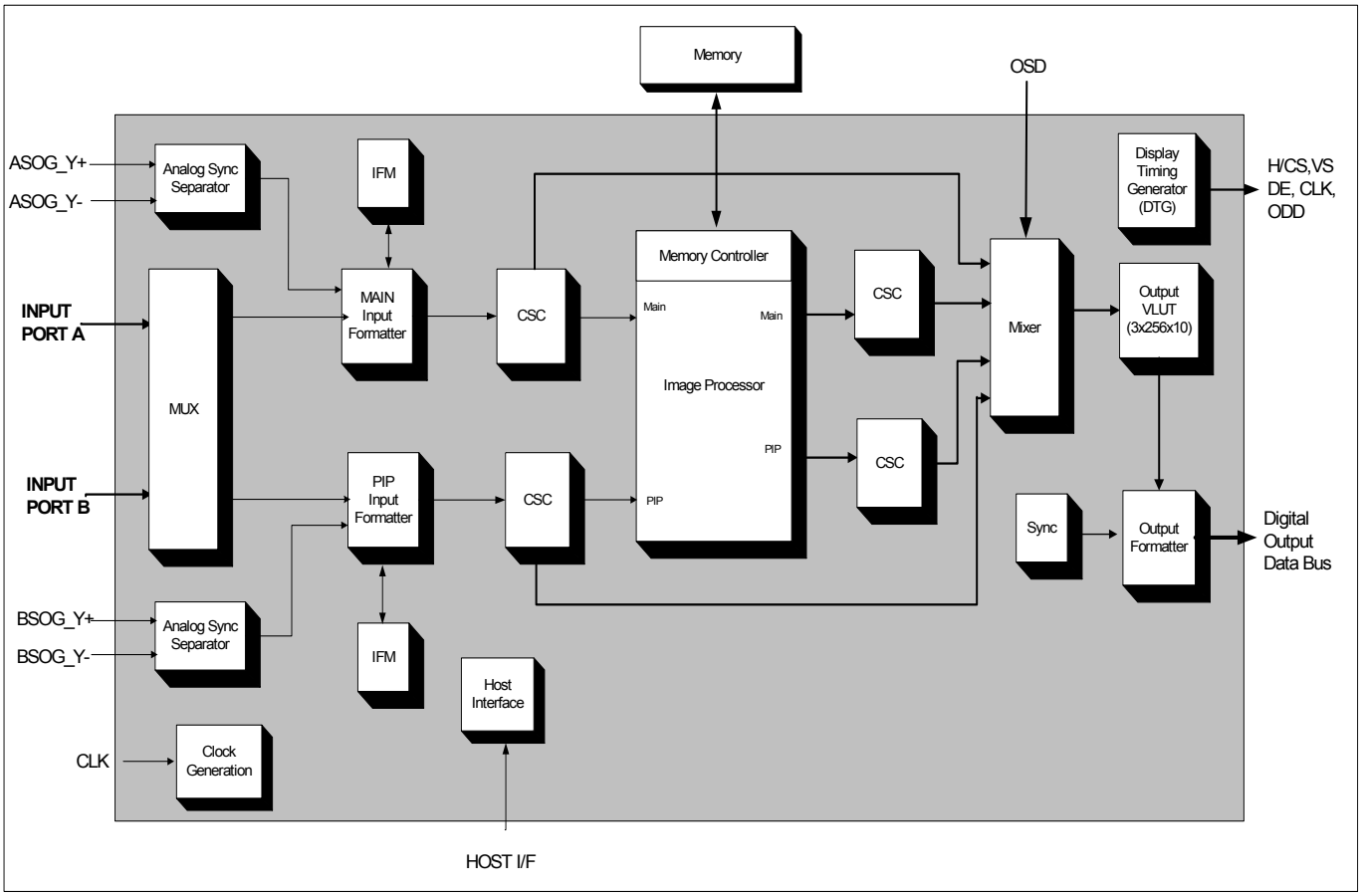


Figure 3. gm6015 Functional Block Diagram

4.1 Reset

4.1.1 Hardware Reset

Hardware reset is performed by holding the /RESET pin low for a minimum of 1µs. The clock from external clock source (typically 14.31818MHz, see Figure 3 and Figure 4) must be present during and after the reset. All registers will be reset to their default values.

4.1.2 Software Reset

Software reset is performed by setting HOST_CTRL register bit SOFT_RESET to 1. This bit will be self-cleared to 0 upon completion of reset. The status of each clock domain after reset can be read from the RESET_STATUS register. All active and status registers will be reset to their default state. Pending and read/write registers are not affected by software reset.

4.2 Bootstrap Configuration

During hardware reset, some SDRAM interface pins (RAMADDR [10:0], RAMBS[1..0], RAMDQ_MSK) are configured as inputs. Pull high or pull low resistors (10KΩ) can be placed in these pins. On the falling edge of /RESET, the value on these lines is captured. This value is readable by the external microcontroller and is used to configure gm6015 host interface and other user defined options.

Table 10. Bootstrap Configuration

Pin Name	Description
RAMADDR[4:0]	1. If 2-wire protocol is selected, this sets device address bit [5..1]. 2. If 3-wire protocol is selected, this pins are ignored.
RAMADDR[5]	1. If 2-wire protocol is selected, this sets device address bit [6]. 2. If 3-wire protocol is selected : - pull high to select active drive on SDATA pin - pull low to select open drain on SDATA pin
RAMADDR[6]	1. If 2-wire protocol is selected, this sets device address bit [7]. 2. If 3-wire protocol is selected : - pull high to select transmit on SCLK falling edge and receive on SCLK rising edge - pull low to select transmit on SCLK rising edge and receive on SCLK falling edge
RAMADDR[7]	1. Pull high to select 3-wire SPI protocol 2. Pull low to select 2-wire I^2C compatible protocol
RAMADDR[8]	User defined option 0
RAMADDR[9]	User defined option 1
RAMADDR[10]	User defined option 2
BS0	User defined option 3
BS1	User defined option 4
DQM	TCLK frequency 1. Pull high : TCLK frequency > 14.31818 MHz 2. Pull low : TCLK frequency <= 14.31818 MHz

4.3 Clock Generation and Distribution

gm6015 has built-in PLLs (Phase Locked Loops) and DDS (Direct Digital Synthesis) to generate all the clocks necessary for all the functional blocks. Each clock can be programmed to route to various functional blocks.

4.3.1 External Crystal / Oscillator

Externally a single crystal or TTL/CMOS level clock oscillator is needed. The following two figures illustrate the use in each case:

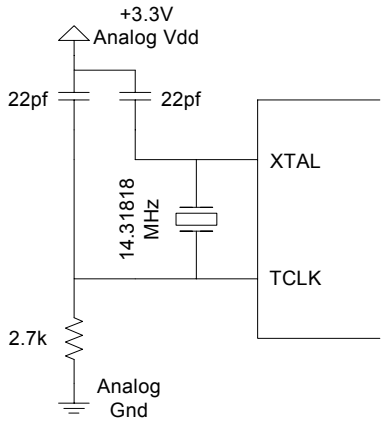


Figure 4. Using crystal

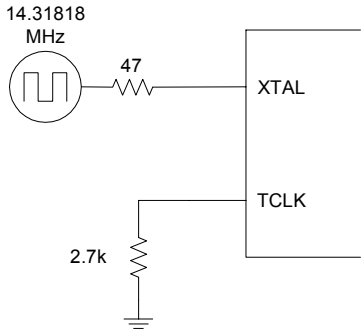


Figure 5. Using oscillator

In Figure 4 all components should be placed close to the chip, with a clean analog ground. In Figure 5 the 47Ω resistor should be placed close to the oscillator. The internal oscillating circuit will generate OSCCLK, which are used by the built-in PLLs to generate all internal clocks, as described in the next section.

4.3.2 PLL / DDS

The built-in PLLs and DDS are used to generate all internal clocks as well as display clock. The following is a block diagram of the PLL/DDS block:

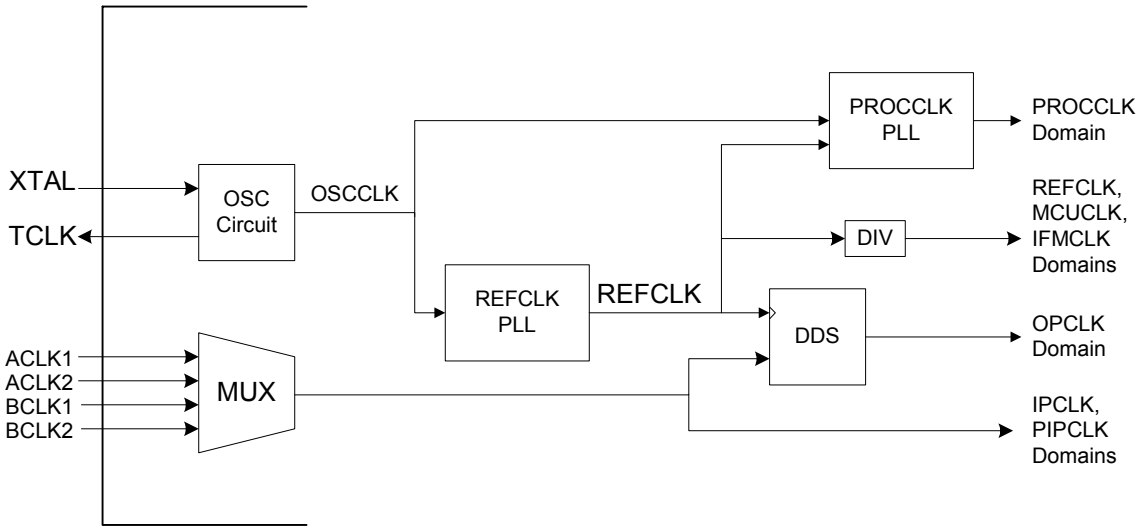


Figure 6. Clock Generation and Distribution

The REFCLK PLL is programmed to generate a 171MHz clock which is used by the PROCCLK PLL, the DDS and other clock domains, namely REFCLK, MCUCLK and IFMCLK domains. REFCLK will be further divided in MCUCLK and IFMCLK domains.

The PROCCLK PLL is programmed to generate a 100MHz clock to be used by other blocks. The DDS locks its output frequency (DDSCLK) to the selected input clock (normally the clock for the MAIN channel) and it can be programmed to generate a wide range of frequency (from 12MHz to 110MHz) for the display clock.

The following equation is used to calculate the output frequency of the 2 PLLs. MULT and DIV are 5-bit numbers, with a valid range from 0 to 31 decimal. PDIV is a 2-bit number, with a value of 0 to 3 decimal.

$$f_{PLLCLK} = f_{OSCCLK} \times \frac{MULT + 1}{DIV + 1} \times \frac{1}{2^{PDIV}}$$

For details in PLL / DDS programming, please refer to “gm6010/6015 Register Programming Guide”

4.3.3 Clock Domains

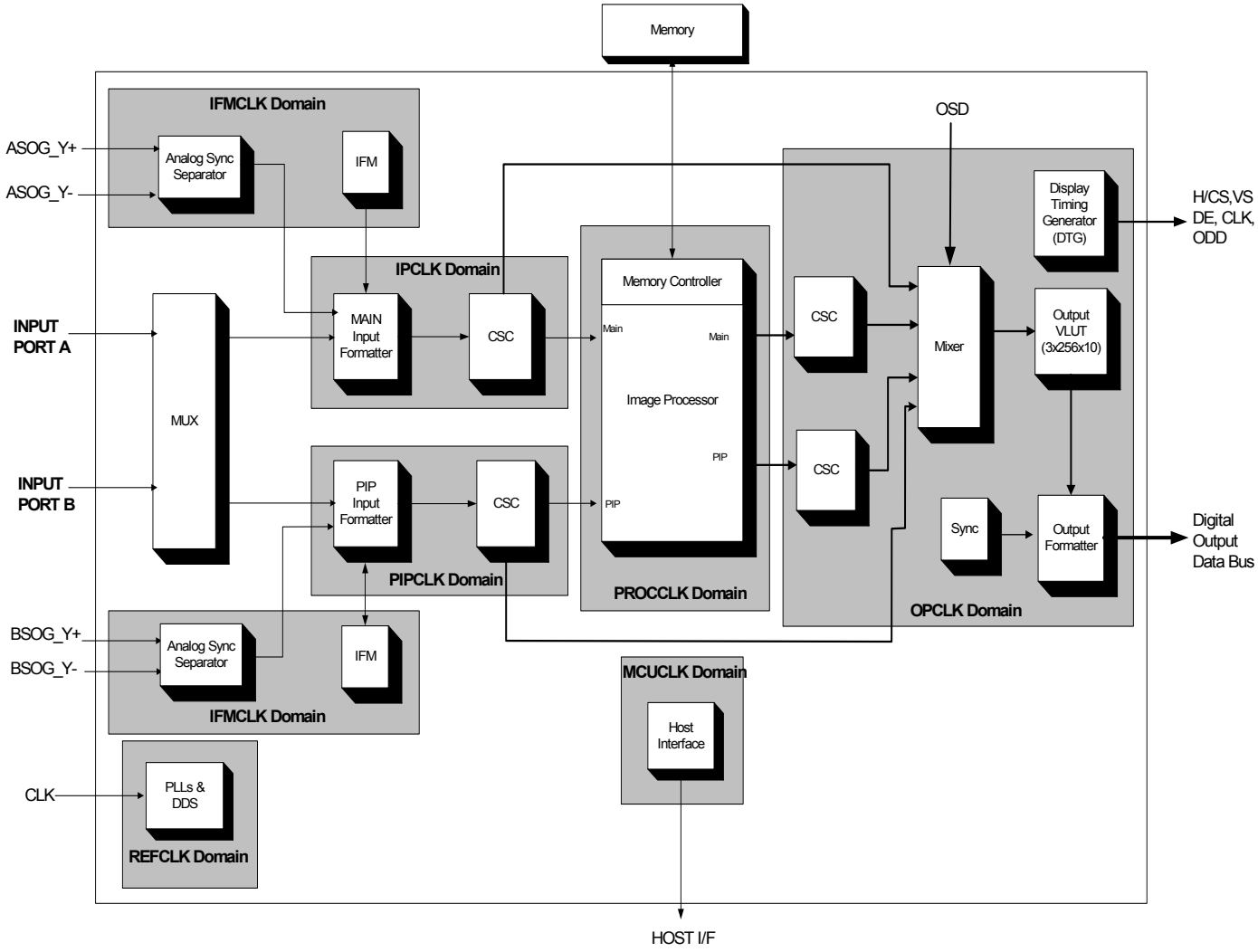


Figure 7. Clock Domains

Each functional block in gm6015 is driven by a clock which is programmable to come from different sources. The following is a list of the clock domains in gm6015:

1. IPCLK domain. This is the clock for the MAIN input channel. This will normally come from ACLK1/ACLK2 or BCLK1/BCLK2, depends on which port is selected as the MAIN channel.
2. PIPCLK domain. This is the clock for the PIP input channel. This will normally come from ACLK1/ACLK2 or BCLK1/BCLK2, depends on which port is selected as the PIP channel.
3. IFMCLK domain. This is the clock for the IFM and the Analog Sync Separator blocks. This will normally be driven by the REFCLK PLL divided by 4 (50 MHz clock).

4. REFCLK domain. This is the clock for the DDS. This comes from the output of the REFCLK PLL (200 MHz clock).
5. MCUCLK domain. This is the clock for the embedded microcontroller and the gm6015 host interface. Since this clock drives the host interface, it must have a stable source at reset. At reset, this clock will be driven by TCLK pin. After the PLLs have had time to lock and settle, the source of this clock will be automatically switched to REFCLK divided by 4 (50 MHz clock). This automatic switching can be disabled or overriden by the use of bootstrap inputs (RAMDQ_MSK).
6. PROCCLK domain. This is the video processing and memory interface clock. The filters in MAIN channel and SDRAM interface run in this clock domain. This comes from the output of the PROCCLK PLL (100 MHz clock).
7. OPCLK domain. This is the display clock for the chip. This normally comes from the DDS (programmable frequency locked to IPCLK).

4.4 Input Interface

Two identical digital input ports (Port A and Port B) are provided as interfaces to input video. Each port can be programmed to accept various input video formats and provide glueless interface to most NTSC/PAL/SECAM video decoders, YCbCr/RGB digitizers (ADC/PLL), MPEG decoders and LVDS/TMDS receivers.

4.4.1 Input Port Selection

Both Port A and Port B can be used as the source for MAIN or PIP display. All parameters in MAIN and PIP input registers (e.g. input capture window size, input lock event, …etc.) need to be set according to the input video format in each port.

gm6015 allows a very flexible configuration on the data bus going into the input ports. Each 24-bit input port can be configured to be:

- Three 8-bit bus port
- One 8-bit bus port and one 16-bit bus port
- One 24-bit bus port

RGB or YCbCr data can be connected to any bus in each configuration. However, all the input timing signal pins (except pixel clock) will also be associated with the data bus selected.

2 input pixel clock pins are available for each input port. The pixel clock to be used can be selected to come from either Port A or Port B.

The data bus configuration of each input port can be selected by bit[2:0] of *MAIN_IP_SRC* and *PIP_IP_SRC* registers, as shown in the following table :

Table 11. Input Video Data Bus Mapping On Port A and Port B

bit[2:0] =	000	001	010	011	100	101
24 bit RGB	DATA[23:16]=G	DATA[23:16]=G	DATA[23:16]=R	DATA[23:16]=B	DATA[23:16]=R	DATA[23:16]=B

	DATA[15:8]=B DATA[7:0]=R	DATA[15:8]=R DATA[7:0]=B	DATA[15:8]=G DATA[7:0]=B	DATA[15:8]=G DATA[7:0]=R	DATA[15:8]=B DATA[7:0]=G	DATA[15:8]=R DATA[7:0]=G
24 bit YUV 4:4:4	DATA[23:16]=Y DATA[15:8]=U DATA[7:0]=V	DATA[23:16]=Y DATA[15:8]=V DATA[7:0]=U	DATA[23:16]=V DATA[15:8]=Y DATA[7:0]=U	DATA[23:16]=U DATA[15:8]=Y DATA[7:0]=V	DATA[23:16]=V DATA[15:8]=U DATA[7:0]=Y	DATA[23:16]=U DATA[15:8]=V DATA[7:0]=Y
16 bit YUV 4:2:2	DATA[23:16]=Y DATA[15:8]='X' DATA[7:0]=UV	DATA[23:16]=Y DATA[15:8]= UV DATA[7:0]='X'	DATA[23:16]= UV DATA[15:8]=Y DATA[7:0]='X'	DATA[23:16]= 'X' DATA[15:8]=Y DATA[7:0]=UV	DATA[23:16]=UV DATA[15:8]= 'X' DATA[7:0]=Y	DATA[23:16]= 'X' DATA[15:8]=UV DATA[7:0]=Y
8 bit YUV 4:2:2	DATA[23:16]='X' DATA[15:8]='X' DATA[7:0]=YUV	DATA[23:16]='X' DATA[15:8]= YUV DATA[7:0]='X'	DATA[23:16]= YUV DATA[15:8]='X' DATA[7:0]='X'	DATA[23:16]= 'X' DATA[15:8]='X' DATA[7:0]=YUV	DATA[23:16]=YUV DATA[15:8]= 'X' DATA[7:0]='X'	DATA[23:16]= 'X' DATA[15:8]=YUV DATA[7:0]='X'

NOTE :

i) bit[2:0] = '110' or '111' are invalid;

ii) 'X' means not used

iii) If output is set to 30-bit RGB or 30-bit 4:4:4 YCbCr, then BDATA[23:18] in input port B are used as 2 LSB bits of 10-bit output data. In such case the input format in port B will be limited. See section 4.4.2.9 for detail.

4.4.2 Input Signals

The following sections describe in details all signals associated with the 2 input ports.

NOTE :

- Each section describes the pins for both Port A and Port B and both pin names will be shown ;
- Some pins have multiple functions and their corresponding pin names are listed for reference. Pin names in bracket are alternate pin functions which need to be enabled by registers.

4.4.2.1 ACLK1
BCLK1

These are the input pixel clocks and they are qualified by ACREF / BCREF respectively. The sampling edge of ACLK / BCLK is programmable and the default is rising edge.

4.4.2.2 ACREF (ACLK2)
BCREF (BCLK2)

- ACREF / BCREF (Default)

  These are the clock qualifiers for ACLK1 / BCLK1 respectively. All data during the sampling edge of ACLK1 / BCLK1 are ignored when ACREF / BCREF is inactive.

- ACLK2 / BCLK2

  These serve as a second input pixel clock pins. When a input port is divided into 2 input data bus, these pins can be used as the input pixel clock for each of the data bus.

4.4.2.3 AODD (ACLAMP)
BODD (BCLAMP)

- AODD / BODD (Default)
  These are the odd / even field indicator input pins and are usually driven by video decoder or MPEG decoder.
- ACLAMP / BCLAMP
  These are the clamp pulse output pins and are usually connected to external ADC to restore the dc level of analog input signal. Location of the start and end of clamp pulse is programmable.

4.4.2.4 AVS (A656VS, ASVS)
BVS (B656VS, BSVS)

- AVS / BVS (Default)
  These pins serve as input vsync pins and are usually connected to video decoder or MPEG decoder.
- A656VS / B656VS
  These pins serve as output vsync pins that are extracted from input video in ITU-BT-656 format. They can be used by external devices which need vsync signal for other timing purposes.
- ASVS / BSVS
  These pins serve as output vsync pins that are extracted from input video with embedded sync on green or Y channel (SOG or SOY). They can be used by external devices which need vsync signal for other timing purposes.

4.4.2.5 AHS_CS (A656HS)
BHS_CS (B656HS)

- AHS_CS / BHS_CS (Default)
  These pins serve as input hsync or composite sync pins and are usually connected from input video decoder or MPEG decoder. For composite sync input, the vsync and hsync will be extracted by the built-in sync separator and can be routed internally to the MAIN and PIP channels. See section 4.4.4.2 “Analog Sync Separator” for detail.
- A656HS / B656HS
  These pins serve as output hsync pins that are extracted from input video in ITU-BT-656 format. They can be used by external devices which need hsync signal for other timing purposes.

4.4.2.6 ASOY_G+, ASOY_G-
BSOY_G+, BSOY_G-

These are differential input sync pins for analog input video with sync signals embedded on green or Y channel. The embedded sync signals will be extracted by the built-in sync separator and can be routed internally to the ASHS / BSHS (for hsync) pins and ASVS / BSVS (for vsync) pins.

4.4.2.7 ARAWHS_CS (ASHS)
BRAWHS_CS (BSHS)

- ARAWHS_CS / BRAWHS_CS (Default)

These pins serve as the raw (unprocessed) input hsync / composite sync pins and they are used for input format measurement

- ASHS / BSHS
  These pins serve as output hsync pins that are extracted from input video with embedded sync on green or Y channel (SOG or SOY).

4.4.2.8 AHREF_DE
BHREF_DE

These are input signals which indicate the presence of active video pixels in a line. HREF signals are usually present in video decoders and DE (Data Enable) signals are usually present in TMDS receivers. All pixels located at the inactive region of these signals are ignored and not processed.

4.4.2.9 ADATA [23:0]
BDATA [23:0]

These are the input video data bus for each port. Video data can be connected to different buses of the same input port. See "Input Port Selection" section for configuration.

ADATA [23:17] and BDATA[23:17] can also be used to interface with external character based OSD (On Screen Display) devices. See next section for details in OSD interface.

NOTE:

When the digital output port is set to output 10-bit per channel RGB or YCbCr 4:4:4 format, BDATA[23:18] will be used as the 2 LSB bits (bit 1 and bit 0) of 10-bit data, as follows:

Table 12. Input Port B bit[23..18] used as output pins

	30-bit RGB	30-bit 4:4:4 YCbCr
BDATA[23]	G[1]	Y[1]
BDATA[22]	G[0]	Y[0]
BDATA[21]	B[1]	Cb[1]
BDATA[20]	B[0]	Cb[0]
BDATA[19]	R[1]	Cr[1]
BDATA[18]	R[0]	Cr[0]

As a result, the input video format that can be applied to input port B is limited to a maximum of 16 bits wide data.

4.4.2.10 AOVACTIV, AOVCLK, AOVVS, AOVHS, AOVCOL [2:0]
BOVACTIV, BOVCLK, BOVVS, BOVHS, BOVCOL [2:0]

These are the pins used for interface to external character based OSD devices (such as Motorola MC141544, etc.). These pins are multiplexed with ADATA[23:17] / BDATA [23:17] and when they are used as OSD interface, the number of video format supported in the corresponding input port will be limited..

Table 13. Input Port pins for OSD interface

Input Port A	Input Port B	OSD in Port A	OSD in Port B	OSD Function
ADATA[17]	BDATA[17]	AOVACTIV	BOVACTIV	OSD active indicator
ADATA[18]	BDATA[18]	AOVCLK	BOVCLK	OSD pixel clock
ADATA[19]	BDATA[19]	AOVVS	BOVVS	OSD vsync
ADATA[20]	BDATA[20]	AOVHS	BOVHS	OSD hsync
ADATA[21]	BDATA[21]	AOVCOL[0]	BOVCOL[0]	OSD color data [0]
ADATA[22]	BDATA[22]	AOVCOL[1]	BOVCOL[1]	OSD color data [1]
ADATA[23]	BDATA[23]	AOVCOL[2]	BOVCOL[2]	OSD color data [2]

Note that although both Port A and Port B have overlay interface, only one can be used at a time.

4.4.3 Input Video Formats

The following video formats are supported by gm6015 input ports :

- ITU-BT-656
- 8-bit 4:2:2 YCbCr
- 16-bit 4:2:2 YCbCr
- 24-bit 4:4:4 YCbCr
- 24-bit RGB

The timing of these video formats are shown in the following figures :

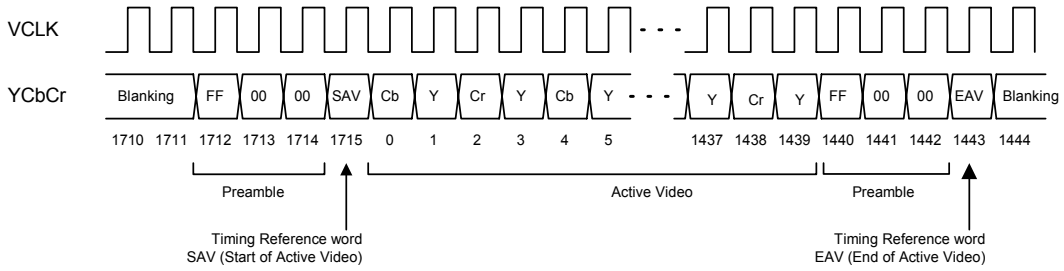


Figure 8. ITU-BT-656

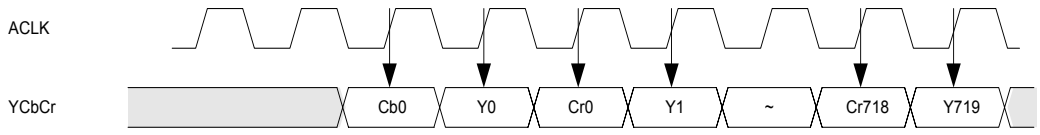


Figure 9. 8-bit 4:2:2 YCbCr

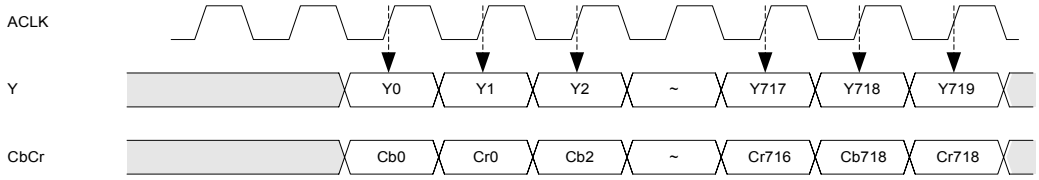


Figure 10. 16-bit 4:2:2 YCbCr

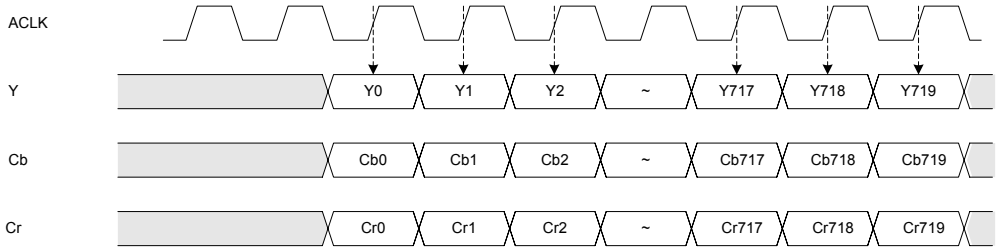


Figure 11. 24-bit 4:4:4 YCbCr data

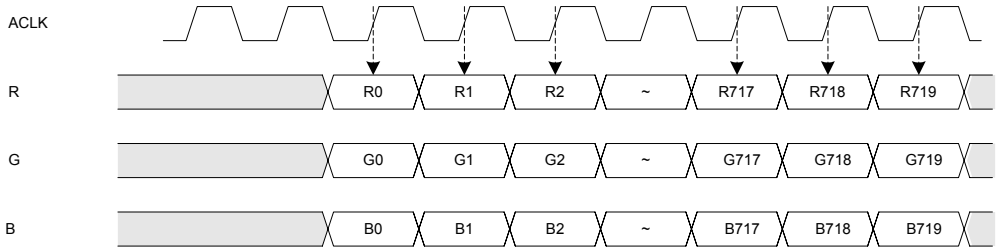


Figure 12. 24-bit RGB data

4.4.4 Input Sync Processing

For input video without separate sync signals, gm6015 has built-in 656 decoder and sync separator to extract embedded sync information. These extracted sync signals can be routed to external pins to be used by external logic for other timing purposes. The figure below illustrates how embedded syncs are extracted and routed to external pins.

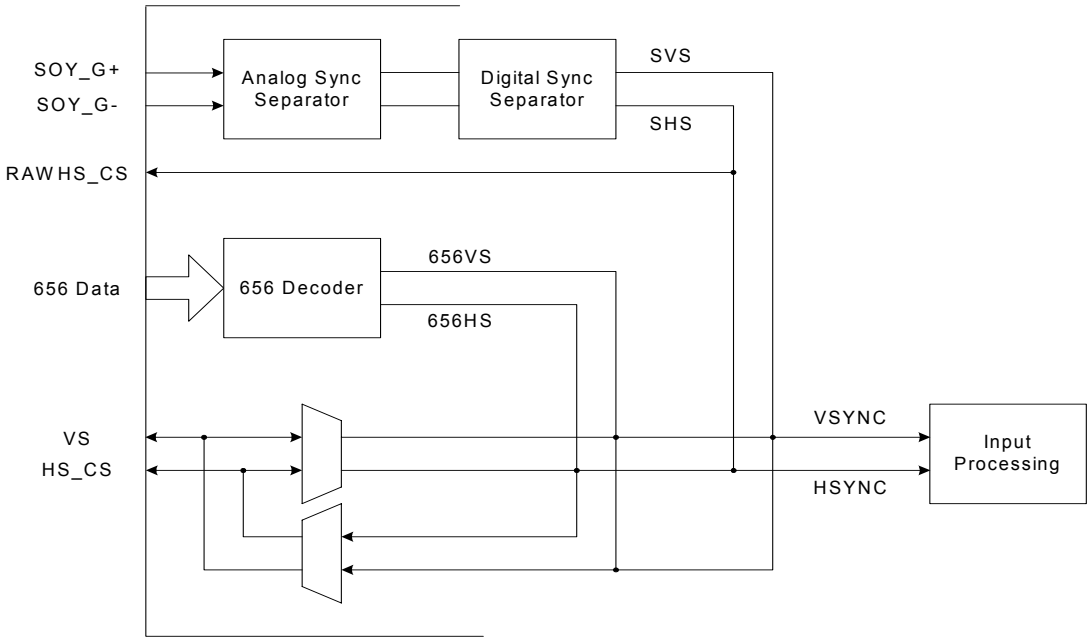


Figure 13. Embedded Sync Extraction

4.4.4.1 656 Decoder

ITU-BT-656 video format consists of pixel clock and 8 bits of data. No separate hsync, vsync and odd signals are present. Timing data is embedded in the data stream. The internal 656 decoder will extract the hsync, vsync and odd signals from the embedded timing data. The extracted hsync and vsync can be routed internally to A656HS / B656HS and A656VS / B656VS pins.

4.4.4.2 Analog Sync Separator

For video format with sync signals embedded on the analog video data, gm6015 built-in analog sync separator can extract the embedded sync signals. Bi-level and tri-level sync are supported. The analog sync separator acts as a "sync slicer" to the analog signal and generates digital composite sync signal to be processed by the digital sync separator.

For details in the operation of analog sync separator, please see "gm6010/6015 Hardware Theory of Operation"

4.4.4.3 Digital Sync Separator

The digital sync separator takes the digital composite sync signal generated from analog sync separator and output separate hsync and vsync signals. The generated hsync signal is of constant period which means all equalization pulses are eliminated.

In addition, the digital sync separator also provides measurement and status on sync signals to the host interface.

For details in the operation of digital sync separator, please see "gm6010/6015 Hardware Theory of Operation"

4.4.5 Input Capture Window

Figure 14 and Figure 15 illustrate the input capture window with active and cropped video. Note that the horizontal and vertical start location is controlled by how bit 2 of *IP_MISC_CTRL* register is set:

- *IP_MISC_CTRL* bit 2 = 0 (HREF_DE signal disabled)

  The horizontal start location is the number of clocks (qualified by CREF) from the leading edge of HSYNC to the 1st active pixel.

  The vertical start location is the number of lines from the leading edge of VSYNC to the 1st active line.

- *IP_MISC_CTRL* bit 2 = 1 (HREF_DE signal enabled)

  The horizontal start location is the number of clocks (qualified by CREF) from the leading edge of HREF to the 1st active pixel.

  The vertical start location is the number of lines from the leading edge of the 1st HREF after VSYNC to the 1st active line.

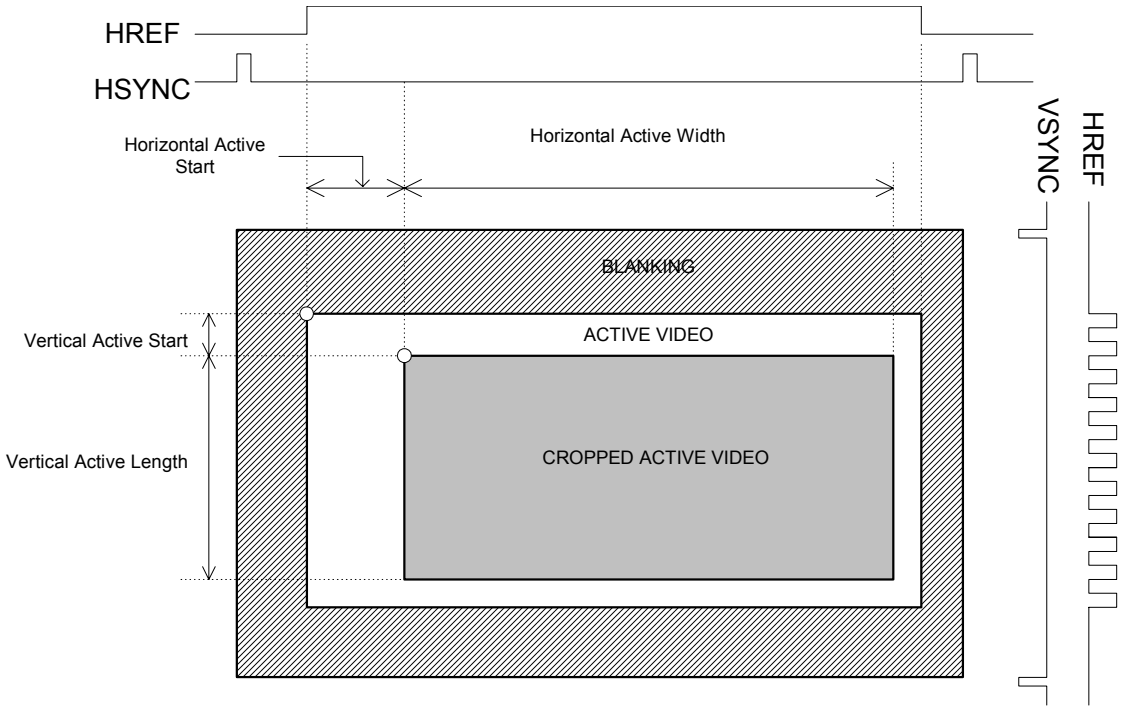


Figure 14. Input Capture Window (HREF/DE enabled)

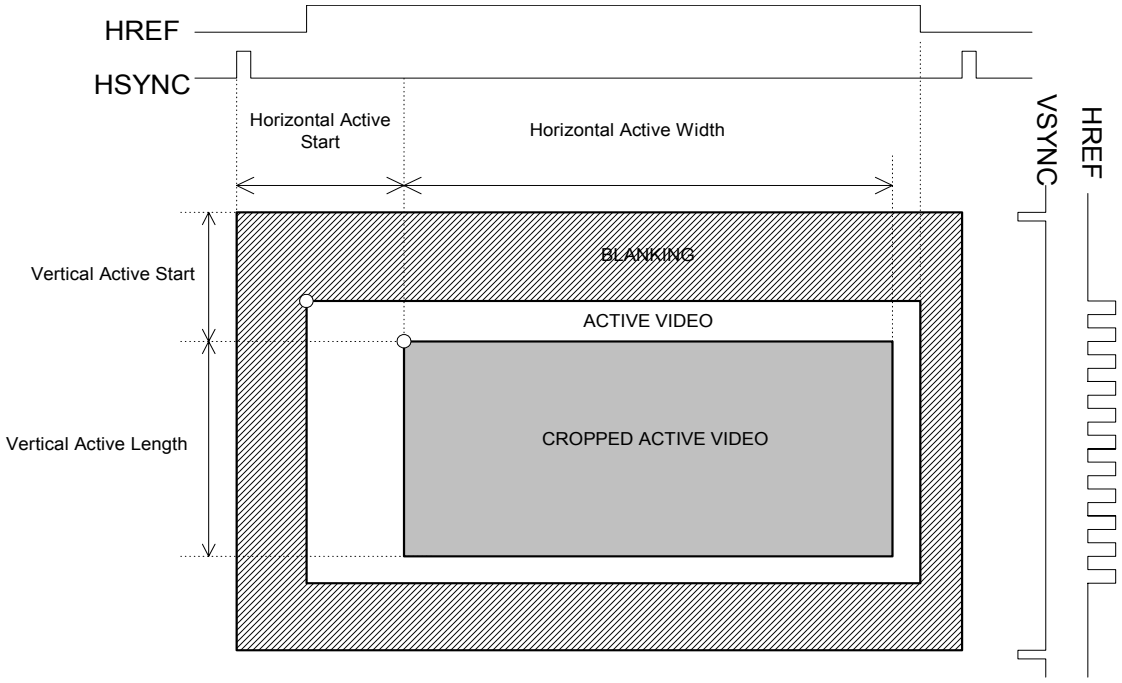


Figure 15. Input Capture Window (HREF/DE disabled)

Input cropping is supported by means of programming the start location and active width/length. The video data that gm6015 will process is the portion named "Cropped Active Video" in Figure 14 and Figure 15.

4.4.6 Input Format Measurement

The gm6015 has an Input Format Measurement block (IFM) providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input format.

Horizontal measurements are measured in terms of the selected IFM_CLK, while vertical measurements are measured in terms of HSYNC pulses.

4.4.6.1 Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock. Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC. When using composite sync input, these measurements use the internally synthesized HSYNC and VSYNC signals.

Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. The measurement will stop after it is completed unless enabled again.

4.4.6.2 Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert the system microcontroller. The microcontroller can set a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

4.4.6.3 Watchdog and Activity Monitoring

The watchdog monitors input VSYNC and HSYNC signals. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), a register bit is set. When any VSYNC period exceeds the programmed timing threshold (in terms HSYNC pulses), another register bit is set. An interrupt can also be programmed to occur.

In addition to the watchdog, there is an activity monitoring circuit that can detect presence of activity in MAIN input, PIP input, display, image processor and SDRAM.

4.4.7 Wide Screen Signal (WSS) decoding

gm6015 has built-in WSS decoder that can extract the data encoded in the vertical blanking intervals (VBI) and store it in host registers. The decoder is programmable so that various standards of VBI data can be decoded. The following are VBI data standards that gm6015 supports:

- EIAJ-CPR 1204-1
- IEC 61880
- EIA-805

4.5 Output Interface

gm6015 digital output port provides glueless interface to common DAC, video encoder and deflection processor. It can also interface directly to single width RGB LCD panels. gm6015 provides 24 bit output data bus for digital video output. It can also support a total of 30 bits data (such as 30-bit RGB and 30-bit YCbCr 4:4:4 formats) by using part of input port B (BDATA[23:18]) as output data bits.

4.5.1 Output Signals

The following are data and control signals associated with the digital output port.

4.5.1.1 DDATA[23:0]

These are the digital output data pins. Various output format uses different part of the data bus, as shown in the table below:

Table 14. Digital Output Port Pin Configuration

	8-bit 4:2:2 YCbCr / 656	16-bit 4:2:2 YCbCr	20-bit 4:2:2 YCbCr	18-bit 4:4:4 RGB	24-bit 4:4:4 YCbCr	24bit 4:4:4 RGB	30-bit 4:4:4 YCbCr	30-bit 4:4:4 RGB
DDATA[23]	X	X	X	R[5]	Cr[7]	R[7]	Cr[9]	R[9]
DDATA[22]	X	X	X	R[4]	Cr[6]	R[6]	Cr[8]	R[8]
DDATA[21]	X	X	X	R[3]	Cr[5]	R[5]	Cr[7]	R[7]
DDATA[20]	X	X	X	R[2]	Cr[4]	R[4]	Cr[6]	R[6]
DDATA[19]	X	X	CbCr[1]	R[1]	Cr[3]	R[3]	Cr[5]	R[5]
DDATA[18]	X	X	CbCr[0]	R[0]	Cr[2]	R[2]	Cr[4]	R[4]
DDATA[17]	X	X	Y[1]	X	Cr[1]	R[1]	Cr[3]	R[3]
DDATA[16]	X	X	Y[0]	X	Cr[0]	R[0]	Cr[2]	R[2]
DDATA[15]	X	CbCr[7]	CbCr[9]	B[5]	Cb[7]	B[7]	Cb[9]	B[9]
DDATA[14]	X	CbCr[6]	CbCr[8]	B[4]	Cb[6]	B[6]	Cb[8]	B[8]
DDATA[13]	X	CbCr[5]	CbCr[7]	B[3]	Cb[5]	B[5]	Cb[7]	B[7]
DDATA[12]	X	CbCr[4]	CbCr[6]	B[2]	Cb[4]	B[4]	Cb[6]	B[6]
DDATA[11]	X	CbCr[3]	CbCr[5]	B[1]	Cb[3]	B[3]	Cb[5]	B[5]
DDATA[10]	X	CbCr[2]	CbCr[4]	B[0]	Cb[2]	B[2]	Cb[4]	B[4]
DDATA[9]	X	CbCr[1]	CbCr[3]	X	Cb[1]	B[1]	Cb[3]	B[3]
DDATA[8]	X	CbCr[0]	CbCr[2]	X	Cb[0]	B[0]	Cb[2]	B[2]
DDATA[7]	YCbCr[7]	Y[7]	Y[9]	G[5]	Y[7]	G[7]	Y[9]	G[9]
DDATA[6]	YCbCr[6]	Y[6]	Y[8]	G[4]	Y[6]	G[6]	Y[8]	G[8]
DDATA[5]	YCbCr[5]	Y[5]	Y[7]	G[3]	Y[5]	G[5]	Y[7]	G[7]
DDATA[4]	YCbCr[4]	Y[4]	Y[6]	G[2]	Y[4]	G[4]	Y[6]	G[6]
DDATA[3]	YCbCr[3]	Y[3]	Y[5]	G[1]	Y[3]	G[3]	Y[5]	G[5]
DDATA[2]	YCbCr[2]	Y[2]	Y[4]	G[0]	Y[2]	G[2]	Y[4]	G[4]
DDATA[1]	YCbCr[1]	Y[1]	Y[3]	X	Y[1]	G[1]	Y[3]	G[3]
DDATA[0]	YCbCr[0]	Y[0]	Y[2]	X	Y[0]	G[0]	Y[2]	G[2]
BDATA[23]	X	X	X	X	X	X	Y[1]	G[1]
BDATA[22]	X	X	X	X	X	X	Y[0]	G[0]
BDATA[21]	X	X	X	X	X	X	Cb[1]	B[1]
BDATA[20]	X	X	X	X	X	X	Cb[0]	B[0]
BDATA[19]	X	X	X	X	X	X	Cr[1]	R[1]
BDATA[18]	X	X	X	X	X	X	Cr[0]	R[0]

Note: The pin locations of 2 LSB bits for formats with 10 bits per channel. For 30-bit 4:4:4 YCbCr and RGB, the 2 LSB bits are located on the Input Port B BDATA[23:18].

4.5.1.2 DCLK

This is the display pixel clock. The internal DDS can be programmed to generate a wide range of frequency for various output video format and resolution.

A secondary display clock (DCLK2) can be programmed to output at GPIO pins.

Both DCLK and DCLK2 can be programmed to be equal to or half of DDS output frequency. The polarity and delay of DCLK and DCLK2 are programmable.

4.5.1.3 DVS (DSYNCT)

- DVS

  This is the display vsync. It can be selected from the internal reference vsync or as a fully programmable vsync. Programmable vsync is recommended.

- DSYNCT

  This is the tri-level sync control signal. It can be applied to external DACs which are able to generate tri-level sync.

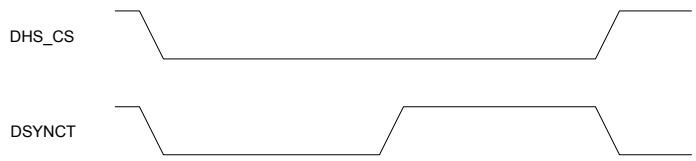


Figure 16. Relationship between DHS_CS and DSYNCT

4.5.1.4 DHS_CS

This is the display hsync or composite sync pin. It can be selected from the internal reference hsync or a fully programmable hsync / composite sync.

4.5.1.5 DODD (GPIO0)

- DODD (Default)

  The is the output odd / even field indicator.

- GPIO0

  For progressive output, this pin can be configured to a general purpose I / O pin.

NOTE that this pin is a GPIO pin with default to the function of output field indicator.

4.5.1.6 DDE_BLANK

This is the display data enable / blanking and it marks the active data in a line.

4.5.2 656 Encoder

gm6015 has built-in 656 encoder which encode the display video data into format as described in ITU-R BT.656 specification. The timing signals are embedded into the data stream and are also available on the corresponding pins at the same time.

4.5.3 VBI Data Insertion

Digital Data can be inserted into the VBI area at the output. Information of the data, such as line number, field (odd / even), start pixel number, data width (upto 24 bits)…etc, are programmable with host registers.

4.5.4 Output Video Formats

gm6015 can output digital video data in the following formats :

- ITU-BT-656
- 8-bit 4:2:2 YCbCr (8-bit bus with Y, Cb and Cr)
- 12-bit 4:2:2 YCbCr (6-bit bus with Y, 6-bit bus with CbCr)
- 16-bit 4:2:2 YCbCr (8-bit bus with Y, 8-bit bus with CbCr)
- 20-bit 4:2:2 YCbCr (10-bit bus with Y, 10-bit bus with CbCr)
- 18-bit 4:4:4 YCbCr (6-bit bus with Y, 6-bit bus with Cb, 6-bit bus with Cr)
- 24-bit 4:4:4 YCbCr (8-bit bus with Y, 8-bit bus with Cb, 8-bit bus with Cr)
- 30-bit 4:4:4 YCbCr (10-bit bus with Y, 10-bit bus with Cb, 10-bit bus with Cr)
- 18-bit RGB (6-bit bus with R, 6-bit bus with G, 6-bit bus with B)
- 24-bit RGB (8-bit bus with R, 8-bit bus with G, 8-bit bus with B)
- 30-bit RGB (10-bit bus with R, 10-bit bus with G, 10-bit bus with B)

For output timing, the gm6015 display timing generator is fully programmable to generate arbitrary timing including (but not limit to) the following:

- All VESA VGA modes
- All VESA SVGA modes
- VESA XGA modes except XGA @ 85Hz
- All SDTV video modes (e.g. NTSC, PAL)
- All EDTV video modes (e.g. 720x480p, 720x576p)
- HDTV video modes except 1920x1080 progressive modes
- PDP modes (852x480p and 1366x768p)
- Others (e.g. 100Hz - PAL, …)

4.5.5 Video Look Up Table

A video look up table (VLUT) is implemented as three 256 x 10-bit RAM tables, one for each color channel. The output of VLUT can be programmed to be 8-bit or 10-bit per color and loading of data into VLUT can be programmed to happen during blanking interval.

The look up table serves the purposes of :

- Gamma correction

3 tables of non-linear (gamma corrected) values are loaded into the VLUT, one for each color. Pixel values from the mixer output is mapped to the corresponding tables and a gamma corrected value is output from the table. Figure 17 below is a simplified illustration of gamma correction of 8-bit input/output VLUT.

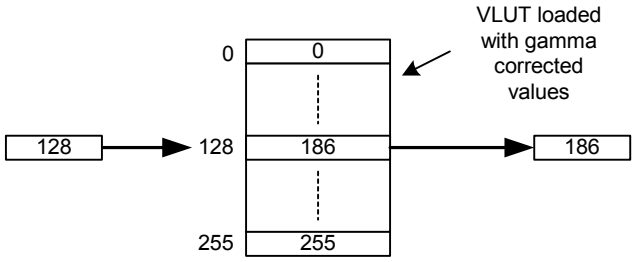


Figure 17. Gamma correction

- Mapping of 8-bit data to 10-bit data

  gm6015 processes data in 8 bits. VLUT can be used to map the 8-bit processed data to 10-bit output by loading the VLUT with values from 0x000 to 0x3FF.

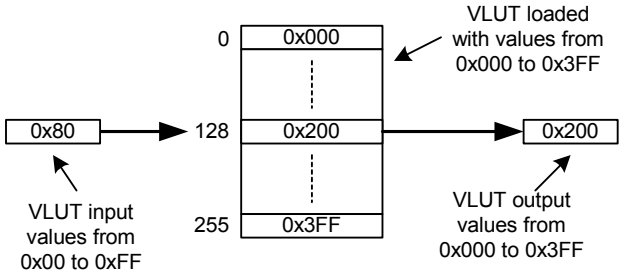


Figure 18. 8-bit to 10-bit mapping

- Pre-scale of digital video data

  If gm6015 output is connected to external device with sync insertion, the output data can be pre-scaled so as to ensure a correct output range after sync insertion.

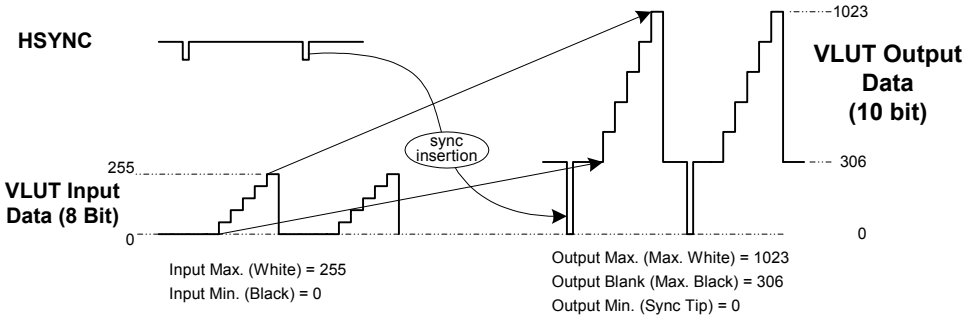


Figure 19. Pre-scale of data for sync insertion (with 8-bit to 10-bit mapping)

The 3 VLUT functions mentioned above can be achieved by a single set of VLUT values. Genesis provides a Window application program to help calculating the correct values needed.

For details of VLUT loading, please refer to "gm6010/6015 register programming guide".

4.5.6 Dithering

The output data from the VLUT can be dithered down to 8-bit / 6-bit per color. Dithering is done by processing the LSBs of data through a dithering algorithm and generates the LSB of the output (Figure 20). Both random dithering and programmable ordered dithering are supported.

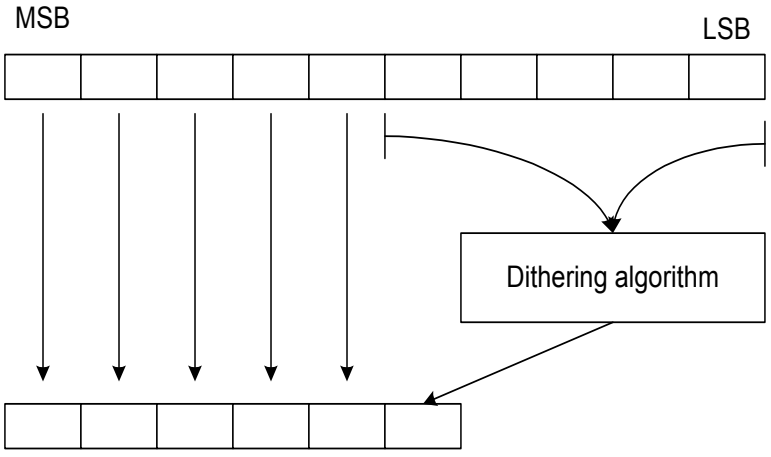


Figure 20. 10-bit to 6-bit dithering

4.5.7 Output Configuration

The MAIN and PIP channel (and OSD, if present) are mixed together at the output. Moreover, multiple PIP channels can be configured at the output. 16 levels of alpha blending is available for mixing of

MAIN and PIP display. gm6015 allows a very flexible multiple PIP display configuration as described below.

4.5.7.1 Output Timing

The output timing can be configured by programming the following parameters:

1. Total output resolution. This is the number of total horizontal pixel per line and the number of total vertical lines per field / frame. Blanking regions are included.
2. Background resolution. This is the area where programmable background color will be displayed to fill the gap between active display window and blanking region.
3. MAIN channel resolution. This is the number of horizontal active pixels per line and number of vertical active lines per field / frame of the MAIN channel.
4. PIP channel resolution. This is the number of horizontal active pixels per line and number of vertical active lines per field / frame of the PIP channel. For single PIP display, the size of PIP display can be configured to be any size up to a maximum of ⅓ of MAIN display size. For multiple PIP display, each PIP display window will have the same size.

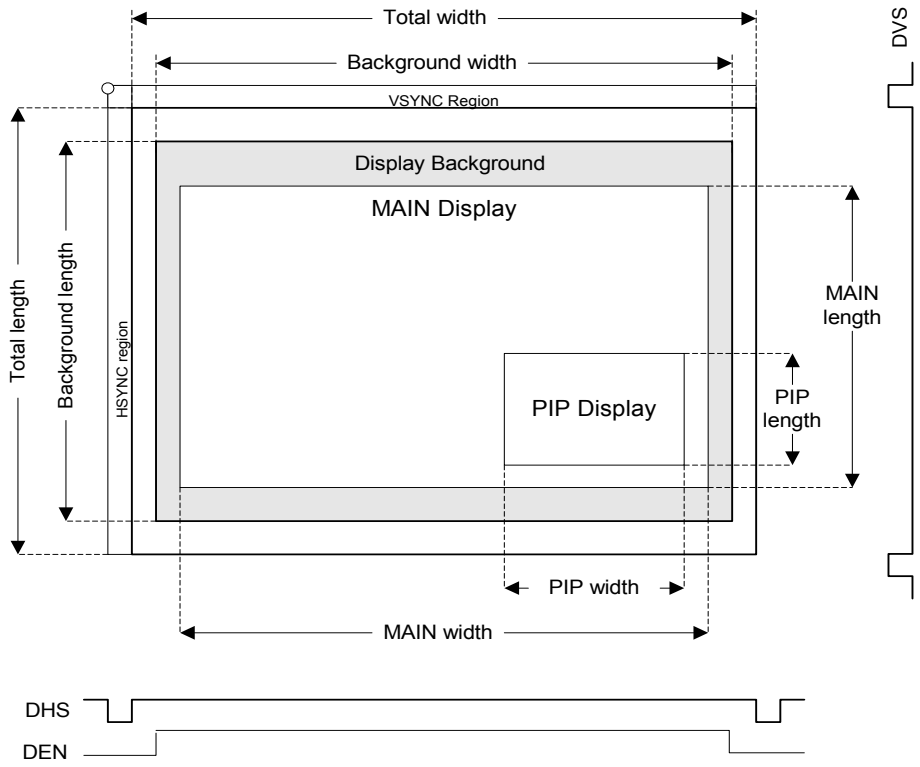


Figure 21. Output Display Windows

4.5.7.2 PIP Display

gm6015 allows a very flexible PIP display configuration. PIP display can be configured as single PIP or multiple PIPs. A PIP border with programmable color and size is available. Moreover, in the case of multiple PIPs, a hi-light border can be created so as to show the active PIP window. Figure 22 shows examples of various PIP configurations

Single PIP allows the PIP display to be placed arbitrarily in the display window. It can be placed within the MAIN display (Figure 22a), partially overlapped with MAIN display (Figure 22c) or fully detached from MAIN display (Figure 22d). The size of the PIP display is fully programmable. Also, single PIP display allows 16 levels of alpha blending within the PIP window.

A special case of single PIP display is side-by-side configuration (Figure 22b). In this case the MAIN and PIP are put side by side in the display

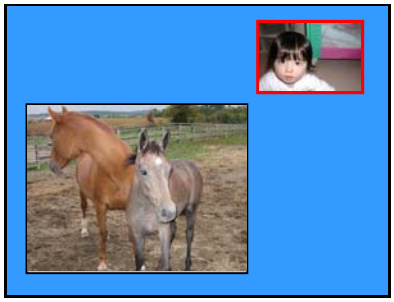
Multiple PIPs display allows a maximum of 16 PIP windows to be displayed at the same time. MAIN and one PIP window will be running at real time. In multiple PIP display each PIP window will be of the same size and is fully opaque. Figure 22(e) to (h) illustrate some examples of multiple PIP configurations.

If OSD interface is used, the OSD can be overlayed on top of the MAIN and PIP display windows.

(a) Fully overlapped

(b) Side-by-side

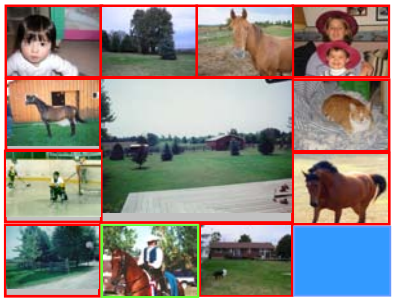
(c) Partially overlapped



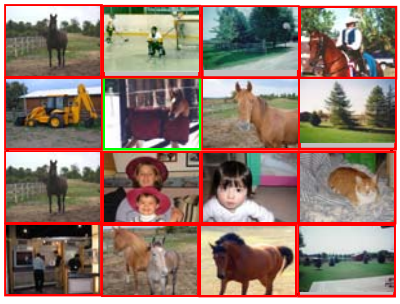
(d) Detached

(e) 2 x 2 multi PIPs

(f) Ring-shaped multi PIPs



(g) Irregular multi PIPs



(h) Tiled multi PIPs

Figure 22. Examples of Different PIP Configurations

4.6 Color Space Conversion (CSC)

All video data is processed internally in YCbCr 4:2:2 format. Input video data is converted to YCbCr 4:2:2 format, if necessary, for processing and then converted to the desired output video format.

4.6.1 Input CSC

Input color space conversion is provided in each input data path to convert input video data to YCbCr 4:2:2.

For input in RGB format, it is first converted to YCbCr 4:4:4 format using a transformation matrix and then downsampled to 4:2:2 by decimation filter.

For input in YCbCr 4:4:4 format, the transformation matrix is bypassed and the data is downsampled to 4:2:2 by decimation filter.

The equation used in the RGB to YCbCr transformation matrix is :

$$YCbCr = (R\_COEFF * R + G\_COEFF * G + B\_COEFF * B + OFFSET) / 256$$

All coefficient and offset value are programmable through host registers. It provides the flexibility to deal with all color space conversion.

For details in calculating CSC coefficients, please refer to “gm6010/6015 register programming guide”.

4.6.2 Output CSC

Output color space conversion is provided to convert the processed video data in YCbCr 4:2:2 format to the desired output format.

For output in YCbCr 4:4:4 format, the processed YCbCr 4:2:2 data is upsampled by linear interpolation or pixel replication.

When the output format is RGB, the CSC output can be programmed to clamp to RGB (16 – 240) or full range (0 – 255).

4.6.3 Color Control

All color controls (brightness, contrast, saturation and hue) can be implemented by manipulating the input color space conversion coefficients. The YCbCr data after color control will be

$$Yout = Yin * contrast + brightness$$

$$Cbout = Cbin * saturation * cos(hue) + Crin * saturation * sin(hue)$$

*Crout = Crin * saturation * cos(hue) + Cbin * saturation * sin(hue)*

Since both MAIN and PIP channels has its own CSC block, it is possible to have color control on one channel while not affecting the other channel.

For details on color controls, please refer to "gm6010/6015 register programming guide".

4.7 Video Processing

gm6015 provides advanced video processing capability. Arbitrary zoom (scale up) and shrink (scale down) are supported in both MAIN and PIP channels. Moreover, advanced de-interlacing (inverse 3:2/2:2 pulldown and motion adaptive process), diagonal interpolation, "3D" noise reduction and image sharpening filter are available in the MAIN channel.

4.7.1 MAIN Channel

MAIN channel provides all the video processing capabilities including:-

- Arbitrary zoom / shrink scaling
- Inverse 3:2 / 2:2 pulldown de-interlacing
- Pixel based motion adaptive de-interlacing
- Diagonal interpolation processing
- "3D' noise reduction filter
- Programmable image sharpening filter

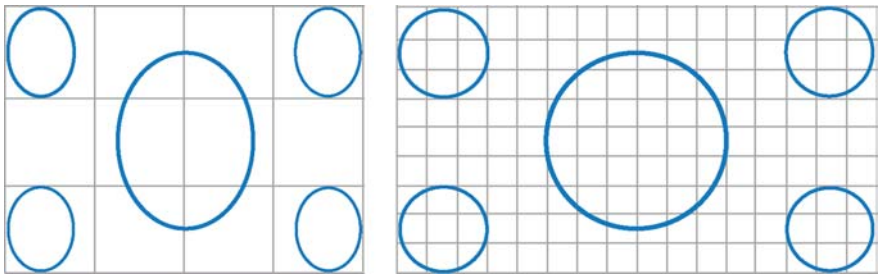
These features will be explained in the following sections.

4.7.1.1 Arbitrary Zoom / Shrink

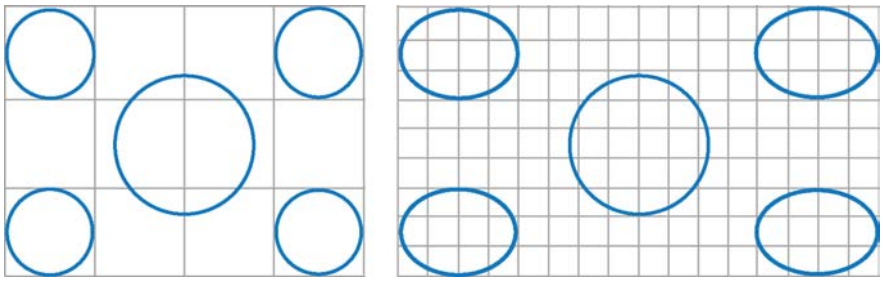
The MAIN channel video can be zoomed or shrunk arbitrarily. The fully programmable input and output active area and the horizontal and vertical scale factors allow a very flexible design for various input / output resolutions.

Panoramic zoom and shrink are also supported by defining 2 zoom areas horizontally – normally the center and the sides. A different scale value can be programmed to each zoom area to achieve a panoramic zoom effect. Panoramic shrink is implemented in a similar manner so that a 16:9 panoramic source can be shrunk to a normal 4:3 display with correct aspect ratio.

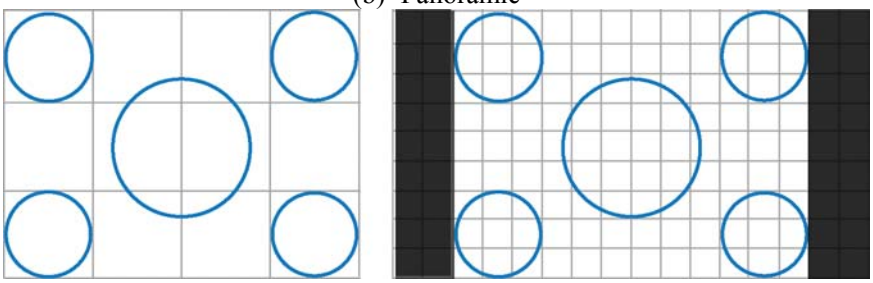
With the fully programmable zoom / shrink capability, a very flexible aspect ratio conversion can be implemented. The following figures show various aspect ratio conversion examples.



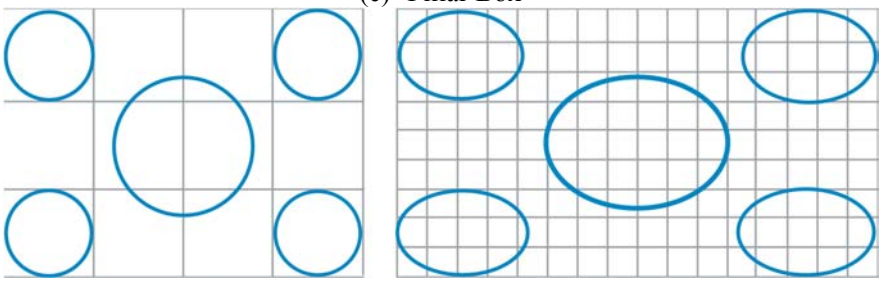
(a) Anamorphic



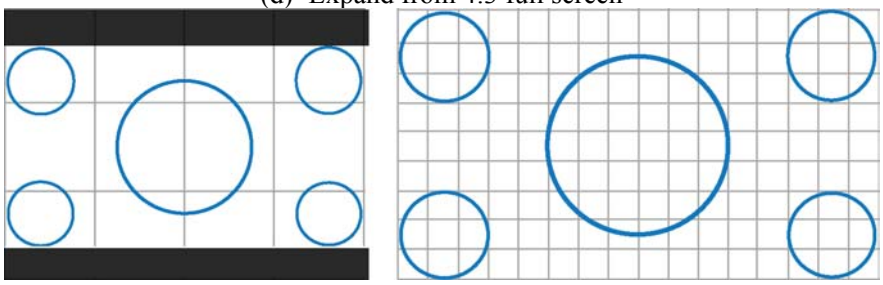
(b) Panoramic



(c) Pillar Box

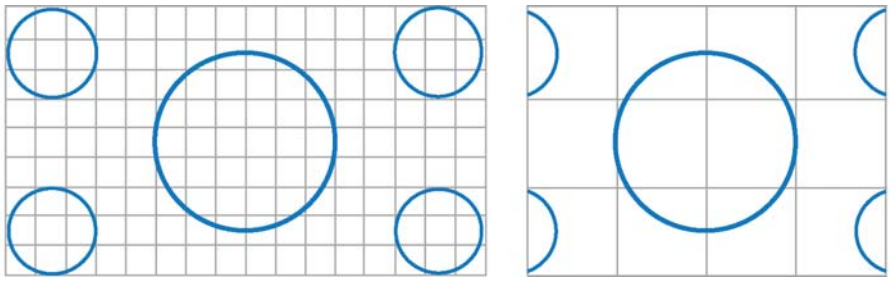


(d) Expand from 4:3 full screen

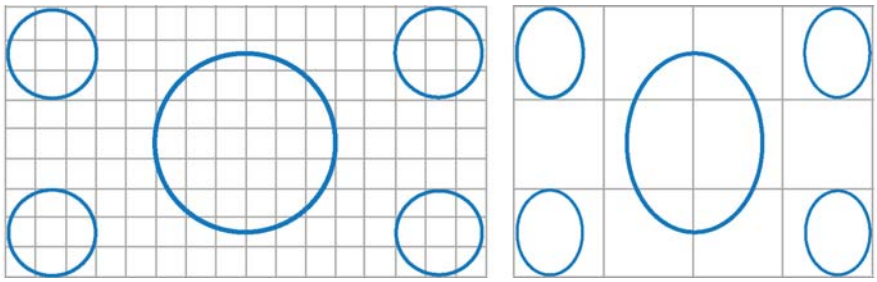


(e) Expand from 4:3 letter box

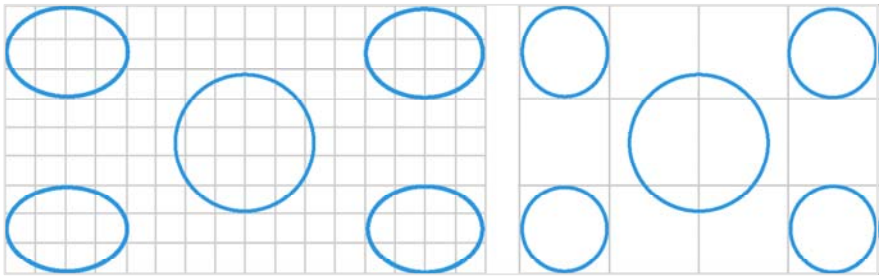
Figure 23. 4:3 to 16:9 aspect ratio conversion



(a) Pan and Crop



(b) Shrink



(c) Panoramic Shrink

Figure 24. 16:9 to 4:3 aspect ratio conversion

4.7.1.2 Inverse 3:2 / 2:2 pulldown de-interlacing

Video with 3:2 / 2:2 field sequence are processed with the built-in Adaptive Film Mode controller. The field sequence is first detected by examining the field motion values and once a field sequence is identified, the corresponding film mode processing is applied. The following figure illustrates the inverse 3:2 pulldown processing.

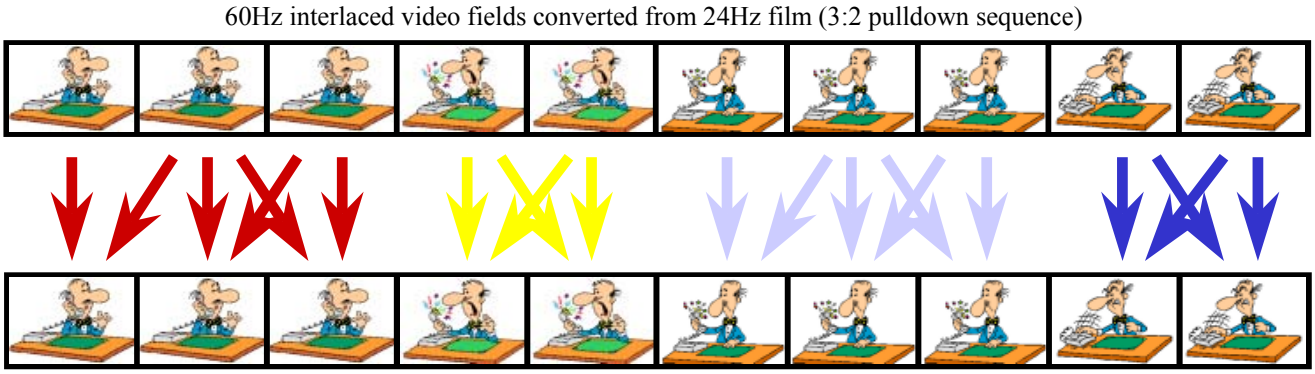


Figure 25. Inverse 3:2 pulldown processing

4.7.1.3 Motion Adaptive De-Interlacing (MADI)

Motion adaptive de-interlacing in gm6015 is a pixel based 2-phase process. Phase 1 is the detection of motion and a motion value is generated for each pixel. These pixel motion values are used as a measure of the "degree of motion". In phase 2, the pixel motion values are used as a reference for different sets of coefficients for de-interlacing.

As a result, the areas that are not moving in an image will be fully static (flicker free) and the objects that are moving will have a smooth edge.

4.7.1.4 Diagonal Interpolation

In addition to the advanced de-interlacing capabilities mentioned in the previous sections, further image enhancement is achieved by applying special processing to moving diagonal pattern in an image.

The diagonal interpolation process involves the detection of diagonal pattern in an image and special interpolation process to the local area with diagonal pattern. The result is a smooth edge on moving objects with diagonal pattern.

4.7.1.5 "3D" Noise Reduction

"3D" noise reduction is implemented by applying temporal (inter-field) and spatial (intra-field) noise reduction filter to the video data.

Temporal noise reduction filter is applied first and it takes pixel values of the same pixel from different fields for noise filtering. It also interacts with MADI process such that the "degree" of noise filtering is derived from the pixel motion value.

Spatial noise reduction is implemented by taking the neighborhood pixels of a target pixel in the same field for noise filtering.

Notice that spatial and "3D" noise reduction filter is only available for interlaced standard definition video.

4.7.1.6 Sharpening Filters

gm6015 provides sharpening filters to enhance high frequency components in an image. Different levels of sharpening can be implemented by selecting different coefficients for the horizontal and vertical sharpening filters.

4.7.2 PIP Channel

Video processing features available in the PIP channel includes:-

- Arbitrary zoom / shrink (programmable PIP size)
- Vertical interpolation or static mesh de-interlacing

Moreover, other settings can be applied to the PIP channel such as:

- Programmable PIP border height and width
- Programmable PIP border color
- Programmable PIP transparency (16 levels of alpha blending)
- Programmable PIP location

4.7.2.1 Arbitrary Zoom / Shrink

PIP channel allows arbitrary zoom and shrink operation. However, panoramic zoom is not available. With arbitrary vertical and horizontal zoom / shrink, it is possible to implement aspect ratio conversion in the PIP channel.

4.7.2.2 Vertical Interpolation / Static Mesh De-interlacing

De-interlacing on PIP channel can be implemented in either vertical interpolation or static mesh. In vertical interpolation the output frame is generated by pixel interpolation in the vertical dimension within the same field. Static mesh involves the meshing of odd and even fields (without considering temporal effect) to form the output frame.

It is recommended that for moving images, vertical interpolation should be used and for static images, static mesh should be used.

For details in how to configure using vertical interpolation and static mesh, please refer to “gm6010/6015 Programming Guide”.

4.7.3 Video Processing Bypass

For input and output having the same resolution and format (RGB or YCbCr), it is possible to select a route from the input CSC to the output CSC, bypassing all video processing functions and color space conversion in the MAIN channel.

This bypass path is most desirable when the input and output are both RGB format and having the same resolution. In this case the RGB input will not go through color space conversion and video processing, which maintain the highest fidelity of the RGB data.

4.8 Synchronization Modes

The gm6015 supports the following synchronization modes :

1. Frame Sync mode 1

   In this mode the display is re-synchronized to the input in every display vsync. This mode is best suited for CRT displays. The display clock can be programmed to lock to the input clock from either MAIN or PIP channel

2. Frame Sync mode 2

   In this mode the display is re-synchronized to the input in every display hsync and every display vsync. This mode is best suited for LCD, PDP or other pixelated displays. The display clock can be programmed to lock to the input clock from either MAIN or PIP channel

3. Free Run mode

   In this mode the display is running at a free running frequency and is not locked to the input. With proper frame buffer setting the internal field controller can assure that no frame tear will happen in free run mode.

4. Frame Rate Conversion

   Frame rate conversion can be implemented with all 3 synchronization modes. Display frame rate can either convert up or convert down from the input frame rate. For standard definition interlaced video, the display frame rate can be set to run at double of the input frame rate, e.g. PAL @ 50Hz can be converted to PAL @ 100Hz.

   Note that frame rate conversion can be implemented in both MAIN and PIP channel

4.9 Frame Store Interface

gm6015 has built in SDRAM controller which can interface to 32-bit wide SDRAM from 64Mbit to 256Mbit. In most applications a single 100 MHz 64Mbit SDRAM with a 32 bit data bus (4 banks x 512K words x 32 bits) is needed. The SDRAM controller is also designed to be compatible with higher speed SDRAM (143 / 166 MHz).

Commonly available 64Mbit SDRAMs are shown below:

- Etron EM638325TS-10
- Hyundai HY57V653220BTC-10
- Micron MT48LC2M32B2-8
- Samsung KM432S2030CT-G/F10
- Toshiba TC59S6432CFT/CFTL-10

The single external SDRAM acts as frame storage for resynchronization and storage for MAIN and PIP input fields/frames, intermediate storage for Image Processor and Adaptive Film Mode Controller and display output fields/frames.

The integrated SDRAM controller arbitrate/control the writing/reading of video data to/from the SDRAM. Input video data is written into the frame buffer for processing and display data are read back from the frame buffer. Frame buffer addresses are fully programmable so as to provide flexibility for memory allocation of MAIN and PIP display. This flexibility also allows the implementation of various multiple PIP display configurations.

For details in programming frame store addresses in multiple PIP display, please refer to "gm6010/gm6015 Programming Guide".

4.10 Interrupt

gm6015 has an interrupt pin which can generate interrupt based on a variety of conditions. The pin can be set to be latched (with programmable polarity) and can be cleared by writing to host register.

Multiple interrupt sources can be enabled and status registers are available for identifying interrupt source. Interrupt sources include:

- Periodic events in input and output

Error conditions of input timing signals – dropout / pulse width error / period error of timing signals in GPIOM both MAIN and PIP inputs.

4.11 GPIO Pins

gm6015 has three GPIO pins -- GPIO0, GPIO1, and GPIO2. These pins can be programmed for the various input / output functions listed below:

- AFM indicator output
- Pulse width modulator output
- Second display clock (DCLK2) output
- General purpose input
- General purpose output
- OSD active indicator output
- Programmable output pulse per line
- Programmable output pulse per line
- Programmable output pulse per field/frame
- Watchdog error indicator output
- Programmable display ODD indicator output
- Display ODD indicator output.

For register setting of input/output functions, refer to the description of registers 0x12 and 0x13 in "gm6010/gm6015 Register Listing".

4.12 Host Interface

The host interface of the gm6015 has two modes of operation: 2-wire mode, and 3-wire mode :

- The 2-wire connection consists of a serial clock (SCLK) and bi-directional serial data line (SDATA).
- The 3-wire connection consists of a serial clock (SCLK), a bi-directional serial data line (SDATA) and a chip select line (/SCS)

The selection of operation mode and other setting is done by placing pull-up / pull-down bootstrap resistors on RAMADDR[7..0], as shown below :

Table 15. Host Protocol Configuration

Pin Name	Description
RAMADDR[4:0]	3. If 2-wire protocol is selected, this sets device address bit [5..1]. 4. If 3-wire protocol is selected, this pins are ignored.
RAMADDR[5]	3. If 2-wire protocol is selected, this sets device address bit [6]. 4. If 3-wire protocol is selected : - pull high to select active drive on SDATA pin - pull low to select open drain on SDATA pin
RAMADDR[6]	3. If 2-wire protocol is selected, this sets device address bit [7]. 4. If 3-wire protocol is selected : - pull high to select transmit on SCLK falling edge and receive on SCLK rising edge - pull low to select transmit on SCLK rising edge and receive on SCLK falling edge
RAMADDR[7]	3. Pull high to select 3-wire protocol 4. Pull low to select 2-wire protocol

These bootstrap resistors are sampled on the rising edge of /RESET signal and allows a flexible configuration in a system with other devices.

4.12.1 2-wire mode

The 2-wire protocol features a serial clock (SCLK) and a bi-directional serial data line (SDATA). The bus master, typically a controller, drives the SCLK clock and either the master or slave may drive the SDATA line. The gm6015 operates as a slave on the interface.

4.12.1.1 Configuration

To select 2-wire mode as host interface, the bootstrap resistor on RAMADDR[7] pin (pin 111) is placed with a pull-down resistor. The device address is set by placing pull-up / pull-down bootstrap resistors on RAMADDR[6..0]. The device address to be used by the serial protocol will be as follows :

RAMADDR[6]	RAMADDR[5]	RAMADDR[4]	RAMADDR[3]	RAMADDR[2]	RAMADDR[1]	RAMADDR[0]	R / W

4.12.1.2 Serial Protocol

A data transfer consists of a stream of serially transmitted bytes formatted as shown in the figure below. A transfer is initiated by a START condition (a high-to-low transition on SDATA while SCLK is held high). A transfer is terminated by a STOP condition (a low-to-high transition on SDATA while SCLK is held high) or by another START condition (to begin another transfer). The SDATA signal must be stable when SCLK is high, it may only change when SCLK is low (to avoid being misinterpreted as START or STOP).

The highlighted sections of the waveform represent moments when the transmitting device (master) must release the SDATA line and wait for an acknowledgement from the gm6015 (slave).

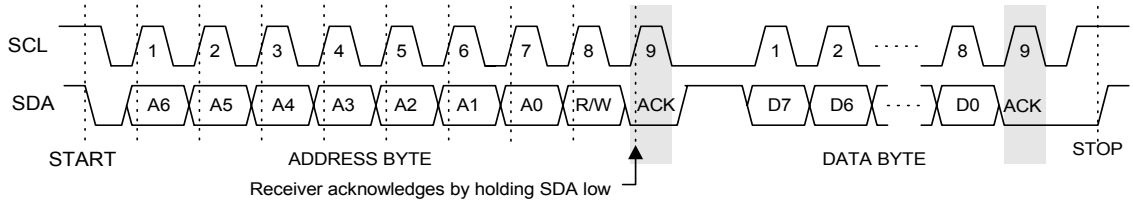


Figure 26. 2-wire protocol

Each transaction on the SDATA is an integer multiples of bytes (8 bits). The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transmitted with the most significant bit (MSB) first. After the 8th data bits, the master releases the SDATA line and the receiver asserts the SDATA line low to acknowledge receipt of the data. The master device generates the SCLK pulse during the acknowledge cycle. The addressed receiver is obliged to acknowledge each byte that has been received.

4.12.1.3 Protocol Format

The serial data format to be transmitted consists of a device address byte, an instruction byte, a register address byte and one or more data byte(s). The following sections describe the format of each byte in more details.

Device Address Byte

The Device Address consists of a 7-bit device address that identifies the slave device for the transfer. This 7-bit device address should match the device address set by the bootstrap resisters in RAMADDR[6..0] pins. The 8th bit (LSB) of the device address byte indicates a read or write operation and also determines the direction for successive data byte transfer. This bit is set low to indicate a write and set high to indicate a read transfer.

Instruction Byte

The Instruction byte indicates the type of operation to be performed to the gm6015. The content of bytes that follow the instruction byte will vary depending on the instruction byte chosen. By utilizing these modes effectively, registers can be quickly configured.

Table 16 below lists the detail bit format of instruction bytes. Bits 'A8' and 'A9' are the least significant 2 bits in the instruction byte, and they represent the 8th and 9th bits of the internal register address respectively.

The unused bits in the instruction byte should be set to '1'. All other bit patterns not shown in the table are reserved.

Table 16. Instruction byte format

Value								Operation	Description
7	6	5	4	3	2	1	0		
0	0	0	1	x	x	A9	A8	Write with Auto-increment	Allows user to write a single byte or multiple bytes to a specified starting address location. The internal register address pointer will increment after each data byte transmission. Termination of the transfer is done by a STOP condition and will cause the register address pointer to increment to the next address location.
0	0	1	0	x	x	A9	A8	Write without Auto-increment (for VLUT loading)	1. Allows user to write a single byte to a specified register address. The internal register address pointer will not increment after data byte transmission. 2. For VLUT loading, multiple bytes can be transmitted to the VLUT location by sending the data bytes sequentially after the register address byte. The internal register address pointer will not increment after each data byte transmission but the VLUT entry pointer will increment and point to the next table entry.
1	0	0	1	x	x	A9	A8	Read with Auto-increment	Allows user to read a single byte or multiple bytes from a specified starting address location. The internal register address pointer will increment after each data byte transmission. Termination of the transfer is done by a STOP condition and will cause the register address pointer to increment to the next address location.
1	0	1	0	x	x	A9	A8	Read without Auto-increment	Allows user to read a single byte from a specified register address. The internal register address pointer will not increment after data byte transmission.

Register Address Byte

The Register Address byte consists of the 8 least significant bits of the 10-bit register address. The most significant 2 bits of the register address are placed in the lease significant 2 bits of the Instruction Byte. Figure 27 below shows the 10-bit register address bit location.

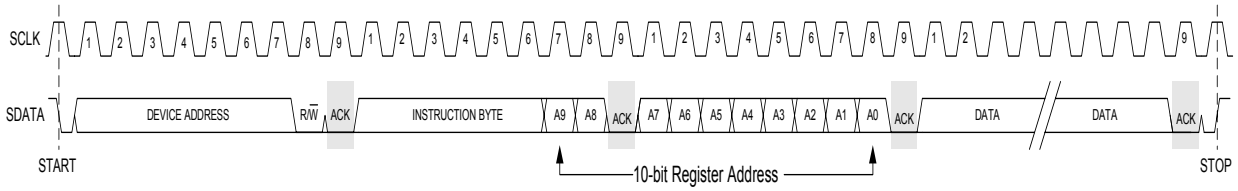


Figure 27. 10-bit Register Address

4.12.1.4 Command Format

The four commands that gm6015 2-wire protocol supports allow single or multiple consecutive registers to be accessed. For loading tables, care must be taken to use the appropriate write command.

Write with Auto-increment

In Write with Auto-increment, the register address pointer is automatically incremented after each byte has been sent and written. This command is best for loading a table of register values.

Write without Auto-increment

In Write without Auto-increment, the register address pointer is not incremented after each byte has been sent and written. This command is mainly for writing one register value. However, it can also be used for loading video look-up table (VLUT) by sending look-up table values continuously to a single register address. See "VLUT Loading" section for more detail.

Read with Auto-increment

In Read with Auto-increment, the address pointer is automatically incremented after each byte has been sent from gm6015. The transmission protocol for this mode is illustrated below.

Note :

1. There is a 2nd START condition after the register address byte is sent.
2. The 1st device address byte being sent consists of a bit '0' in the read/write bit (indicate a 'write') while the 2nd device address byte consists of a bit '1' in the read/write bit (indicate a 'read')
3. After the last byte is read, no acknowledgement is issued to terminate the transfer.

Read without Auto-increment

In Read without Auto-increment, the register address pointer will not be incremented. This command is mainly for reading from a single register.

4.12.2 3-wire mode

The 3-wire SPI protocol features a serial clock (SCLK), a bi-directional serial data (SDATA) and a chip select (/SCS) line. The bus master, typically a microcontroller, drives the SCLK and /SCS lines and either the master or slave may drive the SDATA line.

4.12.2.1 Configuration

To select 3-wire mode as host interface, the bootstrap resistor on RAMADDR[7] pin (pin 111) is placed with a pull-up resistor. Bootstrap resistors on RAMADDR[4..0] are ignored in this mode. The driving capability on the SDATA pin and the clock edge can be configured as below :

SDATA drive

RAMADDR[5] = 1, SDATA pin is an active output

RAMADDR[5] = 0, SDATA pin is an open drain output

SCLK edge

RAMADDR[6] = 1, gm6015 transmit on SCLK falling edge and receive on SCLK rising edge.

RAMADDR[6] = 0, gm6015 transmit on SCLK rising edge and receive on SCLK falling edge.

4.12.2.2 Serial Protocol

A data transfer consists of a stream of serially transmitted bytes formatted as shown in

below. All bytes are transmitted in MSB first. Data must be stable before the sampling edge of SCLK. The sampling clock edge of data bit on SDATA line depends on the setting of bootstrap resistor on RAMADDR[6] (See section 4.12.2.1).

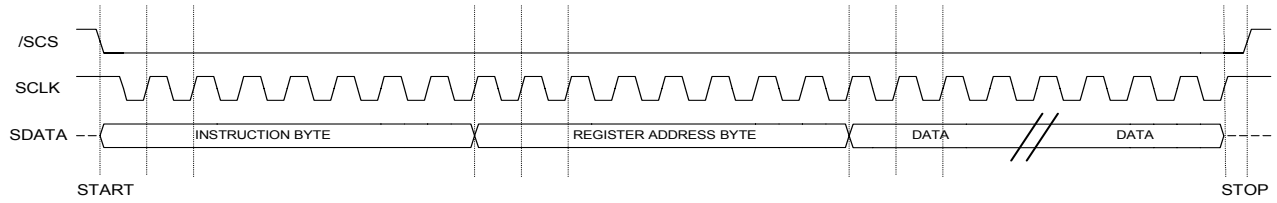


Figure 28. 3-wire protocol

4.12.2.3 Protocol Format

The serial data format to be transmitted consists of an instruction byte, a register address byte and one or more data byte(s). A transfer is initiated by setting /SCS pin low, followed by an instruction byte, a starting register address byte and one or more data byte(s). The /SCS is then set high to terminate the transfer.

Note that there is no device address byte in the format as gm6015 is explicitly selected by the /SCS line. The format of Instruction Byte and Register Address Byte are identical to those described in 2-wire protocol sections.

4.12.2.4 Command Format

3-wire protocol supports the same 4 commands as 2-wire protocol. Please refer to section 4.12.1.4 for details.

5. SYSTEM LAYOUT GUIDELINE

This section outlines the consideration when performing PCB layout with the gm6015. The 6015RD1 board can be used as a reference for PCB layout.

5.1 Power / Ground

In general, a multi-layer PCB approach is desirable and the ground plane area should be maximized. The digital and analog ground should be connected through one point only. All gm6015 ground pins should be connected to the ground plane with a shortest possible trace or directly through via holes.

The supply current to the gm6015 may be distributed through separate power planes. It is suggested that separate regulators be used to supply current to digital and analog part of the chip. Power traces / planes to the PLL and DDS power pins and other power pins should be separate and may come from the same regulator with the connection point close to the regulator.

Bulk electrolytic capacitors should be placed near the regulators and scattered around 2.5V Vdd and 3.3V Vdd pins. De-coupling capacitors should be placed as close as possible to all Vdd pins and one de-coupling capacitors should be used for each Vdd/Gnd pair.

5.2 Signals

1. TCLK and XTAL

   External crystal or oscillator should be placed as close as possible to TCLK and XTAL pins. These 2 pins should also be kept away from other high speed input pins such as input data pins.

2. ASOY_G+/- and BSOY_G+/-

   The 75Ω termination resistor and 47nf ac coupling capacitors should be placed close to the video connector. From the ac coupling capacitors the signal and ground traces should be kept close to each other and in the same length and shape.

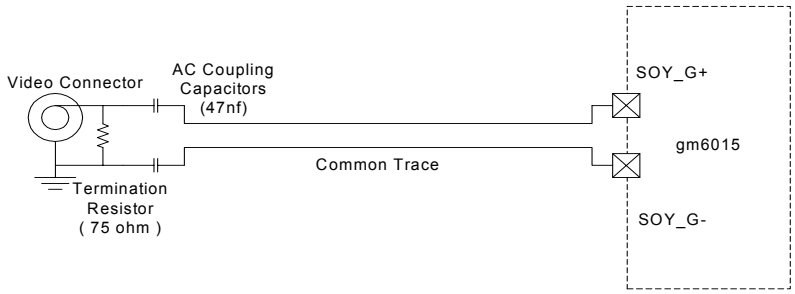


Figure 29. Typical SOY_G +/- connection

3. RAMADDR, RAMDQ and RAMCLK pins

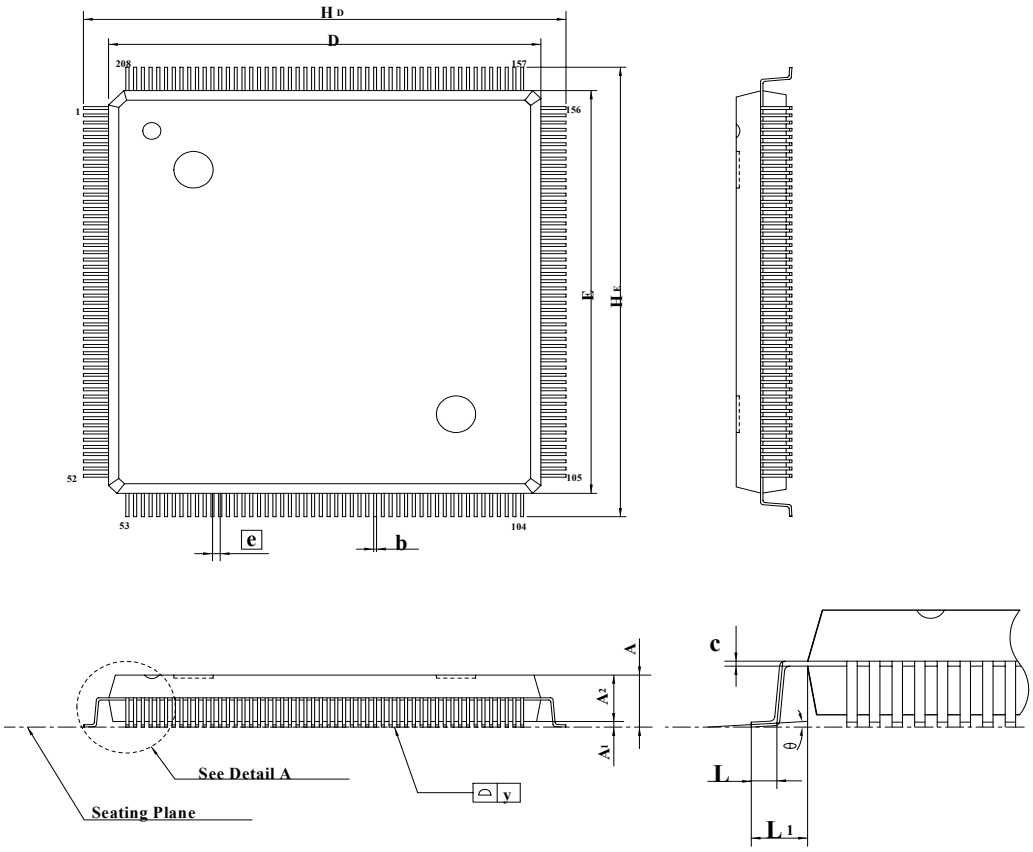
   RAMCLK pin should be connected through a 22Ω resistor to the clock pin of SDRAM with the resistor close to gm6015. The clock trace should be routed on one layer (i.e. no via hole) and kept as

short as possible. For better signal integrity the clock should run on a trace of 75Ω impedance and avoid other signals from running in parallel with the clock trace.

RAMADDR[10..0] and RAMDQ[31..0] pins should be evenly distributed in length and the difference in length of both address and data traces should be less than 1.5 inches.

4. OthersAll unused digital input pins should be tied to ground and unused analog sync separator input pins should be tied high.

6. MECHANICAL SPECIFICATION



Symbol	Dimension in mm		
	Min	Nom	Max
A	3.92	—	4.07
A_1	0.25	—	—
A_2	3.15	3.23	3.30
b	0.18	—	0.28
c	0.13	—	0.23
D	27.90	28.00	28.10
E	27.90	28.00	28.10
e	0.50 BSC		
H_D	30.95	31.20	31.45
H_E	30.95	31.20	31.45
L	0.65	0.80	0.95
L_1	1.60 REF		
y	—	—	0.10
θ	0°	—	7°

Figure 30. gm6015 208 pin PQFP dimension