i5128-L

High-Speed USB Flash Disk Controller

Data Sheet
Version 1.00

iCreate Technologies Corporation

Release date: 2006/08/18

Data sheet marking

iCreate uses various markings in the data sheet to designate each document phase as it relates to the product development stage.

Marking	Description
Objective Specification	The objective specification contains data for new product development.
Advance Information	The information is on products in the design phase. Your designs should not be finalized with this information.
Preliminary	This is preliminary information on new products but not yet fully characterized. The specifications in these data sheets are subject to change in any manner without notice.
No Marking	Information contained in the data sheet is on products in full production.

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1. Introduction

General description

i5128-L is a single-chip High-Speed USB flash disk controller which can handle up to two NAND-like flash memory chips. It is compliant with USB 2.0 and also compatible with USB 1.X. The features of USB-boot-up and driver-less make the flash disk very convenient for end-users.

i5128-L is designed with iCreate flash interface technology to provide wear-leveling and on-the-fly error-correction coding, which enhance the life time of the disk. The flexibility of the interface design also ensures supporting both SLC NAND and MLC NAND flash. i5128-L can also support flash with either 16-bit or 8-bit data bus.

For data security, i5128-L supports multiple protection level. In the non-protection level, data in the disk is fully accessible. In low protection level, disk is read-only to protect from virus and accidental file removal. In high protection level, the disk data cannot be accessed.

User-programmable device name based on USB Mass Storage protocol (SCSI) is also provided.

Features

System Function

- USB 2.0 compliant and USB 1.1 compatible
- USB-ZIP/USB-HDD boot-up
- Support Windows/MacOS Auto-Run
- Support multi-LUN
- Support security
- Compatible with Windows 98/Me/2K/XP, MacOS 9+, and Linux kernel 2.4+
- Configurable Removable or Fixed media
- Support unique serial number for each disk
- Configurable USB vendor/product ID
- Configurable USB vendor/product string
- Single-channel[1] R:18,W:10 Mbyte/s
- Dual-channel[1] R:32,W17 Mbyte/s
- Write protect switch
- Ready/busy LED

Flash Control

- Support 128Mb to 16Gb NAND-type flash
- Dual-channel access boosts data transfer
- Connect up to two flash chips
- Support either x16 or x8 data bus
- Wear-leveling extends product life time
- Defect block concealment and dynamic defect block handling
- On-the-fly 4 byte ECC enhances reliability

Chip Hardware

- On-chip voltage detector for power-on-reset
- Single 3.3V voltage supply
- 12MHz external clock for low EMI
- 48 pin LQFP package

[1] Measured with 2 Samsung K9F2G08U0M-30ns. Read/Write speed varies with flash configuration and operating environment.

2. Pin Configuration and Definition

i5128-L Pin configuration

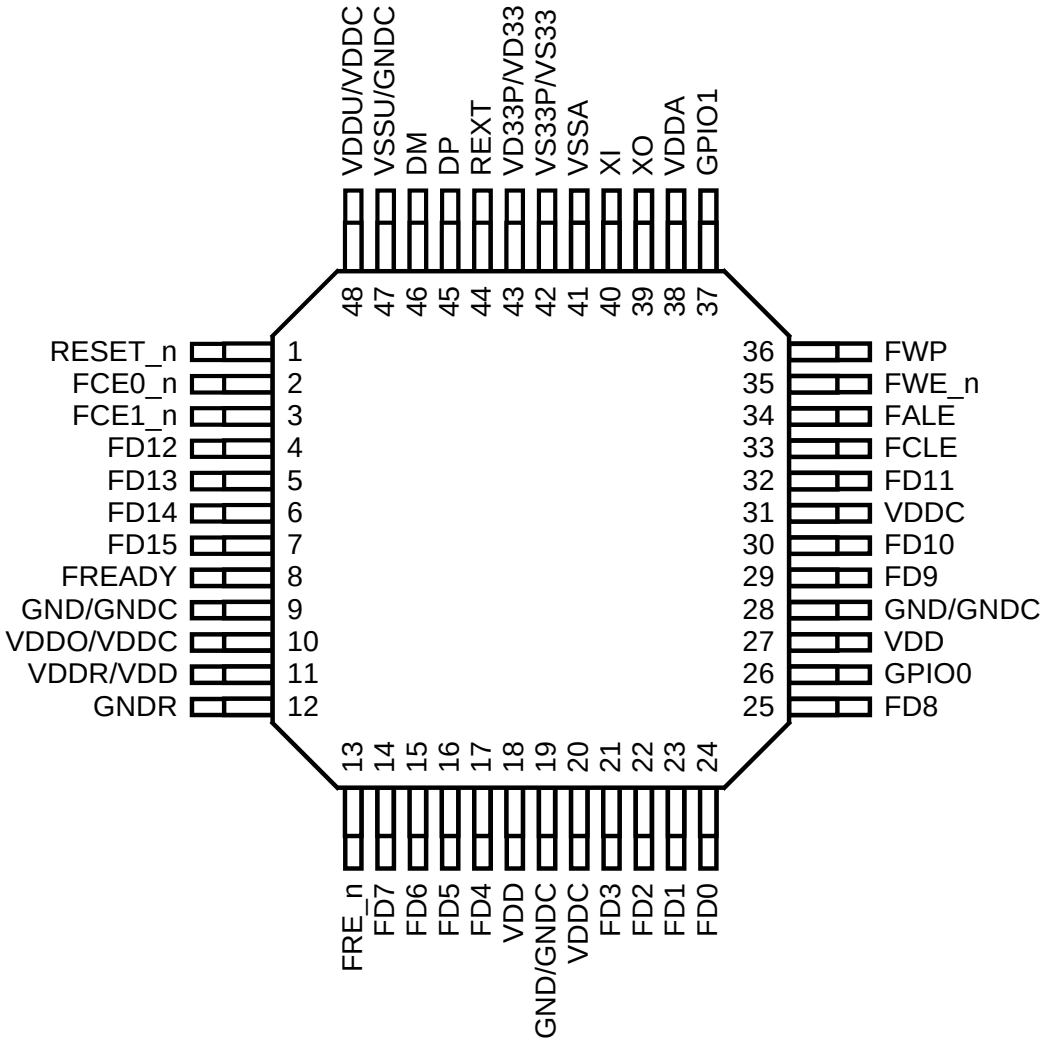


Figure 1. i5128-L Pin configuration

i5128-L Pin definition

Pin Number	Name	IO Type	Function
USB Transceiver			
45	DP	Analog	USB bus D+.
46	DM	Analog	USB bus D-.
44	REXT	Analog	Connect to ground through 330Ohm resistor
Clock			
40	XI	Clock In	12MHz crystal input.

39	XO	Clock Out	12MHz crystal output.
Flash			
7, 6, 5, 4, 32, 30, 29, 25	FD15, FD14, FD13, FD12, FD11, FD10, FD9, FD8	IO8	Bi-directional data bus signals to flash, high 8 bits.
14, 15, 16, 17, 21, 22, 23, 24	FD7, FD6, FD5, FD4, FD3, FD2, FD1, FD0	IO8	Bi-directional data bus signals to flash, low 8 bits.
3, 2	FCE1, FCE0	O2	Active-low chip enable signals to flash.
33	FCLE	O8	Command latch enable to flash.
34	FALE	O8	Address latch enable to flash.
13	FRE_n	O8	Active-low read strobe to flash.
35	FWE_n	O8	Active-low write strobe to flash.
8	FREADY	I, ST, PU	Ready/Busy from flash.
36	FWP	O2	Write protect to flash
System Control and Status			
26	GPIO0	I	Write protect switch
37	GPIO1	O8	Ready/busy LED
1	RESET_n	I, ST, PU	Chip reset
Power and Ground			
18, 27	VDD	Power	3.3V Power
10	VDDO/VDDC	Power	1.8V output of built-in regulator
20, 31	VDDC	Power	1.8V Power
11	VDDR/VDD	Power	3.3V Power
9, 19, 28	GND/GNDC	Ground	Ground
12	GNDR	Ground	Ground
38	VDDA	Power	Analog 1.8V Power
41	VSSA	Ground	Ground
43	VD33P/VD33	Power	3.3V Power
42	VS33P/VS33	Ground	Ground
48	VDDU/VDDC	Power	1.8V Power
47	VSSU/GNDC	Ground	Ground

Function of I/O types

I	Input
ST	Input with Schmitt trigger
PU	Input with internal pull-up
O2	Output buffer with 2mA driving capability
O8	Output buffer with 8mA driving capability
IO8	I/O buffer with 8mA driving capability

3. Electrical Specifications

Maximum Ratings

Parameter	Min	Typ	Max	Units
i5128-L Lead Temperature Range (soldering, 10 seconds)			+235°C	V
i5128-LG Lead Temperature Range (soldering, 10 seconds)			+260°C	V

Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
V_{33}	3.3V Voltage	3.0	3.3	3.6	V
T_{OPR}	Operating temperature	0		70	^{o}C

Symbol	Parameter	Min	Typ	Max	Units
V_{18}	1.8V Voltage	1.65	1.8	1.95	V
T_{OPR}	Operating temperature	0		70	^{o}C

DC Characteristics of Flash Interface and System Pins.

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input LOW voltage			$0.3*V_{33}$	V
V_{IH}	Input HIGH voltage	2.0			V
V_{OL}	Output LOW voltage			0.4	V
V_{OH}	Output HIGH voltage	2.4			V

DC and Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$I_{IDLE-HS}$	High-Speed Idle current (no access, no suspend)		66		mA
I_{RD-HS}	High-Speed Read current		88		mA
I_{WR-HS}	High-Speed Write current		95		mA
$I_{IDLE-FS}$	Full-Speed Idle current (no access, no suspend)		54		mA
I_{RD-FS}	Full-Speed Read current		72		mA
I_{WR-FS}	Full-Speed Write current		64		mA

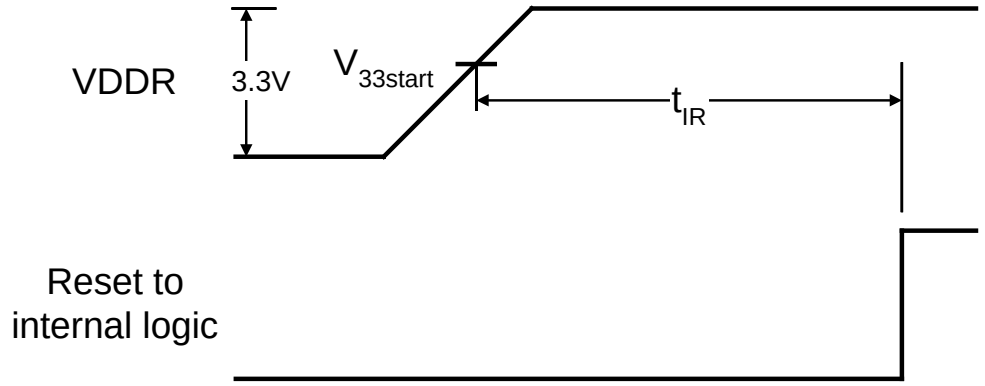
I_{SP}	Suspend current		550		uA

NOTE: We measure the overall current of a reference module with one Samsung K9F1G08U0M.

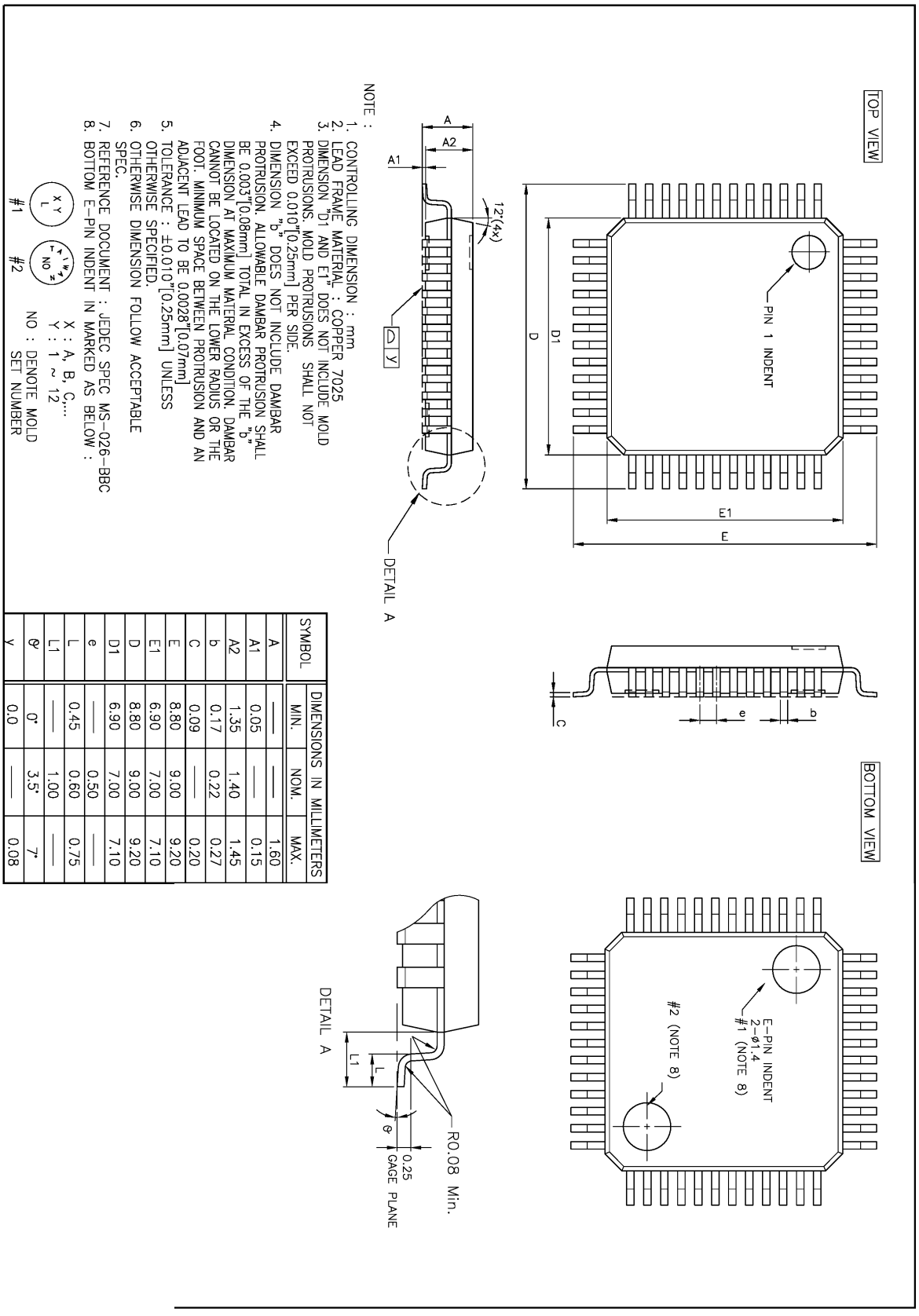
DC Characteristics of Built-in Power-On-Reset

i5128-L builds in voltage detector to detect power ramp-up and then generates reset singal to internal logic, thus external POR device can be eliminated.

Symbol	Parameter	Min	Typ	Max	Units
$V_{33start}$	3.3V threshold of built-in voltage detector		2.1		V
t_{IR}	De-assert time of internal reset		30		ms



4. Package Dimensions



NOTE :

1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : COPPER 7025
3. DIMENSION "D1 AND E1" DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-026-BBC
8. BOTTOM E-PIN INDENT IN MARKED AS BELOW :

#1 #2

X : A, B, C,...
Y : 1 ~ 12
NO : DENOTE MOLD SET NUMBER

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.60
A1	0.05	——	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.09	——	0.20
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
e	——	0.50	——
L	0.45	0.60	0.75
L1	——	1.00	——
θ	0°	3.5°	7°
y	0.0	——	0.08

5. Revision History

Revision	Issue Date	Description of Change
1.00	2006-08-18	Initial release.