iC-MB4
BiSS INTERFACE MASTER

preliminary

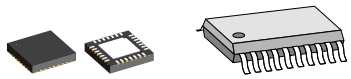
FEATURES

- Bidirectional BiSS communication with up to 8 slaves
- Supports SSI protocol for unidirectional data transmission
- Synchronous sensor data acquisition with cyclic transfer at data rates of up to 10 Mbit/s
- Configurable interface with TTL, CMOS, RS422 or LVDS
- Slave register operations during cyclic data transfers
- Automatic compensation of line delays and conversion times
- Data lengths of up to 64 bit for sensor data, configurable for each slave
- Data verification by CRC polynomials of up to 16 bits per slave
- Separate memory banks enable free controller access during BiSS sensor data transfers
- 64 bytes memory for bidirectional register communication
- Serial controller communication by SPI™-compatible mode
- Parallel interface with 8 bit data/address bus for Intel- and Motorola-devices with combined data and address bus
- Single 3 V to 5 V supply, industrial temperature range

APPLICATIONS

- Bidirectional communication in multi sensor systems
- Linear and rotary encoders
- Motor feedback systems
- PLC systems
- Drives

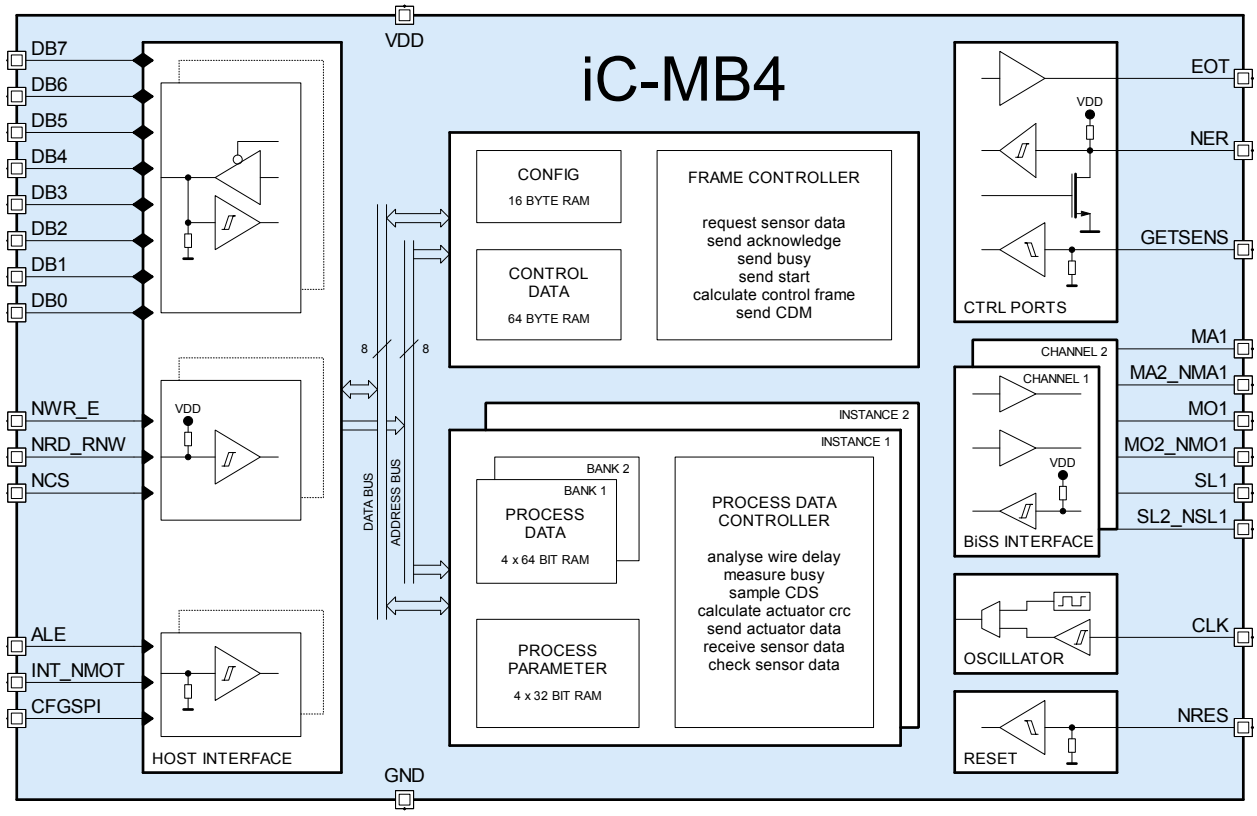
PACKAGES



QFN28
5 mm x 5 mm
RoHS compliant

TSSOP24

BLOCK DIAGRAM



DESCRIPTION

iC-MB4 is a single-chip BiSS/SSI interface master controller featuring an 8-bit bus interface to industrial standard microcontroller. Alternatively an SPI interface enables serial communication between iC-MB4 and the connected microcontroller. The BiSS devices including one or several sensors are connected to the clock line MA and the data return line SL via point-to-point connection (Figure 1). The BiSS devices including actuators and sensors are additionally connected to the data line MO. It is possible to connect multiple devices in chain (Figure 2). RS422 transceivers are used in industrial environments. A maximum of eight BiSS slaves are supported, each with it's own configurable data sections covering:

1. Sensor / actuator data from 0 to 64 bits
   (for measurement data, flags like alarm and warning, Sign of Life cycle counter, . . .)

2. Register data with 64 directly addressable bytes and 256 banks with 64 bytes per slave ID
   (e.g. for device parameters)

iC-MB4 provides two RAM memory banks for each slave enabling simultaneous access by the microcontroller while new sensor data is being read. A 64-byte memory supports register transfers. Sensor data acquisition is started by a microcontroller command or via pin GETSENS. Alternatively, iC-MB4 can also read new sensor data automatically. In this case the cycle time can be set as required. The end of the sensor data acquisition and transmission is indicated at the pin EOT. In case of an error during transmission the pin NER signals a digital low. Errors during communication can be verified by the microcontroller via a status register. A system error message can also access this register if the bidirectional message pin NER is kept digital low by an external intervention. iC-MB4 generates a clock signal for sensor communication using an internal 20 MHz oscillator. The clock can also be supplied externally. iC-MB4 is based on the BiSS master IP family MB100_X.

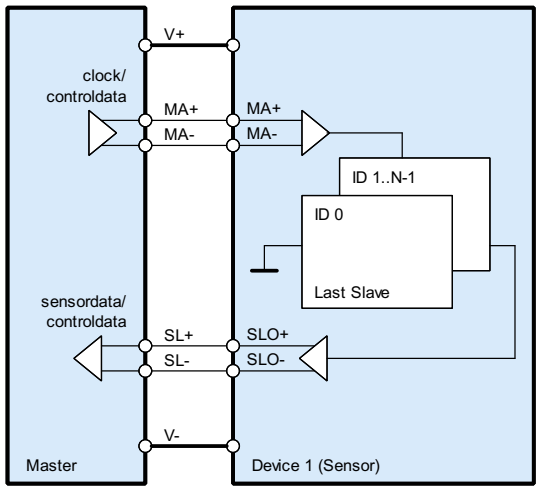


Figure 1: Point-to-point connection of iC-MB4 to one device with several slaves

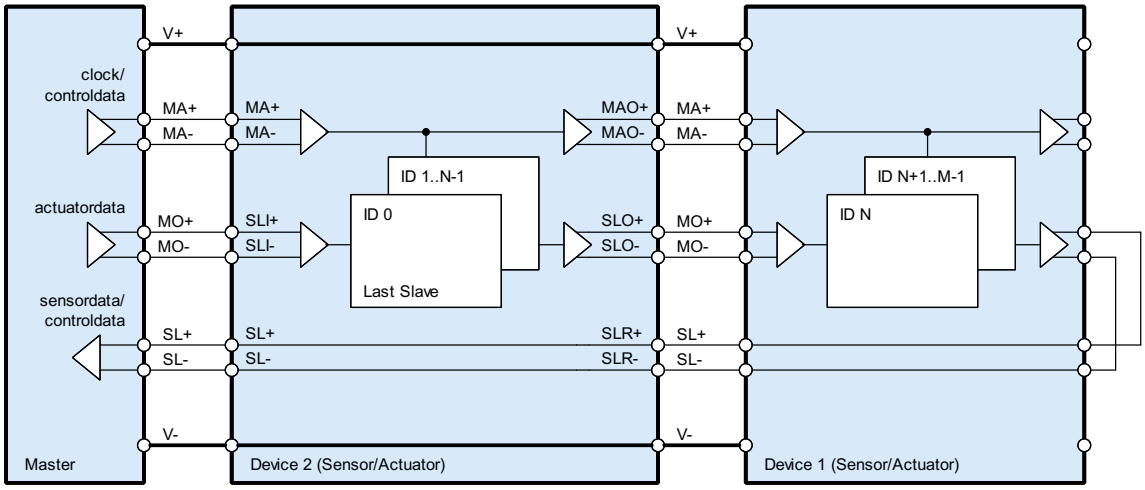
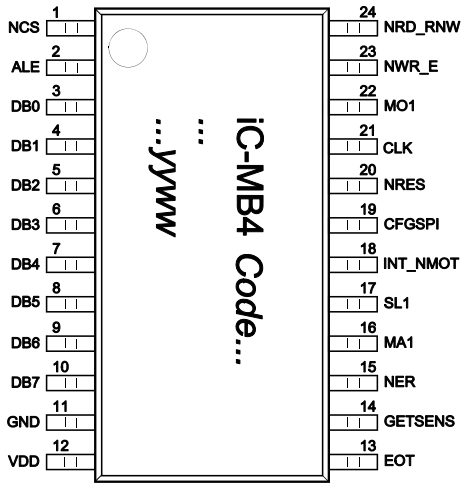


Figure 2: Example network of iC-MB4 and two devices

The device offered here is a multifunctional iC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH. Users benefit from the open BiSS C protocol with a free license which is necessary when using the BiSS C protocol in conjunction with this iC.
Download the license at www.biss-interface.com/BUA

PACKAGING INFORMATION TO JEDEC

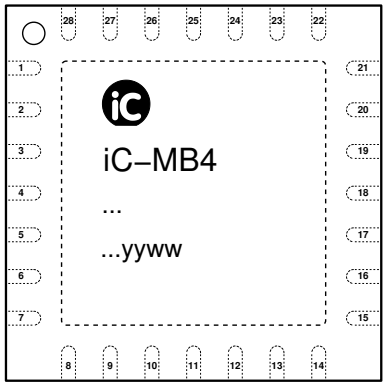
PIN CONFIGURATION TSSOP24 (topview)



PIN FUNCTIONS

No.	Name	Function
		SPI Communication Mode (CFGSPI = 1)
1	NCS	SPI Chip Select Input, active low
2	ALE	SPI Clock Input
3	DB0	SPI Serial Data Input
4	DB1	SPI Serial Data Output
7	DB4	SPI2 Chip Select Input, active low
8	DB5	SPI2 Clock Input
9	DB6	SPI2 Serial Data Input
10	DB7	SPI2 Serial Data Output
		Data Bus Communication Mode (CFGSPI = 0)
1	NCS	Chip Select Input, active low
2	ALE	Address Latch Enable Input
3	DB0	Data Bus Input/Output
4	DB1	Data Bus Input/Output
5	DB2	Data Bus Input/Output
6	DB3	Data Bus Input/Output
7	DB4	Data Bus Input/Output
8	DB5	Data Bus Input/Output
9	DB6	Data Bus Input/Output
10	DB7	Data Bus Input/Output
11	GND	Ground
12	VDD	+3 V . . . +5.5 V Supply Voltage
13	EOT	End of transmission Output
14	GETSENS	Sensor Data Request Input
15	NER	Error Message Input/Output, low active
16	MA1	BiSS Clock Line Output
17	SL1	BiSS Data Line Input
18	INT_NMOT	Communication Mode Select Input (Intel = 1, Motorola = 0)
19	CFGSPI	Serial/Parallel Mode Select Input (serial SPI = 1, parallel = 0)
20	NRES	Reset Input, low active
21	CLK	External Clock Input
22	MO1	BiSS Data Line Output
		Intel Mode (INT_NMOT = 1)
23	NWR_E	Write Input, active low
24	NRD_RNW	Read Input, active low
		Motorola Mode (INT_NMOT = 0)
23	NWR_E	Enable Input, active high
24	NRD_RNW	Read/Not-Write Select Input

PIN CONFIGURATION QFN28 5 mm x 5 mm (topview)

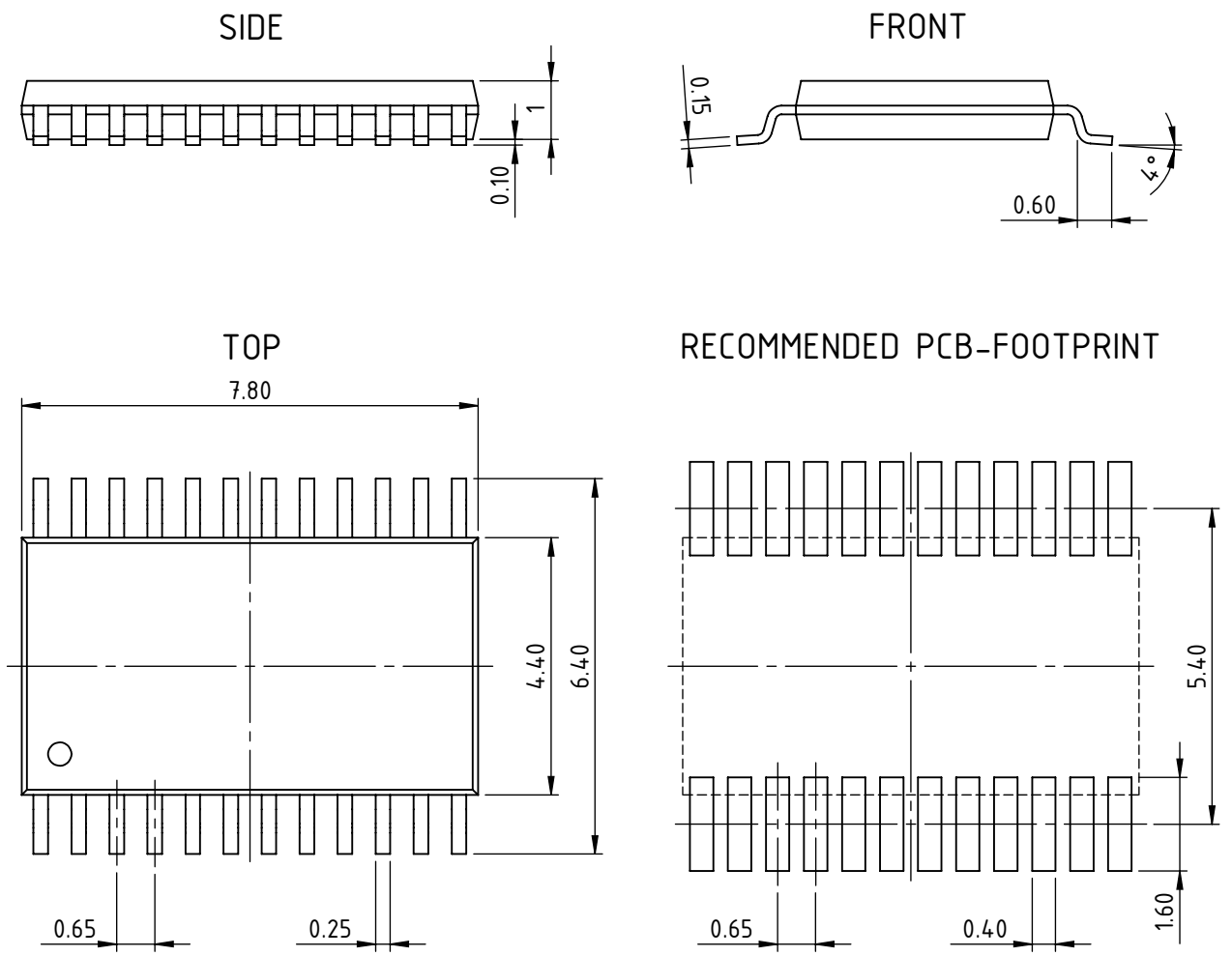


PIN FUNCTIONS

No.	Name	Function
		SPI Communication Mode (CFGSPI = 1)
27	NCS	SPI Chip Select Input, active low
28	ALE	SPI Clock Input
1	DB0	SPI Serial Data Input
2	DB1	SPI Serial Data Output
5	DB4	SPI2 Chip Select Input, active low
6	DB5	SPI2 Clock Input
7	DB6	SPI2 Serial Data Input
8	DB7	SPI2 Serial Data Output
		Data Bus Communication Mode (CFGSPI = 0)
1	DB0	Data Bus Input/Output
2	DB1	Data Bus Input/Output
3	DB2	Data Bus Input/Output
4	DB3	Data Bus Input/Output
5	DB4	Data Bus Input/Output
6	DB5	Data Bus Input/Output
7	DB6	Data Bus Input/Output
8	DB7	Data Bus Input/Output
9	GND	Ground
10	VDD	+3 V . . . +5.5 V Supply Voltage
11	EOT	End of transmission Output
12	GETSENS	Sensor Data Request Input
13	NER	Error Message Input/Output, low active
14	n.c.	not connected
15	MA1	BiSS Clock Line Output
16	MA2_NMA1	BiSS Clock Line Output Channel 2
17	SL1	BiSS Data Line Input
18	SL2_NSL1	BiSS Data Line Input Channel 2
19	INT_NMOT	Communication Mode Select Input (Intel = 1, Motorola = 0)
20	CFGSPI	Serial/Parallel Mode Select Input (serial SPI = 1, parallel = 0)
21	NRES	Reset Input, low active
22	CLK	External Clock Input
23	MO1	BiSS Data Line Output
24	MO2_NMO1	BiSS Data Line Output Channel 2
25	NWR_E	Write Input, active low (Intel) Enable Input, active high (Motorola)
26	NRD_RNW	Read Input, active low (Intel) Read/Not-Write Select Input (Motorola)
27	NCS	Chip Select Input, active low
28	ALE	Address Latch Enable Input
BP		Backside Paddle (GND)

The *Backside Paddle* must be connected to GND.

PACKAGE DIMENSIONS TSSOP24



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-153

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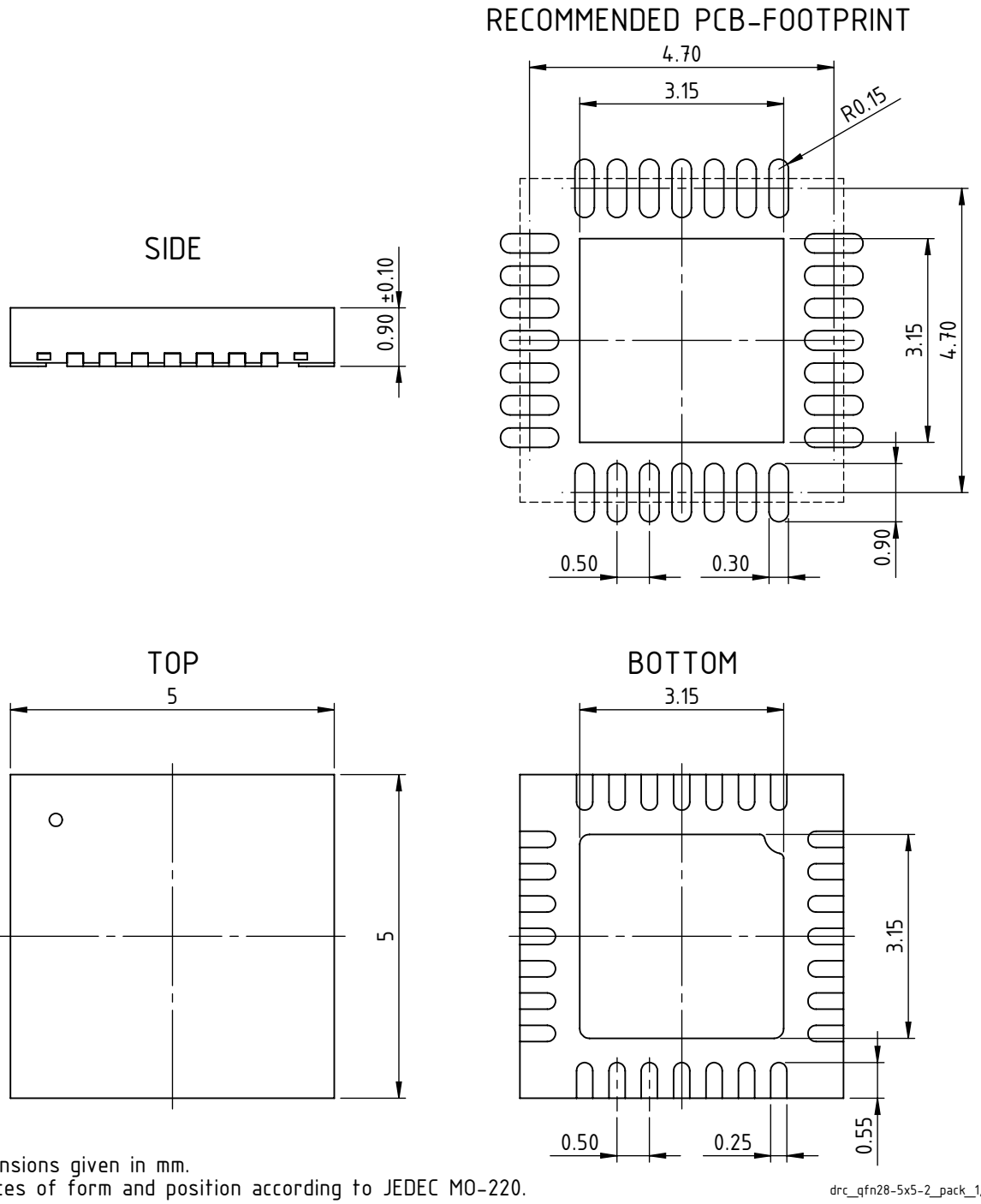
PACKAGE DIMENSIONS QFN28 5 mm x 5 mm



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

drc_qfn28-5x5-2_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	I(VDD)	Current in VDD		-20	30	mA
G003	V()	Voltage at all pins excluding VDD and GND	V() VDD + 0.3 V	-0.3	6	V
G004	I()	Current in all pins excluding VDD and GND		-10	10	mA
G005	V_{esd}()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 Ω		2	kV
G006	Tj	Operating Junction Temperature	VDD = 3.0 V ... 4.5 V VDD = 4.5 V ... 5.5 V	-40 -40	125 140	°C °C
G007	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 3.0 V. . . 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Standard Operating Ambient Temperature Range		-40		85	°C
T02	Ta_{ET}	Extended Operating Ambient Temperature Range	VDD = 4.5 V ... 5.5 V available on request	-40		125	°C
T03	$R_{thjaTSSOP}$	Thermal Resistance Chip to Ambient	TSSOP24 surface mounted, no special heat sink		80		K/W
T04	$R_{thjaQFN}$	Thermal Resistance Chip to Ambient	QFN28 package mounted on PCB, *Backside Paddle* at approx. 2 cm² cooling area		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current in VDD	outputs not loaded, f(CLK) = 20 MHz			20	mA
003	Vc()hi	Clamp Voltage hi at all pins excluding VDD, GND, MA1, MO1, SL1	Vc()hi = V() - VDD, I() = 1 mA; outputs tristate	0.3		1.75	V
004	Vc()lo	Clamp Voltage lo at all pins excluding VDD, GND	I() = -1mA; outputs tristate	-1.6		-0.3	V
µC Interface: CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0							
A01	Vs()hi	Saturation Voltage hi at DB7...0	Vs()hi = VDD - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V; I() = -2 mA			 0.4 0.4	 V V
A02	Vs()lo	Saturation Voltage lo at DB7...0	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
A03	Vt()hi	Threshold Voltage hi at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0				2	V
A04	Vt()lo	Threshold Voltage lo at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0		0.8			V
A05	Vt()hys	Threshold Voltage Hysteresis at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0		150	250		mV
A06	Ipd()	Pull-Down Current at CFGSPI, INT_NMOT, ALE, DB7...0	VDD = 4.5 V, V() = 1 V ... V(VDD) VDD = 3 V, V() = 1 V ... V(VDD)	6 3	30 30	60 60	µA µA
A07	Ipu()	Pull-Up Current at NCS, NRD_RNW, NWR_E	VDD = 4.5 V, V() = 0 V ... V(VDD) - 1 V VDD = 3 V, V() = 0 V ... V(VDD) - 1 V	-60 -60	-30 -30	-6 -3	µA µA
BiSS/SSI Interface							
B01	Rpu()	Pull-up Resistor at SL1, SL2_NSL1			50		kΩ
BiSS/SSI Interface: TTL/CMOS Mode (CFGIF = 00 or 01)							
B02	Vs()hi	Saturation Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	V() = V(VDD) - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V, I() = -2 mA			 0.4 0.4	 V V
B03	Vs()lo	Saturation Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
BiSS/SSI Interface: TTL Mode (CFGIF = 00)							
B04	Vt()hi	Threshold Voltage hi at SL, SL2_NSL1				2	V
B05	Vt()lo	Threshold Voltage lo at SL, SL2_NSL1		0.8			V
B06	Vt()hys	Hysteresis at at SL, SL2_NSL1		150	300		mV
BiSS/SSI Interface: CMOS Mode (CFGIF = 01)							
B07	Vt()hi	Threshold Voltage hi at SL, SL2_NSL1			62	70	%VDD
B08	Vt()lo	Threshold Voltage lo at SL, SL2_NSL1		33	39		%VDD
B09	Vt()hys	Hysteresis at at SL, SL2_NSL1		0.7	1.13		V
BiSS/SSI Interface: RS422 Mode (CFGIF = 10, VDD = 4.5 V ... 5.5 V)							
B10	Vs()hi	Saturation Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	V() = V(VDD) - V(); I() = -50 mA			1.2	V
B11	Vs()lo	Saturation Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	I() = 50 mA			1.2	V
B12	Vcom()	Input Voltage Range at SL, SL2_NSL1		0		3	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B13	Vtdiff()	Threshold Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	-300		300	mV
B14	Vthys()	Hysteresis Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	75	150		mV
BiSS/SSI Interface: LVDS Mode (CFGIF = 11)							
B15	Vs()hi	Output Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 1.25 1.0		 1.6 1.6	 V V
B16	Vs()lo	Output Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 0.9 0.7		 1.125 1.125	 V V
B17	Vadiff	Differential Output Voltage at MA1 - MA2_NMA1, MO1 - MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 250 220	 350 350	 450 450	 mV mV
B18	Vacm	Common Mode Output Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 1.125 0.9	 1.2 1.15	 1.375 1.375	 V V
B19	Vcom()	Input Voltage Range at SL, SL2_NSL1	VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	0.8 0.8		3 1.8	V V
B20	Vtdiff()	Threshold Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	-150		150	mV
B21	Vthys()	Hysteresis Voltage at SL - SL2_NSL1	V()=V(P) - V(N) VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 25 14	 70 40		 mV mV
I/O Ports: EOT, NER, GETSENS							
C01	Vs()hi	Saturation Voltage hi at EOT	Vs()hi = VDD - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V; I() = -2 mA			 0.4 0.4	 V V
C02	Vs()lo	Saturation Voltage lo at EOT, NER	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
C03	Vt()hi	Threshold Voltage hi at NER, GETSENS				2	V
C04	Vt()lo	Threshold Voltage lo at NER, GETSENS		0.8			V
C05	Vt()hys	Threshold Voltage Hysteresis at NER, GETSENS		150	250		mV
C06	Ipd()	Pull-Down Current at GETSENS	VDD = 4.5 V, V() = 1 V ... V(VDD) VDD = 3 V, V() = 1 V ... V(VDD)	6 3	30 30	60 60	µA µA
C07	Ipu()	Pull-Up Current at NER	V() = 0 V ... V(VDD) - 1 V	-950	-300	-35	µA
C08	Tw(GETSENS)	Minimum duration of GETSENS pulse		1/f(CLK)			
Oscillator: CLK							
D01	f(CLK)	Permissible external Clock Rate at CLK	Duty cycle 48% . . . 52%		20	25	MHz
D02	Vt(CLK)hi	Threshold Voltage hi				2	V
D03	Vt(CLK)lo	Threshold Voltage lo		0.4			V
D04	Vt(CLK)hys	Threshold Voltage Hysteresis		150	250		mV
D05	f(CLKI)	Internal Oscillator Clock Frequency	VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	15 10	20 15	25 22	MHz MHz
D06	Ipd()	Pull-Down Current at CLK	VDD = 4.5 V, V() = 1.5 V ... VDD VDD = 3 V, V() = 1.5 V ... VDD	6 3	30 30	60 60	µA µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset Signal Input: NRES							
E01	VDDoff	Undervoltage Reset	VDD decreasing	1.4		2.6	V
E02	VDDon	Undervoltage Release	VDD increasing	1.6		2.8	V
E03	VDDhys	Undervoltage Hysteresis	VDDhys = VDDon - VDDoff	200			mV
E04	Vt()hi	Threshold Voltage hi				2	V
E05	Vt()lo	Threshold Voltage lo		0.4			V
E06	Vt()hys	Threshold Voltage Hysteresis		300	500		mV
E07	Ipd()	Pull-Down Current	V() = 1.5 V ... VDD	4	35	70	µA
E08	td()res	Required Reset Pulse Duration	At NRES	250			ns

OPERATING REQUIREMENTS: µC Interface, INTEL mode

Operating conditions: CFGSPI = 0, INT_NMOT = 1, VDD = 3.0 . . . 5.5 V, Tj = -40 . . . 125 °C
lo input level = 0 . . . 0.8 V, hi input level = 2.0 V . . . VDD, lo output level = 0 . . . 0.4 V, hi output level = 2.4 V . . . VDD
Alias: NRD = NRD_RNW, NWR = NWR_E

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	tsCA	Setup Time: NCS lo before ALE hi→lo		10		ns
I002	tsDA	Setup Time: Data stable before ALE hi→lo		15		ns
I003	thDA	Hold Time: Data stable after ALE hi→lo		15		ns
I004	tAh	Signal Duration: ALE at high level		10		ns
I005	tsAR	Setup Time: ALE lo before NRD hi→lo		10		ns
I006	thAR	Hold Time: ALE lo after NRD lo→hi	NCS = lo	10		ns
I007	tRl	Signal Duration: NRD at low level	NCS = lo	10		ns
I008	tpRD1	Propagation Delay: Data stable after NRD hi→lo	NCS = lo, CL = 5 pF, VDD ≥ 4.5 V, Tj = -40 . . . 85 °C CL = 5 pF, VDD ≥ 4.5 V CL = 50 pF, VDD ≥ 4.5 V, Tj = -40 . . . 85 °C CL = 50 pF, VDD ≥4.5 V CL = 5 pF, Tj = -40 . . . 85 °C CL = 5 pF CL = 50 pF, Tj = -40 . . . 85 °C CL = 50 pF		23 25 29 33 38 42 49 54	ns ns ns ns ns ns ns ns
I009	tpRD2	Propagation Delay: Data bus high impedance after NRD lo→hi	NCS = lo, CL = 50 pF		25	ns
I010	thCR	Hold Time: NCS lo after NRD lo→hi		10		ns
I011	tsAW	Setup Time: ALE lo before NWR hi→lo		10		ns
I012	thAW	Hold Time: ALE lo after NWR lo→hi	NCS = lo	10		ns
I013	tWl	Signal Duration: NWR at low level	NCS = lo	10		ns
I014	tsDW	Setup Time: Data stable before NWR lo→hi	NCS = lo	15		ns
I015	thDW	Hold Time: Data stable after NWR lo→hi	NCS = lo	15		ns
I016	thCW	Hold Time: NCS lo after NWR lo→hi		10		ns

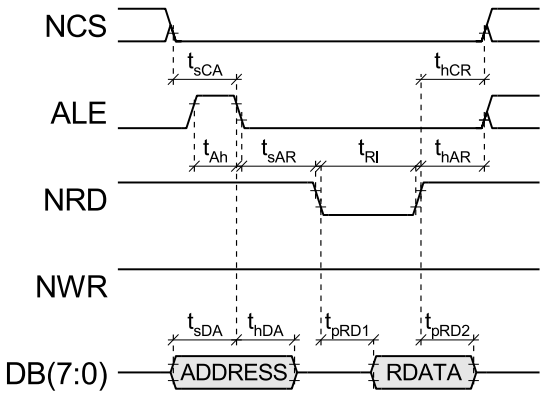


Figure 3: Read cycle (Intel mode)

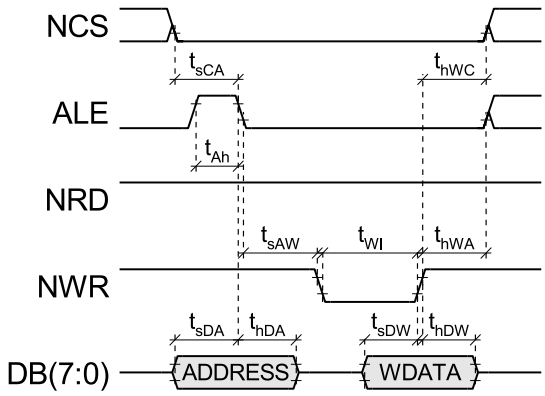


Figure 4: Write cycle (Intel mode)

OPERATING REQUIREMENTS: µC Interface, MOTOROLA mode

Operating conditions: CFGSPI = 0, INT_NMOT = 0 VDD = 3.0 ... 5.5 V, Tj = -40 ... 125 °C;
lo input level = 0 ... 0.8 V, hi input level = 2.0 V ... VDD, lo output level = 0 ... 0.4 V, hi output level = 2.4 V ... VDD
Alias: RNW = NRD_RNW, E = NWR_E

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	tsCA	Setup Time: NCS lo before ALE hi→lo		10		ns
I102	tsDA	Setup Time: Data stable before ALE hi→lo		15		ns
I103	thDA	Hold Time: Data stable after ALE hi→lo		15		ns
I104	tAh	Signal Duration: ALE at high level		10		ns
I105	tsAE	Setup Time: ALE lo before E lo→hi		10		ns
I106	thAE	Hold Time: ALE lo after E hi→lo	NCS = lo	10		ns
I107	tsRE	Setup Time: RNW stable before E lo→hi	NCS = lo	10		ns
I108	thRE	Hold Time: RNW stable after E hi→lo	NCS = lo	10		ns
I109	tEh	Signal Duration: E at high level	NCS = lo	10		ns
I110	tpED1	Propagation Delay: Data stable after E lo→hi	NCS = lo, CL = 5 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 5 pF, VDD ≥ 4.5 V CL = 50 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 50 pF, VDD ≥4.5 V CL = 5 pF, Tj = -40 ... 85 °C CL = 5 pF CL = 50 pF, Tj = -40 ... 85 °C CL = 50 pF		 23 25 29 33 38 42 49 54	 ns ns ns ns ns ns ns ns ns
I111	tpED2	Propagation Delay: Data bus high impedance after E hi→lo	NCS = lo, CL = 50 pF		25	ns
I112	tsDE	Setup Time: Data stable before E hi→lo	NCS = lo	15		ns
I113	thDE	Hold Time: Data stable after E hi→lo	NCS = lo	15		ns
I114	thCE	Hold Time: NCS lo after E hi→lo		10		ns

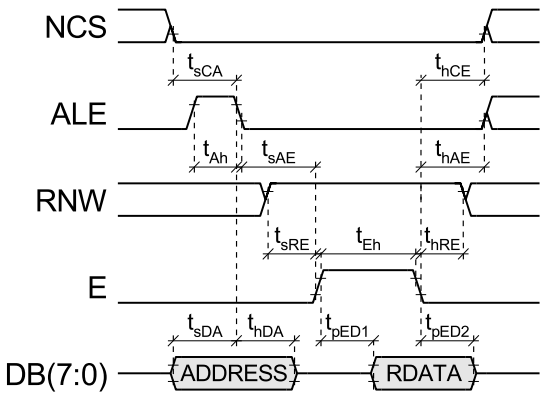


Figure 5: Read cycle (Motorola mode)

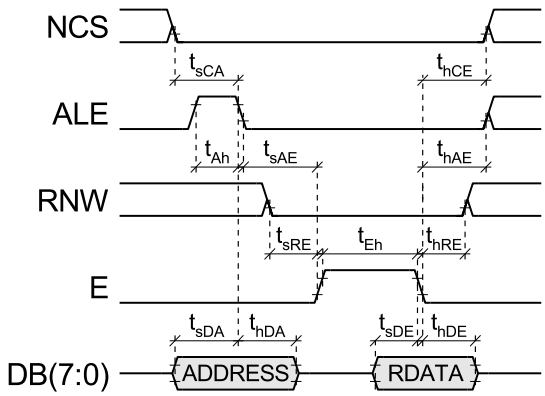


Figure 6: Write cycle (Motorola mode)

OPERATING REQUIREMENTS: µC Interface, SPI mode

Operating conditions: CFGSPI = 1 VDD = 3.0 ... 5.5 V, Tj = -40 ... 125 °C;
lo input level = 0 ... 0.8 V, hi input level = 2.0 V ... VDD, lo output level = 0 ... 0.4 V, hi output level = 2.4 V ... VDD
Alias: NCS = NCS/DB4, SCLK = ALE/DB5, MOSI = DB0/DB6, MISO = DB1/DB7

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I201	tsCS	Setup Time: NCS lo before SCLK lo→hi		10		ns
I202	thCS	Hold Time: NCS lo after SCLK hi→lo		10		ns
I203	tSl	Signal Duration: SCLK lo		10		ns
I204	tSh	Signal Duration: SCLK hi during SPI command 'ReadData' between address and data		10 100		ns ns
I205	tsDS	Setup Time: MOSI stable before SCLK lo→hi		7.5		ns
I206	thDS	Hold Time: MOSI stable after SCLK lo→hi		7.5		ns
I207	tpSD	Propagation Delay: MISO stable after SCLK hi→lo	CL = 5 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 5 pF, VDD ≥ 4.5 V CL = 50 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 50 pF, VDD ≥ 4.5 V CL = 5 pF, Tj = -40 ... 85 °C CL = 5 pF CL = 50 pF, Tj = -40 ... 85 °C CL = 50 pF		23 25 29 33 38 42 49 54	ns ns ns ns ns ns ns ns
I208	tpCD	Propagation Delay: MISO high impedance after NCS lo→hi	CL = 50 pF		25	ns
I209	tCh	Signal Duration: NCS hi		10		ns

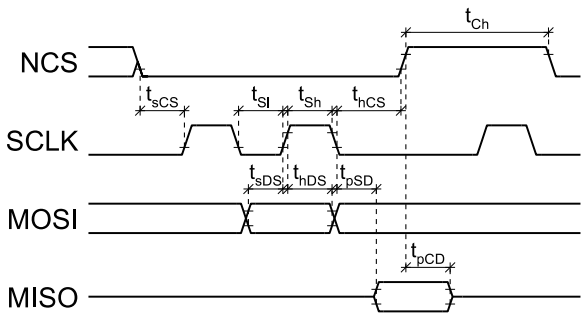


Figure 7: Read/write access (SPI mode)

OPERATING REQUIREMENTS: BiSS Interface - BiSS B/C frame

Operating conditions: register bit SELSSI = 0 VDD = 3.0 . . . 5.5 V, Tj = -40 . . . 125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Frame						
I301	TMAS	Clock Period	FreqSens via FREQ(4:0) selected in accordance with Table 41 on page 32	2	320	1/f(CLK)
I302	tMASl	Clock Signal Lo Level Duration		50	50	% TMAS
I303	tMASh	Clock Signal Hi Level Duration		50	50	% TMAS
I304	tpLine	Permissible Line Delay		0	indefinite	
I305	Δ tpL	Permissible Propagation Delay of Subsequent Clock Cycles vs. 1st Clock Cycle	Δ tpL = max(|tpLine - tpLx|); x= 1 ... n		25	% TMAS
I306	Ttos	Permissible Timeout (Slave)		55		% TMAS

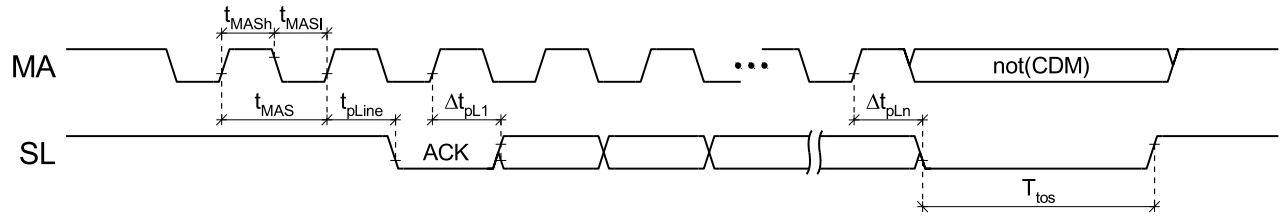


Figure 8: Timing diagram BiSS B/C frame

SLx line sampling
Line delays longer than one clock cycle are permissible in BiSS.
Within one MA clock cycle four equally distributed sampling points are used to evaluate the overall delay from the second rising edge at MAx to the first falling edge at SLx (ACK).
Refer also to the characteristics in BiSS Interface PROTOCOL DESCRIPTION.

OPERATING REQUIREMENTS: BiSS Interface - BiSS B register data cycle

Operating conditions: register bit SELSSI = 0 VDD = 3.0...5.5 V, Tj = -40...125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I401	TMAR	Clock Period	FreqReg via FREQ(7:5) selected in accordance with Table 42 on page 32	2	256	TMAS
I402	tMA0h	"Logic 0" Hi Level Duration		25	25	% TMAR
I403	tMA1h	"Logic 1" Hi Level Duration		75	75	% TMAR
I404	tMAth	Clock Signal Hi Level Duration	register data readout	50	50	% TMAR
I405	tsSM	Setup Time: SL stable before MA lo→hi		30		ns
I406	thSM	Hold Time: SL stable after MA lo→hi		0		ns
I407	Ttor	Permissible Timeout (Slave)	For Ttos details see item i306 BiSS Frame	80		% TMAR

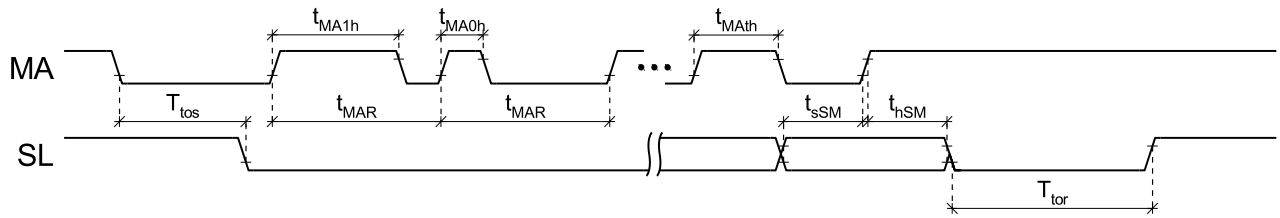


Figure 9: Timing diagram BiSS B register access

OPERATING REQUIREMENTS: BiSS Interface (SSI mode)

Operating conditions: register bit SELSSI = 1; VDD = 3. . . 5.5 V, Tj = -40. . . 125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I501	TMAS	Clock Period	FreqSens via FREQ(4:0) selected in accordance with Table 41 on page 32	2	320	1/f(CLK)
I502	tMASh	Clock Signal Hi Level Duration		50	50	% TMAS
I503	tMASl	Clock Signal Lo Level Duration		50	50	% TMAS
I504	tsSM	Setup Time: SLx stable before MAx lo→hi		30		ns
I505	thSM	Hold Time: SLx stable after MAx lo→hi		0		ns
I506	Ttos	Permissible Timeout (Slave)		55		% TMAS

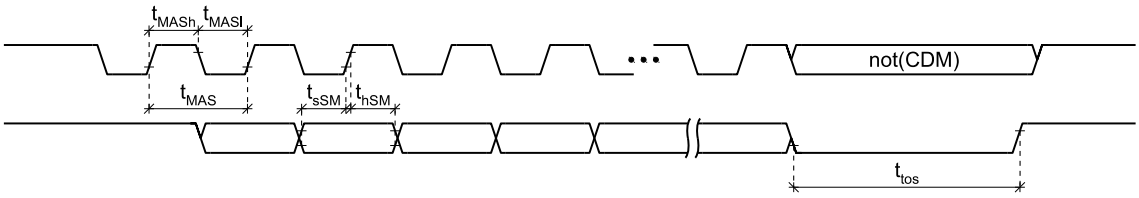


Figure 10: Timing diagram SSI mode

SLx line sampling
In SSI interface mode SLx values are sampled with the rising edge at MAx. An overall delay of the sensor response to the clock at MAx, caused by process times in the sensor or transmission times, is permissible up to the length of one clock cycle minus tsSM.

CONFIGURATION PARAMETERS

REGISTER MAP

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sensor and Actuator Data								
0x00	SCDATA1(7:0)							
0x01 .. 0x07	SCDATA1(63:8)							
0x08 .. 0x3F	SCDATA2(63:0) .. SCDATA8(63:0)							
0x40 .. 0x7F	– *							
Register Data								
0x80 †	RDATA1(7:0)							
0x80 ‡	IDS(7:0)							
0x81 .. 0xBF	RDATA2(7:0) .. RDATA64(7:0)							
Configuration Slave 1								
0xC0	GRAYS1 / LSTOP1	ENSCD1	SCDLEN1(5:0)					
0xC1	SELCRCS1	SCRCLEN1(6:0) / SCRCPOLY1(7:1)						
0xC2	SCRCSTART1(7:0)							
0xC3	SCRCSTART1(15:8)							
0xC4 .. 0xDF	Configuration Slave 2(31:0) .. Configuration Slave 8(31:0)							
Control Communication Configuration								
0xE0	– *							
0xE1	– *							
0xE2	WNR	REGADR(6:0)						
0xE3	– *		REGNUM(5:0)					
0xE4	– *						CHSEL(2:1)	
0xE5 †	CTS	REGVERS	SLAVEID(2:0)			– *	EN_MO	HOLDCDM
0xE5 ‡	CTS	REGVERS	CMD(1:0)		IDA_TEST	– *	EN_MO	HOLDCDM
Master Configuration								
0xE6	FREQR(2:0)			FREQS(4:0)				
0xE7	– *						NOCRC	SINGLEBANK
0xE8	FREQAGS(7:0)							
0xE9	MO_BUSY(7:0)							
0xEA	REVISION(7:0)§							
0xEB	VERSION(7:0)§							

* Reserved or unused register bits highlighted as '–' need to be written with 0 if a byte wide register write access is required.
† Using register access in control communication.
‡ Using command/instructions in control communication.
§ Register bits with constant '0' or '1' are ROM-based values and can not be changed through writing.

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Channel Configuration								
0xEC	'0'	'0'	'0'	SLAVELOC5	'0'	'0'	'0'	'1'
0xED	– *				CFGCH2(1:0)		CFGCH1(1:0)	
0xEE	– *							
Slave Configuration 2								
0xEF	ACTnSENS(8:1)							
Status Information								
0xF0	nERR	nAGSERR	nDELAYERR	nSCDERR	nREGERR	REGEND	'1'	EOT
0xF1	SVALID4	'0'	SVALID3	'0'	SVALID2	'0'	SVALID1	'0'
0xF2	SVALID8	'0'	SVALID7	'0'	SVALID6	'0'	SVALID5	'0'
0xF3	CDMTIME-OUT	CDSSEL	REGBYTES(5:0)					
Instruction Register								
0xF4	BREAK	HOLDBANK	SWBANK	INIT	INSTR(2:0)			AGS
0xF5	MAVO	MAFO	MAVS	MAFS	CFGIF(1:0)		ENTEST	CLKENI
0xF6	– *	– *	– *	– *	– *	– *	– * *	– *
0xF7	– *	– *	– *	– *	– *	– *	– *	– *
Status Information 2								
0xF8	'0'	'1'	'0'	'1'	CDS2	SL2	CDS1	SL1
0xF9	'0'	'1'	'0'	'1'	'0'	'1'	'0'	'1'
0xFA	– *	– *	– *	– *	– *	– *	– *	– *
0xFB	– *	– *	– *	– *	– *	– *	– *	SWBANK-FAILS
Reserved								
0xFC .. 0xFF	– *	– *	– *	– *	– *	– *	– *	– *

Table 10: Register layout

Note: Reserved registers need to be written with 0x00.

Note: iC-MB4 does reset all RAM registers to '0' on a power on reset.

FUNCTIONAL DESCRIPTION

The open source BiSS Interface Protocol implements a realtime interface for digital, serial and secure communication between drive, sensor and actuator. In the point-to-point configuration BiSS uses one clock line MAx from the master to the sensor and one data line SLx from the sensor to the master (see Figure 1). A device may contain multiple slaves. The data input pin SLI of the last slave is set to digital low. The slaves are daisy-chained (SLO $\rightarrow$ SLI) and the data output pin SLO of the first slave is directly connected to the master. A data line from the master to the slave is not mandatory.

In the bus configuration the data output line MO is used to transfer actuator data from the master to the slaves (see figure 2). The BiSS protocol describes cyclic data frames and differentiates between process data and control data. Process data are completely transmitted in each frame (SCD) used as actuator or sensor data and control data are transmitted one bit per frame (CD) used for commands and register access.

BiSS C Frame
The BiSS C Frame starts with a digital high on the clock line MAx and is notified by iC-MB4 with a falling edge at the pin EOT. On the first falling edge of MAx all slaves check the SLI pin for a digital low determining the last slave. With the first rising edge at MAx all sensors start calculating their sensor data. The second rising edge of MAx forces all slaves to acknowledge the BiSS-C frame with a falling edge at SLO. The master uses the acknowledge to measure the line delay. When the sensor data calculation is finished, the last slave in the chain generates the start bit which will be passed synchronously through all slaves to the master. If the master data output MOx is used, the start bit delay has to be configured to ensure sufficient processing time regarding sensor data for all slaves. Subsequent to the start bit follows one control data bit for all slaves (CDS) which is set according to the rules of the control frame. After the CDS bit, the process data including sensor and actuator data is sent with the most significant bit (MSB) first. At the end, the master sends it's control data bit (CDM) inverted on the clock line MAx to conclude the BiSS-C Frame.

During processing the frame all slaves observe the MAx clock line and change into the timeout state, if MAx is stable for a specific time defined within each slave. In the timeout state, only the last slave forces it's SLO pin to digital high. The other slaves in the chain connect SLI and SLO to signal the master that all slaves are in the timeout state. After detecting the slave's timeout with SLO = 1, the master may changes the MAx clock line to digital high or keeps the clock line constant until the next frame begins. This is advantageous if the BiSS-C Frame has not been clocked out completely, e.g. for a fast configuration phase and high control data transmission rates. The difference is indicated in Figures 11 and 12.

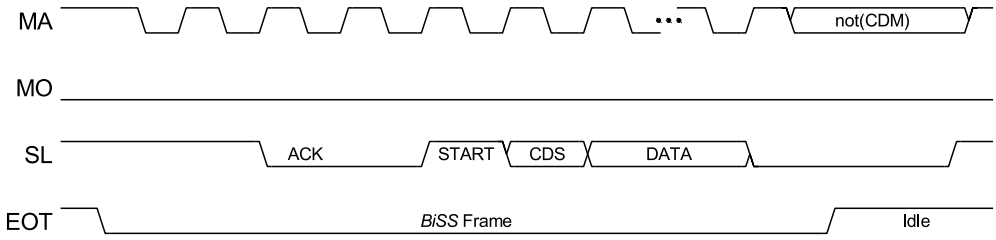


Figure 11: BiSS C frame in point-to-point configuration

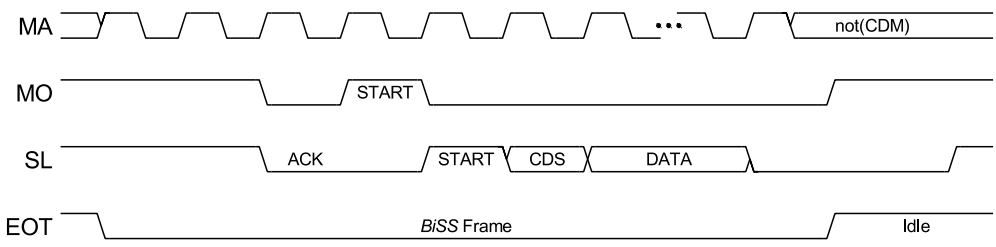


Figure 12: BiSS C frame in bus configuration

BiSS C Initialization Sequence

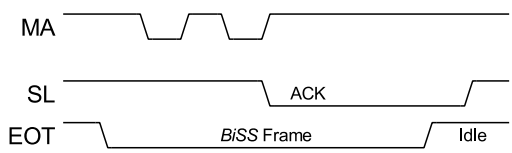


Figure 13: BiSS C initialization sequence

An initialization (INIT) sequence is necessary, if the last slave in the point-to-point configuration is not defined and the data line SLx is digital low. In the initialization sequence, two digital low pulses are generated at MAx. The slave(s) should answer with a falling-edge after the second pulse and with a rising-edge at SLx after the BiSS timeout. The time between the second rising-edge at MAx and the falling-edge at SLx is measured as line delay and stored in the single cycle data RAM, see chapter INSTRUCTION REGISTER on page 37.

Extended SSI BiSS C Register Communication

The extended SSI operation enables the BiSS C register write access to SSI slaves. The master is able to transmit a BiSS C register write access to the slave without the slave's CDS feedback. The master cannot verify that the BiSS C register write access to the slave did succeed. At the end of the SCD frame the master sends the CDM bit inverted on the MA clock line.

BiSS B Register Communication

For the BiSS B protocol the register communication is started by a timing condition and a handshake at the beginning of the frame (see Figure 14). Alternatively, the register communication can be activated at the beginning of the frame with a connected MO line (slave ID "0" remains unused).

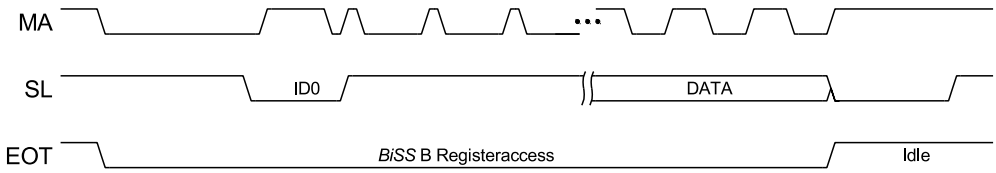


Figure 14: BiSS B register access (EN_MO = 0)

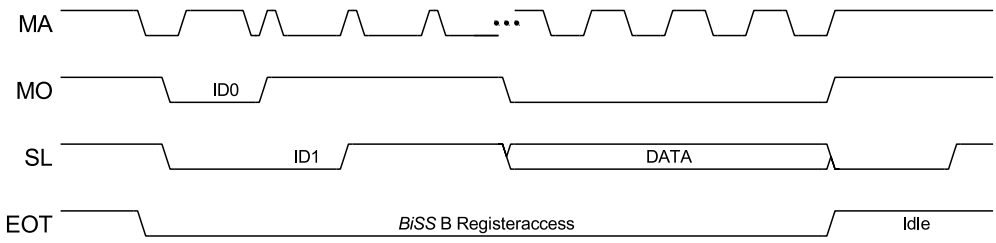


Figure 15: BiSS B register access (EN_MO = 1)

BiSS B Initialization Sequence

In the BiSS-B initialization sequence (init) only the timing handshake with the first falling edge at MA is executed.

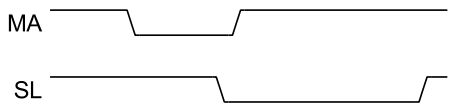


Figure 16: BiSS B initialization sequence

MICROCONTROLLER INTERFACE

The iC-MB4 supports a parallel and a serial microcontroller interface. The input port CFGSPI is used to select the desired interface. The interfaces cannot be used at the same time.

Parallel Microcontroller Interface

With pin CFGSPI = 0 the 8 bit parallel microcontroller interface is selected in which the bidirectional data bus alternately transmits addresses and data in blocks of 8 bits. The pin INT_NMOT selects two different communication types.

CFGSPI	INT_NMOT	Mode
0	0	Motorola 68HC11
0	1	Intel 8051

Table 11: Parallel communication types

In both cases, a digital low at the pin NCS activates the interface and the pin ALE is used to store the address. The data pins are tristate while deactivated via NCS.

If the pin INT_NMOT = 0, the motorola communication type is selected. The pin RNW chooses between read and write access and the pin E executes the access (see Figure 17).

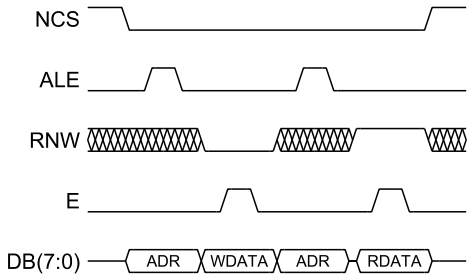


Figure 17: Motorola controller communication

The Intel 8051 controller communication type uses NWR as write enable and NRD as read enable. It is selected with INT_NMOT = 1 (see Figure 18).

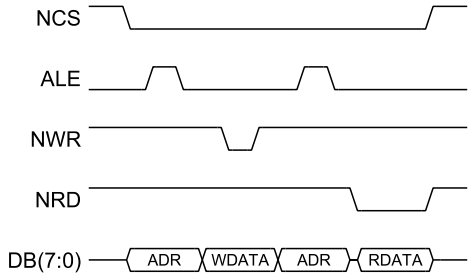


Figure 18: Intel controller communication

SPI Serial Microcontroller Interface

If the pin CFGSPI = 1, the SPI serial microcontroller interfaces with polarity = 0 and phase = 0 are selected.

CFGSPI	INT_NMOT	Mode
1	-	SPI1 (polarity = 0, phase = 0)

Table 12: SPI communication mode

When operating in conjunction with an SPI controller, the pin ALE is used as a clock input (SCK), the pin NCS as an enable input (NCS), the pin DB0 is used as the data input (SI) and the pin DB1 is used as the data output (SO). Data is transmitted serially in successive blocks of 8 bits starting with the command. Depending on the commands, the following blocks represents an address and one or more data bytes (see figure 19). Six commands are available:

SPI-COMMAND		
Code	Description	Address
0x02	Write Data	Transmitted
0x03	Read Data	Transmitted
0x05	Read Status	0xF0
0x07	Write Instruction	0xF4
0x09	Read Data 0	0x00
0x0B	Write Data 0	0x00

Table 13: Command Codes for SPI

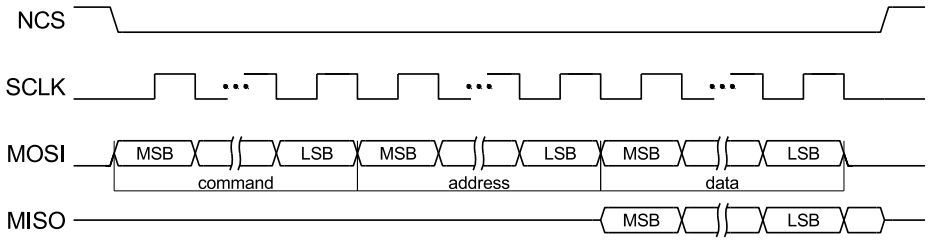


Figure 19: SPI communication

The first two commands in Table 15 can be used to write data to or read data from iC-MB4's registers. In the "read data" command a delay between the address and the first data is necessary (Refer to Op.Require. No. I201). The last four commands are shortened write and read commands with a fixed start address. This means that it is not necessary to send an address as described above. The data can directly be transmitted after the command. With all commands it is possible to transmit several bytes of data consecutively, if the NCS signal remains digital low and ALE/SCK is clocked continuously. The address is internally increased by 1 for each transmitted byte starting at the fixed or transmitted address respectively.

Additional 2nd SPI Serial Microcontroller Interface
If the SPI serial microcontroller interface is activated, an additional SPI interface can be enabled with NWR_E = 0 for dedicated register access with reduced function set.

CFGSPI	NWR_E	Mode
1	0	SPI2, optional (polarity = 0, phase = 0)

Table 14: SPI communication mode

The additional SPI interface at DB4 . . . DB7 is available for an exclusive read access to the SCD single cycle data RAM of the slaves 5 to 8 with the commands "Read Data" and "Read Data 0". Access to the status, the instruction and the parameter registers is not possible.

SPI-COMMAND		
Code	Description	Address
0x03	Read Data	Transmitted
0x09	Read Data 0	0x00

Table 15: Command Codes for SPI2

Note: This 2nd SPI can only be used to read SCDATA from 0x40 . . . 0x7F. It is not possible to read the status or to access the configuration RAM via SPI2.

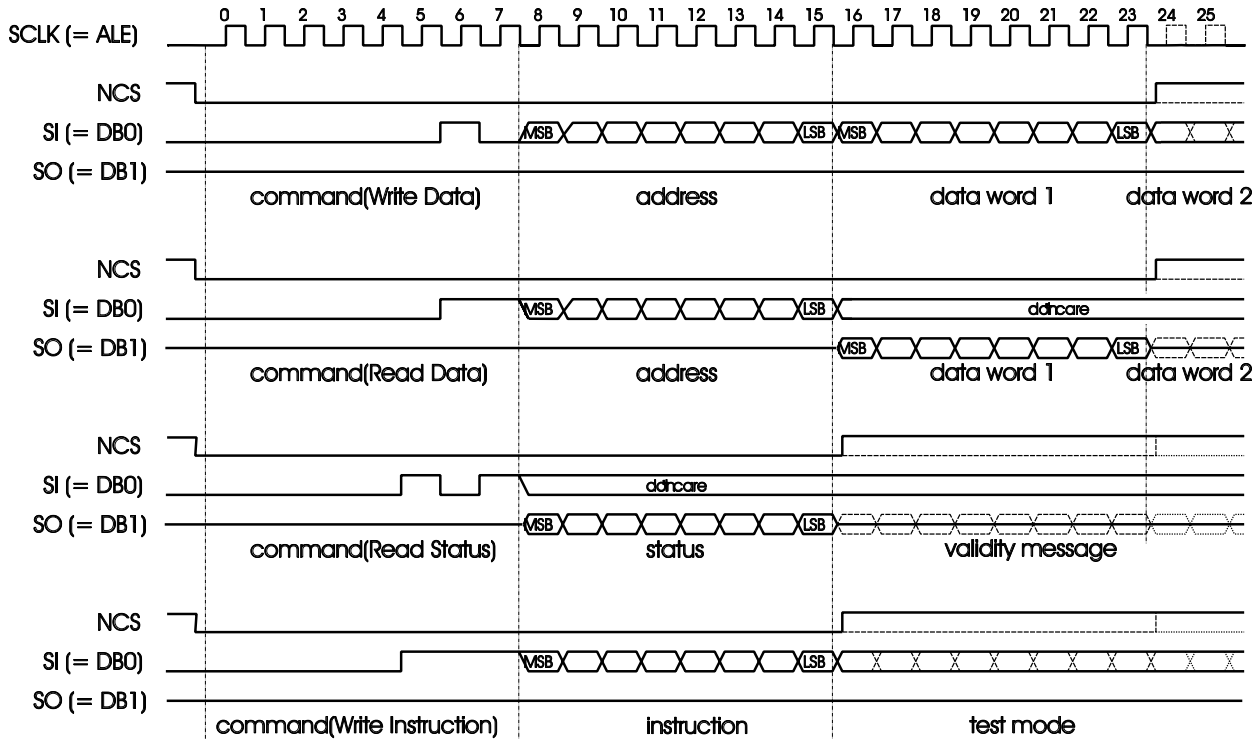


Figure 20: SPI transmission protocol (polarity 0, phase 0)

SENSOR AND ACTUATOR DATA

The process data memory buffers the sensor and actuator data and has eight bytes of memory for each slave. Eight slaves are supported. The address mapping is shown in Table 16.

SCDATA	Addr. 0x00 . . . 0x3F; bit 7:0	R/W
Addr.	Content	
0x00	SCDATA1(7:0)	
0x01	SCDATA1(15:8)	
0x02	SCDATA1(23:16)	
0x03	SCDATA1(31:24)	
0x04	SCDATA1(39:32)	
0x05	SCDATA1(47:40)	
0x06	SCDATA1(55:48)	
0x07	SCDATA1(63:56)	
0x08 . . 0x0F	SCDATA2(63:0)	
0x10 . . 0x17	SCDATA3(63:0)	
0x18 . . 0x1F	SCDATA4(63:0)	
0x20 . . 0x27	SCDATA5(63:0)	
0x28 . . 0x2F	SCDATA6(63:0)	
0x30 . . 0x37	SCDATA7(63:0)	
0x38 . . 0x3F	SCDATA8(63:0)	

Table 16: Address mapping of sensor data

The sensor data is arranged in the memory area with the least significant bit (LSB) at the lowermost address at bit position 0. The memory is written byte-by-byte and unused bits are set to zero. Unused bytes remain unchanged. If there is sufficient free memory available for CRC data, the read and inverted CRC bits are stored beginning at the highest address downwards. The storage of the CRC can be disabled with NOCRC (see Table 44).

Example: BiSS Sensor Bus with 3 Slaves
The following example shows the address mapping of the sensor data and CRC bits generated by three slaves.

Slave 1: 19+2 bits of sensor data, 6 bits of CRC
=> total length of 27 bits

Slave 2: 12+2 bits of sensor data, 5 bits of CRC
=> total length of 19 bits

Slave 3: 24 bits of sensor data, 16 bits of CRC
=> total length of 40 bits

SCDATA	Addr. 0x00 . . . 0x3F							
Addr.	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00	Sensor data 1(7:0)							
0x01	Sensor data 1(15:8)							
0x02	0	0	0	Sensor data 1(20:16)				
0x03 . . 0x06	not changed							
0x07	0	0	CRC 1(5:0)					
0x08	Sensor data 2(7:0)							
0x09	0	0	Sensor data 2(13:8)					
0x0A . . 0x0E	not changed							
0x0F	0	0	0	CRC 2(4:0)				
0x10	Sensor data 3(7:0)							
0x11	Sensor data 3(15:8)							
0x12	Sensor data 3(23:16)							
0x13 . . 0x15	not changed							
0x16	CRC 3(7:0)							
0x17	CRC 3(15:8)							
0x18 . . 0x3F	not changed							

Table 17: Example address mapping of sensor data

In order to import new sensor data during controller accesses, iC-MB4 has two memory banks for sensor data. While sensor data is being read and written into the first RAM bank during processing of the BiSS Frame, the second RAM bank section containing sensor data of the previous frame can be read by the controller. The relevant sensor data memory banks are swapped at the end of the BiSS Frame. This can be prevented by the controller entering the command register bit HOLDBANK (see Table 72). Simultaneously the validity register (SVALIDx, Table 61) is also swapped.

REGISTER DATA

The iC-MB4 has an individual storage area used for the data of the automatic register communication. In case of a write access to the slaves the storage area must be written with the register data before starting the communication. The same memory area is also used for the read data coming from the slave during read access. The memory size of the storage area is 64 bytes.

RDATA	Addr. 0x80 . . . 0xBF; bit 7:0	R/W
Addr.	Content	
0x80	RDATA1(7:0)	
0x81 . . 0xBF	RDATA2(7:0) . . . RDATA64(7:0)	

Table 18: RDATA address range for register communication

The slave addressing IDS which is used in commands must be stored at address 0x80.

IDS	Addr. 0x80; bit 7:0	R/W
Addr.	Content	
0x80	IDS(7:0)	

Table 19: IDS for commands

CONTROL COMMUNICATION

The control frame enables protected and confirmed reading and writing of the registers of a slave. It is also used for protected and confirmed sending of commands to specified slaves or to all slaves. The control frame is compounded of 1 bit per BiSS C frame in each direction. The control bit sent from the master to the slaves is called CDM and control bit sent from the slaves to the master is called CDS. For more information about the control communication refer to the BiSS Interface PROTOCOL DESCRIPTION.

The iC-MB4 does support autonomous register communication with BiSS B and BiSS C. REGVERS is used to select the protocol type. For register write access with extended SSI the BiSS C protocol type needs to be selected.

REGVERS	Addr. 0xE5; bit 6	R/W
Code	Function	
0	Register communication BiSS A/B	
1	Register communication BiSS C	

Table 20: Type of protocol for register access

If more than one physical BiSS channel is used, the one-hot coded parameter CHSEL selects the channel that is used for control communication. For commands it is possible to run the control communication on several channels simultaneously.

CHSEL(1)	Addr. 0xE4; bit 0	R/W
Code	Function	
0	Channel 1 not used *	
1	Channel 1 used for control communication	
CHSEL(2)	Addr. 0xE4; bit 1	R/W
0	Channel 2 not used	
1	Channel 2 used for control communication †	

Table 21: Channel mapping for control communication

The selection between commands and register access is done with the parameter CTS.

CTS	Addr. 0xE5; bit 7	R/W
Code	Function	
0	Command/instruction communication	
1	Register access	
Note	The parameter CTS was called MSEL in former MB100 or iC-MB3 data sheets.	

Table 22: Type of control communication

The parameter HOLDCDM determines the behaviour of the pin MA at the end of the frame. If the pin SL is not digital low at the end of the frame, because the BiSS C frame has not been clocked out completely, the pin MA must be programmed with HOLDCDM to be constant until the next frame begins.

HOLDCDM	Addr. 0xE5; bit 0	R/W
Code	Function	
0	MA changes to digital after detecting the slave's timeout	
1	MA remains constant until the next frame begins	

Table 23: Behaviour of the pin MA at the end of frame

* Channel 1 is selected if CHSEL(2:1)=0.
† Channel 2 is not available with iC-MB4 TSSOP24.

The Commands

The following registers are used to configure the BiSS C control communication for command transfer. The command/instruction communication is a subset of the control communication. The command can address one or several slaves by setting the appropriate bits in the IDS register. To address all slaves via broadcast command IDS has to be reset to zero.

IDS(0:7)	Addr. 0x80; bit 7:0	R/W
Code	Function	
0x00	All slaves addressed (broadcast)	
IDS7	Addr. 0x80; bit 0	R/W
0	Slave with ID 7 is not addressed	
1	Slave with ID 7 is addressed	
IDS6	Addr. 0x80; bit 1	R/W
0	Slave with ID 6 is not addressed	
1	Slave with ID 6 is addressed	
IDS4	Addr. 0x80; bit 2	R/W
0	Slave with ID 5 is not addressed	
1	Slave with ID 5 is addressed	
IDS4	Addr. 0x80; bit 3	R/W
0	Slave with ID 4 is not addressed	
1	Slave with ID 4 is addressed	
IDS3	Addr. 0x80; bit 4	R/W
0	Slave with ID 3 is not addressed	
1	Slave with ID 3 is addressed	
IDS2	Addr. 0x80; bit 5	R/W
0	Slave with ID 2 is not addressed	
1	Slave with ID 2 is addressed	
IDS1	Addr. 0x80; bit 6	R/W
0	Slave with ID 1 is not addressed	
1	Slave with ID 1 is addressed	
IDS0	Addr. 0x80; bit 7	R/W
0	Slave with ID 0 is not addressed	
1	Slave with ID 0 is addressed	

Table 24: IDS command/instruction addressing

The command code is determined with CMD. Some commands are predefined in the BiSS Interface PROTOCOL DESCRIPTION, others can be used for application specific functionality.

CMD(1:0)	Addr. 0xE5; bit 5:4	R/W
Code	Command / instruction	
0x00	"00"	
0x01	"01"	
0x02	"10"	
0x03	"11"	

Table 25: Command of addressed slave

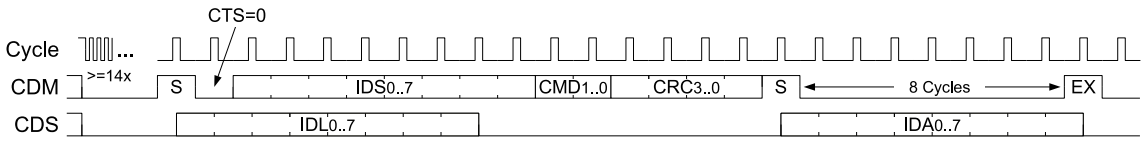
In contrast to the broadcast commands, the reception of a command addressed to specific slaves is confirmed. Each addressed slave confirms the command during IDA. The parameter IDA_TEST defines, if the master triggers the command execution immediately or after successfully checking the IDA bits (see Fig. 21 and 22).

IDA_TEST	Addr. 0xE5; bit 3	R/W
Code	Function	
0	Immediate execution	
1	The slaves feedback (IDA) is tested before execution	

Table 26: Command/instruction execution control

(S=Start, IDL=ID-Lock, IDS=ID-Select, CMD=Command, EX=Execute)

Figure 21: Control frame (broadcast command)



(S=Start, IDL=ID-Lock, IDS=ID-Select, IDA=ID-Acknowledge, CMD=Command, EX=Execute)

Figure 22: Control frame (addressed command)

The register access
The register start address REGADR, register access direction RNW, number of bytes REGNUM and slave address SLAVEID are used to configure the BiSS C control communication for register access. A byte count of 0 entered for REGNUM signals the transmission of a single register value.

REGADR	Addr. 0xE2; bit 6:0	R/W
Code	Function	
0x00 . . . 0x7F	Start address for register access	

Table 27: Register access start address

WNR	Addr. 0xE2; bit 7	R/W
Code	Function	
0	Read register data	
1	Write register data	

Table 28: Register access direction

REGNUM	Addr. 0xE3; bit 5:0	R/W
Code	Register count	
0x00	1	
0x01 . . . 0x3E	Code + 1	
0x3F	64	

Table 29: Number of consecutive registers to access

SLAVEID	Addr. 0xE5; bit 5:3	R/W
Code	Slave ID	
0 . . . 7	Code	

Table 30: Slave ID of accessed slave

The Figure 23 exemplarily shows a control frame including a register read access.

Note: All configuration parameter must be stable during control communication frame.

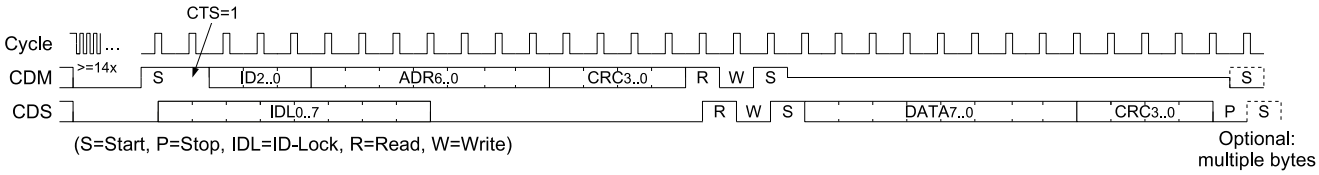


Figure 23: Control frame (register read)

SLAVE CONFIGURATION

The process data consists of a maximum of eight logical data channels. The slave configuration determines the setup of each data channel. The iC-MB4 provides a programmable data length, CRC polynomial and CRC start value for each logical data slave.

ENSCD1	Addr. 0xC0; bit 6	R/W
ENSCD2	Addr. 0xC4; bit 6	R/W
ENSCD3	Addr. 0xC8; bit 6	R/W
ENSCD4	Addr. 0xCC; bit 6	R/W
ENSCD5	Addr. 0xD0; bit 6	R/W
ENSCD6	Addr. 0xD4; bit 6	R/W
ENSCD7	Addr. 0xD8; bit 6	R/W
ENSCD8	Addr. 0xDC; bit 6	R/W
Code	Function	
0	Single cycle data not available	
1	Single cycle data available	

Table 31: Enable single cycle data for slave x

SCDLEN1	Addr. 0xC0; bit 5:0	R/W
SCDLEN2	Addr. 0xC4; bit 5:0	R/W
SCDLEN3	Addr. 0xC8; bit 5:0	R/W
SCDLEN4	Addr. 0xCC; bit 5:0	R/W
SCDLEN5	Addr. 0xD0; bit 5:0	R/W
SCDLEN6	Addr. 0xD4; bit 5:0	R/W
SCDLEN7	Addr. 0xD8; bit 5:0	R/W
SCDLEN8	Addr. 0xDC; bit 5:0	R/W
Code	Single cycle data length	
0	1	
. . .	Code + 1	
63	64	

Table 32: Single cycle data length of slave x

SELCRCS1	Addr. 0xC1; bit 7	R/W
SELCRCS2	Addr. 0xC5; bit 7	R/W
SELCRCS3	Addr. 0xC9; bit 7	R/W
SELCRCS4	Addr. 0xCD; bit 7	R/W
SELCRCS5	Addr. 0xD1; bit 7	R/W
SELCRCS6	Addr. 0xD5; bit 7	R/W
SELCRCS7	Addr. 0xD9; bit 7	R/W
SELCRCS8	Addr. 0xDD; bit 7	R/W
Code	Function	
0	CRC bit length in SCRCLENx apply predefined CRC polynomials	
1	CRC polynomial(7:1) in SCRCPOLYx	

Table 33: CRC polynomial selection

BiSS uses CRC polynomials depending on the data length predefined in the EDS and Profile Definitions. The parameter SELCRCS chooses between predefined polynomials selected according to the CRC length and non predefined polynomials for CRCs with a length of up to seven bits. If CRCLEN = 0, the CRC verification is deactivated.

SCRCLEN1	Addr. 0xC1; bit 6:0	R/W
SCRCLEN2	Addr. 0xC5; bit 6:0	R/W
SCRCLEN3	Addr. 0xC9; bit 6:0	R/W
SCRCLEN4	Addr. 0xCD; bit 6:0	R/W
SCRCLEN5	Addr. 0xD1; bit 6:0	R/W
SCRCLEN6	Addr. 0xD5; bit 6:0	R/W
SCRCLEN7	Addr. 0xD9; bit 6:0	R/W
SCRCLEN8	Addr. 0xDD; bit 6:0	R/W
Code	CRC polynomial for single cycle data	
0	CRC verification deactivated	
3	0b1011 = 0xB	
4	0b1.0011 = 0x13	
5	0b10.0101 = 0x25	
6	0b100.0011 = 0x43	
7	0b1000.1001 = 0x89	
8	0b1.0010.1111 = 0x12F	
16	0b1.1001.0000.1101.1001 = 0x190D9	
. . .	Other codes are not permitted.	

Table 34: CRC length with predefined CRC polynomial

Since the least significant bit of the CRC polynomial is always 1, there is no need to store this information in the CRC polynomial register. Therefore a maximum polynomial length of 8 bit is possible. If the maximum 8 bit polynomial length is not required, the used polynomial (without the LSB bit) is stored right aligned and leading bits are filled with 0.
Example: The CRC polynomial 0x43 = 100 0011b is stored as 010 0001b (register value 0x21).

SCRCPOLY1	Addr. 0xC1; bit 6:0	R/W
SCRCPOLY2	Addr. 0xC5; bit 6:0	R/W
SCRCPOLY3	Addr. 0xC9; bit 6:0	R/W
SCRCPOLY4	Addr. 0xCD; bit 6:0	R/W
SCRCPOLY5	Addr. 0xD1; bit 6:0	R/W
SCRCPOLY6	Addr. 0xD5; bit 6:0	R/W
SCRCPOLY7	Addr. 0xD9; bit 6:0	R/W
SCRCPOLY8	Addr. 0xDD; bit 6:0	R/W
Code	CRC polynomial for single cycle data	
0x00	CRC verification deactivated	
0x01 . . 0x7F	Code & '1'	

Table 35: CRC polynomial

The CRC start values can be used to safely differentiate between SCD data words e.g. two position words

provided by two different sensors. The same CRC start value that is used in the sensor needs to be applied in the master to validate the received single cycle data. The CRC start value has a length of 16 bit and is divided into two consecutive 8-bit registers. A typical default slave CRC start value is 0x0000.

SCRCSTART1_L	Addr. 0xC2; bit 7:0	R/W
SCRCSTART1_H	Addr. 0xC3; bit 7:0	R/W
SCRCSTART2_L	Addr. 0xC6; bit 7:0	R/W
SCRCSTART2_H	Addr. 0xC7; bit 7:0	R/W
SCRCSTART3_L	Addr. 0xCA; bit 7:0	R/W
SCRCSTART3_H	Addr. 0xCB; bit 7:0	R/W
SCRCSTART4_L	Addr. 0xCE; bit 7:0	R/W
SCRCSTART4_H	Addr. 0xCF; bit 7:0	R/W
SCRCSTART5_L	Addr. 0xD2; bit 7:0	R/W
SCRCSTART5_H	Addr. 0xD3; bit 7:0	R/W
SCRCSTART6_L	Addr. 0xD6; bit 7:0	R/W
SCRCSTART6_H	Addr. 0xD7; bit 7:0	R/W
SCRCSTART7_L	Addr. 0xDA; bit 7:0	R/W
SCRCSTART7_H	Addr. 0xDB; bit 7:0	R/W
SCRCSTART8_L	Addr. 0xDE; bit 7:0	R/W
SCRCSTART8_H	Addr. 0xDF; bit 7:0	R/W

Code	CRC start value for single cycle data
0x0000 .. 0xFFFF	SCRSTARTx_HI & CRCSTARTx_LO

Table 36: CRC calculation start value

Each data channel can be enabled to contain actuator data or sensor data. The ACTnSENS parameter defines the functionality of each BiSS slave on the BiSS bus.

ACTnSENS1	Addr. 0xEF; bit 0	R/W
ACTnSENS2	Addr. 0xEF; bit 1	R/W
ACTnSENS3	Addr. 0xEF; bit 2	R/W
ACTnSENS4	Addr. 0xEF; bit 3	R/W
ACTnSENS5	Addr. 0xEF; bit 4	R/W
ACTnSENS6	Addr. 0xEF; bit 5	R/W
ACTnSENS7	Addr. 0xEF; bit 6	R/W
ACTnSENS8	Addr. 0xEF; bit 7	R/W

Code	Function
0	Slave is configured as sensor
1	Slave is configured as actuator

Table 37: Slave functionality control

Typically, a BiSS slave expects a leading stop bit before the actuator data which must be enabled with LSTOP (refer to BiSS Interface PROTOCOL DESCRIPTION).

LSTOP1	Addr. 0xC0; bit 7	R/W
LSTOP2	Addr. 0xC4; bit 7	R/W
LSTOP3	Addr. 0xC8; bit 7	R/W
LSTOP4	Addr. 0xCC; bit 7	R/W
LSTOP5	Addr. 0xD0; bit 7	R/W
LSTOP6	Addr. 0xD4; bit 7	R/W
LSTOP7	Addr. 0xD8; bit 7	R/W
LSTOP8	Addr. 0xDC; bit 7	R/W

Code	Function
0	No leading STOP bit on single cycle actuator data
1	Leading STOP bit on single cycle actuator data

Table 38: Actuator stop bit control

The parameter GRAY activates a GRAY to binary conversion for SSI encoder.

GRAYS1	Addr. 0xC0; bit 7	R/W
GRAYS2	Addr. 0xC4; bit 7	R/W
GRAYS3	Addr. 0xC8; bit 7	R/W
GRAYS4	Addr. 0xCC; bit 7	R/W
GRAYS5	Addr. 0xD0; bit 7	R/W
GRAYS6	Addr. 0xD4; bit 7	R/W
GRAYS7	Addr. 0xD8; bit 7	R/W
GRAYS8	Addr. 0xDC; bit 7	R/W

Code	Function
0	SSI single cycle data binary coded
1	SSI single cycle data GRAY coded

Table 39: SSI format is GRAY code

MASTER CONFIGURATION

System clock

The system clock is either generated by the internal 20 MHz oscillator or by an external clock oscillator connected to the pin CLK.

CLKENI	Addr. 0xF5; bit 0	R/W
Code	Function	
0	External oscillator via pin CLK	
1	Internal oscillator	

Table 40: System clock source

Master Clock MA

The master clock at MA for both BiSS and SSI is generated from the system clock depending on the frequency division register FREQ. With a system clock frequency of 20 MHz, the clock frequency at MA ranges from 10 MHz down to 62.5 kHz.

FREQS	Addr. 0xE6; bit 4:0	R/W
Code	Single cycle data clock frequency (FSCD)	
0x00	f_{CLK} / 2	
0x01 .. 0x0F	f_{CLK} / 2 / (Code + 1)	
0x10	"not permitted"	
0x11	f_{CLK} / 40	
0x12 .. 0x1F	f_{CLK} / 20 / (Code - 15)	

Table 41: Single cycle data clock frequency at MA

Both BiSS and SSI slave devices recognize an idle bus at the end of a transmission frame via timeout detection (see $t_{BiSS\text{-}Timeout}$ in BiSS Interface PROTOCOL DESCRIPTION). Thus, the choice of possible clock frequencies is limited as the duration of each logic level may not exceed the shortest timeout of all the connected slaves.

BiSS B devices switch to register mode when recognizing that the bus is idle after a falling-edge on the clock input MA. The master is notified about entering register mode via data line SL, see item 306 Ttos.

The clock frequency in BiSS B register mode is selected depending on the single cycle data clock frequency via parameter FREQR and is in the range of 244 Hz to 5 MHz. The selection is also limited since a different timeout detection does now recognize the idle bus at the end of the cycle (timeoutREG, see BiSS B protocol).

FREQR	Addr. 0xE6; bit 7:5	R/W
Code	Register data clock frequency	
0	FSCD / 2	
1 .. 6	FSCD / 2 / (Code+1)	
7	FSCD / 256	

Table 42: BiSS B register data frequency

BiSS B devices typically require a minimum clock frequency (such as 250 kHz) because the MA clock possibly has to be evaluated as a PWM signal for register communication. BiSS C devices generally permit a lower clock frequency. BiSS C devices do not use a MA clock duty cycle (PWM signal) and can be operated down to 80 kHz. SSI devices generally permit a lower clock frequency and with extended SSI, the register access is similar to BiSS C and can be operated down to 80 kHz.

BiSS frame rate

The FREQAGS controls the automatic data transmission (AutoGetSens) enabled by the instruction bit AGS (see Table 68). With FREQAGS the frame rate can be set to a dedicated ratio of the system clock frequency f_{CLK}. With a system clock frequency of 20 MHz frame repetition rates from 1 µs to 4 ms are possible. FREQAGS must be set in a way that the time in between two frames is greater than a complete cycle. One cycle consists of the transmission of a request, an acknowledge signal (including line delay), a start bit (including processing time), a control data bit (BiSS C), the sensor data and CRC bits of each slave and the longest BiSS timeout of all connected slaves.

FREQAGS	Addr. 0xE8; bit 7:0	R/W
Code	Register data clock frequency	
0x00	f_{CLK} / 20	
0x00 .. 0x7B	f_{CLK} / 20 / (Code +1)	
0x7C	AGSMIN	
0x7D .. 0x7F	AGSINFINITE	
0x80 .. 0xFF	f_{CLK} / 625 / (Code - 127)	

Table 43: AutoGetSens frequency

AGSMIN

With AGSMIN the master automatically restarts the next frame after the previous frame is finished. If AGSMIN is chosen the iC-MB4 automatically generates the highest frame rate possible. AGSMIN requires complete BiSS frames to ensure a low level at SL at the end of each

frame. The rate depends on the configured sensor data clock frequency, the slave configurations, the longest processing time of the slaves and the total system line delay.

AGSINFINITE
With AGSINFINITE the master does not automatically restart the next cycle. AGSINFINITE requires a trigger event to start the next frame. Possible trigger events are a digital impulse at the GETSENS pin accessing the instruction register (see Table 69).

Data handling
The received and inverted CRC bits are stored at the most significant SCDATA bits (refer to sensor and actuator data, page 25). This can be disabled with the parameter NOCRC = 1.

NOCRC	Addr. 0xE7; bit 1	R/W
Code	Function	
0	CRC of SCD is stored in process data memory	
1	CRC of SCD not stored in process data memory	

Table 44: Storage of received CRC in process data memory

Two RAM banks are available for buffering the SCDATA (refer to sensor and actuator data, page 25). A downgrade is possible with the parameter SINGLEBANK = 1.

SINGLEBANK	Addr. 0xE7; bit 1	R/W
Code	Function	
0	Two RAM banks are used for SCD	
1	One RAM bank is used for SCD	

Table 45: Usage of single RAM bank for SCD

The data output pin MO is used to set the processing time per parameter for all slaves and to send the actuator data. The usage of the the output MO must be enabled with EN_MO = 1.

EN_MO	Addr. 0xE5; bit 1	R/W
Code	Function	
0	Set and keep MO to low state	
1	Data output at MO enabled	

Table 46: Enable data output at MO

The processing time per parameter is set by the delay of the start bit at MO. The delay is configured with MO_BUSY in periods of MA.

MO_BUSY	Addr. 0xE9; bit 7:0	R/W
Code	Start bit delay at MO	
0x00	No start bit delay	
0x01 .. 0x0F	Code * 1 / FSCD	

Table 47: Processing time per parameter

BiSS Master Device Identification
The BiSS master device is identifiable with the two registers VERSION and REVISION. A host software can use VERSION and REVISION to identify the present device and verify the compatibility of the software and the device.

VERSION	Addr. 0xEB; bit 7:0	R
Code	Version	
0x83	iC-MB3	
0x84	iC-MB4	
...	...	
0xFF		

Table 48: iC-MB version

REVISION	Addr. 0xEA; bit 7:0	R
Code	Revision	
0x10	Z(first revision)	
0x11	Z1	
0x20	Y	
...		
0xFF		

Table 49: iC-MB4 redesign ID

The device factory test may not be activated, keep ENTEST = 0.

ENTEST	Addr. 0xF5; bit 1	R/W
Code	Function	
0	Device in normal operation mode	
1	Not permitted	

Table 50: Enable device factory test mode

CONFIGURATION CHANNELS

The iC-MB4 assembled in the QFN28 package provides two options. Option one is a second physical BiSS channel and option two is differential line drivers for each BiSS pin MAx, MOx and SLx. When using two physical channels it is possible to arrange up to eight slaves to one channel or up to four slaves to each of the channels. Therefor the parameter SLAVELOC5 is used to select the locations for the slaves number five to eight.

SLAVELOC5	Addr. 0xEC; bit 4	R/W
Code	Function	
0	Slaves 5-8 are assigned to channel 1	
1	Slaves 5-8 are assigned to channel 2*	

Table 51: Slave location

The protocol for each channel is separately defined with CHSEL.

CFGCH1	Addr. 0xED; bit 1:0	R/W
CFGCH2*	Addr. 0xED; bit 3:2	R/W
Code	Function	
0x00	BiSS B	
0x01	BiSS C	
0x02	SSI	
0x03	Channel is not used (no device connected)	
Notes	In previous MB100 or iC-MB3 data sheets this configuration was applied by the former parameter SELSSI and BISSMOD.	

Table 52: Channel configuration

The physical Interface is configured with CFGIF.

CFGIF	Addr. 0xF5; bit 3:2	R/W
Code	Function	
0x00	TTL	
0x01	CMOS	
0x02	RS422* † ‡	
0x03	LVDS* †	

Table 53: Configure physical interface

* The second BiSS interface channel 2 is only available with iC-MB4 QFN28.
† RS422 and LVDS interfaces are only available with iC-MB4 QFN28.
‡ RS422 interfaces are only operating with VDD = 4.5 V ... 5.5 V.

STATUS INFORMATION

The status registers indicate all states of the master. The status information is combined in a set of register. The status contains the state of the device and communication.

The EOT flag is connected to the pin EOT and signals a running frame see chapter FUNCTIONAL DESCRIPTION on page 21.

EOT	Addr. 0xF0; bit 0	R
Code	Function	
0	Data transmission active	
1	Data transmission not active	

Table 54: End of transmission

An error in the single cycle data detected by checksum verification (CRC) is shown with nSCDERR. If a sensor data error is signaled, the faulty sensor can be verified by reading SVALIDx (see Table 61). The nSCDERR flag is set after power on and after executing INIT (see Table 70).

nSCDERR	Addr. 0xF0; bit 4	R
Code	Function	
0	Error in last single cycle data transmission	
1	No error in last single cycle data transmission	

Table 55: SCD transmission error

The control communication including the register access uses three dedicated flags. The REGEND signals a finished control communication and nREGERR signals the status. A missing start bit is shown with NDELAYERR. The REGEND flag is reset after power on and by starting a new control communication.

REGEND	Addr. 0xF0; bit 2	R
Code	Function	
0	Control communication running or not started since reset	
1	Control communication completed	

Table 56: End of register communication

The nREGERR and the nDELAYERR flags are set after power on and after executing INIT (see Table 70). If a register data error is detected, the number of bytes transmitted correctly before the error occurred is provided by the register message REGBYTES (see Table 63). In case of an error the transmission of data is terminated.

nREGERR	Addr. 0xF0; bit 3	R
Code	Function	
0	Error in last register data transmission	
1	No error in last register data transmission	

Table 57: Register communication error

nDELAYERR	Addr. 0xF0; bit 5	R
Code	Function	
0	Missing start bit in last register data transmission	
1	No error in last register data transmission	

Table 58: Start bit in register communication

An AGS watchdog error nAGSERR is set during the automatic transmission of sensor data enabled by the instruction bit AGS (see Table 68) if no new cycle could be initiated. If the last BiSS frame has not been finished in time, the next BiSS frame will be omitted. The following BiSS frame will be executed if possible. The nAGSERR flag is set when resetting the instruction bit AGS (typically by writing BREAK into the instruction register (see Table 71).

nAGSERR	Addr. 0xF0; bit 6	R
Code	Function	
0	At least one BiSS frame has been omitted	
1	No missing BiSS frames	

Table 59: AGS error

The nERR flag indicates the state of the pin NER. It is possible to connect other components to pin NER using an open collector low active error signal. Additionally the summary of all internal errors is also output to the NER pin.

nERR	Addr. 0xF0; bit 7	R
Code	Function	
0	External or internal error occured	
1	No error occurred	

Table 60: State of the pin NER

The CRC verification result of the received single cycle sensor data of every BiSS frame is written to the validity message register SVALID for each slave separately. If the CRC is disabled in the slave configuration the correspondent SVALID flag is set after the reading of the sensor data is complete. After reading the sensor data, it is recommended to reset the validity flags by writing to the SVALID register. This way, it is possible to recognize updated sensor data.

SVALID1	Addr. 0xF1; bit 1	R/W
SVALID2	Addr. 0xF1; bit 3	R/W
SVALID3	Addr. 0xF1; bit 5	R/W
SVALID4	Addr. 0xF1; bit 7	R/W
SVALID5	Addr. 0xF2; bit 1	R/W
SVALID6	Addr. 0xF2; bit 3	R/W
SVALID7	Addr. 0xF2; bit 5	R/W
SVALID8	Addr. 0xF2; bit 7	R/W
Code	Function	
0	SCD invalid	
1	SCD valid	

Table 61: SCDATAx validity indication

Switching the SCDATA RAM bank which is executed at the end of a BiSS frame does also switch the SVALIDx flags. It fails, if the user disables switching via HOLDBANK in the instruction register (see Table 72). The lastly received data are overwritten. This event is signaled with SWBANKFAILS.

SWBANKFAILS	Addr. 0xFB; bit 0	R
Code	Function	
0	Bank switching (SCD) successful	
1	Bank switching (SCD) not successful	

Table 62: Bank switching status

In case of an error in a sequential register access, the number of faultless transmitted register values are stored in REGBYTES.

REGBYTES	Addr. 0xF3; bit 5:0		R
Code	nREGERR	Number of valid register bytes	
0	1	All	
0x00 .. 0x3F	0	Code	

Table 63: Number of valid register bytes

For BiSS C control communication a minimum number of SCD cycles with exclusively CDM = 0 must be sent before starting a new control communication frame. For a manual control communication by host control the CDMTIMEOUT bit indicates that $\geq$ 14 SCD cycles with exclusively CDM = 0 have already been sent.

CDMTIMEOUT	Addr. 0xF3; bit 7	R
Code	Function	
0	CDMTIMEOUT not reached	
1	CDMTIMEOUT reached	

Table 64: CDM timeout reached

The value of the control data slave bit (CDS) is sampled for each channel in CDS. Additionally, the CDS of the selected channel (refer to Table 21, page 27) is provided by CDSSEL.

CDSSEL	Addr. 0xF3; bit 6	R
Code	CDS value from the selected channel	
0	0	
1	1	

Table 65: CDS bit from the selected channel

CDS1	Addr. 0xF8; bit 1	R
CDS2	Addr. 0xF8; bit 3	R
Code	CDS value from appropriate channel	
0	CDSx = 0	
1	CDSx = 1	

Table 66: CDSx bit of channels

Note: According to SCDATA two banks for SVALID, CDSSEL and CDS exists which switch simultaneous to the SCDATA RAM banks.

The actual state of the BiSS data input is available at SL.

SL1	Addr. 0xF8; bit 0	R
SL2	Addr. 0xF8; bit 2	R
Code	Function	
0	SLx line level low	
1	SLx line level high	

Table 67: SLx input lines state

INSTRUCTION REGISTER

The instruction register controls all functions based on the configuration. Data transmissions are triggered by program, by pin event or automatically. The automatic data transmission is enabled with AGS and the frame rate is set with the parameter FREQAGS (refer to Table 43, page 32).

AGS	Addr. 0xF4; bit 0	R/W
Code	FREQAGS	Function
0		No automatic data transmission
1	AGSMIN	Start of data transmission after TIMEOUTSENS
1	AGSINFINITE	Start of data transmission triggered by pin GETSENS
1	Rest	Start of data transmission equally spaced

Table 68: Automatic Get Sensor Data

The register INSTR can be used to trigger data transmission by program. With AGS = 0 the master starts the data transmission after finishing writing the instruction register (rising edge of NWR on parallel interface, last rising edge of SCLK on SPI interface) and resets INSTR after executing the frame automatically. An nAGSERR error will be generated if the SLx line is low at the start of the frame. The error can be suppressed by setting FREQAGS to AGSMIN due to waiting for a high state at SLx. A BiSS-B register access or a BiSS C control communication (refer to REGVERS, page 27) can be triggered via INSTR as well. Also, it is possible to enable reduced BiSS frames for control communication with broadcast addressing. Within a running control communication the CDM bit is generated automatically otherwise the generation of CDM depends on INSTR according to Table 69.

INSTR	Addr. 0xF4; bit 3:1	R/W
Code	AGS	Function
010	0	Start one frame with CDM = 0. INSTR automatically resets.
010	1	Upcoming frames with CDM = 0.
001	0	Start one frame with CDM = 1. INSTR automatically resets.
001	1	Upcoming frames with CDM = 1.
011	0	Start one frame with CDM = not(CDSSEL). INSTR autom. resets.
011	1	Upcoming frames with CDM = not(CDSSEL).
100	0	Start one frame and start control communication. INST autom. resets.
100	1	Upcoming frames with control communication
111	0	Start one reduced frame and control communication. INST autom. resets.
111	1	Upcoming reduced frames with control communication

Table 69: SCD Control Instruction

Note: With automatic data transmission (AGS = 1) at the end of a control communication INSTR will be reset

Typically, the BiSS data line SLx is set after timeout to digital high by the last slave. After power on or after a failure the last slave may not be defined and the SLx line is digital low. An initialisation sequence started by the instruction bit INIT can be used to initialize the slave chain. Additionally an INIT sets the status bits nSCDERR, nREGERR, nDELAYERR and nAGSERR to 1 an resets REGEND to 0.

INIT	Addr. 0xF4; bit 4	R/W
Code	REGVERS	Function
0	-	No operation
1	0	BiSS-B initialize (see)
1	1	BiSS-C initialize (see)

Table 70: Start initialisation sequence

With an initialisation sequence the iC-MB4 stores the measured channel 1 line delay in the register SCDATA1(7:0) and the channel 2 line delay in the register SCDATA5(7:0).
The unit of these values is 1/4 of the configured MA clock frequency.

$$t_{\text{Line Delay Channel 1}} = \frac{SCDATA1(7:0)}{4 * f_{MA}}$$

$$t_{\text{Line Delay Channel 2}} = \frac{SCDATA5(7:0)}{4 * f_{MA}}$$

For the init sequence the maximum line delay is 255. If exceeding this limit the init sequence is aborted and nAGSERR is reset (see 59). The init sequence does not test the SLx state. A constant SLx = 0 state is ignored and does not set any error state.

All current actions can be aborted using the BREAK command so that the iC-MB4 enters a defined state if one of the sensors does not response correctly.

BREAK	Addr. 0xF4; bit 7	R/W
Code	Function	
0	No operation	
1	Abort data transmission	
Note	An INIT should be executed after BREAK to ensure resetting status bits	

Table 71: Start BREAK Sequence

During reading of more than one sensor data register by the controller it is possible that the RAM banks in the master could be swapped once a sensor data transmission is complete. To avoid unexpected bank swaps, the controller can set HOLDBANK before the read sequence and releases it afterwards.

HOLDBANK	Addr. 0xF4; bit 6	R/W
Code	Function	
0	No bank switching permitted	
1	Bank switching permitted	

Table 72: RAM Bank Control

Every set or reset of the bit SWBANK forces the sensor data banks to be swapped.

SWBANK	Addr. 0xF4; bit 5	R/W
Code	Function	
0	No operation	
1	RAM banks are switched	

Table 73: RAM Bank Switching

The following parameters are used to control the the MA clock line which is selected with the parameter CHSEL (see Table 21).

MAFS	Addr. 0xF5; bit 4	R/W
Code	Function	
0	Selected MA line not controlled	
1	Selected MA line forced with MAVS	

Table 74: Control of the selected MA line

MAVS	Addr. 0xF5; bit 5	R/W
Code	Force value for selected MA	
0	Low	
1	High	

Table 75: Selected MA line force level

The following parameters are used to control the MA clock lines for the remaining channels which are not selected with CHSEL.

MAFO	Addr. 0xF5; bit 6	R/W
Code	Function	
0	Not selected MA lines not controlled	
1	Not selected MA lines forced with MAVO	

Table 76: Control of the not selected MA line

MAVO	Addr. 0xF5; bit 7	R/W
Code	Force value for not selected MA	
0	Low	
1	High	

Table 77: Not selected MA lines force level

GETSENS PIN CONTROL

The pin GETSENS can be used to start a SCD cycle. The default pin state of GETSENS is digital low due to the pull down resistor at this pin. The GETSENS pin operates statically: A digital high at GETSENS will start a SCD cycle. The minimum signal duration at the GETSENS pin is one system clock period. A digital high that is longer than the SCD cycle will restart the next SCD cycle.

For high precision capturing it is recommended to use a system clock based GETSENS digital high pulse.

DESIGN REVIEW

Function Notes

iC-MB4 Z1		
No.	Function, Parameter/Code	Description and application notes
1	**MO_BUSY**	Control communication max fail, if MO_BUSY /= 0 and output MO is **not** connected to slave input SLI.
2	**Actuator data**	Transmission of actuator data on both channels with different SCD length fail, if CDM = 0.
3	**BiSS C initialize sequence**	Line delay measurement fails, if line delay of one channel is bigger than line delay plus timeout of the other channel.

Table 78: Notes on chip functions regarding iC-MB4 chip release Z1.

All listed chip functions are adjusted with iC-MB4 chip release Y.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	14-06-24		Initial Release.	

Rel.	Rel. Date*	Chapter	Modification	Page
B1	14-11-20	PACKAGING INFORMATION	Function text on pin 25 NWR_E swapped with Function text on pin 26 NRD_RNW: • NWR_E: Read Input, active low (Intel) Read/Not-Write Select Input (Motorola) • NRD_RNW: Write Input, active low (Intel) Enable Input, active high (Motorola)	4
		ELECTRICAL CHARACTERISTICS	Vc()hi Clamp Voltage hi MAX updated from 1.65 V to 1.75 V	8
		ELECTRICAL CHARACTERISTICS	f(CLKI) Oscillator Clock Frequency VDD = 3.0 V ... 3.6 V MAX updated from 20 MHz to 22 MHz	9
		FUNCTIONAL DESCRIPTION	INIT = 1 updated	21
		INSTRUCTION REGISTER	”All configuration parameter must be stable during data transmission” added	28
		CONFIGURATION MASTER	AUTOMATIC REQUEST FOR SENSOR DATA moved into chapter CONFIGURATION MASTER	29
		CONFIGURATION CHANNEL	CFGIF footnote added: RS422 interfaces are only operatable with VDD = 4.5 V ... 5.5 V	31
		CONFIGURATION SLAVE	Slave Configuration CRC Verification: • CRC for single cycle data not present, CRC verification deactivated, SELCRCSx = 0b0 • CRC polynomial(7:1) in SCRCPOLYx SELCRCSx = 0b1 not applicable with CRC polynomial SCRCPOLYx(7:1) = 0x00 • CRC polynomial 0x00 not applicable with SELCRCSx = 0b1 • Other CRC lengths in SCRCLENx are not permitted with SELCRCSx = 0b0	32
		STATUS INFORMATION 1	Bit address of nDELAYERR 0xF0 updated to 5	35
		APPLICATION DESIGN TRANSFER FROM iC-MB3 TSSOP24 TO iC-MB4 TSSOP24	Disabling SCD CRC verification To deactivate the SCD CRC verification select: • SELCRCSx = 0b0 • CRC bit length in SCRCLENx = 0 • Extend the SCDLEN by the length of the present CRC that is subject to be ignored A CRC polynomial SCRCPOLYx = 0x00 is not applicable with SELCRCSx = 0b1.	38
		DESIGN REVIEW	Chapter DESIGN REVIEW added	39
		FUNCTIONAL DESCRIPTION	Measuring the line delay on channel 1 and channel 2, measuring unit added	21

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2015-07-07	DESCRIPTION	BiSS BUA added	2
		FUNCTIONAL DESCRIPTION	Maximum line delay while INIT = 255, overflow abort and AGERR is set	21
		INSTRUCTION REGISTER	All configuration parameter must be stable during SCD data transmission	28

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2018-09-11	All	Minor text details updated	all
		ELECTRICAL CHARACTERISTICS	Bxx section: SSI added	8
		ELECTRICAL CHARACTERISTICS	Item D05 updated	9
		ELECTRICAL CHARACTERISTICS	Item C08 added	9
		ELECTRICAL CHARACTERISTICS	Item I008 updated	13
		ELECTRICAL CHARACTERISTICS	Item I110 updated	13
		ELECTRICAL CHARACTERISTICS	Item I207 updated	13
		ELECTRICAL CHARACTERISTICS	Item I506 Ttos permissible timeout (slave) added	17
		REGISTER LAYOUT, OVERVIEW	Existing or missing ” on bit states replaced by ’	18, 19
		INSTRUCTION REGISTER	Note added: an INIT should be executed after BREAK to ensure resetting status bits, Table 71	38
		APPLICATION DESIGN TRANSFER FROM iC-MB3 TSSOP24 TO iC-MB4 TSSOP24	Chapter removed	39

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MB4	TSSOP24	iC-MB4 TSSOP24
iC-MB4	QFN28-5x5	iC-MB4 QFN28-5x5
Evaluation Board		iC-MB4 EVAL MB4_1D