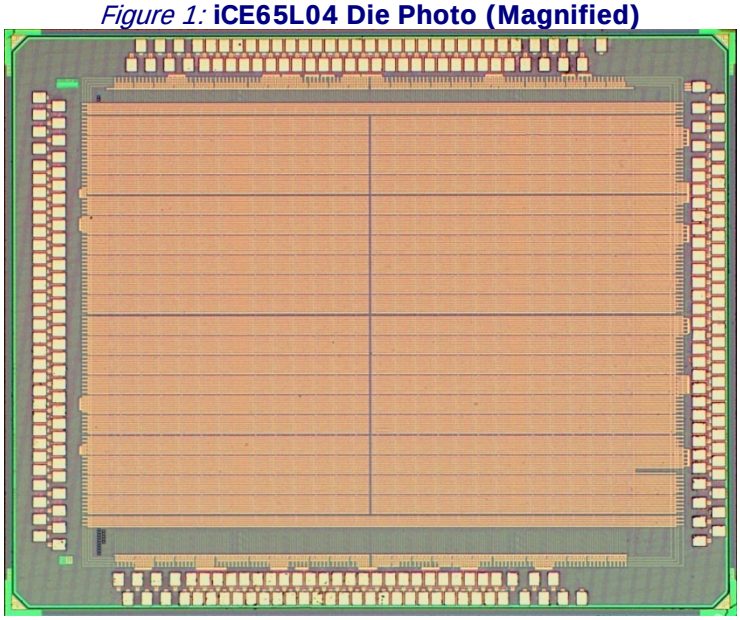
iCE DiCE™: iCE65L04 Ultra Low-Power FPGA Known Good Die

March 23, 2009 (1.5.3) **Preliminary** (SUBJECT TO CHANGE)

Features

- **First ultra low-power programmable logic family specifically designed for hand-held applications and long battery life**
  - Less than 15 µA typical standby current (-U); no special power down modes required
  - Lowest active power consumption of any comparable programmable logic family
  - Lowest heat dissipation on power-sensitive applications
- **Known Good Die (KGD)**
  - Ideal for System-in-Package (SiP), stacked-die, or multi-chip module applications
  - Ideal for Chip on Board (COB) mounting in low-cost consumer products
  - Various temperature range, thickness, and delivery method options
- **Reprogrammable from a variety of sources**
  - Self-loading from secure, internal Nonvolatile Configuration Memory (NVCM)
    - Superior design and intellectual property (IP) protection; no exposed configuration data
    - Single-chip programmable solution
    - Low-cost, high-volume configuration source
  - Self-loading from external, commodity SPI serial Flash PROM
  - Downloaded by processor using SPI-like serial interface
  - **Built on proven, high-volume 65 nm, low-power CMOS technology delivering lowest possible power and cost**

Figure 1: **iCE65L04 Die Photo (Magnified)**



- **Up to 200+ MHz internal performance**
- **Flexible programmable logic and programmable interconnect fabric**
  - Over 3,500K four-input look-up tables (LUT4) and flip-flops
  - Low-power logic and interconnect
- **On-chip, 4Kbit RAM blocks; 20 per device**
- **Flexible I/O blocks to simplify system interfaces**
  - 176 programmable I/O pads
  - Four independently-powered I/O banks support 3.3V, 2.5V, or 1.8V voltage standards
  - Differential LVDS I/O pairs

Table 1: **iCE65 Ultra Low-Power Programmable Logic Family Summary**

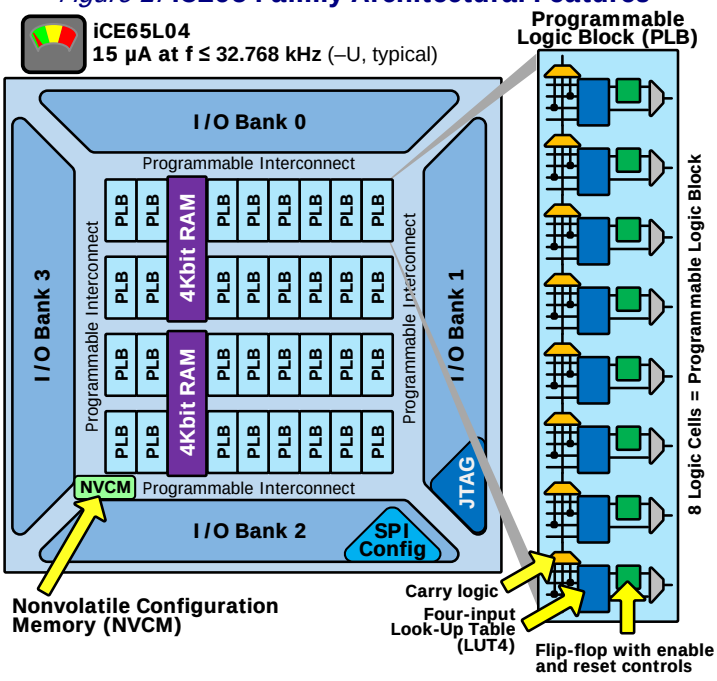
	iCE65L02	iCE65L04	iCE65L08	iCE65L16
Logic Cells (LUT + Flip-Flop)	1,792	3,520	7,680	16,896
Approximate System Gate Count	100K	200K	400K	800K
Typical Equivalent Macrocells	1,400	2,700	6,000	13,000
RAM4K Memory Blocks	16	20	32	96
RAM4K RAM bits	64K	80K	128K	384K
Configuration bits (Kbits maximum)	314 Kb	533 Kb	1,057 Kb	2,404 Kb
Typical Current at ≤ 32.768 kHz (-U)	**8 µA**	**15 µA**	**30 µA**	**75 µA**
Maximum Programmable I/O Pins	128	176	222	384
Maximum Differential Input Pairs	16	20	25	54

Overview

The SiliconBlue Technologies iCE65 programmable logic family is specifically designed to deliver the lowest standby and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 components are available in two versions. The standard product, designed for cost-sensitive, single-program, high-volume applications, provides on-chip, nonvolatile configuration memory (NVCM) to customize the iCE device for a specific application. Both the standard version with NVCM memory and the optional development version without NVCM memory can be self-configured from a program saved in an external commodity SPI serial Flash PROM or downloaded from an external processor over an SPI-like serial port.

The four iCE components, highlighted in Table 1 deliver from approximately 2K to nearly 17K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE device includes between 16 to 96 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

Figure 2: **iCE65 Family Architectural Features**



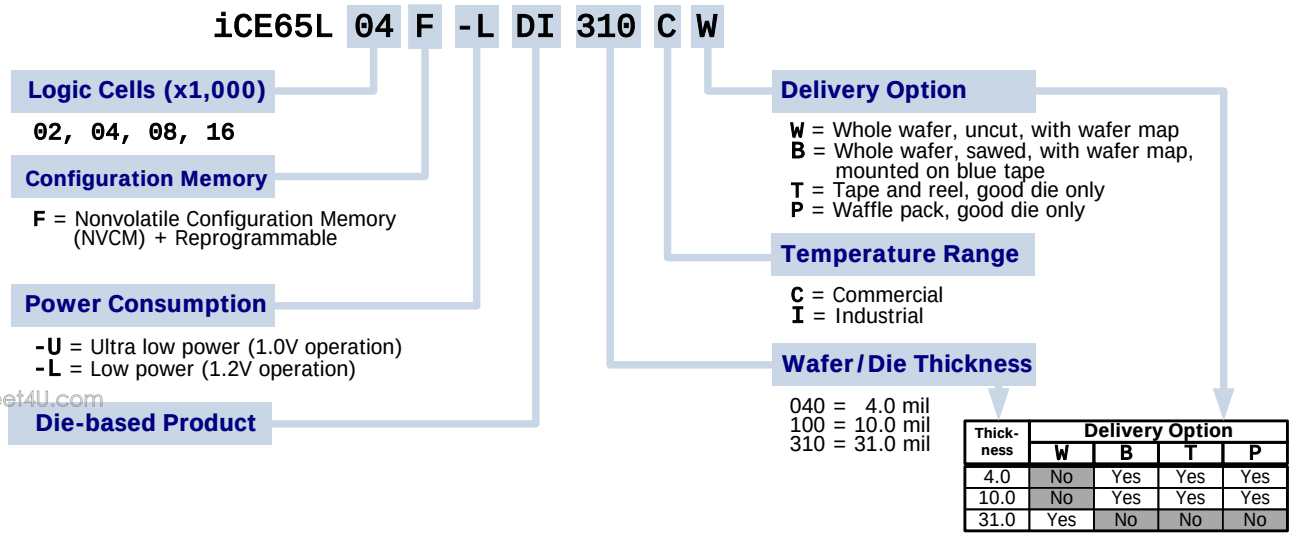
As pictured in Figure 2, each iCE device consists of four primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of ...
    - A fast, four-input look-up table (LUT4) capable of implement any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input, clock-enabled input, and optional set/reset control input to PLB shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Ordering Information

Figure 3 describes the iCE65 die-based product ordering codes.

Figure 3: **iCE65 Ordering Codes**



Thick-ness	Delivery Option			
	W	B	T	P
4.0	No	Yes	Yes	Yes
10.0	No	Yes	Yes	Yes
31.0	Yes	No	No	No

iCE65 devices are available with two power consumption options. Standard products ("**-L**" ordering code) have low standby and dynamic power consumption. The "**-U**" option specifies the ultra low power version.

Please consult the die distributor or SiliconBlue Technologies Corporation before ordering to verify long-term availability of these die products.

Specifications discussed herein are subject to change without notice. This product is sold "as is" and is delivered with no guarantees or warranties, express or implied.

Functional Specifications

Please refer to the packaged product data sheet found on the SiliconBlue Technologies web site (www.siliconbluetech.com) for functional and parametric specifications. The specifications are provided for reference only.

Physical Specifications

Figure 4 shows the physical outlines of iCE65L04 die on a wafer, including pad orientation and physical origin. The bond pad identification and coordinates are provided in Table 3. Table 2 lists key physical characteristics of each iCE65L04 die.

Figure 4: **iCE65L04 Die Outline**

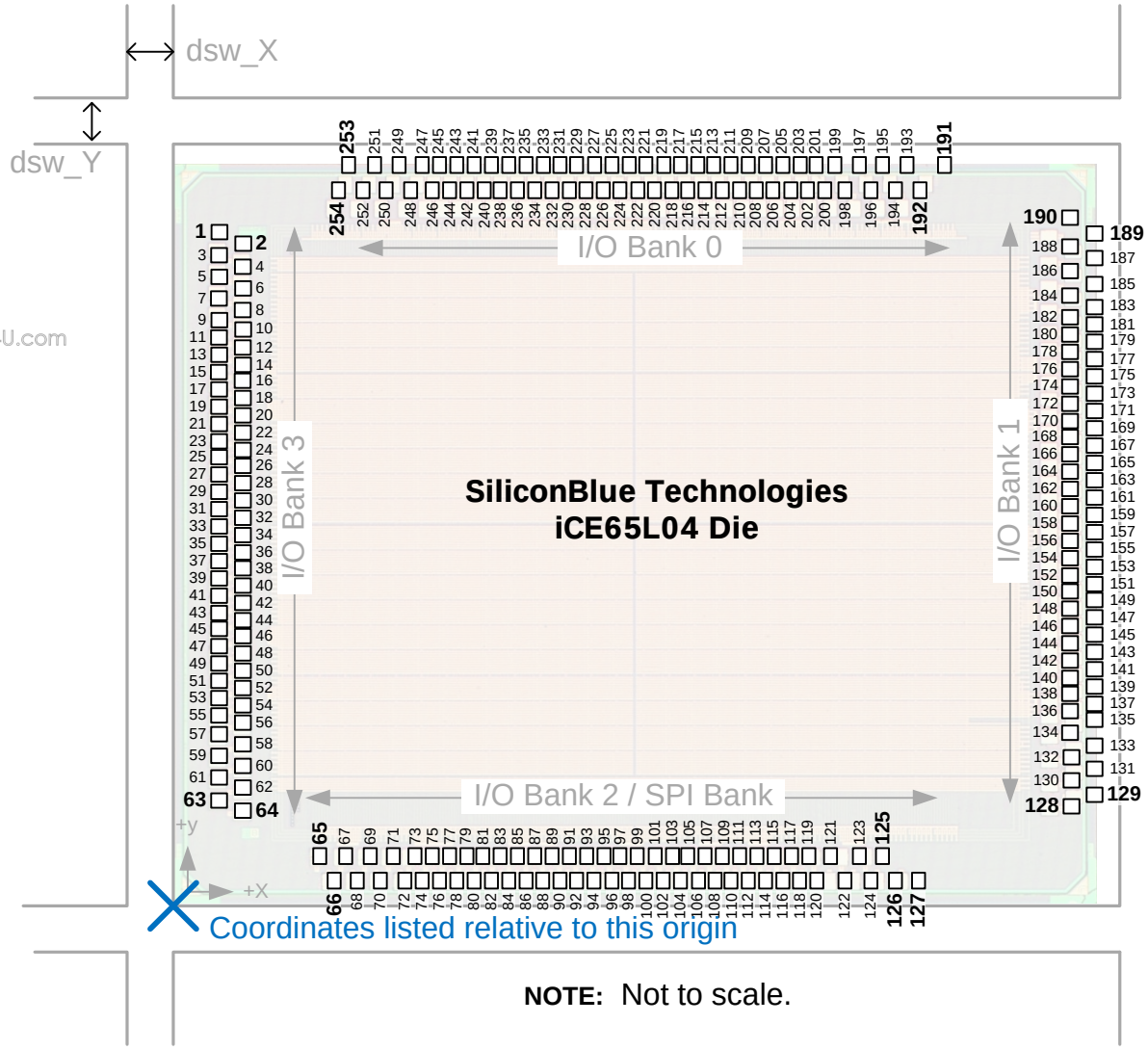


Table 2: **iCE65L04 DiCE Physical Specifications**

Feature	Dimension
Wafer Diameter	300 mm (12 inches)
Wafer Thickness	31 mil, 15 mil, or 10 mil, specified in order code, Figure 3.
Stepping Interval	3,870 µm x 3,200
Scribe Width Along X-Axis (dsw_X)	80 µm
Scribe Width Along Y-Axis (dsw_Y)	160 µm
Bond Pad Size (min)	61 µm x 75 µm
Passivation Openings (min)	58 µm x 72 µm
Minimum Bond Pad Pitch (staggered)	35 µm

Bond Pad Listing and Coordinates

Table 3 lists each of the 254 bonding pads on an iCE65L04 device. The pad number begins in the upper left corner of the die, as shown in Figure 4, and increments in a counter-clockwise direction around the perimeter of the die. . Each bonding pad is identified. Signal names are color-coded by function. I/O pairs are grouped together with a thick surrounding box. These pairs in I/O Bank 3 represent an optional differential input or output. In all other banks, these pairs represent an optional differential output. The pad coordinates are measured relative to the origin, in the lower left corner of the die.

Table 3: **iCE65L04 Bond Pad Listing and Coordinates (Relative to Origin)**

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
1	PIO3_00/DP00A	129.40	2,687.75
2	PIO3_01/DP00B	231.40	2,642.74
3	PIO3_02/DP01A	129.40	2,597.75
4	PIO3_03/DP01B	231.40	2,552.74
5	GND	129.40	2,507.75
6	GND	231.40	2,462.74
7	VCCIO_3	129.40	2,417.75
8	VCCIO_3	231.40	2,372.74
9	PIO3_04/DP02A	129.40	2,327.75
10	PIO3_05/DP02B	231.40	2,292.74
11	PIO3_06/DP03A	129.40	2,257.75
12	PIO3_07/DP03B	231.40	2,222.74
13	VCC	129.40	2,187.75
14	PIO3_08/DP04A	231.40	2,152.74
15	PIO3_09/DP04B	129.40	2,117.75
16	PIO3_10/DP05A	231.40	2,082.74
17	PIO3_11/DP05B	129.40	2,047.75
18	GND	231.40	2,012.74
19	PIO3_12/DP06A	129.40	1,977.75
20	PIO3_13/DP06B	231.40	1,942.74
21	GND	129.40	1,907.75
22	GND	231.40	1,872.74
23	PIO3_14/DP07A	129.40	1,837.75
24	PIO3_15/DP07B	231.40	1,802.74
25	VCCIO_3	129.40	1,767.75
26	VCC	231.40	1,732.74
27	PIO3_16/DP08A	129.40	1,697.75
28	PIO3_17/DP08B	231.40	1,662.74
29	PIO3_18/DP09A	129.40	1,627.75
30	GBIN7/PIO3_19/DP09B	231.40	1,592.74
31	VCCIO_3	129.40	1,557.75
32	VREF	231.40	1,522.74
33	GND	129.40	1,487.75
34	GBIN6/PIO3_20/DP10A	231.40	1,452.74
35	PIO3_21/DP10B	129.40	1,417.75
36	GND	231.40	1,382.74
37	PIO3_22/DP11A	129.40	1,347.75
38	PIO3_23/DP11B	231.40	1,312.74
39	VCCIO_3	129.40	1,277.75
40	VCCIO_3	231.40	1,242.74
41	GND	129.40	1,207.75
42	GND	231.40	1,172.74
43	PIO3_24/DP12A	129.40	1,137.75
44	PIO3_25/DP12B	231.40	1,102.74
45	GND	129.40	1,067.75
46	PIO3_26/DP13A	231.40	1,032.74
47	PIO3_27/DP13B	129.40	997.75
48	PIO3_28/DP14A	231.40	962.74
49	PIO3_29/DP14B	129.40	927.75
50	PIO3_30/DP15A	231.40	892.74
51	PIO3_31/DP15B	129.40	857.75
52	VCC	231.40	822.74
53	PIO3_32/DP16A	129.40	787.75
54	PIO3_33/DP16B	231.40	752.74
55	VCCIO_3	129.40	717.75
56	VCCIO_3	231.40	682.74
57	GND	129.40	637.75
58	GND	231.40	592.74
59	PIO3_34/DP17A	129.40	547.75
60	PIO3_35/DP17B	231.40	502.74
61	PIO3_36/DP18A	129.40	457.75
62	PIO3_37/DP18B	231.40	412.74
63	PIO3_38/DP19A	129.40	367.75
64	PIO3_39/DP19B	231.40	322.74
65	PIO2_00	545.00	139.20
66	PIO2_01	595.00	37.20
67	PIO2_02	645.00	139.20
68	GND	695.00	37.20
69	PIO2_03	745.00	139.20
70	PIO2_04	795.00	37.20
71	PIO2_05	845.00	139.20
72	PIO2_06	895.00	37.20
73	PIO2_07	930.00	139.20
74	PIO2_08	965.00	37.20
75	VCCIO_2	1,000.00	139.20
76	PIO2_09	1,035.00	37.20

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
77	PIO2_10	1,070.00	139.20
78	GND	1,105.00	37.20
79	PIO2_11	1,140.00	139.20
80	PIO2_12	1,175.00	37.20
81	PIO2_13	1,210.00	139.20
82	PIO2_14	1,245.00	37.20
83	PIO2_15	1,280.00	139.20
84	PIO2_16	1,315.00	37.20
85	PIO2_17	1,350.00	139.20
86	PIO2_18	1,385.00	37.20
87	GND	1,420.00	139.20
88	PIO2_19	1,455.00	37.20
89	PIO2_20	1,490.00	139.20
90	VCC	1,525.00	37.20
91	PIO2_21	1,560.00	139.20
92	PIO2_22	1,595.00	37.20
93	GBIN5/PIO2_23	1,630.00	139.20
94	GBIN4/PIO2_24	1,665.00	37.20
95	PIO2_25	1,700.00	139.20
96	VCCIO_2	1,735.00	37.20
97	PIO2_26	1,770.00	139.20
98	PIO2_27	1,805.00	37.20
99	GND	1,840.00	139.20
100	PIO2_28	1,875.00	37.20
101	PIO2_29	1,910.00	139.20
102	PIO2_30	1,945.00	37.20
103	PIO2_31	1,980.00	139.20
104	PIO2_32	2,015.00	37.20
105	PIO2_33	2,050.00	139.20
106	PIO2_34	2,085.00	37.20
107	PIO2_35	2,120.00	139.20
108	VCC	2,155.00	37.20
109	VCC	2,190.00	139.20
110	PIO2_36	2,225.00	37.20
111	PIO2_37	2,260.00	139.20
112	VCCIO_2	2,295.00	37.20
113	PIO2_38	2,330.00	139.20
114	GND	2,365.00	37.20
115	PIO2_39	2,400.00	139.20
116	PIO2_40	2,435.00	37.20
117	PIO2_41	2,470.00	139.20
118	PIO2_42/CBSEL0	2,505.00	37.20
119	PIO2_43/CBSEL1	2,540.00	139.20
120	CDONE	2,575.00	37.20
121	CRESET_B	2,625.00	139.20
122	PIOS_00/SPI_SO	2,690.00	37.20
123	PIOS_01/SPI_SI	2,740.00	139.20
124	GND	2,790.00	37.20
125	PIOS_02/SPI_SCK	2,840.00	139.20
126	PIOS_03/SPI_SS_B	2,890.00	37.20
127	SPI_VCC	2,990.00	37.20
128	TDI	3,610.80	342.00
129	TMS	3,712.80	392.00
130	TCK	3,610.80	442.00
131	TDO	3,712.80	492.00
132	TRST_B	3,610.80	542.00
133	PIO1_00	3,712.80	592.00
134	PIO1_01	3,610.80	642.00
135	PIO1_02	3,712.80	692.00
136	PIO1_03	3,610.80	727.00
137	GND	3,712.80	762.00
138	GND	3,610.80	797.00
139	PIO1_04	3,712.80	832.00
140	PIO1_05	3,610.80	867.00
141	VCCIO_1	3,712.80	902.00
142	VCCIO_1	3,610.80	937.00
143	PIO1_06	3,712.80	972.00
144	PIO1_07	3,610.80	1,007.00
145	PIO1_08	3,712.80	1,042.00
146	PIO1_09	3,610.80	1,077.00
147	PIO1_10	3,712.80	1,112.00
148	VCC	3,610.80	1,147.00
149	VCC	3,712.80	1,182.00
150	PIO1_11	3,610.80	1,217.00
151	PIO1_12	3,712.80	1,252.00
152	PIO1_13	3,610.80	1,287.00
153	PIO1_14	3,712.80	1,322.00
154	PIO1_15	3,610.80	1,357.00
155	PIO1_16	3,712.80	1,392.00
156	PIO1_17	3,610.80	1,427.00
157	GND	3,712.80	1,462.00
158	GND	3,610.80	1,497.00
159	PIO1_18	3,712.80	1,532.00
160	GBIN3/PIO1_19	3,610.80	1,567.00
161	GBIN2/PIO1_20	3,712.80	1,602.00
162	PIO1_21	3,610.80	1,637.00
163	VCCIO_1	3,712.80	1,672.00
164	VCCIO_1	3,610.80	1,707.00
165	PIO1_22	3,712.80	1,742.00
166	PIO1_23	3,610.80	1,777.00
167	PIO1_24	3,712.80	1,812.00
168	PIO1_25	3,610.80	1,847.00
169	PIO1_26	3,712.80	1,882.00
170	PIO1_27	3,610.80	1,917.00

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
171	GND	3,712.80	1,952.00
172	GND	3,610.80	1,987.00
173	PIO1_28	3,712.80	2,022.00
174	PIO1_29	3,610.80	2,057.00
175	PIO1_30	3,712.80	2,092.00
176	PIO1_31	3,610.80	2,127.00
177	VCC	3,712.80	2,162.00
178	VCC	3,610.80	2,197.00
179	PIO1_32	3,712.80	2,232.00
180	PIO1_33	3,610.80	2,267.00
181	VCCIO_1	3,712.80	2,302.00
182	VCCIO_1	3,610.80	2,337.00
183	PIO1_34	3,712.80	2,377.00
184	PIO1_35	3,610.80	2,427.00
185	GND	3,712.80	2,477.00
186	PIO1_36	3,610.80	2,527.00
187	PIO1_37	3,712.80	2,577.00
188	PIO1_38	3,610.80	2,627.00
189	PIO1_39	3,712.80	2,677.00
190	VPP_2V5	3,610.80	2,739.68
191	VPP_FAST	3,097.00	2,962.80
192	VCC	2,997.00	2,860.80
193	VCC	2,947.00	2,962.80
194	PIO0_00	2,897.00	2,860.80
195	PIO0_01	2,847.00	2,962.80
196	PIO0_02	2,797.00	2,860.80
197	PIO0_03	2,747.00	2,962.80
198	PIO0_04	2,697.00	2,860.80
199	PIO0_05	2,647.00	2,962.80
200	PIO0_06	2,612.00	2,860.80
201	PIO0_07	2,577.00	2,962.80
202	GND	2,542.00	2,860.80
203	GND	2,507.00	2,962.80
204	PIO0_08	2,472.00	2,860.80
205	PIO0_09	2,437.00	2,962.80
206	PIO0_10	2,402.00	2,860.80
207	PIO0_11	2,367.00	2,962.80
208	PIO0_12	2,332.00	2,860.80
209	PIO0_13	2,297.00	2,962.80
210	PIO0_14	2,262.00	2,860.80
211	PIO0_15	2,227.00	2,962.80
212	VCCIO_0	2,192.00	2,860.80
213	VCCIO_0	2,157.00	2,962.80
214	PIO0_16	2,122.00	2,860.80
215	PIO0_17	2,087.00	2,962.80

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
216	PIO0_18	2,052.00	2,860.80
217	PIO0_19	2,017.00	2,962.80
218	PIO0_20	1,982.00	2,860.80
219	PIO0_21	1,947.00	2,962.80
220	PIO0_22	1,912.00	2,860.80
221	GBIN1/PIO0_23	1,877.00	2,962.80
222	GND	1,842.00	2,860.80
223	GND	1,807.00	2,962.80
224	GBIN0/PIO0_24	1,772.00	2,860.80
225	PIO0_25	1,737.00	2,962.80
226	PIO0_26	1,702.00	2,860.80
227	PIO0_27	1,667.00	2,962.80
228	VCC	1,632.00	2,860.80
229	VCC	1,597.00	2,962.80
230	PIO0_28	1,562.00	2,860.80
231	PIO0_29	1,527.00	2,962.80
232	PIO0_30	1,492.00	2,860.80
233	PIO0_31	1,457.00	2,962.80
234	GND	1,422.00	2,860.80
235	GND	1,387.00	2,962.80
236	PIO0_32	1,352.00	2,860.80
237	PIO0_33	1,317.00	2,962.80
238	PIO0_34	1,282.00	2,860.80
239	PIO0_35	1,247.00	2,962.80
240	PIO0_36	1,212.00	2,860.80
241	VCCIO_0	1,177.00	2,962.80
242	VCCIO_0	1,142.00	2,860.80
243	PIO0_37	1,107.00	2,962.80
244	PIO0_38	1,072.00	2,860.80
245	PIO0_39	1,037.00	2,962.80
246	PIO0_40	1,002.00	2,860.80
247	PIO0_41	967.00	2,962.80
248	PIO0_42	917.00	2,860.80
249	GND	867.00	2,962.80
250	PIO0_43	817.00	2,860.80
251	PIO0_44	767.00	2,962.80
252	PIO0_45	717.00	2,860.80
253	PIO0_46	667.00	2,962.80
254	PIO0_47	617.00	2,860.80

Die Testing Procedures

SiliconBlue Technologies die products are tested to ensure product functionality in our standard package. Each die has gone through wafer probe test of various functional and parametric conditions.

SiliconBlue Technologies retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. SiliconBlue Technologies reserves the right to change the probe program at any time for continuous product improvement.

Die users may experience differences in performance relative to SiliconBlue Technologies' data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing QRA reliability evaluations. From these evaluations, samples are subjected to a battery of tests known as "Accelerated Life and Environmental Stress Tests." During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Storage Requirements

SiliconBlue Technologies' die products are packaged in a cleanroom environment for shipping. Upon receipt, transfer the die or wafers to a similar environment for storage. SiliconBlue Technologies recommends that the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

SiliconBlue®

SiliconBlue Technologies Corporation

3255 Scott Blvd.
Building 7, Suite 101
Santa Clara, California 95054
United States of America

Tel: +1 408-530-8800
Fax: +1 408-530-0177

www.SiliconBlueTech.com