iP7300

功率因素校正控制芯片

1. Description

iP7300 为一峰值电流模式功率因素控制芯片(具过渡电流启动)。此芯片用于升压电路上的整流二极管之后，输入电流的波形跟随输入电压波形改变。
iP7300 内部有一个 18v 的稳压管作钳位，VDD 的操作范围极宽。关闭功能设于一号引脚。软驱动的延迟功能有助于波谷电压切换并且能够使启动电流尖峰最小化，因此也可以实现更高的效率。
由于 iP7300 comp 引脚之最大电压为 4V，为维持足够的动态范围，comp (引脚 2)的参考值降低为 1.2V。
iP7300 使用小型 SOP-8 封装，且与其它外部的零件搭配使用极为方便。此芯片有具有低电压保护 (UVLO)以及极小起动电流。

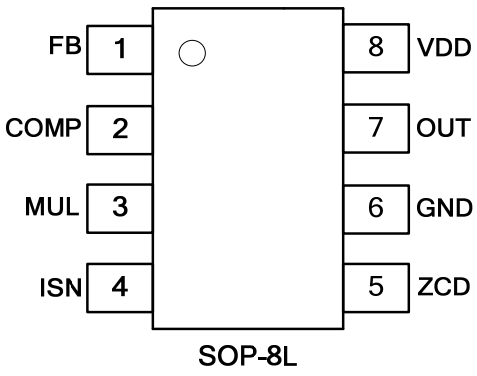
2. 芯片特色

- 极宽 VDD 操作范围，内部输出限制电压值为 18V
- 低电压保护及低待机电流
- 可降低启动电流突波的软驱动功能
- 零电流的电压波谷切换功能
- 低操作电流
- SOP-8 封装，只需少数外部零件
- 高功因值以及低 THD

3. 应用领域

- 镇流器
- 电源供应器

4. 引脚外观



SOP-8L

5. 外观打印方式

产品名称	打印
iP7300	iP7300 XXXXX X : Date Code

6. 订购信息编码

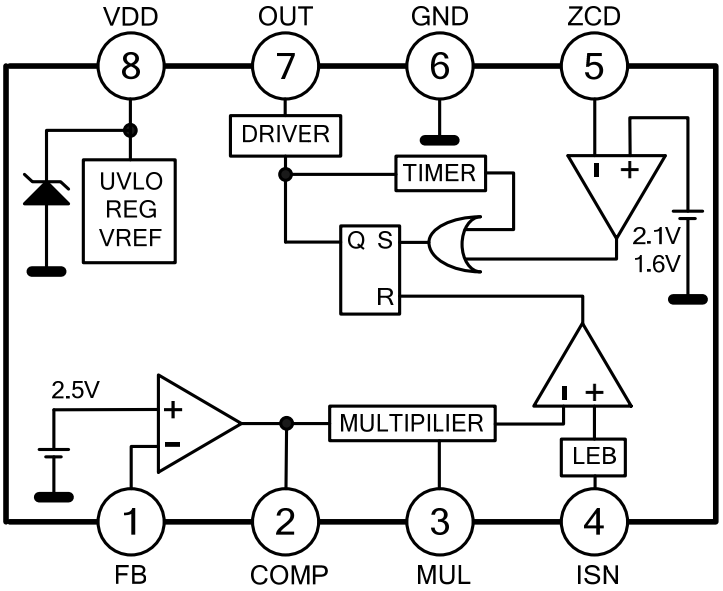
iP7300 □ └── Assembly Material	Assembly Material G: Halogen and Lead Free Device

Note: inergy defines “Green” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight ; Follow IEC 61249-2-21 and IPC/JEDEC J-STD-020C)

7. 引脚定义

脚位	名称	说明
1	FB	差动放大器的反向输入引脚。将电阻分压连接在COMP引脚及此引脚，以提供电压反馈讯号
2	COMP	差动放大器输出引脚。将反馈补偿置于FB引脚及此引脚
3	MUL	乘法器输入引脚。将电阻分压连接在整流二极管及此引脚，以提供正弦波电压参考讯号给乘法器
4	ISN	PWM 比较器输入引脚。藉由连接在MOSFET 的电流侦测电阻提供此引脚电压讯号
5	ZCD	升压电感的去磁讯号侦测输入引脚，用以临介导通模式。负端触发MOSFET导通。
6	GND	接地引脚
7	OUT	MOS 组件闸极驱动输出引脚
8	VDD	驱动及控制电路电源引脚

8. 电路方块图



9. 绝对操作范围

Parameter	Symbol	Value	Unit
Supply voltage	VDD	20	V
Maximum voltage on FB, COMP, MUL, ISN, ZCD	V	- 0.3 ~ 6	V
ESD capability, HBM model	V	2.0	kV
ESD capability, MM model	V	200	V

10. 热阻及功率

Parameter	Symbol	Value	Unit
Maximum junction temperature	T_{jmax}	150	ºC
Operating junction temperature	T_j	- 40 ~ 150	ºC
Storage temperature	T_{STG}	- 60 to 150	ºC
Thermal Resistance, Junction-to-ambient	$R_{th\ j\text{-}amb}$	150	ºC/W

11. 标准电气特性数值

(VDD = 15 V, for typical values T_J = 25 ºC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE SECTION						
Operating Range	VDD	after turn-on	10.5	-	17.5	V
Turn-on Threshold	VDD on		10.5	11.5	12.5	V
Turn-off Threshold	VDD off		8.5	9.5	10.5	V
On/Off Hysteresis	Hys		1.8	2	2.2	V
SUPPLY CURRENT SECTION						
Start-up Current	IDD_{st}	before turn-on (VDD = 11 V)	-	16	-	uA
Quiescent Current	Iq		-	0.8	-	mA
Operating Current	IDD_{op}	PWM loaded, f = 20kHz, C = 1nF	-	3.6	-	mA
ERROR AMPLIFIER SECTION						
Input Bias Current	I_{FB}		-	-	1	uA
Input Reference Voltage	Vref		2.45	2.5	2.55	V
Line Regulation		VDD = 12 to 18 V	-	2	5	mV
Voltage Gain	Gv	Open loop	-	80	-	dB
Bandwidth	GB		-	1	-	MHz
Source Current	I_{COMP}	V_{COMP} = 4V, V_{FB} = 2.4 V	0.6	1	1.6	mA
Sink Current		V_{COMP} = 4V, V_{FB} = 2.6 V	1.4	2.8	4.2	mA
Upper Clamp Voltage	V_{COMP}	Isource = 0.2 mA	-	3.9	-	V
MULTIPLIER SECTION						
Input Bias Current	I_{MUL}		-	-	1	uA
Linear Operation Voltage	V_{MUL}		0 to 4	-	0 to 4.5	V
Gain	K	V_{MUL} = 1 V V_{COMP} = 3 V	0.45	0.5	0.55	1/V
ZERO CURRENT DETECTOR						
Input Bias Current	I_{ZCD}		-	-	1	uA
Zero Current Detect	V_{ZCD}	Negative slope	-	1.6	-	V
Zero Current Detect Hysteresis	V_H		-	0.5	-	V
Delay To Turn On	t_{ZCD}		-	400	-	ns
Upper Clamp Voltage	V_{ZCD}	I_{ZCD} = 20 uA	-	4.8	-	V
Upper Clamp Voltage	V_{ZCD}	I_{ZCD} = 3 mA	-	5.9	-	V
Lower Clamp Voltage	V_{ZCD}	I_{ZCD} = -3 mA	-	0.2	-	V
Input Capacitance	C_{par}	V_{ZCD} = 1.0 V	-	10	-	pF
Maximum Off Time	t_{OFF}		80	160	320	us

标准电气特性数值(续)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE COMPARATOR						
Input Bias Current	I_{CS}		-	-	1	uA
Delay To Turn Off	t_{delay}		-	250	450	ns
LEB	t_{LEB}		-	380	-	ns
Current Sense Limit	V_{limit}	V_{COMP} = Upper Clamp	1.7	1.8	1.9	V
OUTPUT SECTION						
Output Clamp	Vo_clamp		-	18	-	V
Dropout Voltage	V_{GD}	IGDsource = 200 mA	-	3.4	-	V
		IGDsource = 20 mA	-	0.8	-	V
		IGDsink = 200 mA	-	2.8	-	V
		IGDsink = 20 mA	-	0.3	-	V
PROTECTION SECTION						
V_{COMP} Dynamic OVP	I_{OVP}		28	40	52	uA
V_{COMP} Static OVP	V_{OVP}		0.9	1.0	1.1	V
V_{FB} Disable Threshold	Vdis		-	0.5	-	V

12. 标准电气特性图形

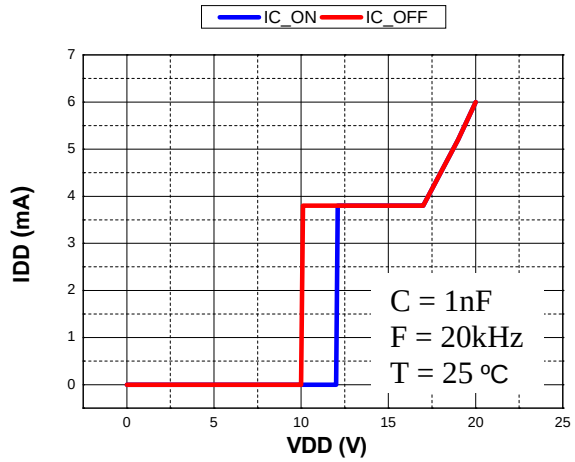


Figure 1. IDD vs. VDD_ON/OFF Voltage

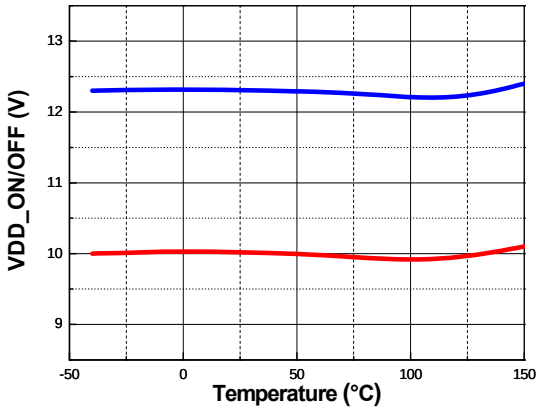


Figure 2. VDD_ON/OFF Voltage vs. Ambient Temperature

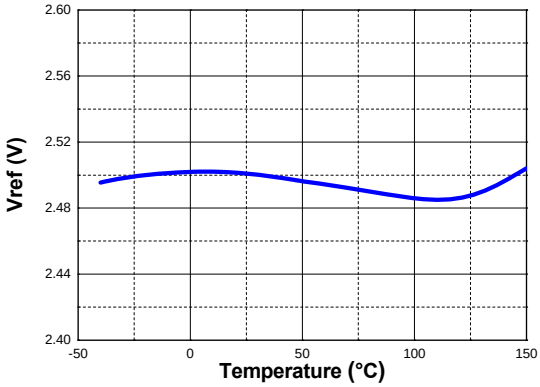


Figure 3. Voltage Feedback Input Threshold vs. Ambient Temperature

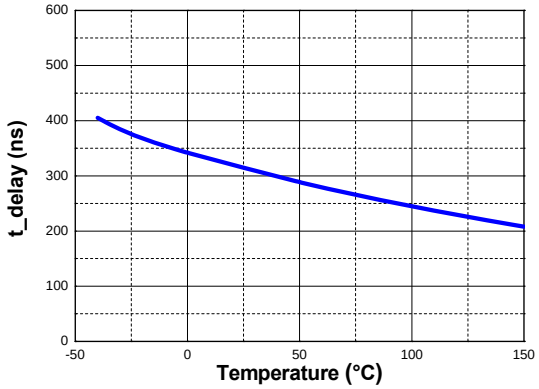


Figure 4. Delay To Turn Off vs. Ambient Temperature

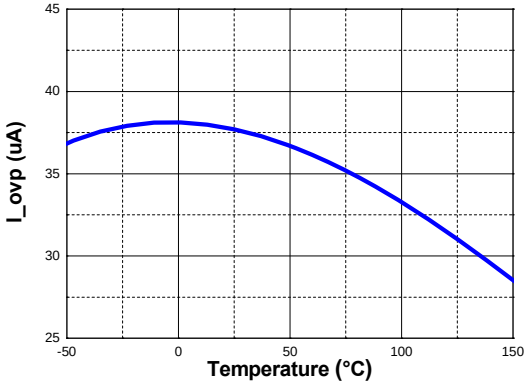


Figure 5. OVP Current Threshold vs. Ambient Temperature

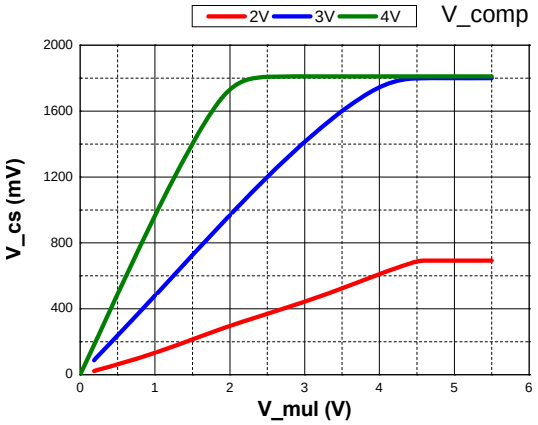
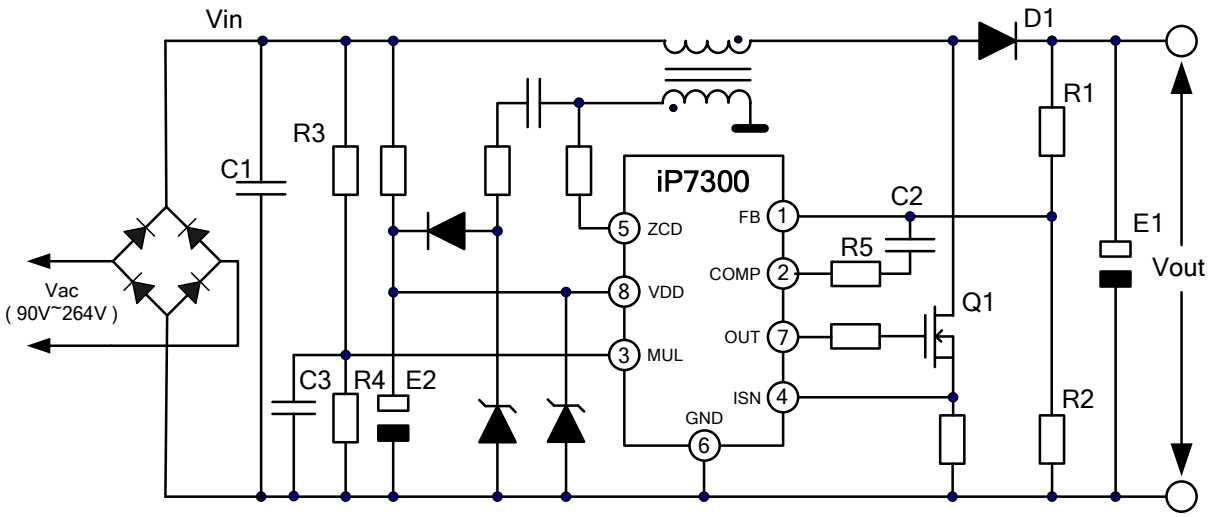


Figure 6. Multiplier Characteristics Family

13. 应用电路及功能叙述

13.1 Typical application circuit



Suggesting Value: R3 = 1.5MΩ, R4 = 18KΩ

a. Power supply

Power is supplied between VDD and GND pin. At VDD below UVLO off, IC is in Under Voltage Lock Out (UVLO) state. The IC does not operate and consumes very low current at this situation. As voltage increases above UVLO on, the IC starts to operate. During this time, IC power is provided by E2 capacitor, so its voltage decreases. Before the voltage drops to UVLO off, since some auxiliary power provides continuous power, the IC continues to operate. However, if the voltage drops below UVLO off, it enters UVLO state.

b. PWM

During operation, if the iP7300 is off for more than t_{OFF}, an internal timer triggers the output on. It happens at very beginning. The output drives the external MOSFET(Q1) on, and hence the current passes through inductor, Q1 increases with di/dt = Vin/L, and the voltage across secondary winding of inductor becomes negative.

The current is sensed through ISN pin by detecting voltage across a sense resistor. If the current exceeds target values, output is turned off. As the current through inductor must be continuous, so it flows through boost diode (D1) to output capacitor(E1). Voltage of E1 is always higher than that of input, so the current is decreasing with di/dt = -(Vout – Vin)/L, and the voltage across sensed by ZCD pin secondary winding of inductor becomes positive.

Re-turn on is initiated by two mechanism: maximum off time and zero current detection(ZCD). As the current decreases to zero, the diode is off, and the drain voltage of Q1 is oscillating about Vin. As it swings through Vin, the secondary winding voltage swings through zero. When it swings across 1.6 V, ZCD trigger the output on. This process is repeated as PWM switching.

c. Current shaping

For transition conduction mode, current always start from zero when Q1 is on; Q1 is off when current reaches a target value that follows the input voltage. As Q1 is turn off, the current is diverted to output capacitor and decreasing. The input current looks like a triangle, and its peak follows input voltage.

Therefore, if the current ripple at switching frequency is filtered (using C1), the average input current, which is half of its peak, would look like the input sinusoidal voltage. High power factor and low total Harmonics Distortion (THD) could be achieved.

d. Feedback output control

As current is pumped in E1, output voltage, Vout, sensed through resistor divider (R1,R2) to FB pin increases. A capacitor-resistor (C2-R5) compensator is between FB and Comp pins, which constitutes an error amplifier for output voltage controller. The controller's output governs the amplitude of target input current. Its form is referred to input voltage, which is sensed by Mul pin, through resistor divider (R3, R4). This combination is accomplished through internal analog multiplier.

The input current by purpose is proportional to sinusoidal input voltage. The output power is pulsating twice line frequency, as $\cos^2 \omega t = \left(1+\cos 2\omega t\right)/2$, and that is also for output current. The constant term should match to load current, and the integration of sinusoidal current error becomes output voltage error, which is inversely proportional to E1.

The comp output should resemble Vin voltage to produce target input current. In order to compensate, the capacitor should be large enough to achieve the integration time which is larger than the line period, 16ms for 60Hz or 20ms for 50Hz. Since the voltage error of output capacitor E1 is integral of current error, if controller is pure integrator, the controller occurs 180 degree phase delay that leads to instability. Therefore, a resistor (R5) is put in series to add proportional factor for controller. This would speed up controller and the phase is decreases. But it distorts the output comp voltage from quasi dc signal. Therefore, proportional control should not be too large since this signal is proportional to output error signal, which always exist for finite E1.

e. Output over voltage protection

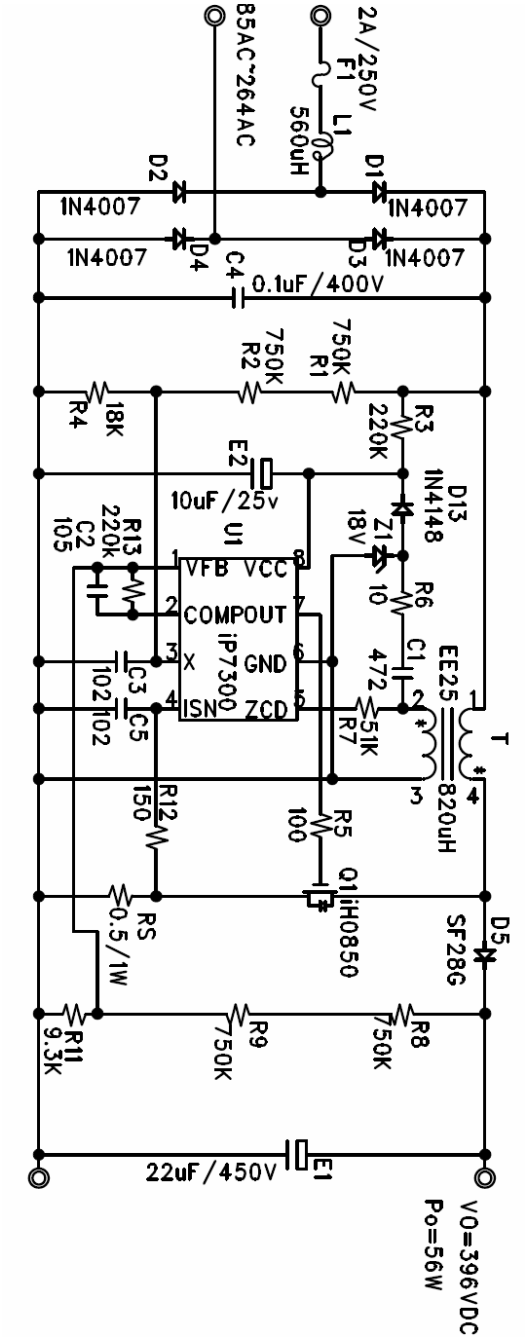
On this structure, the FB pin is kept 2.5V. Since input is resistor, so output error may be detected by the current output of error amplifier. When sink current at comp pin is detected higher than 40uA, OVP protection is triggered. 40 uA x R1 corresponds to output error limit.

The other feature is static OVP. It works as comp decreases below zero output reference point, 1.0V. When this happens, output is off.

In case output voltage sense resistor is open, the protection should be triggered. When lower resistor is open, the FB sees high signal. The controller inherently decreases it output to zero. When upper resistor is open, the FB see low signal below shutdown threshold. Under that situation, IC would be shutdown.

14. 参考应用电路

14.1 400V/65W (85 ~ 265V_{AC})

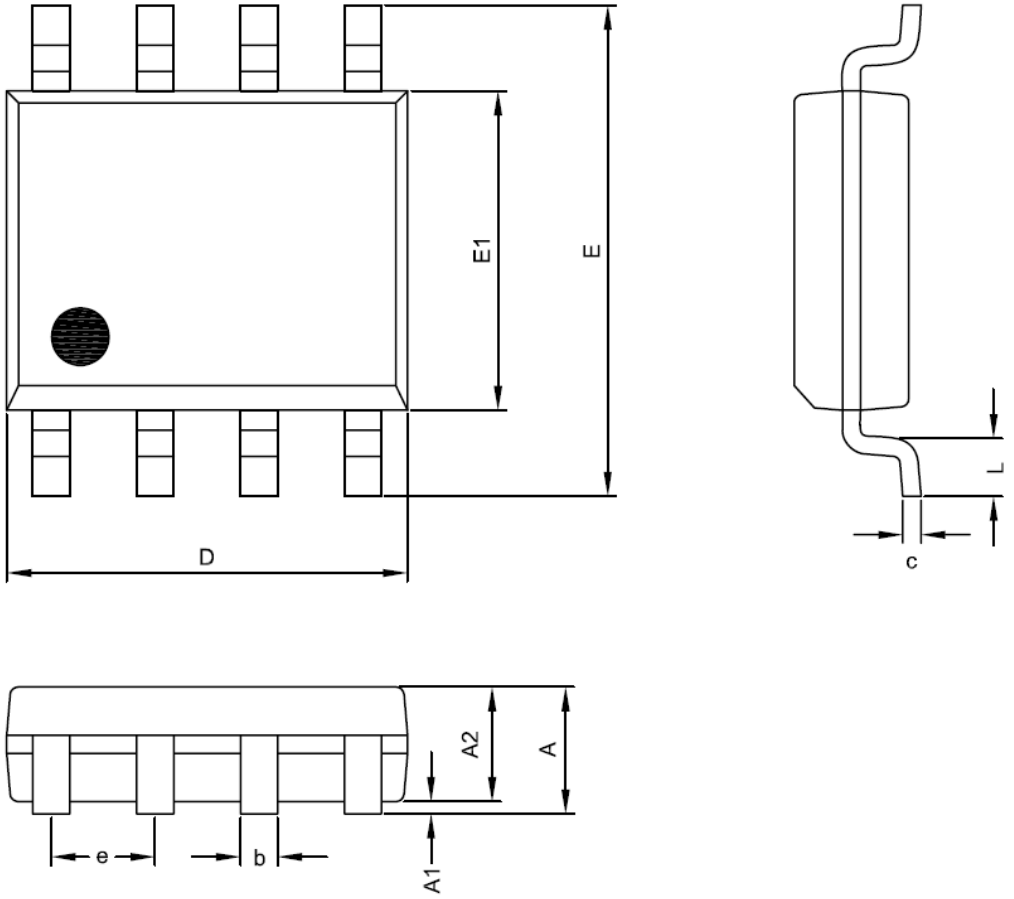


14.2 BOM

Item	PCB DECAL	Value
C1	S0805	103
C2	S0805	105
C3.C5	S0805	102
C4	DIP	0.1uF/400V
D1-4	DIP	1N4007
D5	DIP	SF28G
D13	SD1	1N4148
E1	DIP	22F/450V
E2	DIP	10uF/25V
F1	DIP	2A/250V
L1	DIP	560uH
Q1	TO220V (DIP)	iH0850
U1	SO8	iP7300
R1-2	S0805	750K
R3	S1206	220K
R5-6	S0805	100
R7	S0805	51K
R8	S0805	750K
R4	S0805	18K
R9	S0805	750K
R10	R5	0.5/1W
R11	S0805	9.3K
R12	S0805	150
R13	S0805	220K
T	EI25/8-4	820uH
Z1	SZ1	18V

15. 封装信息

SOP- 8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes：

1. Jedec outline ： MS-012AA
2. Dimensions ” D ” does not include mold flash, protrusions and gate burrs shall not exceed 15 mm (.006 in) per side .
3. Dimensions “ E1 ” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.