iT2002
2 to 26.5 GHz
Dual-Channel, High-Power Amplifier
(Preliminary Information)

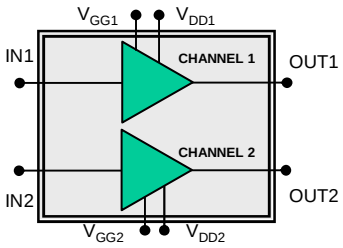
Description

The iT2002 is dual-channel broadband GaAs MMIC traveling-wave amplifier designed for applications requiring high output power. The iT2002 provides a saturated output power of 1 W per channel up to 10 GHz and greater than 28.5 dBm up to 20 GHz. Medium gain of 10 dB with flatness of +/-1dB is provided up to 26.5 GHz. DC power consumption as low as 2.7 W per channel is obtained in bias condition for best output power and good linear performance. Input and output ports are DC coupled.

Features

(Power output is per channel)

- Frequency range: 2 to 26.5 GHz
- Psat (2 to 7 GHz): 30 dBm
- Psat (7 to 15 GHz): 29 dBm
- Psat at 26.5 GHz: 25 dBm
- Gain with +/-1dB flatness: 10 dB
- DC power consumption: 2.7 W
- DC bias conditions: 9 V at 300 mA
- Full chip passivation for high reliability



Absolute Maximum Ratings

(per channel)

Symbol	Parameters/conditions	Min.	Max.	Units
$V_{DD1,2}$	Positive supply voltage		11	V
$V_{GG1,2}$	Negative supply voltage	-2	0	V
$I_{DQ}1,2$	Positive supply current		800	mA
$I_{G1,2}$	Negative supply current		1.6	mA
Pin	RF input power		27	dBm
Pdiss_DC	DC power dissipation (no RF)		5	W
Tch	Operating channel temperature		150	℃
Tm	Mounting temperature (30 s)		320	℃
Tst	Storage temperature	-65	150	℃

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tb	Operating temperature range (backside)	-40		85	°C
$V_{DD1,2}$	Positive bias supply			9	V
$V_{GG1,2}$	Negative bias supply	-0.4	-0.6	-0.9	V
$I_{DQ1,2}$	DC supply drain current		300	400	mA

Electrical Characteristics

(per channel)

(at 25 ℃)
50 ohm system
V_{DD} = +9 V
Quiescent current (I_{DQ}) = 300 mA

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	Frequency range	2		26.5	GHz
S21	Small signal gain	7	10		dB
	Gain flatness		+/-1		dB
S11	Input return loss	8	10		dB
S22	Output return loss	8	10		dB
S12	Isolation	30			dB
Psat	Saturated output power at 3-dB gain compression				
	2 - 10 GHz	27.5	29.5		dBm
	2 - 20 GHz	26.5	28.5		dBm
	2 - 26.5 GHz	23	25		dBm
P_{1dB}	Output power at 1-dB gain compression				
	2 - 10 GHz	27	29		dBm
	2 - 20 GHz	26	28		dBm
	2 - 26.5 GHz	22.5	24.5		dBm

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Thermal Characteristics

Symbol	Parameters/conditions	Rth_jb (°C/W)	Tch (°C)	MTFF (h)
Rth_jb	Thermal resistance junction-back side of die No RF: DC bias V_{DD} = 9 V, I_{DD} = 600 mA , P_{DC} = 5.4 W Tbase = 70 C	5	97.0	>> +1E7
Rth_jb	Thermal resistance junction - back side of die RF Applied: Saturated power 1 W, $V_{D\ D}$= 9 V, Pdiss = 7 W Tbase = 70 C	5	105.0	>> +1E7

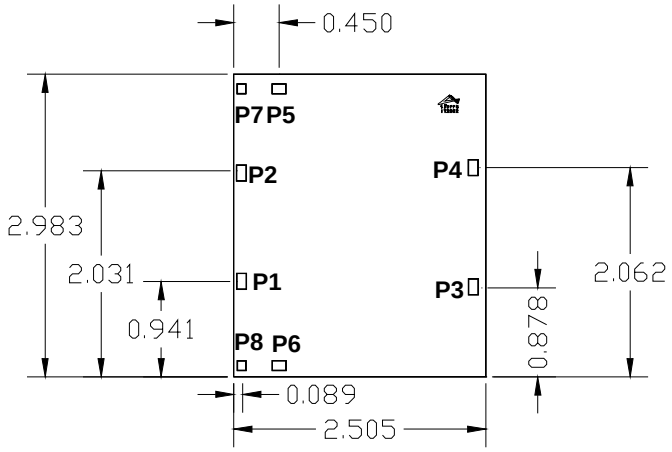
Chip Layout And Pad Locations

Dimensions are in millimeters

Back of chip is RF and DC ground)

Chip size tolerance: ± 20 µm

Chip thickness: 4 mil with ± 0.4 mil tolerance



Pin Out and Pad Dimensions

P1: RF input-1 (100 x 150 µm)
P2: RF input-2 (100 x 150 µm)
P3: RF output-1 and V_{DD1} bias (option 2) by means of bias-tee (100 x 150 µm)
P4: RF output-2 and V_{DD1} bias (option 2) by means of bias-tee (100 x150 µm)
P5: V_{DD1} positive voltage (option 1) by means of choke (150 x100 µm)
P6: V_{DD2} positive voltage (option 1) by means of choke (150 x 100 µm)
P7: V_{GG1}, negative voltage (100 x 100 µm)
P8: V_{GG2}, negative voltage (100 x 100µm)

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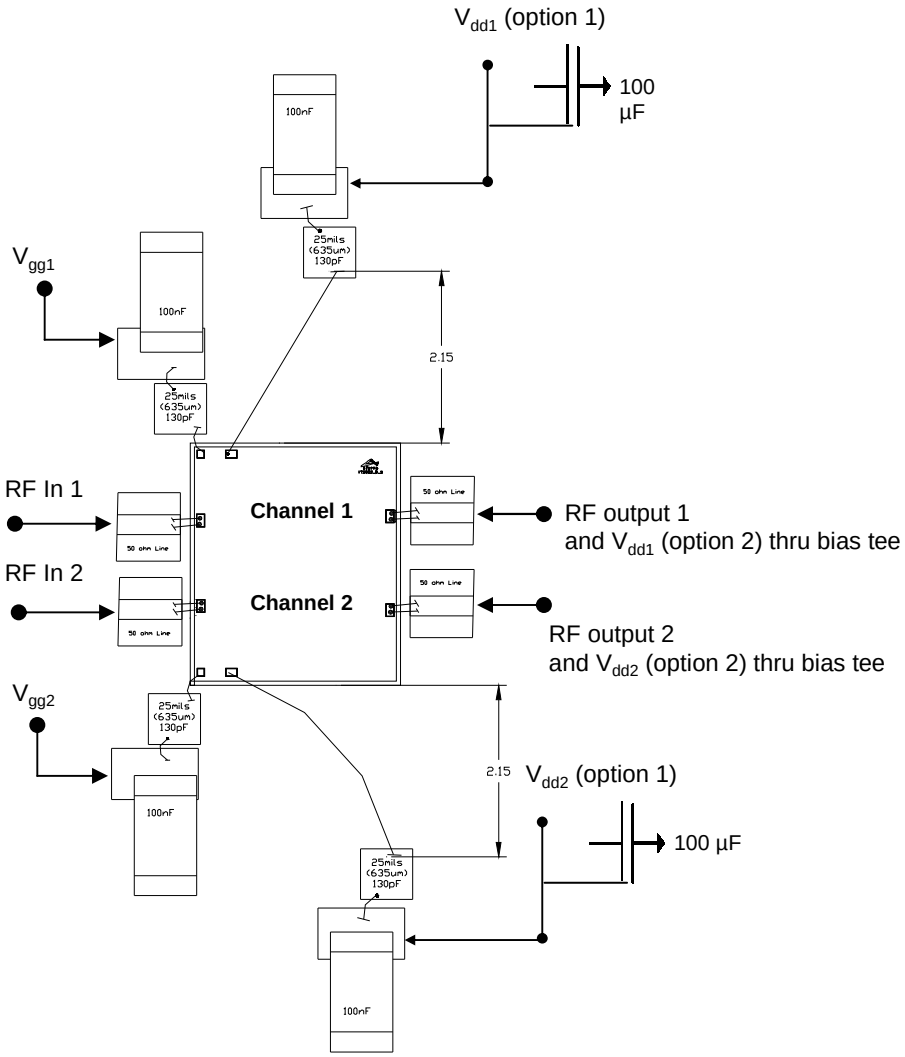
Recommended Chip Mounting for 2 to 26.5 GHz Applications



Note: Bypass capacitor must be large enough to isolate bias supply (>10 µF)

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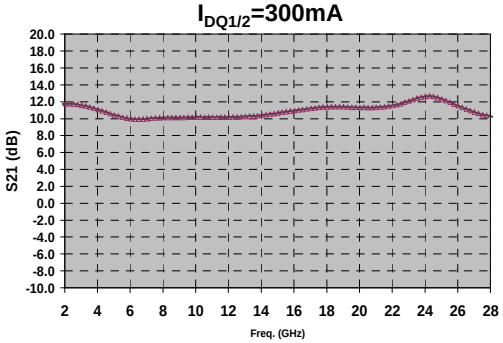
Performance Data

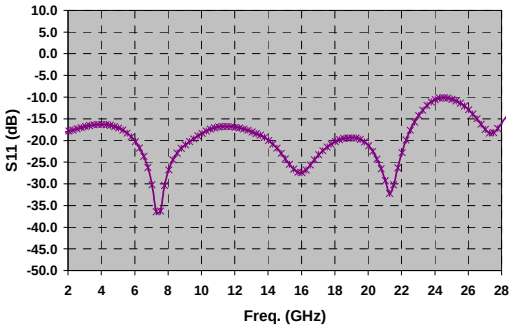
(T = 25°C)

Measured data includes the effect of two parallel RF input/output bond wires.

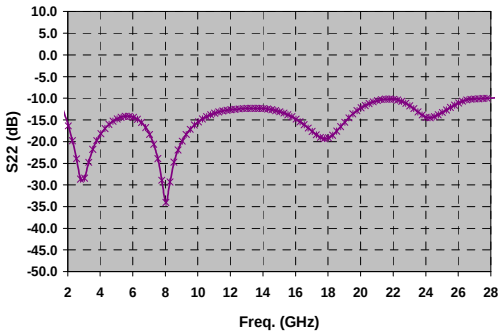
Small Signal Gain, $V_{DD1/2}$=9V, $I_{DQ1/2}$=300mA



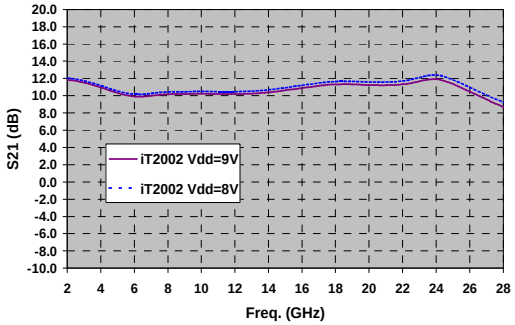
Input Return loss, $V_{DD1/2}$=9V, $I_{DQ1/2}$=300mA



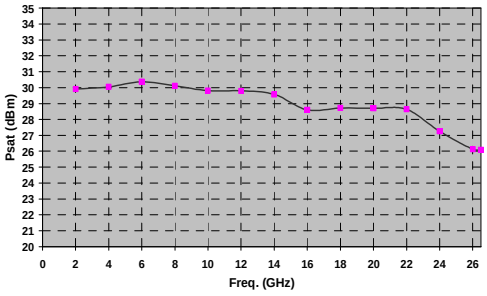
Output Return loss, $V_{DD1/2}$=9V, $I_{DQ1/2}$=300mA



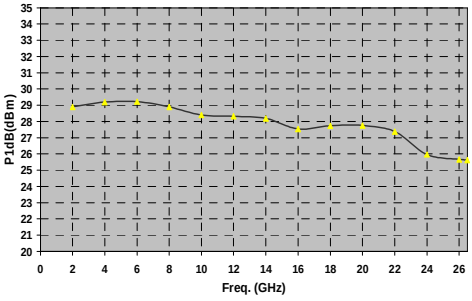
Gain vs. Drain Bias $V_{DD1/2}$, $I_{DQ1/2}$=300mA



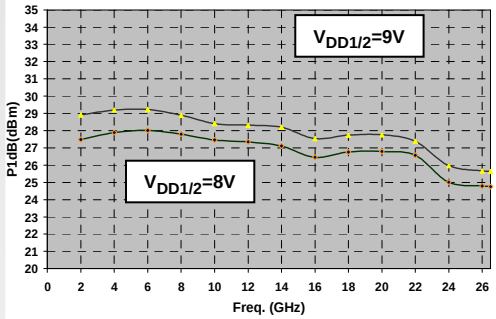
Saturated Power, $V_{DD1/2}$=9V, $I_{DQ1/2}$=300mA



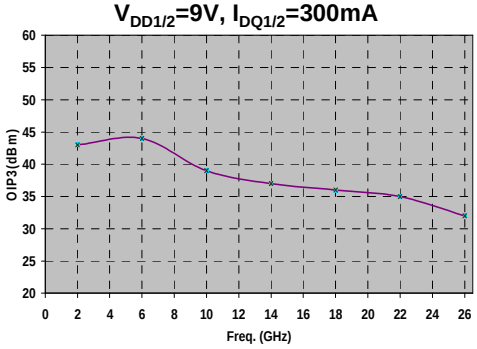
P_{1dB}, $V_{DD1/2}$=9V, $I_{DQ1/2}$=300mA



P_{1dB} vs. $V_{DD1/2}$, $I_{DQ1/2}$=300mA



Output Third Order Intercept Point, $V_{DD1/2}$=9V, $I_{DQ1/2}$=300mA



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Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE ($V_{gg1,2}$) WHILE CORRESPONDING DRAIN VOLTAGE ($V_{dd1,2}$) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following procedure must be considered to properly test the amplifier.

The iT2002 amplifier is biased with a positive drain supply ($V_{DD1,2\ per\ channel}$) and one negative gate supply ($V_{GG1,2\ per\ channel}$) (Channel 1 and Channel 2). The recommended bias condition for the iT2002 is $V_{DD1,2}$= 9.0 V, $I_{DQ1,2}$ = 300 mA. To achieve this drain current level, $V_{GG1,2}$ is typically biased between –0.7 V and –0.9 V. The gate voltage ($V_{GG1/2}$) MUST be applied prior to the drain voltage ($V_{DD1,2}$) during power up and removed after the drain voltage is removed during the power down. Drain bias $V_{DD1,2}$ can be applied to the drain (P5-P6). Alternatively, the positive power supply can be applied through an external bias tee to the RF output pad (P3-P4) .

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs-compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel, and be capable of withstanding 325°C for 15 min.

Die attachment for power devices should utilize gold/tin (80/20) eutectic alloy solder and should avoid a hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD-sensitive devices and should be handled with caution, including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses gold ribbon 3 mil wide and 0.5 mil thick as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mil long corresponding to a typical 2 mil gap between the chip and the substrate material.

Eutectic Die Attachment

iTerra recommends 80/20 AuSn preforms be used for eutectic attachment of its high-power GaAs die. Die attachment should be performed under forming gas or dry nitrogen. All passive components should be attached prior to mounting the GaAs die. Place the chip carrier or package on a heated stage that has a temperature of 290° C controlled to +/- 5° C, with a maximum temperature of less than 300° C. Before and after placing the die on the 290° C heated stage, the die should be placed on a 150° C heated stage to minimize thermal shock. This is essential for die with dimensions greater than 1 mm. Place the AuSn preform on the carrier or package and let it melt. Using tweezers, pick up the GaAs die and scrub it several times for 5 to 15 s. After the die is positioned, remove the carrier or substrate from the heated stage. Maximum dwell time is 1 min., and typically 30 s or less.

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