iT2005F

30 kHz to 18 GHz Power Amplifier

Description

The iT2005F is a RoHS-6-compliant packaged broadband amplifier designed for medium output power applications where low-frequency capabilities are also required. The iT2005F provides saturated output power of 25 dBm up to 8 GHz and greater than 23 dBm up to 18 GHz with average gain of 15 dB. DC power consumption is as low as 1.76 W. Input/output ports are DC coupled.

Features

- Frequency range: 30 KHz – 18 GHz
- 25 dBm nominal Psat (30 KHz – 12 GHz)
- 23 dBm nominal Psat (12 GHz – 18 GHz)
- 15 dB nominal gain
- 1.76 W DC power consumption
- Nominal DC bias conditions: 8 V at 220 mA
- “F” type 5x5 mm QFN RoHS-6-compliant package

Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Positive supply voltage		10	V
Vg_1	Negative supply voltage	-2	0	V
Idd	Positive supply current		600	mA
Ig_1	Negative supply current		1.8	mA
Pin	RF input power		23	dBm
Pdiss_DC	DC power dissipation (no RF)		4	W
Tch	Operating channel temperature		150	°C
Tm	Mounting temperature (30 s)		320	°C
Tst	Storage temperature	-65	150	°C

Electrical Characteristics

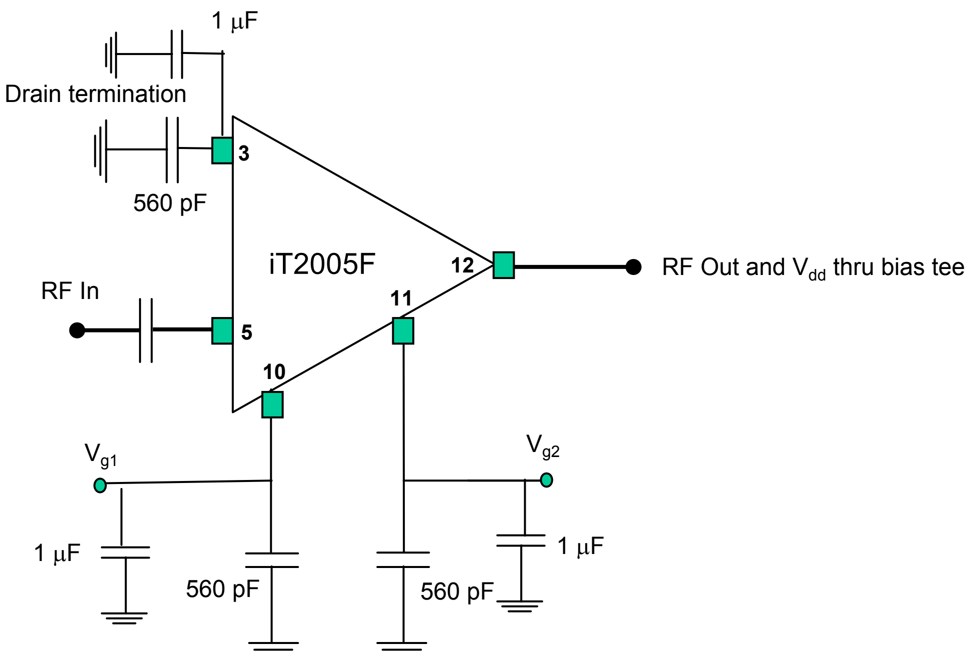
(at 25 °C) 50-ohm system, V_{dd}= +8 V, Quiescent current (I_{DQ}) = 220 mA V_{g2} = +3.4 V

Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	30KHz – 2.0			2.0 – 12.0			12.0 – 18.0			GHz
Gain		16.5			15.5			12.0		dB
Gain flatness		±0.5			±1			±1		dB
S11	-8	-12		-10	-12		-8	-12		dB
S22	-15	-20		-12	-18		-8	-10		dB
P_{sat}	24	26		23	25		21	23		dBm
P_{1dB}	23	25		22	24		19	21		dBm
OIP3					28			24		dBm

Thermal Characteristics

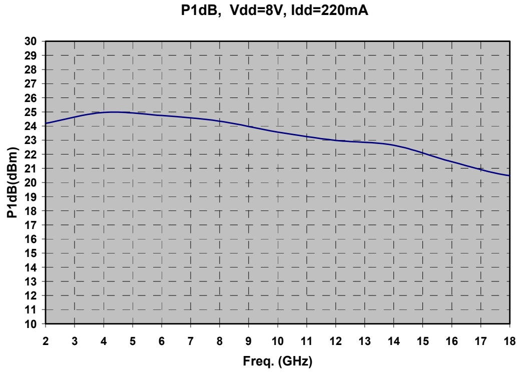
Symbol	Parameters/conditions	Rth_jb (ºC/W)	Tch (º C)	MTTF (h)
Rth_jb	Thermal resistance junction: Ground paddle. No RF: DC bias Vdd = 8 VDC, I_{DD} = 220 mA, P_{DC} = 1.76 W, Tbase = 70º C	18.5	99.0	>>+1E7
Rth_jb	Thermal resistance junction: Ground paddle. RF applied: Saturated power 500 mW, Vdd = 8 VDC, Pdiss = 2.15 W, Tbase = 70º C	18.5	113.0	>>+1E7

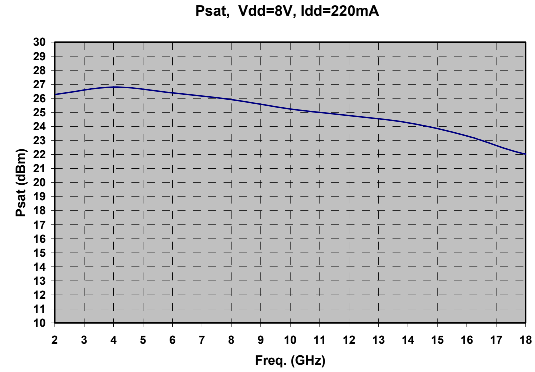
Device Diagram

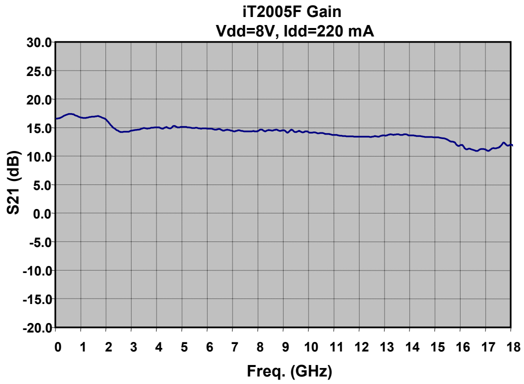


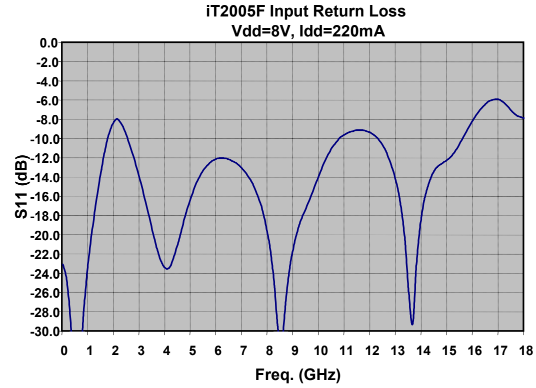
Performance Data

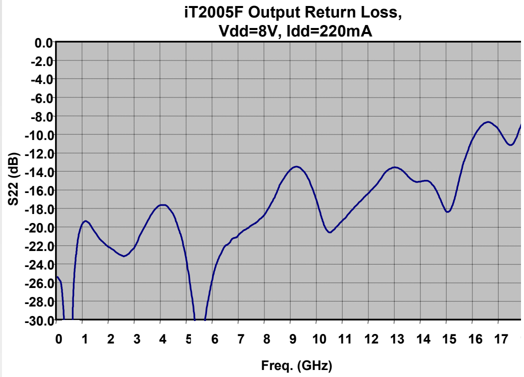
At 25º C

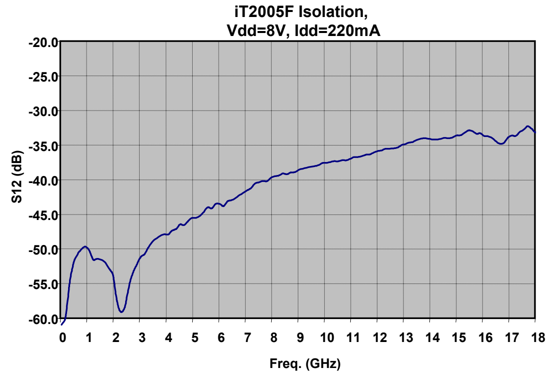












"F" Package Drawing, Pinouts, and Marking

Notes:

Dimensions in inches (mm)
Tolerances are ±0.0039 in. (0.100 mm)

Package drawing encompasses JEDEC MO-220 Version VHHC-2

See iTerra Application Note 10 for recommended pad layout. RoHS parts are backward compatible if application note pad layout is followed.

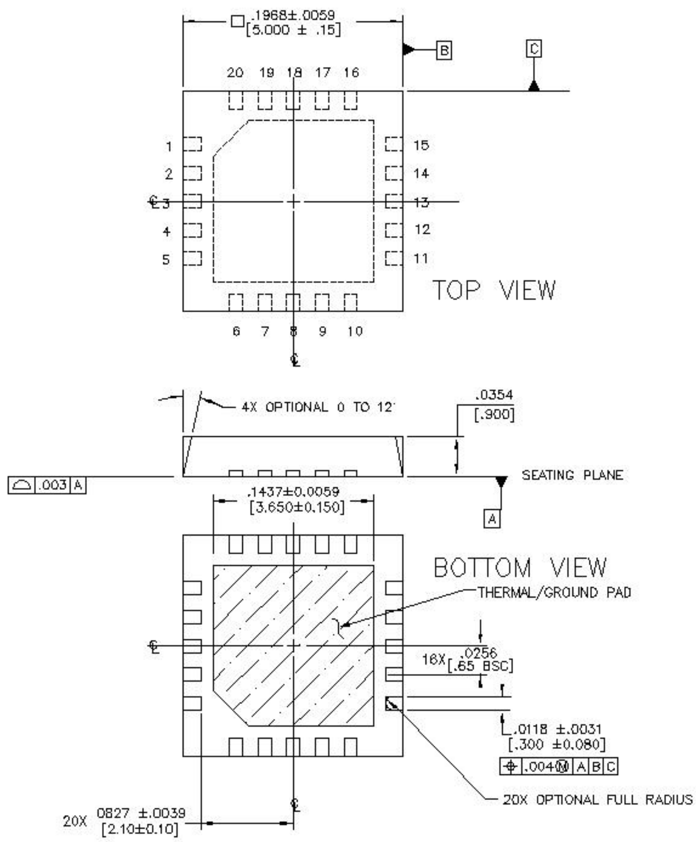
Lead frame material is copper alloy

Mold compound is UL94V0 compliant

Lead finish is NiPdAu

Marking Information
iTerra
MMMMFA
XXNNNN
LLYYWW

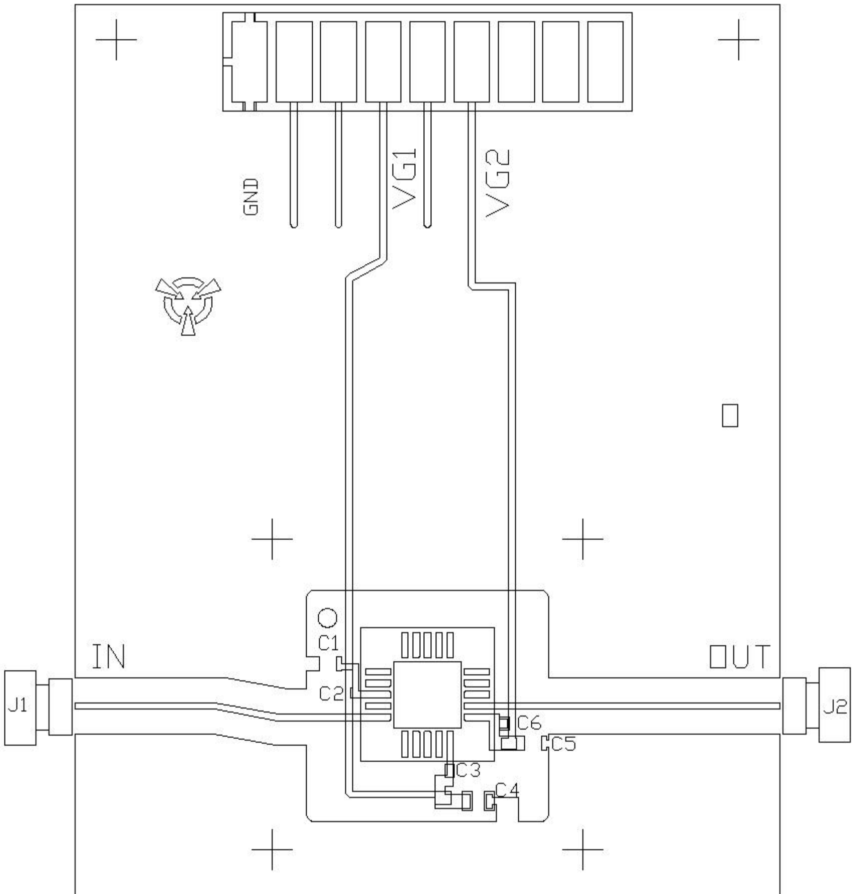
Where
MMMM = part number
F = Package Type
A = Temp. Range
XX = Wafer Lot
NNNN=Ser. No.
LLYYWW = MFG D/C



Pinouts

P1: N/C	P11: Vg2
P2: N/C	P12: RF Out & Vdd
P3: Drain Term.	P13: N/C
P4: N/C	P14: N/C
P5: RF IN	P15: N/C
P6: N/C	P16: N/C
P7: N/C	P17: N/C
P8: N/C	P18: N/C
P9: N/C	P19: N/C
P10: Vg1	P20: N/C

Evaluation Board



List of materials

J1, J2	SMA connectors
C2,C3,C6	560 pF capacitor 0402 Pkg.
C1,C4,C5	1 µF capacitor 0603 Pkg.

For the RF input/output pads, it is very important to maintain a 50-ohm impedance to guarantee good matching with the package transition and achieve good overall signal integrity. For the C2, C3, and C6 capacitances, the PCB pads must be as close as possible to the package in order to minimize parasitics. The PCB layout shown in the figure minimizes parasitics and allows for package placement by automated assembly equipment. The evaluation board shown is available upon request.

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (V_{GG1}) WHILE CORRESPONDING DRAIN VOLTAGE (V_{DD}) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following procedure must be employed to properly test the amplifier.

The iT2005F amplifier is biased with a positive drain supply (V_{DD}) and one negative gate supply (V_{GG1}).

The positive power supply is applied through an external bias tee to the RF output.

The recommended bias conditions for the iT2005F is V_{DD} = 8.0 V, I_{DD} = 220 mA. To achieve this drain current level, V_{GG1} is typically biased between –0.5 V and –0.9 V.

The gate voltage (V_{GG1}) MUST be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage is removed during the power down.

For the second gate V_{GG2} a voltage in the range of 3.4 V is required (V_{DD} = 8 V, V_{GG1} = -0.6 V).

In general $V_{GG2} = V_{DD}/2 – |V_{G1}|$. For example, when V_{DD} = 8 V and V_{GG1} = -0.6, the recommended voltage operation is: V_{GG2} = (8 V/2)-0.6 V = 3.4 V. Bias V_{DD} should be applied before or at the same time of V_{GG2}.